TPS25740、TPS25740A USB Type-C 和 USB PD 源控制器

1 特性

- 通过 USB 供电 (PD) 2.0 认证的供电设备，符合 USB Type-C™ 版本 1.2 的源控制器
- 可通过引脚选择的电压通告
  - 5V、12V 和/或 20V (TPS25740)
  - 5V、9V 和/或 15V (TPS25740A)
- 可通过引脚选择的峰值功率设置
  - 12 个选项，取值范围为 15W 至 100W (TPS25740)
  - 11 个选项，取值范围为 15W 至 81W (TPS25740A)
- 高电压和安全集成
  - 过压、过流、过热保护以及 V_{BUS} 放电
  - CC1 和 CC2 上具有 IEC 61000-4-2 保护
  - 用于故障状态下快速关断的输入引脚
  - 外部 N 沟道 MOSFET 控制
  - 2 引脚外部电源控制
  - 宽 VIN 电源 (4.65V – 25V)
- 断开时的静态电流低于 10 µA
- 端口连接指示器
- 端口电源管理
- 内置 1.8V/35mA 电源输出

2 应用

- USB-PD 适配器（数据较少）
- 专用充电端口（数据较少）
- 电源集线器（数据较少）
- 移动电源
- 点烟器适配器 (CLA)

3 说明

TPS25740 和 TPS25740A 实现了符合 USB 供电 2.0 版本 1.2 和 Type-C 版本 1.2 的源控制器。该器件可通过监控 CC 引脚来检测 USB Type-C 接收设备何时接入，然后通过使能 N 沟道 MOSFET 栅极驱动器接通 VBUS。该器件可通过 USB 供电提供多达 3 种不同的电压，并且使用 4 个输入引脚（PSEL、HIPWR、PCTRL 和 $\overline{EN12V}/EN9V$）配置通告电压和通告电流。该器件会根据接入接收设备的电压请求，使用 CTL1 和 CTL2 引脚从 3 种电源电压中选择一个符合要求的电压。该器件会按照 USB PD 要求自动使 VBUS 输出放电。

未连接设备时，TPS25740/TPS25740A 的流耗通常为 8.5µA（VDD = 3.3V 时为 5.8µA）。此外，还可以在未连接设备时通过端口连接指示器 ($\overline{UFP}$) 输出来禁用电源，从而节省更多的系统功耗。

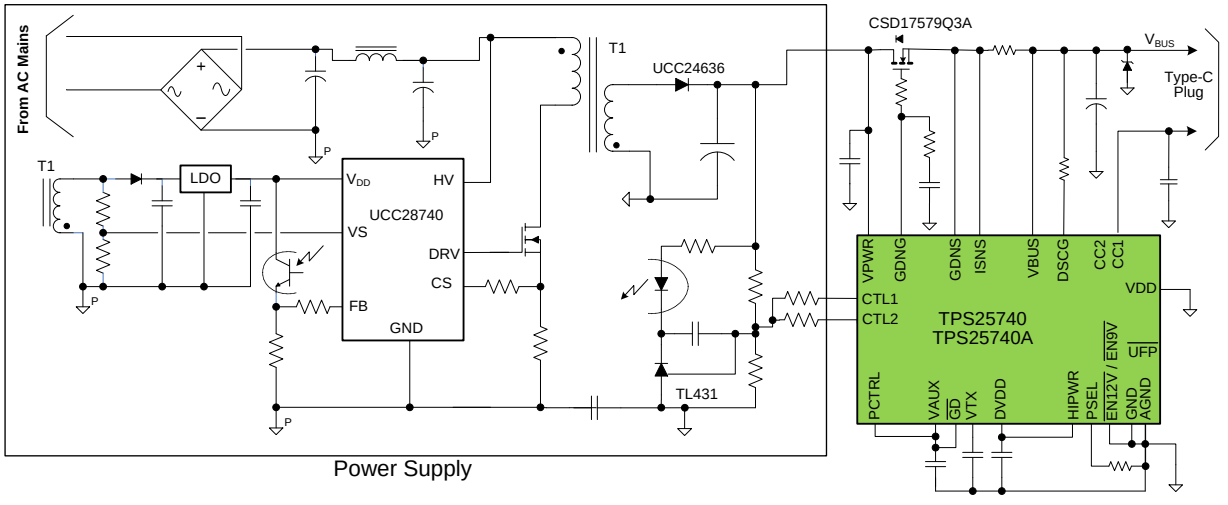
保护 特性 包括过压保护、过流保护、过热保护、CC 引脚上的 IEC 保护以及用于禁用栅极驱动器的系统重写引脚 ($\overline{GD}$)。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS25740	QFN (24)	4.00mm x 4.00mm
TPS25740A		

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

Changes from Revision A (May 2016) to Revision B **Page**

- 添加了*特性*：端口电源管理 ... 1
- Changed the Input resistance MAX value From: 5 MΩ To: 6 MΩ in the *Electrical Characteristics* table ... 9
- Changed the unloaded output voltage on CC pin, $V_{(OCN)}$) MIN value From: 2.8 V To: 2.7 V and the MAX value From 5.5 V To: 4.35 V in the *Electrical Characteristics* table ... 10
- Deleted t_{WD} Watchdog Timer From the *Timing Requirements* table ... 11
- Changed the t_{ST} TYP value From: 24 ms To: 30 ms in the *Switching Characteristics* table ... 12
- Deleted sentence from *Output Power Supply (DVDD)*: "It will also be pulsed high for t_{CcDeb} every t_{WD} when there is nothing connected." ... 34
- Deleted the last sentence from the *Sleep Mode* section: "The device also wakes up every t_{WD} and checks for a connection before returning to sleep mode." ... 35
- Added test: "The TPS25740/TPS25740A Design Calculator Tool.." to the *Application Information* section ... 36
- Changed capacitor From: 10 µF To: 6.8 µF in the Figure 36 ... 36
- Added sentence "All slew rate control methods" to the *Voltage Transition Requirements* section ... 41
- Changed section title From: V_{OUT} Ripple Filtering using R_F and C_F To: Tuning OCP Using R_F and C_F. Updated section text ... 43
- Changed From: A 10 µF, 25 V, ±10% X5R or X7R ceramic capacitor To: A 6.8 µF, 25 V, ±10% X5R or X7R ceramic capacitor in the *Configurable Components* section ... 45
- Changed From: "Type-C receptacle" To: "Type-C plug" in Figure 56 ... 48
- Changed From: A 10 µF, 25 V, ±10% X5R or X7R ceramic capacitor to: A 6.8 µF, 25 V, ±10% X5R or X7R ceramic capacitor in the *Configurable Components* section ... 49
- Changed section title From: Dual-Port A/C Power Source (Wall Adaptor) To: Dual-Port Power Managed A/C Power Source (Wall Adaptor) ... 53
- 在*文档支持*部分中添加了 TPS25740/TPS25740A 设计计算器工具链接以及 TPS25740EVM-741 和 TPS25740AEVM-741 EVM 用户指南链接 ... 57

Changes from Original (March 2016) to Revision A **Page**

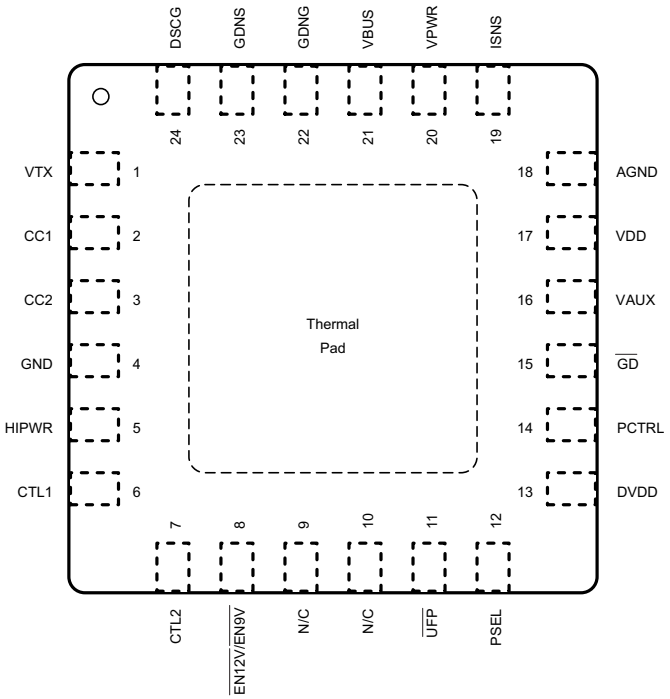
- 已从“产品预览”改为“量产数据”..... 1

5 Device Comparison Table

DEVICE NUMBER	VOLTAGE OPTION
TPS25740	Offers 5 V, 12 V, and 20 V
TPS25740A	Offers 5 V, 9 V, and 15 V

6 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VTX	1	O	Bypass pin for transmit driver supply. Connect this pin to GND via the recommended ceramic capacitor.
CC1	2	I/O	Multifunction configuration channel interface pin to USB Type-C. Functions include connector polarity, end-device connection detect, current capabilities, and PD communication.
CC2	3	I/O	Multifunction configuration channel interface pin to USB Type-C. Functions include connector polarity, end-device connection detect, current capabilities, and PD communication.
GND	4	—	Power ground is associated with power management and gate driver circuits. Connect to AGND and PAD.
HIPWR	5	I	Four-state input pin used to configure the voltages and currents that will be advertised. It may be connected directly to GND or DVDD, or it may be connected to GND or DVDD via a resistance $R_{(SEL)}$.
CTL1	6	O	Digital output pin used to control an external voltage regulator.
CTL2	7	O	Digital output pin used to control an external voltage regulator.
$\overline{\text{EN12V}}$ / $\overline{\text{EN9V}}$	8	I	For TPS25740: If it is pulled low, then the 12 V PDO may be transmitted. If it is not pulled low, the 12-V PDO will not be advertised. For TPS25740A: If it is pulled low, then the 9 V PDO may be transmitted. If it is not pulled low, the 9-V PDO will not be advertised.
N/C	9		Connect to GND.
N/C	10		Connect to GND.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{UFP}$	11	O	Open drain output pin used to indicate that either CC1 or CC2 (but not both) is pulled down by a USB Type-C Sink.
PSEL	12	I	A four-state input used for selecting the maximum power that can be provided. It may be connected directly to GND or DVDD, or it may be connected to GND or DVDD via a resistance $R_{(SEL)}$
DVDD	13	O	Internally regulated 1.85 V rail for external use up to 35 mA. Connect this pin to GND via the recommended bypass capacitor .
PCTRL	14	I	Input pin used to control the power that will be advertised. It may be pulled high or low dynamically.
$\overline{GD}$	15	I	Master enable for the GDNG/GDNS gate driver. The system can drive this low to force the power path switch off.
VAUX	16	O	Internally regulated rail for use by the power management circuits. Connect this pin to GND via the recommended bypass capacitor.
VDD	17	I	Optional input supply.
AGND	18	—	Analog ground associated with monitoring and power conditioning circuits. Connect to GND and PAD.
ISNS	19	I	The ISNS input is used to monitor a VBUS-referenced sense resistor for over-current events.
VPWR	20	I	Connect to an external voltage as a source of bias power. If VDD is supplied, this supply is optional while $\overline{UFP}$ is high.
VBUS	21	I	The voltage monitor for the VBUS line.
GDNG	22	O	High-voltage open drain gate driver which may be used to drive NMOS power switches. Connect to the gate terminal.
GDNS	23	I	High-voltage open drain gate driver which may be used to drive NMOS power switches. Connect to the source terminal.
DSCG	24	O	Discharge is an open-drain output that discharges the system VBUS line through an external resistor.
PAD			Connect PAD to GND / AGND plane.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin Voltage (sustained)	VDD , $\overline{EN12V}$, $\overline{EN9V}$, CTL1, CTL2, $\overline{UFP}$, PCTRL, CC1, CC2	–0.3	6	V
	VTX(2)	–0.3	2.1	V
	VAUX(2)	–0.3	4.5	V
	$\overline{GD}$ (3)	–0.3	7	V
	HIPWR, PSEL, DVDD (2)	–0.3	2.1	V
	GDNG(2)	–0.5	40	V
	VBUS,VPWR, ISNS, DSCG, GDNS	–0.5	30	V
Pin Voltage (transient for 1ms)	VBUS,VPWR, ISNS, DSCG, GDNS	–1.5	30	V
Pin-to-pin voltage	$V_{(GDNG)} – V_{(GDNS)}$	–0.3	20	V
	AGND to GND	–0.3	0.3	V
	ISNS to VBUS	–0.3	0.3	V
Sinking current (average)	CTL1, CTL2, $\overline{UFP}$		8	mA
	$\overline{GD}$		100	µA
	DSCG		10	mA
Sinking current (transient, 50 ms pulse 0.25% duty cycle)	DSCG		375	mA
Current sourcing	VTX	Internally limited		mA
	CC1, CC2	Internally limited		mA
	VAUX	0	25	µA
Operating junction temperature range, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Do not apply voltage to these pins.
(3) Voltage allowed to rise above Absolute Maximum provided current is limited.

7.2 ESD Ratings(1)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	
		IEC (4) 61000-4-2 contact discharge, CC1, CC2	±8000	
		IEC (4) 61000-4-2 air-gap discharge, CC1, CC2	±15000	

(1) This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(4) These results were passing limits that were obtained on an application-level test board. Individual results may vary based on implementation. Surges per IEC61000-4-2, 1999 applied between CC1/CC2 and ground of TPS25740EVM-741 and TPS25740AEVM-741

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply Voltage	VDD	0		5.5	V
		VPWR	4.65		25	V
V_I	Applied Voltage	$\overline{EN12V}$, $\overline{EN9V}$, PCTRL, CC1, CC2, CTL1, CTL2	0		5.5	V
		$\overline{GD}$	0		6.5	V
		DSCG, GDNS, VBUS	0		25	V
		HIPWR, PSEL	0		DVDD	V
V_I	Pin-to-pin voltage	ISNS - VBUS	–0.1		0.1	V
V_{IH}	High-Level Input Voltage	$\overline{EN12V}$, $\overline{EN9V}$	1.4			V
		PCTRL	2			V
		$\overline{GD}$	2			V
V_{IL}	Low-Level Input Voltage	$\overline{EN12V}$, $\overline{EN9V}$			0.5	V
		PCTRL			1.6	V
		$\overline{GD}$			1.6	V
I_S	Sinking Current	CTL1, CTL2, $\overline{UFP}$			5	mA
		$\overline{GD}$			80	µA
		DSCG, transient sinking current 50 ms pulse, 0.25% duty cycle			350	mA
		DSCG, average			5	mA
C_S	Shunt capacitance	CC1, CC2 ($C_{(RX)}$)	200	560	600	pF
		VBUS ($C_{(PDIN)}$)			10	µF
		DVDD ($C_{(DVDD)}$)	0.198	0.22	0.242	µF
		VAUX ($C_{(VAUX)}$)	0.09	0.1	0.11	µF
		VTX ($C_{(VTX)}$)	0.09	0.10	0.11	µF
		VDD ($C_{(VDD)}$)	0.09			µF
R_S	Sense resistance	Configured for 3 A		5	6.4	mΩ
		Configured for 5 A		5	5.8	mΩ
$R_{(PUD)}$	Pull up/down resistance	HIPWR, PSEL (direct to GND or direct to DVDD)	0		1	kΩ
		HIPWR, PSEL ($R_{(SEL)}$)	80	100	120	kΩ
$R_{(DSCG)}$	Series resistance	Maximum VBUS voltage of 25 V	80			Ω
		Maximum VBUS voltage of 15 V	43			Ω
		Maximum VBUS voltage of 6 V	20			Ω
T_J	Operating junction temperature		-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS25740 TPS25740A RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF, $\overline{EN12V}$ = GND and $\overline{EN9V}$ = GND; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Comparator (VBUS)						
$V_{(VBUS\_RTH)}$	VBUS Threshold (Rising voltage)		4.25	4.45	4.65	V
$V_{(VBUS\_FTH)}$	VBUS Threshold (Falling voltage)		3.5	3.7	3.9	V
	VBUS Threshold (Hysteresis)			0.75		V
Power Supply (VDD, VPWR)						
$V_{(VDD\_TH)}$	VDD UVLO threshold	Rising voltage	2.8	2.91	2.97	V
		Falling voltage	2.8	2.86	2.91	
		Hysteresis, comes into effect once the rising threshold is crossed.		0.05		
$V_{(VPWR\_RTH)}$	VPWR UVLO threshold rising	Rising voltage	4.2	4.45	4.65	V
$V_{(VPWR\_FTH)}$	VPWR UVLO threshold falling	Falling voltage	3.5	3.7	3.9	V
	VPWR UVLO threshold hysteresis	Hysteresis, comes into effect once the rising threshold is crossed.		0.75		V
	Supply current drawn from VDD in sleep mode	VPWR = 0 V, VDD = 5 V, CC1 and CC2 pins are open.		9.2	20	µA
		VPWR = 0 V, VDD = 5 V,CC1 pin open, CC2 pin tied to GND.		94	150	µA
	Supply current drawn from VPWR in sleep mode	VPWR = 5 V, VDD = 0 V, CC1 and CC2 pins are open.		8.5	15	µA
		VPWR = 5 V, VDD = 0 V, CC1 pin open, CC2 pin tied to GND.		90	140	µA
$I_{(SUPP)}$	Operating current while sink attached	PD Sourcing active, VBUS = 5 V, VPWR = 5 V, VDD = 3.3 V	1	1.8	3	mA
Over/Under Voltage Protection (VBUS)						
$V_{(FOVP)}$	Fast OVP threshold, always enabled	5 V PD contract	5.8	6.05	6.3	V
		12 V PD contract (TPS25740)	13.2	13.75	14.3	V
		20 V PD contract (TPS25740)	22.1	23.05	24.0	V
		9 V PD contract (TPS25740A)	10.1	10.55	11.0	V
		15 V PD contract (TPS25740A)	16.2	16.95	17.7	V
$V_{(SOVP)}$	Slow OVP threshold, disabled during voltage transitions. (See Figure 1)	5 V PD contract	5.5	5.65	5.8	V
		12 V PD contract (TPS25740)	13.1	13.4	13.7	V
		20 V PD contract (TPS25740)	21.5	22.0	22.5	V
		9 V PD contract (TPS25740A)	10	10.2	10.4	V
		15 V PD contract (TPS25740A)	16.3	16.5	17	V
$V_{(SUVP)}$	UVP threshold, disabled during voltage transitions (See Figure 1)	5 V PD contract	3.5	3.65	3.8	V
		12 V PD contract (TPS25740)	9.2	9.45	9.7	V
		20 V PD contract (TPS25740)	15.7	16.1	16.5	V
		9 V PD contract (TPS25740A)	6.8	6.95	7.1	V
		15 V PD contract (TPS25740A)	11.7	11.95	12.2	V
VAUX						
$V_{(VAUX)}$	Output voltage	0 ≤ $I_{(VAUX)}$ ≤ $I_{(VAUXEXT)}$	2.875	3.2	4.1	V
	VAUX Current limit		1		5	mA
$I_{(VAUXEXT)}$	External load that may be applied to VAUX.				25	µA
DVDD						
$V_{(DVDD)}$	Output voltage	0 mA ≤ $I_{(DVDD)}$ ≤ 35 mA, CC1 or CC2 pulled to ground via 5.1 kΩ, or both CC1 and CC2 pulled to ground via 1 kΩ	1.75	1.85	1.95	V
	Load Regulation	Overshoot from $V_{(DVDD)}$, 10-mA minimum, 0.198-µF bypass capacitor	1.7		2	V
	Current limit	DVDD tied to GND	40		150	mA

Electrical Characteristics (continued)

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF, $\overline{EN12V}$ = GND and $\overline{EN9V}$ = GND; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VTX						
	Output voltage	Not transmitting or receiving, 0 to 2 mA external load	1.050	1.125	1.200	V
	Current Limit	VTX tied to GND	2.5		10	mA
Gate Driver Disable ($\overline{GD}$)						
$V_{(GD\_TH)}$	Input enable threshold voltage	Rising voltage	1.64	1.725	1.81	V
		Hysteresis		0.15		V
$V_{(GDC)}$	Internal clamp voltage	$I_{(\overline{GD})}$ = 80 µA	6.5	7	8.5	V
$R_{(GD)}$	Internal pulldown resistance	From 0 V to 6 V	3	6	9.5	MΩ
Discharge (DSCG) (1)(2)						
$V_{(DSCGT)}$	ON state (linear)	$I_{(DSCG)}$ = 100 mA	0.15	0.42	1	V
$I_{(DSCGT)}$	ON state (saturation)	$V_{(DSCG)}$ = 4 V, pulsed mode operation	220	553	1300	mA
$R_{(DSCGB)}$	Discharge bleeder	While CC1 is pulled down by 5.1 kΩ and CC2 is open, $V_{(DSCG)}$ = 25 V	6.6	8.2	10	kΩ
	Leakage current	0 V ≤ $V_{(DSCG)}$ ≤ 25 V			2	µA
N-ch MOSFET Gate Driver (GDNG,GDNS)						
$I_{(GDNON)}$	Sourcing current	0 V ≤ $V_{(GDNS)}$ ≤ 25 V, 0 V ≤ $V_{(GDNG)}$ – $V_{(GDNS)}$ ≤ 6 V	13.2	20	30	µA
$V_{(GDNON)}$	Sourcing voltage while enabled ($V_{(GDNG)}$– $V_{(GDNS)}$)	0 V ≤ $V_{(GDNS)}$ ≤ 25 V, $I_{(GDNON)}$ ≤ 4 µA, VPWR = 0 V	7		12	V
		0 V ≤ $V_{(GDNS)}$ ≤ 25 V, $I_{(GDNON)}$ ≤ 4 µA, VDD = 0 V	8.5		12	V
$R_{(GDNGOFF)}$	Sinking strength while disabled	$V_{(GDNG)}$ – $V_{(GDNS)}$= 0.5 V, 0 ≤ $V_{(GDNS)}$ ≤ 25 V		150	300	Ω
	Sinking strength UVLO (safety)	VDD = 1.4 V, $V_{(GDNG)}$ = 1 V, $V_{(GDNS)}$ = 0 V, VPWR = 0 V		145		µA
		VPWR = 1.4 V, $V_{(GDNG)}$ = 1 V, $V_{(GDNS)}$ = 0 V, VDD = 0 V		145		µA
	Off-state leakage	$V_{(GDNS)}$ = 25 V, $V_{(GDNG)}$ open			7	µA
Power Control Input (PCTRL)						
$V_{(PCTRL\_TH)}$	Threshold voltage(3)	Voltage rising	1.65	1.75	1.85	V
		Hysteresis		100		mV
	Input resistance	0 V ≤ $V_{(PCTRL)}$ ≤ $V_{(VAUX)}$	1.5	2.9	6	MΩ
Voltage Select (HIPWR), Power Select (PSEL) (4)						
	Leakage current	0 V ≤ $V_{(HIPWR)}$ ≤ $V_{(DVDD)}$, 0 V ≤ $V_{(PSEL)}$ ≤ $V_{(DVDD)}$	–1		1	µA
Port Status and Voltage Control (CTL1, CTL2, $\overline{UFP}$) (5)						
V_{OL}	Output low voltage	I_{OL} = 4 mA sinking			0.4	V
	Leakage Current (6)	In Hi-Z state, 0 ≤ $V_{(CTLx)}$ ≤ 5.5 V or 0 ≤ $V_{\overline{UFP}}$ ≤ 5.5V	–0.5		0.5	µA

(1) If T_{J1} is perceived to have been exceeded an OTSD occurs and the discharge FET is disabled.
(2) The discharge pull-down is not active in the sleep mode.
(3) When voltage on the PCTRL pin is less than $V_{(PCTRL\_TH)}$, the amount of power advertised is reduced by half.
(4) Leaving HIPWR or PSEL open is an undetermined state and leads to unpredictable behavior.
(5) These pins are high-z during a UVLO, reset, or in Sleep condition.
(6) The pins were designed for less leakage, but testing only verifies that the leakage does not exceed 0.5 µA.

Electrical Characteristics (continued)

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF, $\overline{EN12V}$ = GND and $\overline{EN9V}$ = GND; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Enable 9 V, 12 V Capability ($\overline{EN9V}$, $\overline{EN12V}$)						
	Input low threshold voltage				0.585	V
	Input high threshold voltage		1.225			V
	Input hysteresis			0.25		V
Transmitter Specifications (CC1, CC2)						
R_{TX}	Output resistance (zDriver from USB PD in 文档支持)	During transmission	33	45	75	Ω
$V_{(TXHI)}$	Transmit high voltage	External Loading per Figure 25	1.05	1.125	1.2	V
$V_{(TXLO)}$	Transmit low voltage	External Loading per Figure 25	–75		75	mV
Receiver Specifications (CC1, CC2)						
$V_{(RXHI)}$	Receive threshold (rising)		800	840	885	mV
$V_{(RXLO)}$	Receive threshold (falling)		485	525	570	mV
	Receive threshold (Hysteresis)			315		mV
$V_{(INT)}$	Amplitude of interference that can be tolerated	Interference is 600 kHz square wave, rising 0 to 100 mV.			100	mV
		Interference is 1 MHz sine wave			1	V_{PP}
DFP Specifications (CC1, CC2)						
$V_{(DSTD)}$	Detach threshold when cable is detached.	In standard DFP mode(7), voltage rising	1.52	1.585	1.65	V
		Hysteresis		0.02		V
$V_{(D1.5)}$		In 1.5 A DFP mode(8), voltage rising	1.52	1.585	1.65	V
		Hysteresis		0.02		V
$V_{(D3.0)}$		In 3 A DFP mode(9), voltage rising	2.50	2.625	2.75	V
		Hysteresis		0.05		V
$V_{(OCN)}$	Unloaded output voltage on CC pin	normal mode	2.7		4.35	V
$V_{(OCDS)}$		VPWR = 0 V (in UVLO) or in sleep mode	1.8		5.5	V
$I_{(RPSTD)}$	Loaded output current while connected through CCx	In standard DFP mode1, CCy open, 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	64	80	96	µA
$I_{(RP1.5)}$		In 1.5 A DFP mode 2, CCy open, 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	166	180	194	µA
$I_{(RP3.0)}$		In 3 A DFP mode 3, CCy open, 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	304	330	356	µA
$V_{(RDSTD)}$	Ra, Rd detection threshold (falling)	In standard DFP mode1, 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	0.15	0.19	0.23	V
		Hysteresis		0.02		V
$V_{(RD1.5)}$		In 1.5 A DFP mode2, CCy open 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	0.35	0.39	0.43	V
		Hysteresis		0.02		V
$V_{(RD3.0)}$		In 3 A DFP mode3, CCy open 0 V ≤ V_{CCx} ≤ 1.5 V (vRd)	0.75	0.79	0.83	V
		Hysteresis		0.02		V
$V_{(WAKE)}$	Wake threshold (rising and falling), exit from sleep mode	VPWR = 4.65 V , 0 V ≤ V_{DD} ≤ 3 V	1.6		3.0	V
$I_{(DSDFP)}$	Output current on CCx in sleep mode to detect Ra removal.	CCx = 0V, CCy floating	40	73	105	µA

(7) Standard DFP mode is active after a USB Type-C sink, debug accessory, or audio accessory is attached until the first USB PD message is transmitted (after GDNG has been enabled).
(8) 1.5 A DFP mode is active after a USB PD message is received.
(9) 3 A DFP mode is active after GDNG has been enabled until a USB PD message is received.

Electrical Characteristics (continued)

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF, $\overline{EN12V}$ = GND and $\overline{EN9V}$ = GND; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OverCurrent Protection (ISNS, VBUS)						
$V_{I(TRIP)}$	Current trip shunt voltage	Specified as $V_{(ISNS)}$-$V_{(VBUS)}$. 3.5 V(10) ≤ VBUS ≤ 25 V				
		HIPWR: 5 A not enabled	19.2		22.6	mV
		HIPWR = DVDD (5 A enabled)	29		34	mV
OTSD						
T_{J1}	Die Temperature (Analog)(11)	T_J ↑	125	135	145	°C
		Hysteresis		10		
T_{J2}	Die Temperature (Analog) (12)	T_J ↑	140	150	163	°C
		Hysteresis		10		

(10) Common mode minimum aligns to VBUS UVLO. VBUS must be above its UVLO for the OCP function to be active.
(11) When T_{J1} trips a hard reset is transmitted and discharge is disabled, but the bleed discharge is not disabled.
(12) T_{J2} trips only when some external heat source drives the temperature up. When it trips the DVDD, and VAUX power outputs are turned off.

7.6 Timing Requirements

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF, $\overline{EN12V}$ = GND and $\overline{EN9V}$ = GND; all other pins open (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{FOVPDG}	Deglitch for fast over-voltage protection			5		µs
t_{OCP}	Deglitch Filter for over-current protection				15	µs
	Time power is applied until CC1 and CC2 pull-ups are applied.	$V_{(VPWR)}$ > $V_{(VPWR\_TH)}$ OR $V_{(VDD)}$ > $V_{(VDD\_TH)}$		2.5	4	ms
t_{CC}	Falling/Rising voltage deglitch time for detection on CC1 and CC2			120		µs
Transmitter Specifications (CC1, CC2)						
t_{UI}	Bit unit Interval		3.05	3.3	3.70	µs
	Rise/fall time, t_{Fall} and t_{Rise} (refer to USB PD in 文档支持)	External Loading per Figure 25	300		600	ns

7.7 Switching Characteristics

Unless otherwise stated in a specific test condition the following conditions apply: –40°C ≤ T_J ≤ 125°C; 3 ≤ VDD ≤ 5.5 V, 4.65 V ≤ VPWR ≤ 25 V; HIPWR = GND, PSEL = GND, $\overline{GD}$ = VAUX, PCTRL = VAUX, AGND = GND; VAUX, VTX, bypassed with 0.1 µF, DVDD bypassed with 0.22 µF, $\overline{EN12V}$ = GND and $\overline{EN9V}$ = GND; all other pins open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{VP}	Delay from enabling external NFET until under-voltage and OCP protection are enabled	VBUS = GND		190		ms
t_{STL}	Source settling time, time from CTL1 and CTL2 being changed until a PS_RDY USB PD message is transmitted to inform the sink is may draw full current. (refer to USB PD in 文档支持)			260		ms
t_{SR}	Time that GDNG is disabled after a hard reset. This is $t_{SrcRecover}$. (refer to USB PD in 文档支持)	$T_J > T_{J1}$		765		ms
t_{HR}	Time after hard reset is transmitted until GDNG is disabled. This is $t_{PSHardReset}$. (refer to USB PD in 文档支持)			30		ms
t_{CCDeb}	Time until $\overline{UFP}$ is pulled low after sink attachment, this is the USB Type-C required debounce time for attachment detection called $t_{CCDebounce}$. (refer to USB Type-C in 文档支持)			185		ms
t_{ST}	Delay after sink request is accepted until CTL1 and/or CTL2 is changed. This is called $t_{SnkTransition}$. (refer to USB PD in 文档支持)			30		ms
t_{FLT}	The time in between hard reset transmissions in the presence of a persistent supply fault.	$\overline{GD}$ = GND or VPWR=GND, sink attached		1395		ms
t_{SH}	The time in between retries (hard reset transmissions) in the presence of a persistent VBUS short.	VBUS = GND, sink attached		985		ms
t_{ON}	The time from $\overline{UFP}$ being pulled low until a hard reset is transmitted. Designed to be greater than $t_{SrcTurnOn}$. (refer to USB PD in 文档支持)	$\overline{GD}$ = 0 V or VPWR = 0 V		600		ms
	Retry interval if USB PD sink stops communicating without being removed or if sink does not communicate after a fault condition. Time GDNG remains enabled before a hard reset is transmitted. This is the $t_{NoResponse}$ time. (refer to USB PD in 文档支持)	Sink attached		4.8		s
t_{DVDD}	Delay before DVDD is driven high	After sink attached			5	ms
t_{GDoff}	Turnoff delay, time until $V_{(\overline{GDNG})}$ is below 10% of its initial value after the $\overline{GD}$ pin is low.	$V_{\overline{GD}}$: 5 V → 0 V in < 0.5 µs.			5	µs
t_{FOVP}	Response time when VBUS exceeds the fast-OVP threshold	VBUS ↑ to GDNG OFF ($V_{(GDNG)}$ below 10% its initial value)			30	µs
	OCP large signal response time	5 A enabled, $V_{(ISNS)}$ -$V_{(VBUS)}$: 0 V → 42 mV measured to GDNG transition start.			30	µs
	Time until discharge is stopped after T_{J1} is exceeded.	0 V ≤ $V_{(DSCG)}$ ≤ 25 V			10	µs
	Digital output fall time	$V_{(PULLUP)}$ = 1.8 V, C_L = 10 pF, $R_{(PULLUP)}$ = 10 kΩ, $V_{(CTLx)}$ or $V_{(\overline{UFP})}$: 70% V_{PULLUP} → 30% V_{PULLUP}	20		300	ps

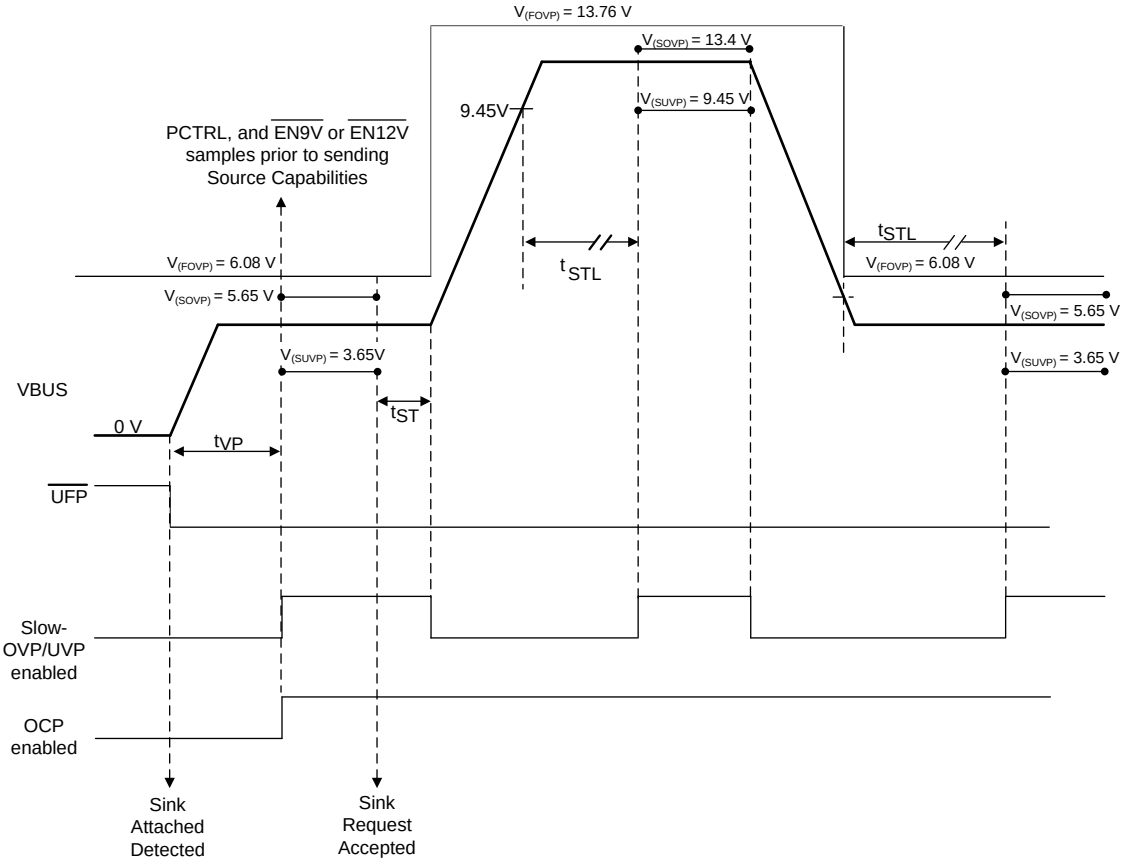


Figure 1. Timing Illustration for t_{VP}, t_{ST} and t_{STL}, After Sink Attachment negotiation to 12 V then back to 5 V. $V_{(SOVP)}$ and $V_{(SUVP)}$ are Disabled Around Voltage Transitions.

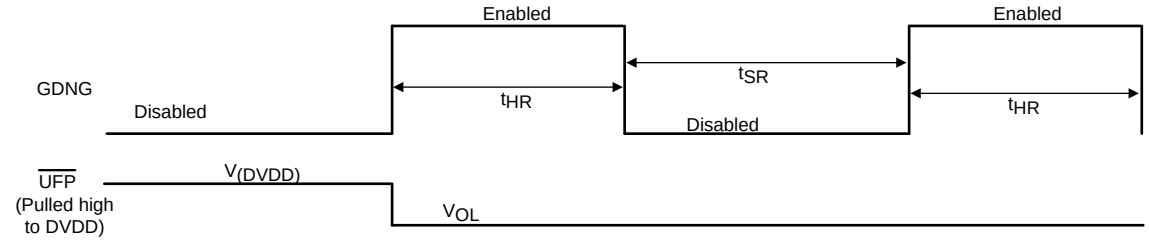


Figure 2. Timing Illustration for t_{HR} and t_{SR}, After Sink Attachment with persistent $T_J > T_{J1}$

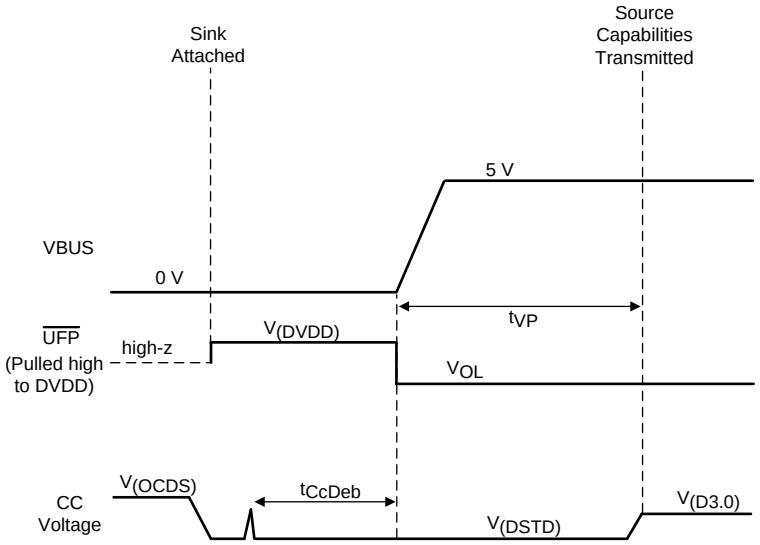


Figure 3. Timing Illustration for t_{CcDeb} and t_{VP}, Under Persistent Fault Condition

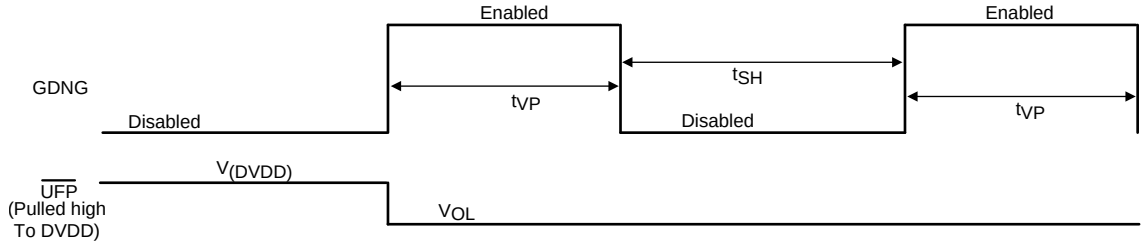


Figure 4. Timing Illustration for t_{SH} and t_{VP}, with VBUS Shorted to Ground

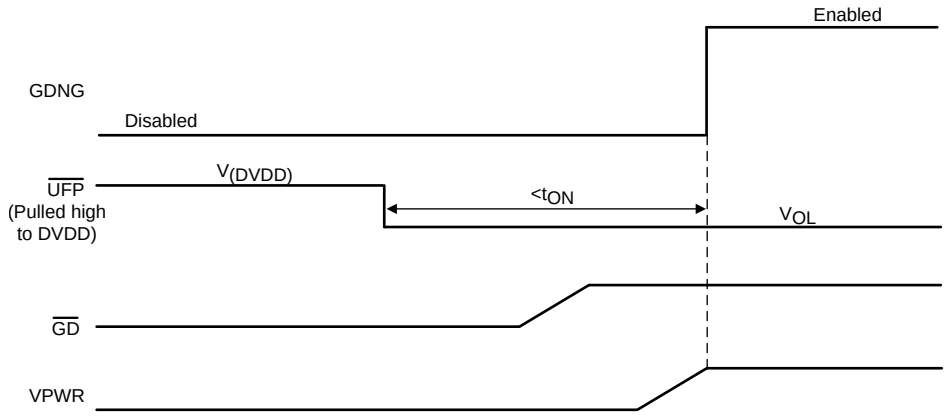


Figure 5. Timing Illustration for t_{ON}

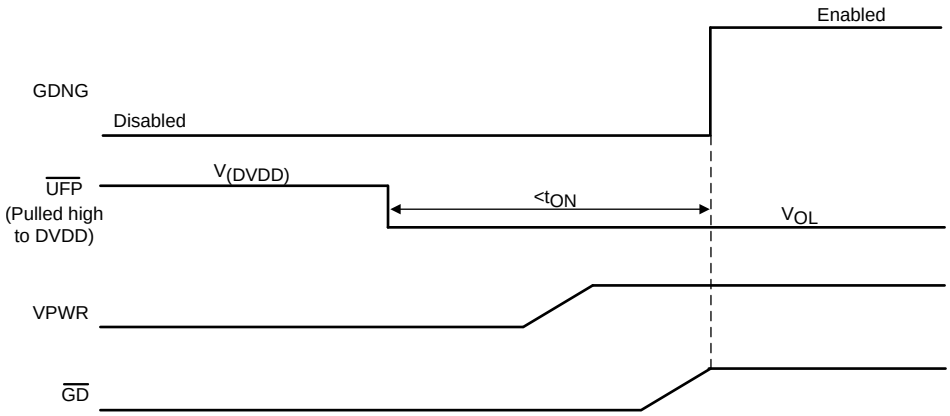
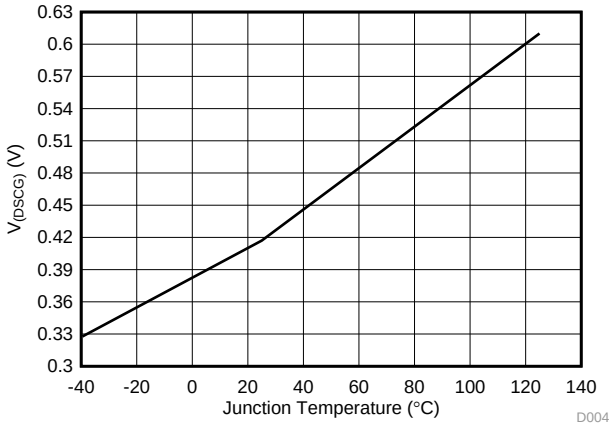


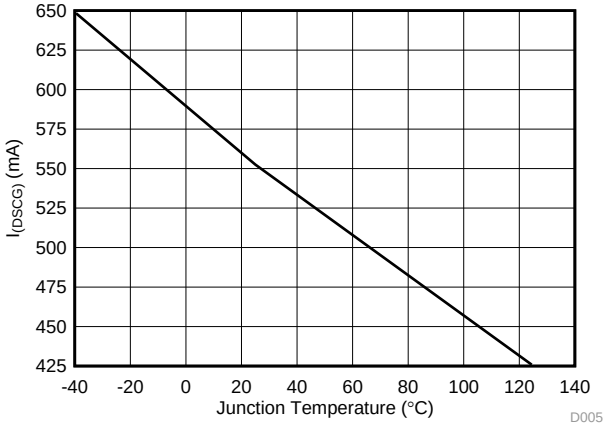
Figure 6. Timing Illustration for t_{ON}

7.8 Typical Characteristics



$I_{(DSCG)}$ = 100 mA

Figure 7. $V_{(DSCG)}$ while $V_{(VPWR)}$ > 4.65 V after an unplug



$V_{(DSCG)}$ = 4 V Pulsed Testing

Figure 8. $I_{(DSCG)}$ while $V_{(VPWR)}$ > 4.65 V after an unplug

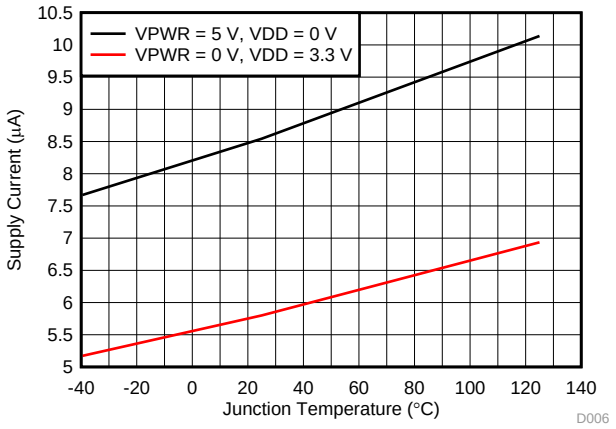


Figure 9. Supply Current While CC pins Unattached

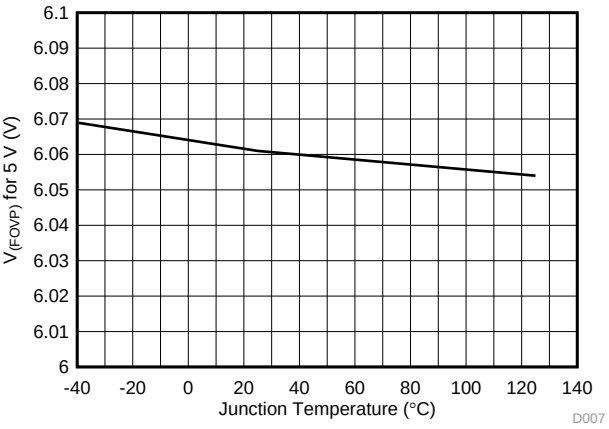


Figure 10. $V_{(FOVP)}$ While Supplying 5 V

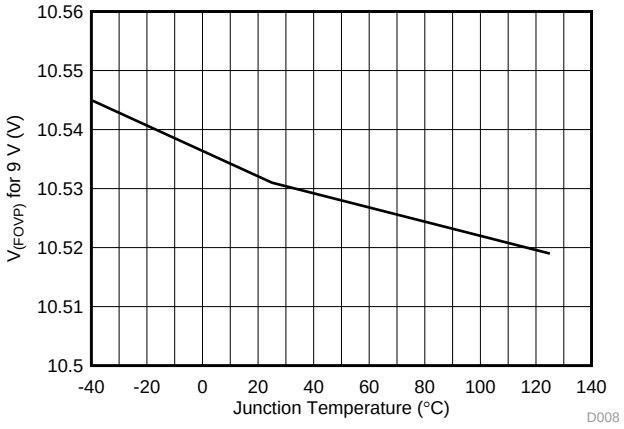


Figure 11. $V_{(FOVP)}$ While Supplying 9 V

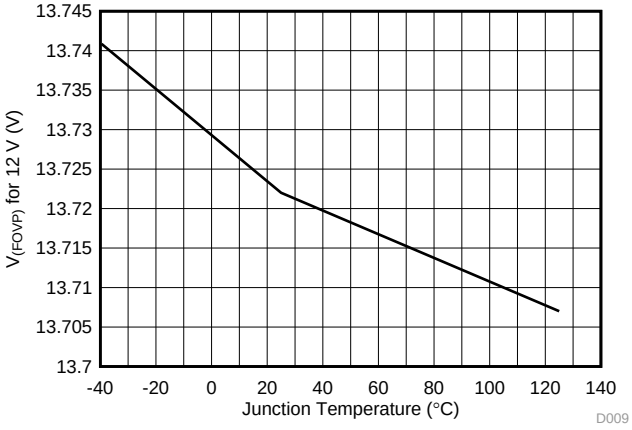


Figure 12. $V_{(FOVP)}$ While Supplying 12 V

Typical Characteristics (continued)

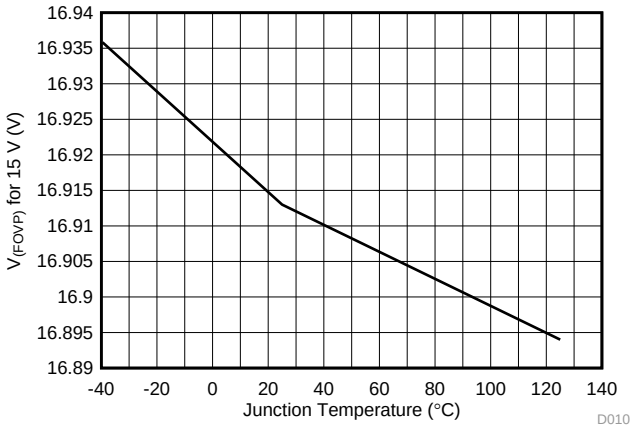


Figure 13. $V_{(FOVP)}$ While Supplying 15 V

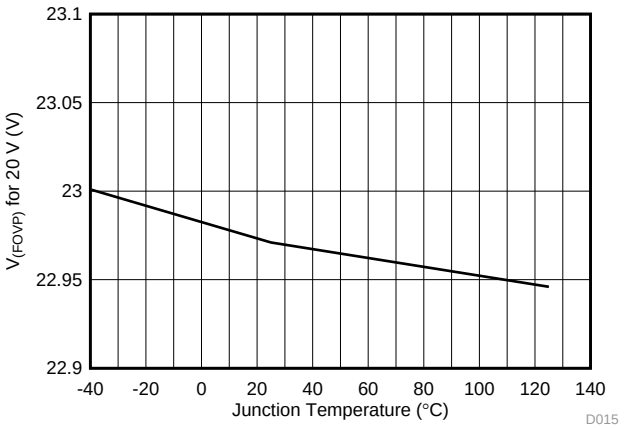
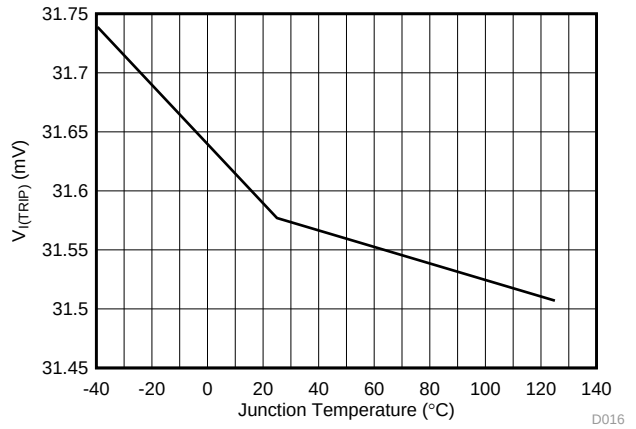
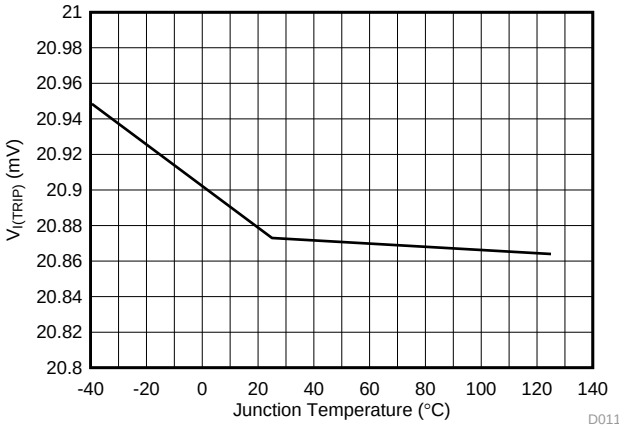


Figure 14. $V_{(FOVP)}$ While Supplying 20 V



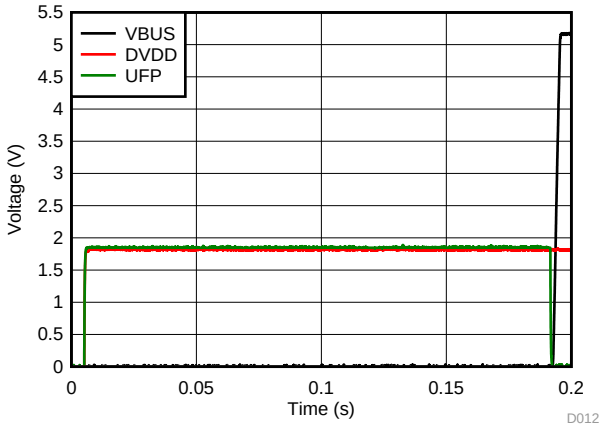
5 A enabled

Figure 15. $V_{I(TRIP)}$ When $V_{(VPWR)}$ > 4.65 V



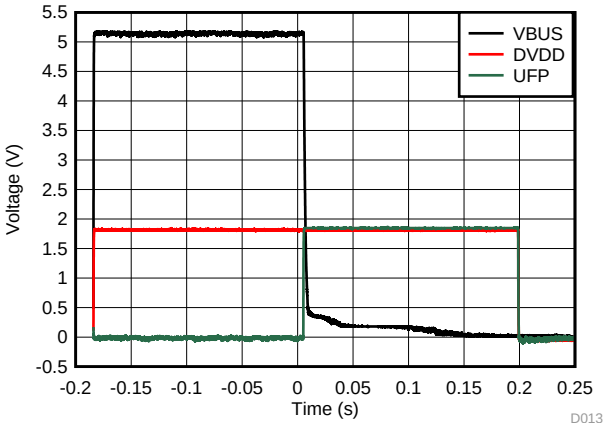
3 A enabled

Figure 16. $V_{I(TRIP)}$ When $V_{(VPWR)}$ > 4.65 V



Sink attached at time 0
$\overline{\text{UFP}}$ pulled up to DVDD

Figure 17. DVDD and $\overline{\text{UFP}}$ Upon Sink Attachment



Sink detached at time 0s
Sleep mode entered at time 0.19s.
$\overline{\text{UFP}}$ pulled up to DVDD

Figure 18. DVDD and $\overline{\text{UFP}}$ Upon Sink Attachment

8 Detailed Description

8.1 Overview

The TPS25740 or TPS25740A and supporting circuits perform the functions required to implement a USB Power Delivery (PD) 2.0 as a provider-only and a USB Type-C revision 1.2 source. It uses its CC pins to detect the attachment of a sinking device or upward facing port (UFP) and to determine which of CC1 or CC2 is connected to the CC wire of the cable. It then communicates over the CC wire in the cable bundle using USB PD to offer a set of voltages and currents. USB PD is a technology that utilizes the ubiquitous USB communications and hardware infrastructure to extend the amount of power available to devices from the 7.5 W range for USB BC1.2 to as high as 100 W in a dock. It is a compatible overlay to USB 2.0 and USB 3.0, coexisting with the existing 5 V powered universe of devices by use of adapter cables. Some basic characteristics of this technology relevant to the device include:

- Increased power achieved by providing higher current and/or higher voltage.
- New 3 A cable and 5 A connector to support greater than the traditional 1.5 A.
  - Cables have controlled voltage drop
- Voltages greater than 5 V are negotiated between PD partners.
  - Standard 5 V is always the default source voltage.
  - Voltage and current provisions are negotiated between PD partners.
- PD partners negotiate over the CC line to avoid conflict with existing signaling (that is, D+, D-)
- Layered communication protocol defined including PHY, Protocol Layer, Policy Engine, and Device Policy Manager all implemented within the device.
- The Type-C connector standard implements pre-powerup signaling to determine:
  - Connector orientation
  - Source 5-V capability
  - Detect through connection of a UFP (upward facing port) to a DFP (downward facing port).
  - Detection of when the connected UFP is disconnected. VBUS is unpowered until a through-connection is present

Figure 19 and Figure 20 show a typical configuration for the device.

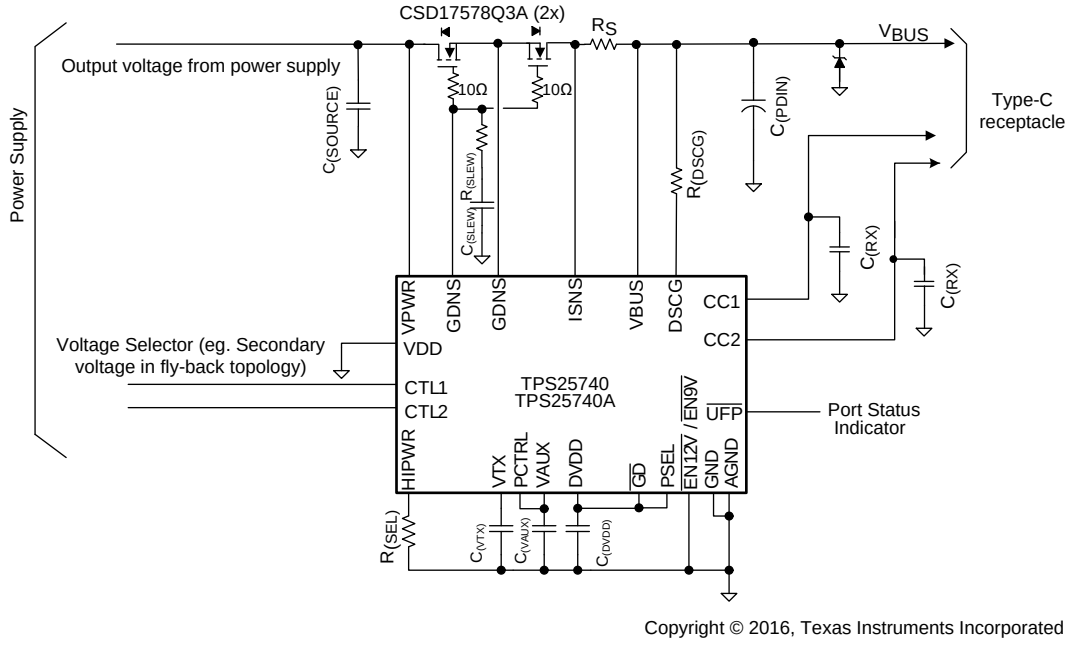


Figure 19. Schematic 1

Overview (continued)

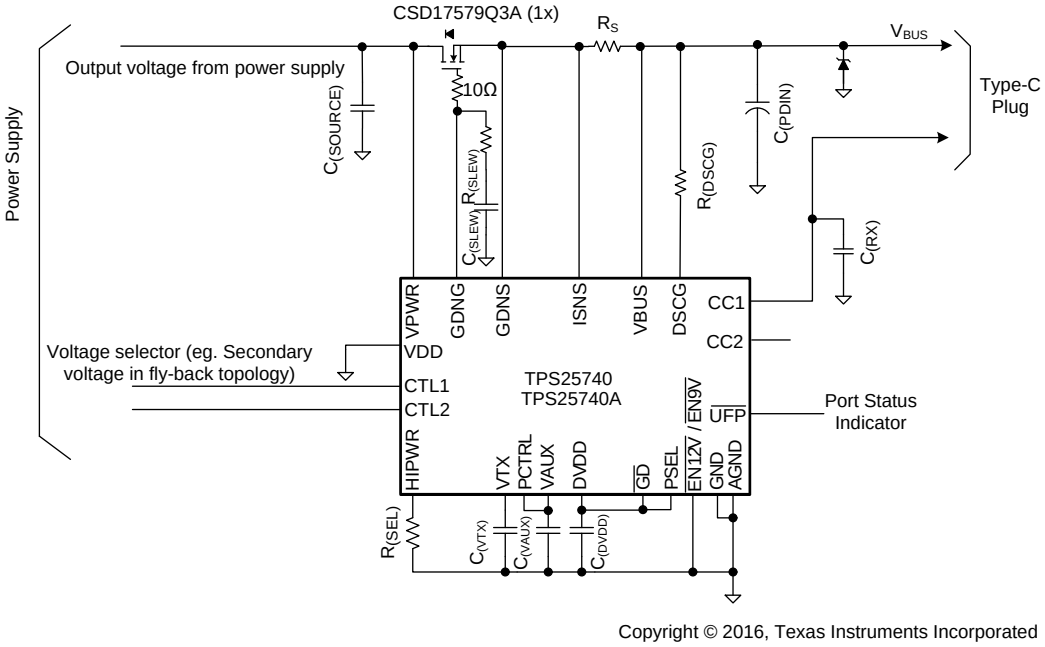


Figure 20. Schematic 2

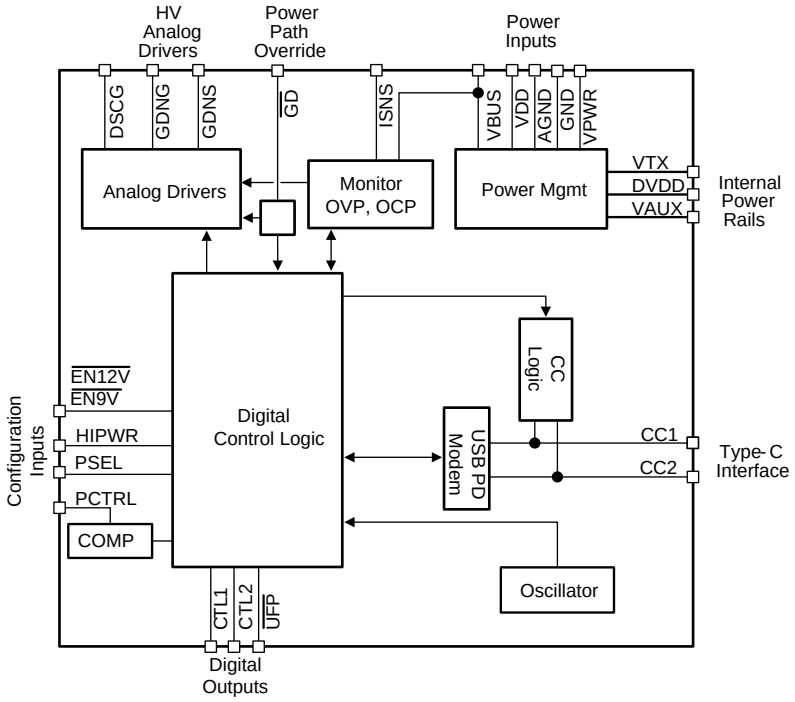
8.1.1 VBUS Capacitance

The USB Type-C specification requires that the capacitance on the VBUS pin of an empty receptacle be below 10 µF. This is to protect legacy USB sources that are not designed to handle the larger inrush capacitance and which may be connected via an A-to-C cable. For applications with USB Type-C receptacles and large bulk capacitance, this means back-to-back blocking FETs are required as shown in Figure 19. However, for applications with a USB Type-C plug (that is, a captive cable) this requirement does not apply since an adaptor cable with a USB Type-C receptacle and a Type-A plug is not defined or allowed by the USB I/F. Figure 20 is a schematic for such applications.

8.1.2 USB Data Communications

The USB Power Delivery specification requires that sources such as the device advertise in the source capabilities messages they transmit whether or not they are in a product that supports USB data communications. The device is designed for systems without data communication, so it has this bit hard-coded to 0.

8.2 Functional Block Diagram



8.3 Feature Description

This section describes the features associated with each pin for the TPS25740 and TPS25740A.

8.3.1 USB Type-C CC Logic (CC1, CC2)

The device uses a current source to implement the pull up resistance USB Type-C requires for Sources. While waiting for a valid connection, the device applies a default pullup of $I_{(RPSTD)}$. A sink attachment is detected when the voltage on one (not both) of the CC pins remains between $V_{(RDSTD)}$ and $V_{(DSTD)}$ for t_{CcDeb} and the voltage on the VBUS pin is below $V_{(VBUS\_FTH)}$. Then after turning on VBUS and disabling the Rp current source for the CCx pin not connected through the cable, the device applies $I_{(RP3.0)}$ to advertise 3 A to non-PD sinks. Finally, if it is determined that the attached sink is PD-capable, the device applies $I_{(RP1.5)}$. During this sequence if the voltage on the monitored CC pin exceeds the detach threshold then the device removes VBUS and begins watching for a sink attachment again.

The TPS25740 or TPS25740A digital logic selects the current source switch as illustrated in Figure 21. The schematic shown is replicated for each CC pin.

Feature Description (continued)

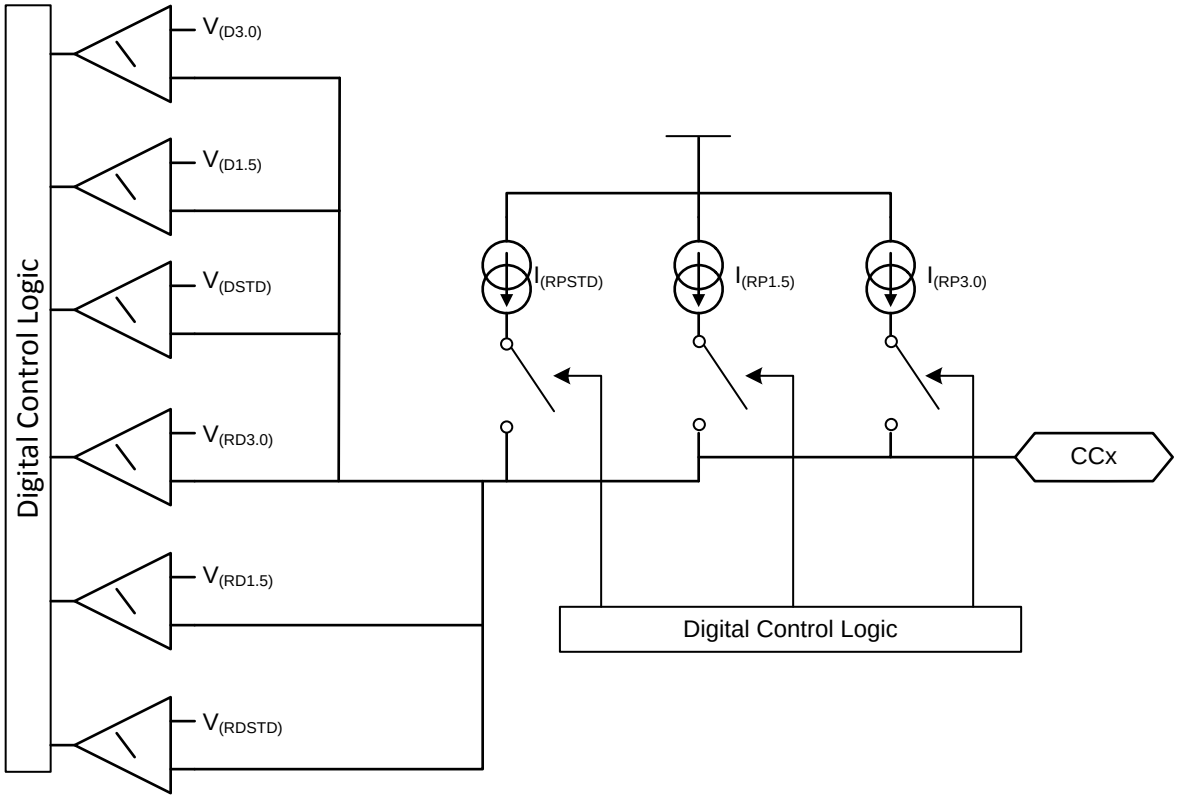


Figure 21. USB Type-C Rp Current Sources and Detection Comparators

If the voltage on both CC pins remains above $V_{(RDSTD)}$ for t_{CcDeb}, then the TPS25740 or TPS25740A goes to the sleep mode. In the sleep mode a less accurate current source is applied and a less accurate comparator watches for attachment (see $V_{(WAKE)}$, and $I_{(DSDFP)}$).

8.3.2 USB PD BMC Transmission (CC1, CC2, VTX)

An example of the BMC signal, specifically the end of the preamble and beginning of start-of-packet (SOP) is shown below. There is always an edge at the end of each bit or unit interval, and ones have an edge half way through the unit interval.

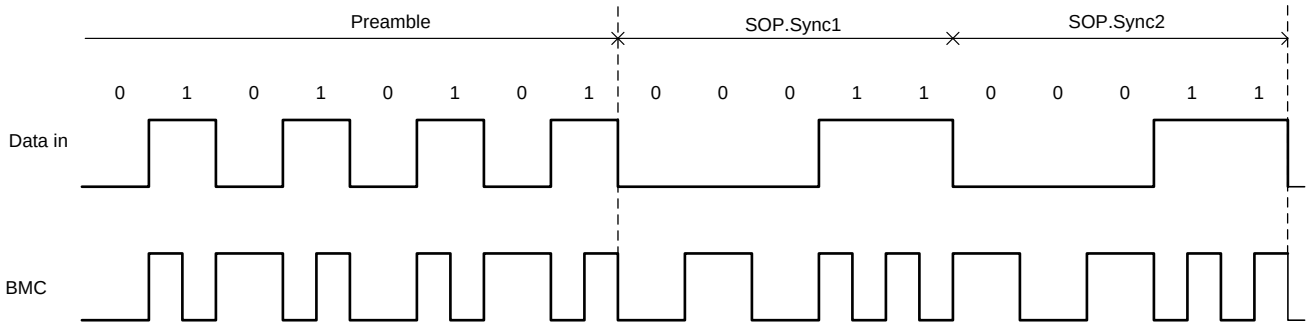


Figure 22. BMC Encoded End of Preamble, Beginning of SOP

Feature Description (continued)

While engaging in USB PD communications, the TPS25740 or TPS25740A is applying $I_{(RP1.5)}$ or $I_{(RP3.0)}$, so the CC line has a DC voltage of 0.918 V or 1.68 V, respectively. When the BMC signal is transmitted on the CC line, the transmitter overrides this DC voltage as shown in Figure 23. The transmitter bias rail (VTX) is internally generated and may not be used for any other purpose in the system. The VTX pin is only high while the TPS25740 or TPS25740A is transmitting a USB PD message.

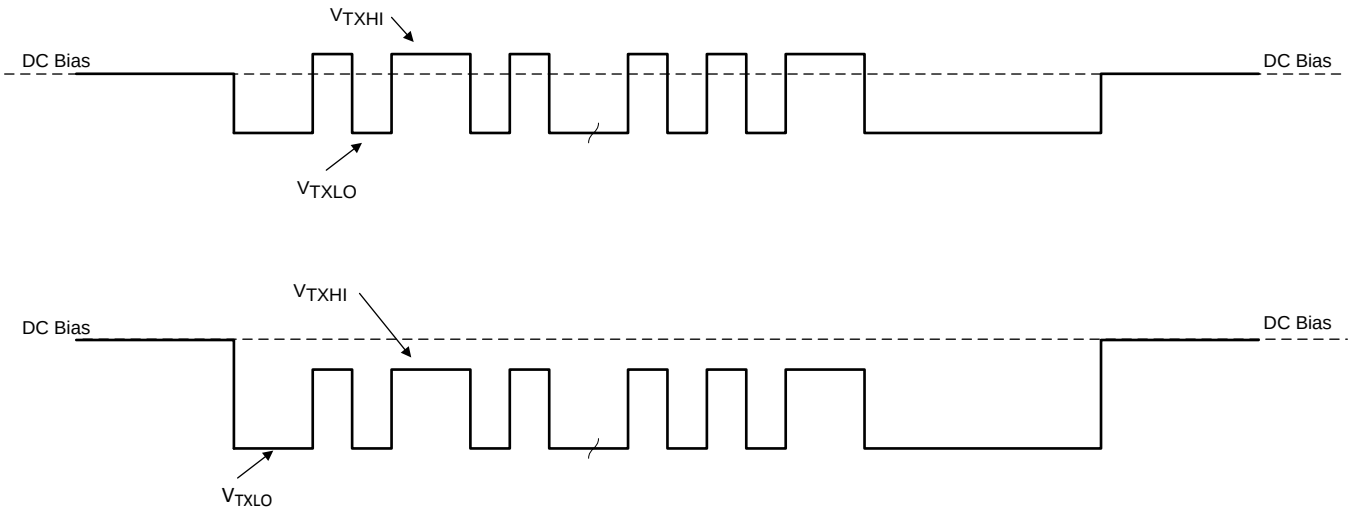


Figure 23. USB PD BMC Transmission on the CC Line

The device transmissions meet the eye diagram USB PD requirements (refer to USB PD in 文档支持) across the recommended temperature range. Figure 24 shows the transmitter schematic.

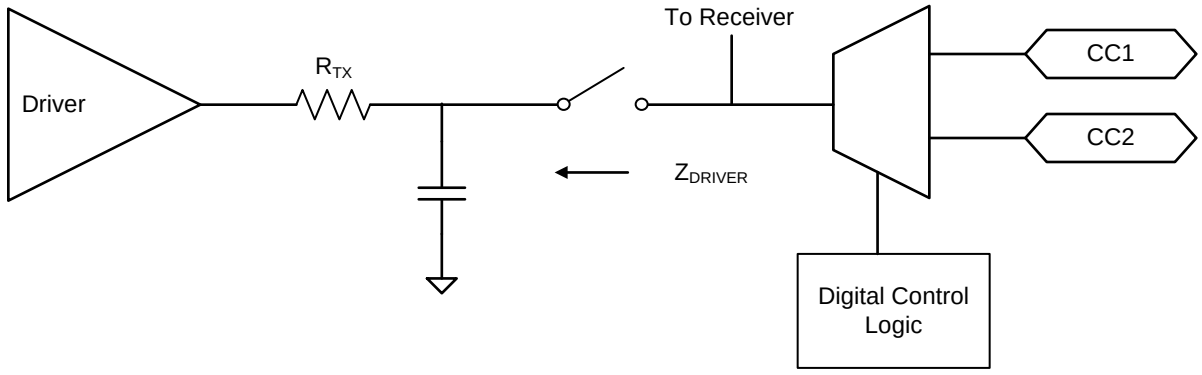


Figure 24. USB PD BMC Transmitter Schematic

The transmit eye diagram shown in Figure 26 was measured using the test load shown in Figure 25 with a C_{LOAD} within the allowed range. The total capacitance C_{LOAD} is computed as:

$$C_{LOAD} = C_{(RX)} + C_{CablePlug} \times 2 + Ca + C_{Receiver} \quad (1)$$

Where:

- 200 pF < $C_{(RX)}$ < 600 pF
- $C_{CablePlug}$ < 25 pF
- Ca < 625 pF
- 200 pF < $C_{Receiver}$ < 600 pF

Therefore, 400 pF < C_{LOAD} < 1850 pF.

Feature Description (continued)

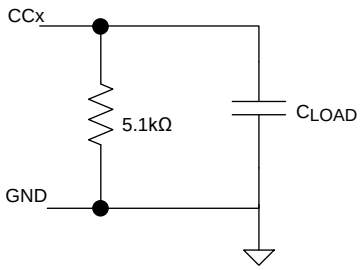


Figure 25. Test Load for BMC Transmitter

Figure 26 shows the transmit eye diagram for the TPS25740 and TPS25740A.

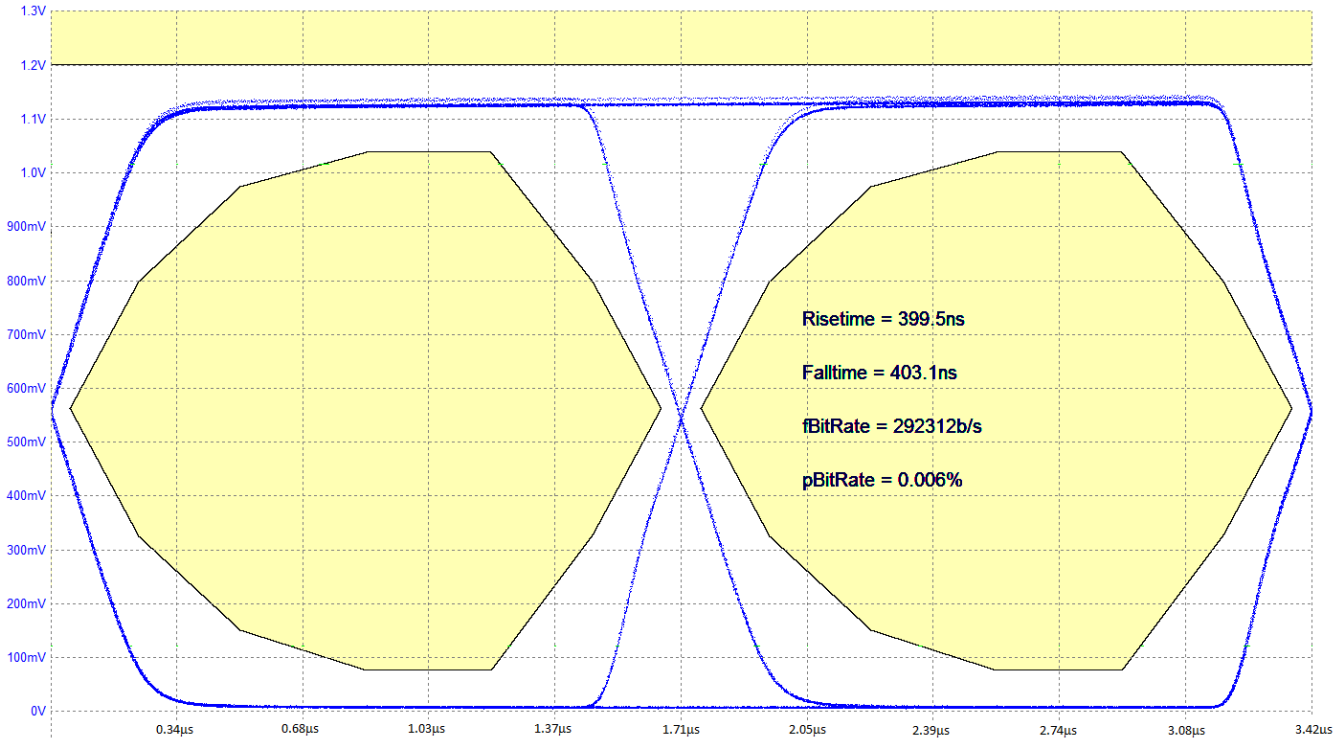


Figure 26. Transmit Eye Diagram (BMC)

Feature Description (continued)

8.3.3 USB PD BMC Reception (CC1, CC2)

The TPS25740 or TPS25740A BMC receiver follows the USB PD requirements (refer to USB PD in 文档支持) using the schematic shown in Figure 27.

The device low-pass filter design and receiver threshold design allows it to reject interference that may couple onto the CC line from a noisy VBUS power supply or any other source (refer to $V_{(INT)}$).

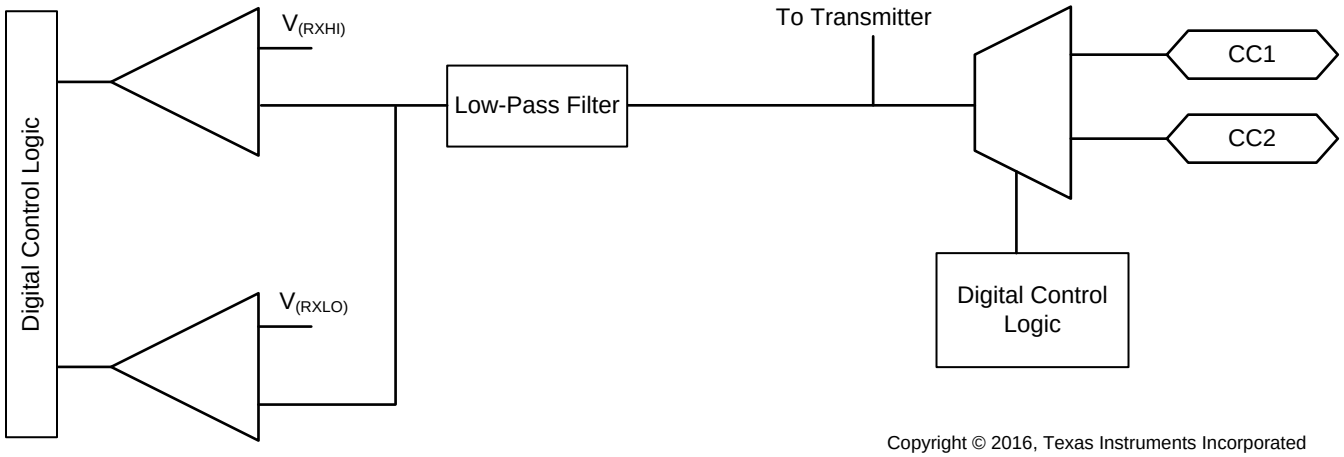


Figure 27. USB PD BMC Receiver Schematic

8.3.4 Discharging (DSCG, VPWR)

The DSCG pin allows for two different pull-downs that are used to apply different discharging strengths. In addition, the VPWR pin is used to apply a load to discharge the power supply bulk capacitance.

If too much power is dissipated by the device (that is, the T_{J1} temperature is exceeded) an OTSD occurs that disables the discharge FET; therefore, an external resistor is recommended in series with the DSCG pin to absorb most of the dissipated power. The external resistor $R_{(DSCG)}$ should be chosen such that the current sunk by the DSCG pin does not exceed $I_{(DSCGT)}$.

The VPWR pin should always be connected to the supply side (as opposed to the connector side) of the power-path switch (Figure 28 shows one example). This pin is monitored before enabling the GDNG gate driver to apply the voltage to the VBUS pin of the connector.

From sink attachment, and while the device has not finalized a USB PD contract, the device applies $R_{(DSCGB)}$.

Also from sink attachment, and while the device has not finalized a USB PD contract, the device draws $I_{(SUPP)}$ through the VPWR pin even if VDD is above its UVLO. This helps to discharge the power supply source.

Feature Description (continued)

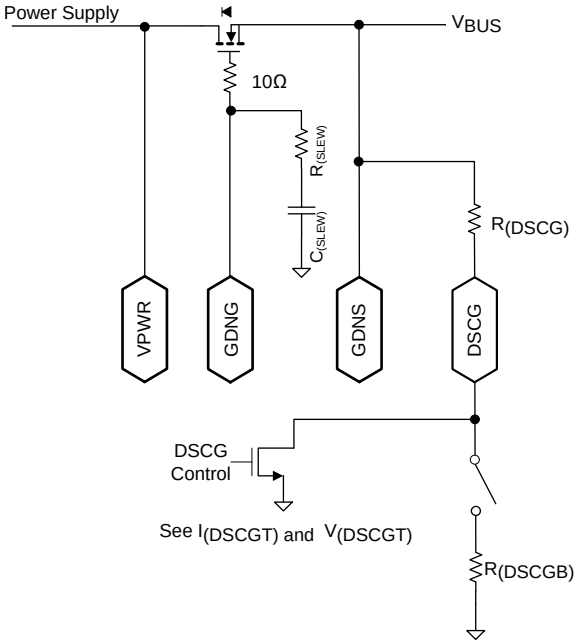


Figure 28. Discharge Schematic

The discharge procedure used in the TPS25740 or TPS25740A is intended to allow the DSCG pin to help pull the power supply down from high voltage, and then also pull VBUS at the connector down to the required level (refer to USB PD in 文档支持).

8.3.4.1 Discharging after a Fault (VPWR)

There are two types of faults that cause the TPS25740 or TPS25740A to begin a full discharge of VBUS: Slow-shutdown faults and fast-shutdown faults. When a slow-shutdown fault occurs, the device does not disable GDNG until after VBUS is measured below $V_{(SOVP)}$ for a 5V contract. When a fast-shutdown fault occurs, the device disables GDNG immediately and then discharges the connector side of the power-path. In both cases, the bleed discharge is applied to the DSCG pin and $I_{(SUPP)}$ is drawn from the VPWR

Slow-shutdown faults that do not include transmitting a hard reset:

- Receiving a Hard Reset signal (25 ms < $t_{ShutdownDelay}$ < 35 ms)
- Cable is unplugged ($t_{ShutdownDelay}$ < 20 µs)

Slow-shutdown faults that include transmitting hard reset (25 ms < $t_{ShutdownDelay}$ < 35 ms)

- T_J exceeds T_{J1} (an overtemperature event)
- Low voltage alarm occurring outside of a voltage transition
- High voltage alarm occurring outside of a voltage transition (but not high enough to cause OVP)
- Receiving an unexpected PD message during a voltage transition
- Failure of power supply to transition voltages within required time of 600 ms ($t_{PSTransition}$ (refer to USB PD in 文档支持).
- A Soft Reset USB PD message is not acknowledged or Accepted (refer to USB PD in 文档支持).
- A Request USB PD message is not received in the required time (refer to USB PD in 文档支持).
- Failure to discharge down to 0.725 V after a fault of any kind.

Feature Description (continued)

Fast-shutdown faults (hard reset always sent):

- Fast OVP event occurring at any time.
- OCP event occurring at any time starting from the transmission of the first USB PD message.
  - VBUS falling below $V_{(VBUS\_FTH)}$ is treated as an OCP event.
- $\overline{GD}$ falling edge

The DSCG pin is used to discharge the supply line after a slow-shutdown fault occurs. Figure 29 illustrates the signals involved. Depending on the specific slow-shutdown fault the time $t_{ShutdownDelay}$ in Figure 29 is different as indicated in the list above. If the slow-shutdown fault triggers a hard reset, it is sent at the beginning of the $t_{ShutdownDelay}$ period. However, the device behavior after the time $t_{ShutdownDelay}$ is the same for all slow-shutdown faults. After the $t_{ShutdownDelay}$ period, the device sets CTL1 and CTL2 to select 5 V from the power supply and puts the DSCG pin into its ON state (Full Discharge). This discharging continues until the voltage on the VBUS pin reaches $V_{(SOVP)}$ for a 5-V contract. The device then disables GDNG and again puts the DSCG pin into its ON state. This discharging state lasts until the voltage on VBUS reaches 0.725 V (nominal). If the discharge does not complete within 650 ms, then the device sends a Hard Reset signal and the process repeats. In Figure 29, the times labeled as $t_{20\rightarrow5}$ and $t_{5\rightarrow0}$ can vary, they depend on the size of the capacitance to be discharged and the size of the external resistor between the DSCG pin and VBUS. The time labeled as t_S is a function of how quickly the NFET opens.

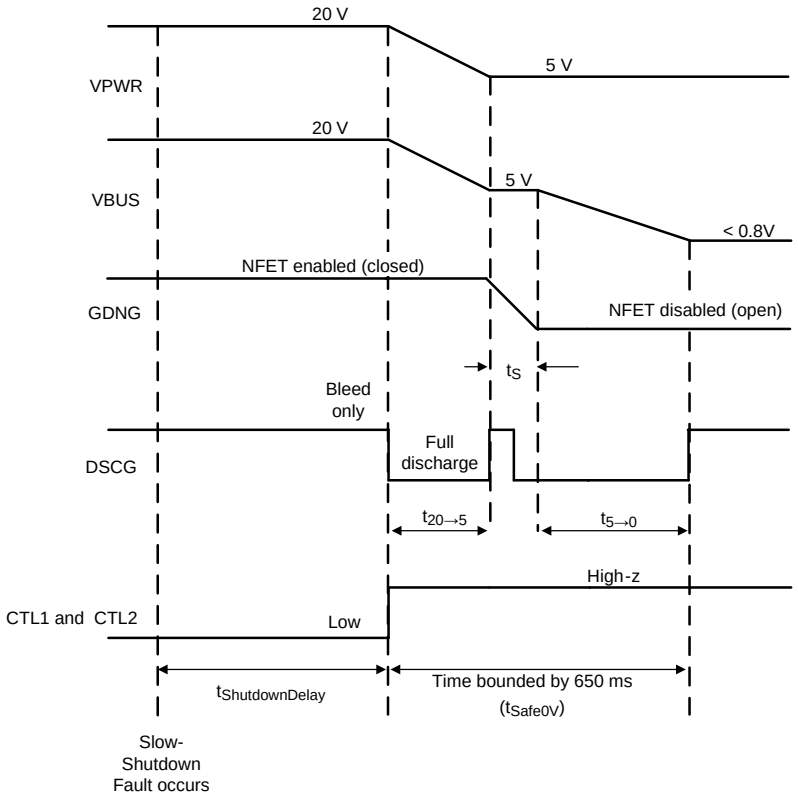


Figure 29. Illustration of Slow-Shutdown VBUS Discharge

Figure 30 illustrates a similar discharge procedure for fast-shutdown faults. The main difference from Figure 29 is that the NFET is opened immediately. It is assumed for the purposes of this illustration that the power supply output capacitance (that is, $C_{(SOURCE)}$ in the reference schematics shown in Figure 19 and Figure 20) is not discharged by the power supply itself, but the VPWR pin is bleeding current from that capacitance. The VPWR pin then draws $I_{(SUPP)}$ after GDNG disables the external NFET. So, as shown in the figure, the VPWR voltage discharges slowly, while the VBUS pin is discharged once the full discharge is enabled. If the voltage on the VPWR pin takes longer than $t_{20\rightarrow5}$ + $t_{5\rightarrow0}$ + 0.765s to discharge below $V_{(FOVP)}$, then it causes an OVP event and the process repeats.

Feature Description (continued)

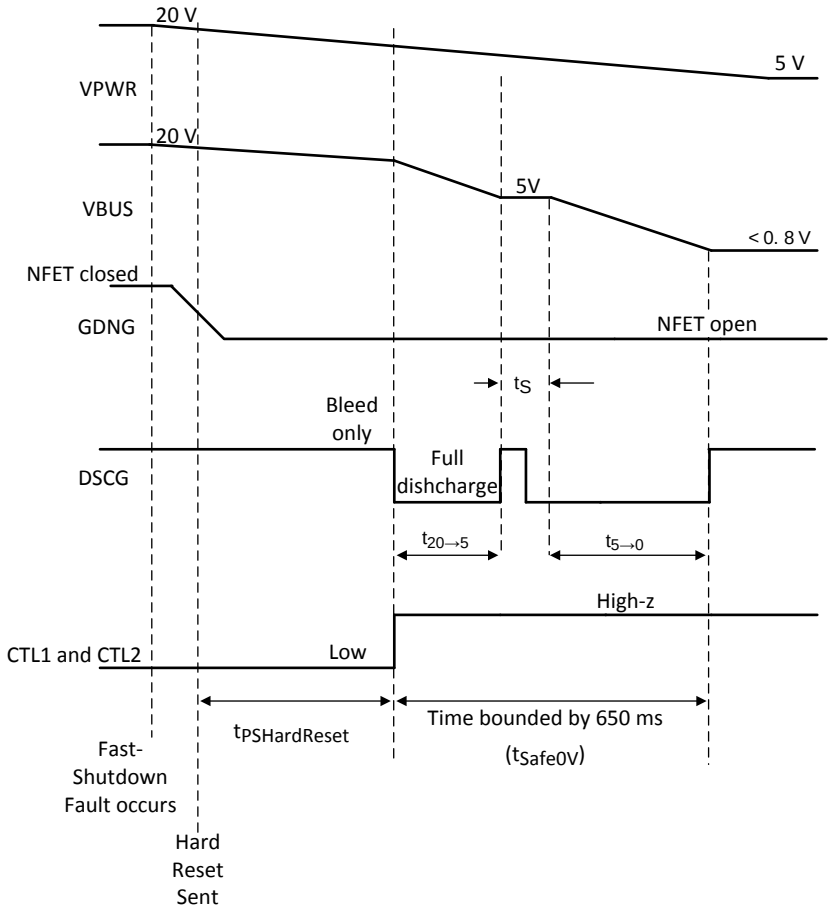


Figure 30. Illustration of Fast-Shutdown Discharge

If the discharge does not complete successfully it is treated as a slow-shutdown fault, and the TPS25740 or TPS25740A repeats the discharge procedure until it does complete successfully. Once the discharge completes successfully as described above (that is, VBUS on connector is below 0.725 V), the device waits for 0.765 s (nominal) before trying to source VBUS again.

8.3.5 Configuring Voltage Capabilities (HIPWR, $\overline{\text{EN9V}}$, $\overline{\text{EN12V}}$)

The voltages advertised to USB PD-capable sinks can be configured to one of four different sets. The $\overline{\text{EN9V}}$, or $\overline{\text{EN12V}}$ pin is not envisioned to be changed dynamically in the system, so changing its state does not trigger sending source capabilities. However, the TPS25740A checks the status of the pin each time before it sends a source capabilities message using USB PD. Note that changing the state of the PCTRL pin forces capabilities to be re-transmitted. The device reads the HIPWR pin after a reset and latches the result.

Table 1. Voltage Programming (TPS25740)

$\overline{\text{EN12V}}$ PIN	HIPWR PIN	VOLTAGES ADVERTISED via USB PD [V]
Low	Connected to DVDD or GND directly	5, 12, 20
Low	Connected to DVDD or GND via $R_{(SEL)}$	5, 12
High	Connected to DVDD or GND directly	5, 20
High	Connected to DVDD or GND via $R_{(SEL)}$	5

Table 2. Voltage Programming (TPS25740A)

$\overline{EN9V}$ PIN	HIPWR PIN	VOLTAGES ADVERTISED via USB PD [V]
Low	Connected to DVDD or GND directly	5, 9, 15
Low	Connected to DVDD or GND via $R_{(SEL)}$	5, 9
High	Connected to DVDD or GND directly	5, 15
High	Connected to DVDD or GND via $R_{(SEL)}$	5

8.3.6 Configuring Power Capabilities (PSEL, PCTRL, HIPWR)

The power advertised to non-PD Type-C Sinks is always 15 W. However, the TPS25740 or TPS25740A only advertises Type-C default current until it debounces the Sink attachment for t_{CcDeb} and the VBUS voltage has been given t_{VP} to stabilize.

The device does not communicate with the cable to determine its capabilities. Therefore, unless the device is in a system with a captive cable able to support 5 A, the HIPWR pin should be used to limit the advertised current to 3 A.

PCTRL is an input pin used to control how much of the maximum allowed power the port will advertise. This pin may be changed dynamically in the system and the device automatically updates any existing USB PD contract. If the PCTRL pin is pulled below $V_{(PCTRL\_TH),}$ then the source capabilities offers half of the maximum power specified by the PSEL pin.

The devices read the PSEL and HIPWR pins after a reset and latches the result, but the PCTRL pin is read dynamically by the device and if its state changes new capabilities are calculated and then transmitted.

While USB PD allows advertising a power of 100 W, UL certification for Class 2 power units (UL 1310) requires the maximum power remain below 100 W. The TPS25740 only advertises up to 4.65 A for a 20-V contract, this allows the V_{BUS} overshoot to reach 21.5 V as allowed by USB PD while remaining within the UL certification limits. Therefore, the TPS25740 allows delivering 100 W of power without adding additional voltage tolerance constraints on the power supply.

The PSEL pin offers four possible maximum power settings, but the devices can actually advertise more power settings depending upon the state of the HIPWR and PCTRL pins. Table 3 summarizes the four maximum power settings that are available via PSEL, again note this is not necessarily the maximum power that is advertised.

Table 3. PSEL Configurations

Maximum Power (PSEL) [W]	PSEL
$P_{(SEL)}$ = 36	Direct to GND
$P_{(SEL)}$ = 45	DVDD via $R_{(SEL)}$
$P_{(SEL)}$= 65	GND via $R_{(SEL)}$
$P_{(SEL)}$ = 93	Direct to DVDD

Equation 2 provides a quick reference which applies to both TPS25740 and TPS25740A to see how the HIPWR, PSEL and PCTRL pins affect what current is advertised with each voltage in the source capabilities message:

$$Ix = \min\left(\frac{P\max}{V\max}, I\max\right) \quad (2)$$

Where:

- For a voltage Vx, the advertised current is Ix
- If the PCTRL pin is low, then Pmax = $P_{(SEL)}$ / 2
- If the PCTRL pin is high, then Pmax = $P_{(SEL)}$.
- If the HIPWR pin is pulled high, then Imax = 3 A.
- If the HIPWR pin is pulled low, then Imax = 5 A.

Table 4 and Table 5 provide a comprehensive list of the currents and voltages that are advertised for each voltage.

Table 4. Maximum Current Advertised in the Power Data Object for a Given Voltage (TPS25740)

PSEL	VOLTAGE [V]	HIPWR	MAXIMUM CURRENT PCTRL = LOW [A]	MAXIMUM CURRENT PCTRL = HIGH [A]
Direct to GND	5	Max = 3 A DVDD through $R_{(SEL)}$ or Direct to DVDD	3	3
DVDD via $R_{(SEL)}$			3	3
GND via $R_{(SEL)}$			3	3
Direct to DVDD			3	3
Direct to GND	12		1.5	3
DVDD via $R_{(SEL)}$			1.87	3
GND via $R_{(SEL)}$			2.7	3
Direct to DVDD			3	3
Direct to GND	20	Max = 3 A Direct to DVDD	0.9	1.8
DVDD via $R_{(SEL)}$			1.12	2.24
GND via $R_{(SEL)}$			1.62	3
Direct to DVDD			2.32	3
Direct to GND	5	Max = 5 A GND through $R_{(SEL)}$ or Direct to GND	3.6	5
DVDD via $R_{(SEL)}$			4.5	5
GND via $R_{(SEL)}$			5	5
Direct to DVDD			5	5
Direct to GND	12		1.5	3
DVDD via $R_{(SEL)}$			1.87	3.74
GND via $R_{(SEL)}$			2.7	5
Direct to DVDD			4.16	5
Direct to GND	20	Max = 5 A Direct to GND	0.9	1.8
DVDD via $R_{(SEL)}$			1.12	2.24
GND via $R_{(SEL)}$			1.62	3.24
Direct to DVDD			2.32	4.64

Table 5. Maximum Current Advertised in the Power Data Object for a Given Voltage (TPS25740A)

PSEL	VOLTAGE [V]	HIPWR	MAXIMUM CURRENT PCTRL = LOW [A]	MAXIMUM CURRENT PCTRL = HIGH [A]
Direct to GND	5	Max = 3 A DVDD through $R_{(SEL)}$ or Direct to DVDD	3	3
DVDD via $R_{(SEL)}$			3	3
GND via $R_{(SEL)}$			3	3
Direct to DVDD			3	3
Direct to GND	9		2	3
DVDD via $R_{(SEL)}$			2.5	3
GND via $R_{(SEL)}$			3	3
Direct to DVDD			3	3
Direct to GND	15	Max = 3 A Direct to DVDD	1.2	2.4
DVDD via $R_{(SEL)}$			1.5	3
GND via$R_{(SEL)}$			2.17	3
Direct to DVDD			3	3

Table 5. Maximum Current Advertised in the Power Data Object for a Given Voltage (TPS25740A) (continued)

PSEL	VOLTAGE [V]	HIPWR	MAXIMUM CURRENT PCTRL = LOW [A]	MAXIMUM CURRENT PCTRL = HIGH [A]
Direct to GND	5	Max = 5 A GND through $R_{(SEL)}$ or Direct to GND	3.6	5
DVDD via $R_{(SEL)}$			4.5	5
GND via $R_{(SEL)}$			5	5
Direct to DVDD			5	5
Direct to GND	9		2	4
DVDD via $R_{(SEL)}$			2.5	5
GND via $R_{(SEL)}$			3.61	5
Direct to DVDD			5	5
Direct to GND	15	Max = 5 A Direct to GND	1.2	2.4
DVDD via $R_{(SEL)}$			1.5	3
GND via $R_{(SEL)}$			2.17	4.34
Direct to DVDD			3.1	5

8.3.7 Gate Driver (GDNG, GDNS)

The GDNG and GDNS pins may control a single NFET or back-to-back NFETs in a common-source configuration. The GDNS is used to sense the voltage so that the voltage differential between the pins is maintained.

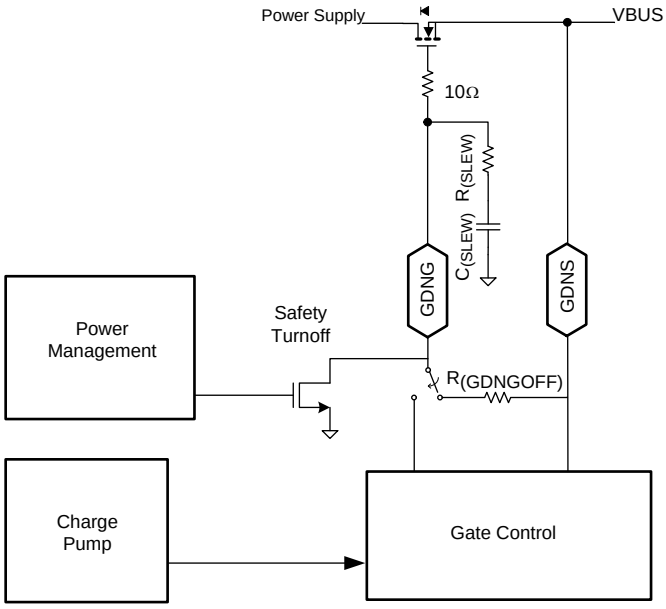


Figure 31. GDNG/GDNS Gate Control

8.3.8 Fault Monitoring and Protection

8.3.8.1 Over/Under Voltage (VBUS)

The TPS25740 or TPS25740A uses the VBUS pin to monitor for overvoltage or undervoltage conditions and implement the fast-OVP, slow-OVP and slow-UVP features.

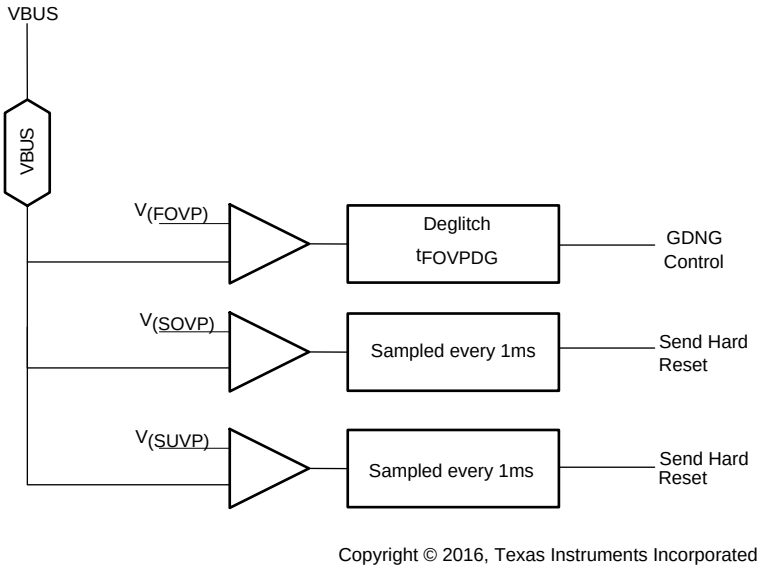


Figure 32. Voltage Monitoring Circuits

If an over-voltage condition is sensed by the Fast OVP mechanism, GDNG is disabled within t_{FOVP} + t_{FOVPDG}, then a Hard Reset is transmitted and the VBUS discharge sequence is started. At power up the voltage trip point is set to $V_{(FOVP)}$ (5 V contract). When a contract is negotiated the trip point is set to the corresponding $V_{(FOVP)}$ value.

The devices employ another slow over-voltage protection mechanism as well that sends the Hard Reset before disabling the external NFET. It catches many OV events before the Fast OVP mechanism. During intentional positive voltage transitions, this mechanism is disabled (see Figure 1). However, t_{VP} after the external NFET has been enabled, if the voltage on the VBUS pin exceeds $V_{(SOVP)}$ then a Hard Reset is transmitted to the Sink and the VBUS discharge sequence is started.

The devices employ a slow under-voltage protection mechanism as well that sends the Hard Reset before disabling GDNG. During intentional negative voltage transitions, this mechanism is disabled (see Figure 1). However, t_{VP} after the external NFET has been enabled if the voltage on the VBUS pin falls below $V_{(SUVP)}$, then a Hard Reset is transmitted to the Sink and the VBUS discharge sequence is started.

8.3.8.2 Over-Current Protection (ISNS, VBUS)

OCP protection is enabled t_{VP} after the voltage on the VBUS pin has exceeded $V_{(VBUS\_RTH)}$. Prior to OCP being enabled, the $\overline{GD}$ pin can be used to protect against a short.

The OCP protection circuit monitors the differential voltage across an external sense resistor to detect when the current outflow exceeds $V_{I(TRIP)}$ which in turn activates an over-current circuit breaker and disables the GDNG / GDNS gate driver. Once the OCP is enabled, if the voltage on the VBUS pin falls below $V_{(VBUS\_FTH)}$ then that is also treated like an OCP event.

Following the recommended implementation of a 5-mΩ sense resistor, when the device is configured to deliver 3 A (via HIPWR pin), the OCP threshold lies between 3.8 A and 4.5 A. When configured to deliver 5 A (via HIPWR pin), the OCP threshold lies between 5.8 A and 6.8 A. The resistance of the sense resistor may be tuned to adjust the current that causes $V_{I(TRIP)}$ to be exceeded.

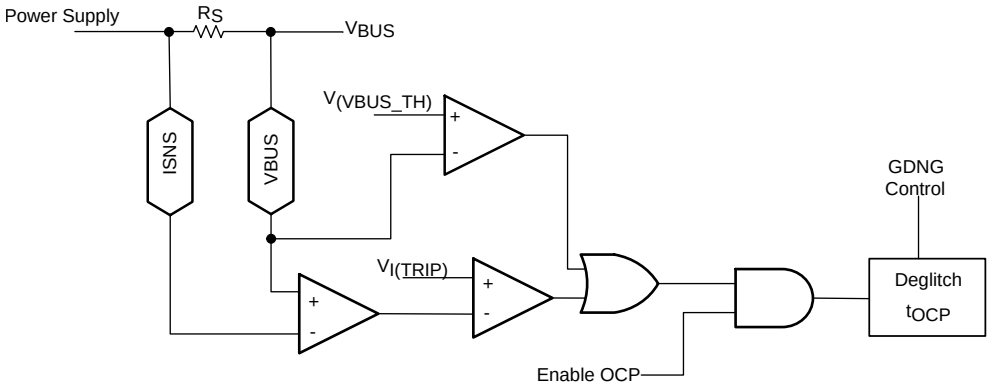


Figure 33. Overcurrent Protection Circuit, (ISNS, VBUS)

8.3.8.3 System Fault Input ($\overline{GD}$, VPWR)

The gate-driver disable pin provides a method of overriding the internal control of GDNG and GDNS. A falling edge on $\overline{GD}$ disables the gate driver within t_{GDoff}. If $\overline{GD}$ is held low after a sink is attached for 600 ms then a hard reset will be generated and the device sends a hard reset and go through its startup process again.

The $\overline{GD}$ input can be controlled by a voltage or current source. An internal voltage clamp is provided to limit the input voltage in current source applications. The clamp can safely conduct up to 80 µA and will remain high impedance up to 6.5 V before clamping

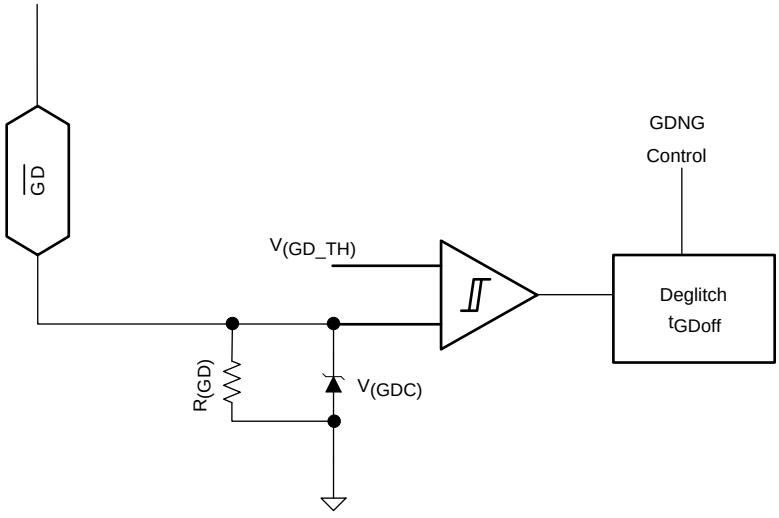


Figure 34. Overcurrent Protection Circuit, ($\overline{GD}$)

If the VPWR pin remains below its falling UVLO threshold ($V_{(VPWR\_TH)}$) for more than 600 ms after a sink is attached then the devices consider it a fault and will not enable GDNG. If the VPWR pin is between the rising and falling UVLO threshold, the TPS25740/TPS25740A may enable GDNG and proceed with normal operations. However, after GDNG is enabled, if the VBUS pin does not rise above its UVLO within 190 ms the devices consider it a fast-shutdown fault and disables GDNG. Therefore, in order to ensure USB Type-C compliance and normal operation, the VPWR pin must be above its rising UVLO threshold ($V_{(VPWR\_TH)}$) within 275 ms of when $\overline{UFP}$ is pulled low and the VBUS pin must be above $V_{(VBUS\_RTH)}$ within 190 ms of GDNG being enabled.

8.3.9 Voltage Control (CTL1, CTL2)

CTL1 and CTL2 are open-drain output pins used to control an external power supply as summarized in Table 6. Depending upon the voltage requested by the sink, the device sets the CTL pins accordingly. No current flows into the pin in its high-z state.

Table 6. States of CTL1 and CTL2 as a Function of Target Voltage on VBUS for TPS25740

VOLTAGE CONTAINED in PDO REQUESTED by UFP	CTL2 STATE	CTL1 STATE
5V	High-z	High-z
9 V (TPS25740A)	Low	High-z
12 V (TPS25740)	Low	High-z
15 V (TPS25740A)	Low	Low
20 V (TPS25740)	Low	Low

8.3.10 Sink Attachment Indicator ($\overline{\text{UFP}}$, DVDD)

$\overline{\text{UFP}}$ is an open-drain output pin used to indicate the status of the port. It is high-z unless a sink is attached to the port, in which case it is pulled low. A sink attachment is detected when the voltage on one (not both) of the CC pins remains between $V_{(RDSTD)}$ and $V_{(DSTD)}$ for t_{CcDeb} and the voltage on the VBUS pin is below $V_{(VBUS\_FTH)}$. After being pulled low, $\overline{\text{UFP}}$ remains low until the sink has been removed for t_{CcDeb}.

DVDD is a power supply pin that is high-z until a sink or debug accessory or audio accessory is attached, in which case it is pulled high. Therefore, it can be used as a sink attachment indicator that is active high.

8.3.11 Power Supplies (VAUX, VDD, VPWR, DVDD)

The VAUX pin is the output of a linear regulator and the input supply for internal power management circuitry. The VAUX regulator draws power from VDD after establishing a USB PD contract unless it is not available in which case it draws from VPWR. Changes in supply voltages will result in seamless switching between supplies.

If there is a load on the DVDD pin, that current will be drawn from the VPWR pin unless the device has stabilized into a USB PD contract or VPWR is below its UVLO.

The device cannot function properly until VPWR is above its UVLO. However, for improved system efficiency when $\overline{\text{UFP}}$ is high-z, VPWR can be low (the high voltage power supply can be disabled) if VDD is above its UVLO.

Connect VAUX to GND via the recommended bypass capacitor. Do not connect any external load that draws more than $I_{(VAUXEXT)}$. Locate the bypass capacitor close to the pin and provide a low impedance ground connection from the capacitor to the ground plane.

VDD should either be grounded or be fed by a low impedance path and have input bypass capacitance. Locate the bypass capacitors close to the VDD and VPWR pins and provide a low impedance ground connection from the capacitor to the ground plane.

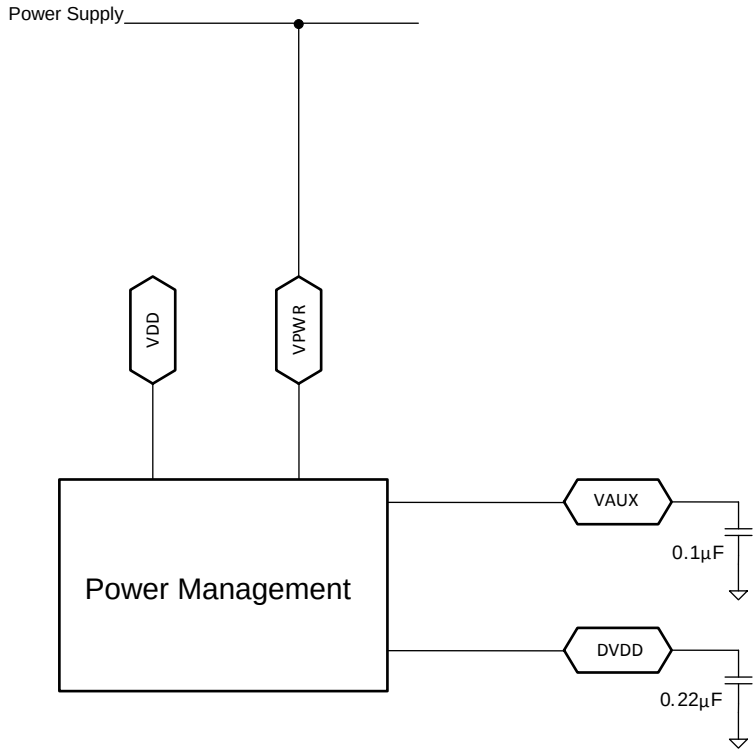


Figure 35. Power Management

8.3.12 Grounds (AGND, GND)

GND is the substrate ground of the die. Most circuits return to GND, but certain analog circuitry returns to AGND to reduce noise and offsets. The power pad (on those devices that possess one) is electrically connected to GND. Connect AGND, GND and the power pad (if present) to the ground plane through the shortest and most direct connections possible.

8.3.13 Output Power Supply (DVDD)

The DVDD pin is the output of an internal 1.85 V linear regulator, and the input supply for internal digital circuitry. This regulator normally draws power from VPWR until a USB PD contract has stabilized, but will seamlessly swap to drawing power from VDD in the event that VPWR drops below its UVLO threshold. External circuitry can draw up to 35 mA from DVDD. Note that as more power is drawn from the DVDD pin more heat is dissipated in the device, and if excessive the OTSD could be tripped which resets the device. Connect DVDD to GND via the recommended ceramic bypass capacitor.

The DVDD pin will only be high when a USB Type-C sink, or audio accessory, or debug accessory is attached, refer to Figure 17 and Figure 18.

Locate the bypass capacitor close to the pin and provide a low impedance ground connection from the capacitor to the ground plane.

8.4 Device Functional Modes

8.4.1 Sleep Mode

Many adaptors that include USB PD must consume low quiescent power to meet regulatory requirements (that is, “Green,” Energy Star, or such). The device supports the sleep mode to minimize power consumption when the receptacle or plug is unattached. The device enters sleep mode when there is no valid plug termination attached; a valid plug termination is defined as one of: sink, Audio accessory, or Debug accessory. If an active cable is attached but its far-end is left unconnected or “dangling,” then the device also enters sleep mode. It exits the sleep mode whenever the plug status changes, that could be a dangling cable being removed or a sink being connected.

8.4.2 Checking VBUS at Start Up

When first powered up, the device will not enable GDNG if the voltage on VBUS is already above its UVLO. This is a protective measure taken to avoid the possibility of turning on while connected to another active power supply in some non-compliant configuration.

This means that the VBUS pin must be connected between the power-path NFET and the USB connector. This also allows for a controlled discharge of VBUS all the way down to the required voltage on the connector (refer to USB PD in 文档支持).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS25740 or TPS25740A implements a fully compliant USB Power Delivery 2.0 provider and Type-C source (also known as downward facing port (DFP)). The device basic schematic diagram is shown in Figure 36. Subsequent sections describe detailed design procedures for several applications with differing requirements. The TPS25740/TPS25740A Design Calculator Tool (refer to the *文档支持*) is available for download and use in calculating the equations in the following sections.

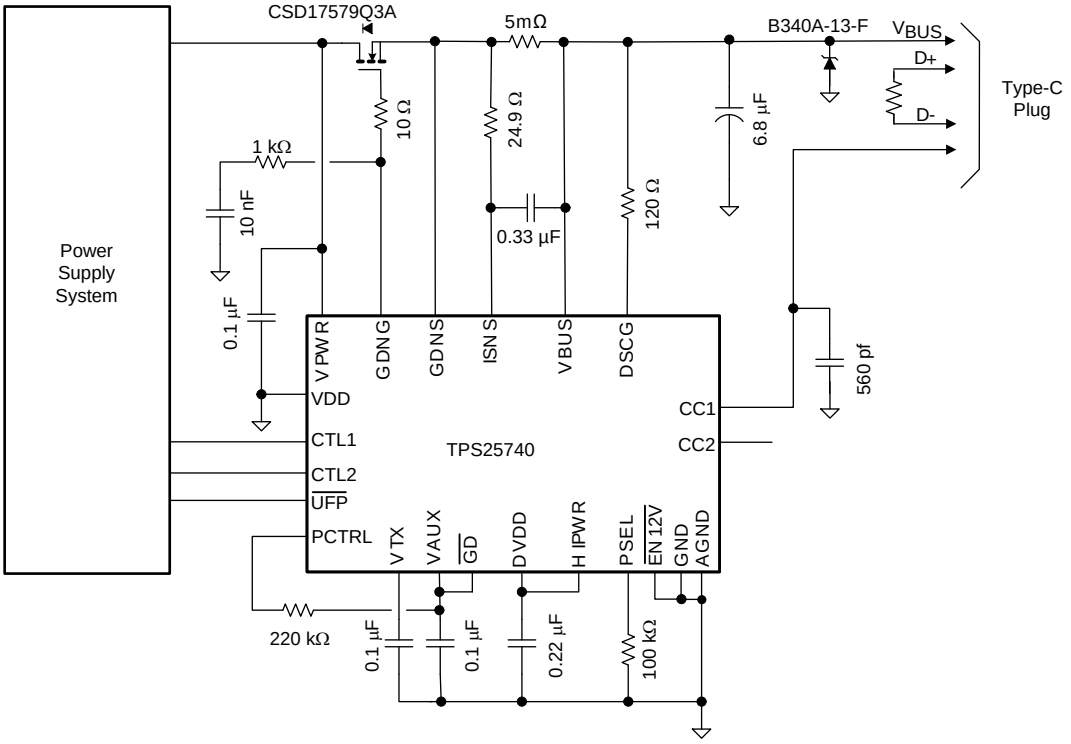


Figure 36. Basic Schematic Diagram ($P_{(SEL)}$ = 65 W at 5 V, 12 V, 20 V)

9.1.1 System-Level ESD Protection

System-level ESD (per EN61000-4-2) may occur as the result of a cable being plugged in, or a user touching the USB connector or cable. Figure 37 shows an example ESD protection for the VBUS path that helps protect the VBUS pin, ISNS and DSCG pins of the device from system-level ESD. The device has ESD protection built into the CC1 and CC2 pins so that no external protection is necessary. Refer to the *Layout Guidelines* section for external component placement and routing recommendations.

The Schottky diode is to protect against VBUS being drawn below ground by an inductive load, the cable inductance may be as high as 900 nH.

Application Information (continued)

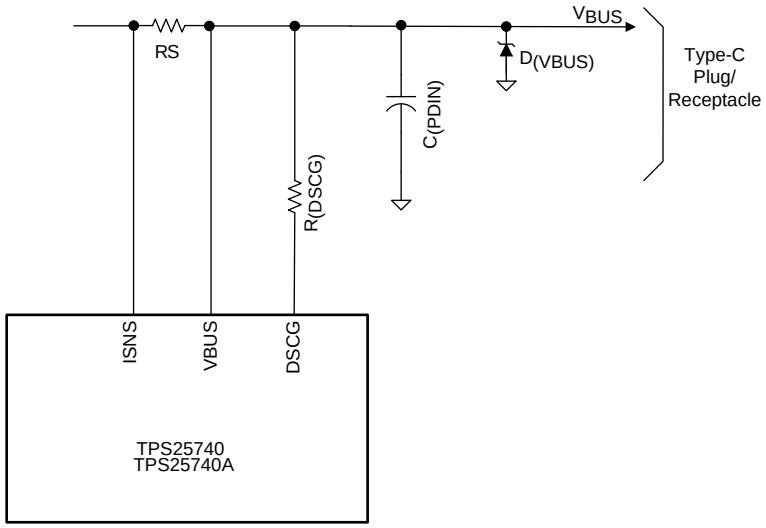


Figure 37. VBUS ESD Protection

9.1.2 Use of $\overline{GD}$ Internal Clamp

As described in the *Configuring Power Capabilities (PSEL, PCTRL, HIPWR)* section, the $\overline{GD}$ pin has an internal clamp. Figure 38 shows an example of how it may be used. V_{OUT} is the voltage from a power supply that is to be provided onto the VBUS wire of the USB Type-C cable through an NFET resistor. If V_{OUT} drops, the NFET should be automatically disabled by the device. This can be accomplished by tying the $\overline{GD}$ pin to V_{OUT} via a resistor.

The internal resistance of the $\overline{GD}$ pin is specified to exceed $R_{(GD)}$, and the input threshold is $V_{(GD\_TH)}$. The $\overline{GD}$ pin would therefore draw no more than $V_{(GD\_TH)\ max}$ / $R_{(GD)\ min}$ < 603 nA. As an example, assume the minimum value of V_{OUT} for which $\overline{GD}$ should be high is 4.5 V, then the resistor between $\overline{GD}$ and V_{OUT} may not exceed (4.5 – $V_{(GD\_TH)\ max}$) / 603e-9 = 4.5 MΩ. To make it robust against board leakage a smaller resistor such as 1 MΩ can be chosen, but the smaller the resistance the more leakage current into the $\overline{GD}$ pin. In this example, when V_{OUT} is 25 V, the current into the $\overline{GD}$ pin is (25-$V_{(GDC)}$) / 1e6 < 1.85 µA.

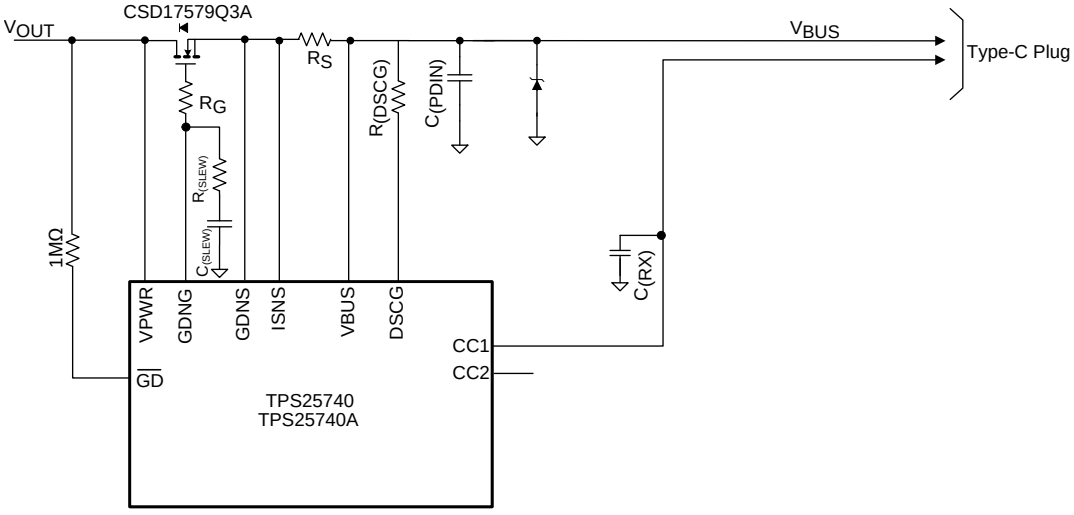


Figure 38. Use of $\overline{GD}$ Internal Clamp

Application Information (continued)

9.1.3 Resistor Divider on $\overline{GD}$ for Programmable Start Up

Figure 39 shows an alternative usage of the $\overline{GD}$ pin can help protect against shorts on the VBUS pin in the receptacle. A resistor divider is used to minimize the time it takes the $\overline{GD}$ pin to be pulled low. Consider the situation where the VBUS pin is shorted at startup. At some point, the device closes the NFET switch to supply 5 V to VBUS. At that point, the short pulls down on the voltage seen at the VPWR pin. With the resistor values shown in Figure 39, once the voltage at the VPWR pin reaches 3.95 V the voltage at the $\overline{GD}$ pin is specified to be below $V_{(GD\_TH)\ min}$. Without the 700-kΩ resistor, the voltage at the VPWR pin would have to reach $V_{(GD\_TH)\ min}$ which takes longer. This comes at the expense of increased leakage current.

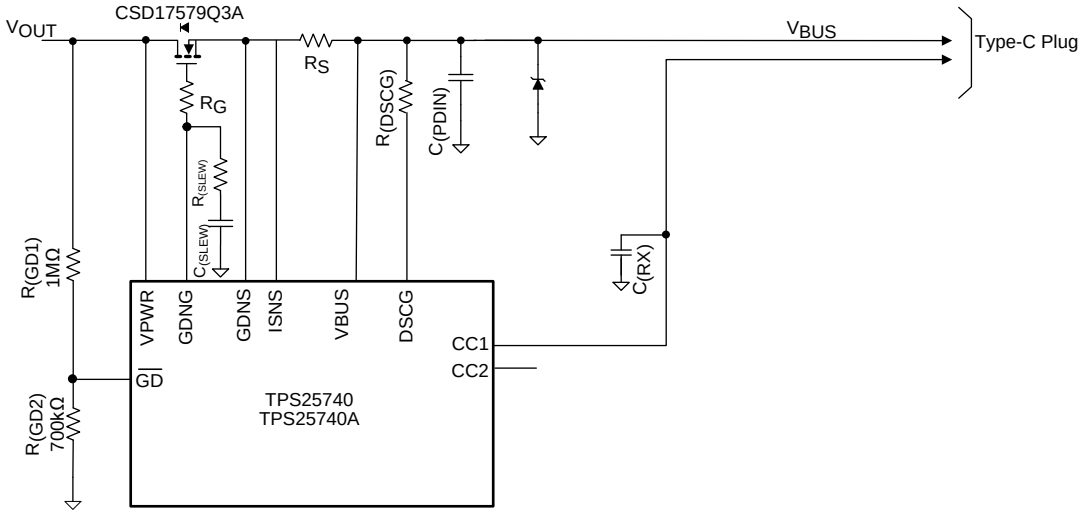


Figure 39. Programmable $\overline{GD}$ Turn On

The $\overline{GD}$ resistor values can be calculated using the following process. First, calculate the smallest $R_{(GD1)}$ that should be used to prevent the internal clamp current from exceeding $I_{(GD)}$ of 80 µA. For a 20 V advertised voltage, the OVP trip point could be as high as 24 V. Using $V_{(GDC)\ min}$ = 6.5 V and V_{OUT} = $V_{(FOVP20)\ max}$ = 24 V, provides Equation 3:

$$R_{(GD1)} > \frac{V_{(FOVP20)} - V_{(GDC)}}{I_{(GD)}} = \frac{24\ V - 6.5\ V}{80\ \mu A} = 219\ k\Omega \tag{3}$$

The actual clamping current is less than 80 µA as some current flows into $R_{(GD2)}$. Next, $R_{(GD2)}$ can be calculated as shown in Equation 4:

$$R_{(GD2)} < R_{(GD1)} \times \frac{V_{(GD\_TH)}}{V_{(VPWR)} - V_{(GD\_TH)}} \tag{4}$$

where

- $V_{(VPWR)}$ = $V_{(VPWR\_TH)}$ falling (max) and $V_{(GD\_TH)}$ = $V_{(GD\_TH)}$ falling (min).

9.1.4 Selection of the CTL1 and CTL2 Resistors ($R_{(FBL1)}$ and $R_{(FBL2)}$)

$R_{(FBL1)}$ and $R_{(FBL2)}$ provide a means to change the power supply output voltage when switched in by the CTL1 and CTL2 open drain outputs, respectively. When 12 V is requested by the UFP then CTL2 will go low and place $R_{(FBL2)}$ in parallel with $R_{(FBL)}$. When 20 V is requested by the UFP then CTL2 remains low and CTL1 goes low placing $R_{(FBL1)}$ in parallel with $R_{(FBL2)}$ and $R_{(FBL)}$.

Application Information (continued)

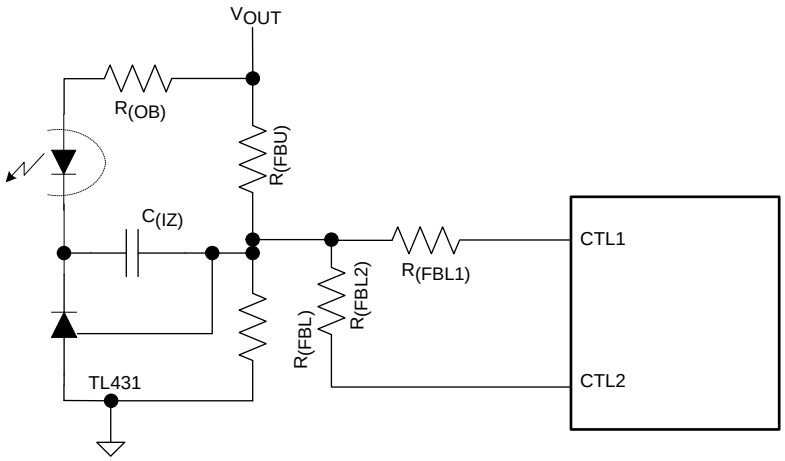


Figure 40. Circuit to Change V_{OUT} Upon Sink/UFP Request

$R_{(FBL2)}$ is calculated using Equation 5. In this example, V_{OUT12} is 12 V and V_{OUT20} is 20 V. V_{OUT} is the default output voltage (5 V) for the regulator and is set by $R_{(FBU)}$, $R_{(FBL)}$ and error amplifier V_{REF}.

$$R_{(FBL2)} = \frac{R_{(FBL)} \times R_{(FBU)} \times V_{REF}}{R_{(FBL)} \times \left(V_{OUT12} - V_{REF}\right) - R_{(FBU)} \times V_{REF}} \quad (5)$$

$R_{(FBL1)}$ is calculated using Equation 6 after a standard 1% value for $R_{(FBL2)}$ is chosen.

$$R_{(FBL1)} = \frac{\frac{R_{(FBL2)} \times R_{(FBL)}}{R_{(FBL2)} + R_{(FBL)}} \times R_{(FBU)} \times V_{REF}}{\frac{R_{(FBL2)} \times R_{(FBL)}}{R_{(FBL2)} + R_{(FBL)}} \times \left(V_{OUT20} - V_{REF}\right) - R_{(FBU)} \times V_{REF}} \quad (6)$$

$R_{(FBL1)}$ and $R_{(FBL2)}$ should be large enough so that the CTL1 and CTL2 sinking current is minimized (< 1 mA). The sinking current for CTL1 and CTL2 is V_{REF} / $R_{(FBL1)}$ and $V_{REF}/R_{(FBL2)}$ respectively.

9.1.5 Voltage Transition Requirements

During VBUS voltage transitions, the slew rate ($v_{SrcSlewPos}$) must be kept below 30 mV/µs in all portions of the waveform, settle ($t_{SrcSettle}$) in less than 275 ms, and be ready ($t_{SrcReady}$) in less than 285 ms. For most power supplies, these requirements are met naturally without any special circuitry but in some cases, the voltage transition ramp rate must be slowed in order to meet the slew rate requirement.

The requirements for linear voltage transitions are shown in Table 7. In all cases, the minimum slew time is below 1 ms.

Table 7. Minimum Slew-Rate Requirements

Voltage Transition	5 V ↔ 12 V	5 V ↔ 20 V	12 V ↔ 20 V	5 V ↔ 9 V	5 V ↔ 15 V	9 V ↔ 15 V
Minimum Slew Time	233 µs	500 µs	267 µs	133 µs	333 µs	200 µs

When transition slew control is required, the interaction of the slew mechanism and dc/dc converter loop response must be considered. A simple R-C filter between the device CTL pins and converter feedback node may lead to instability under some conditions. Figure 41 shows a method which manages the slew control without adding capacitance to the converter feedback node.

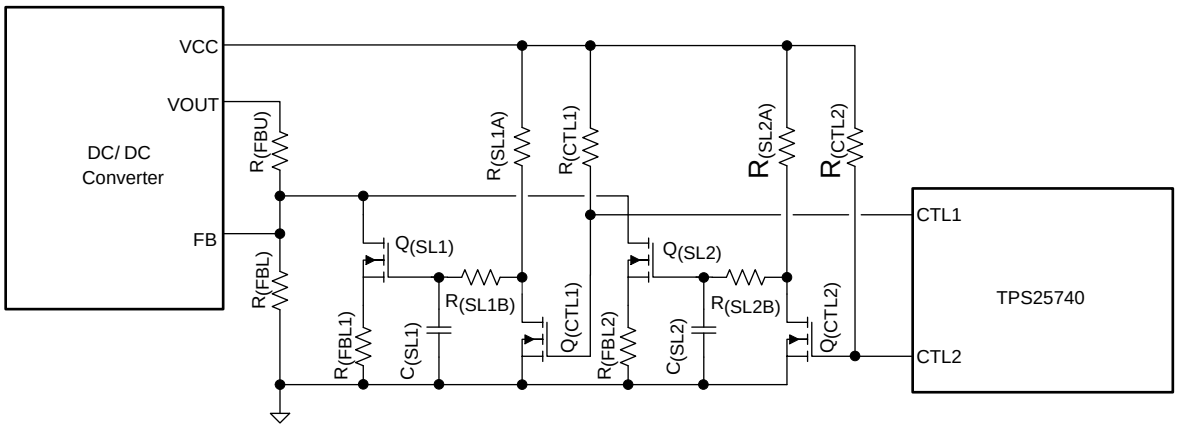


Figure 41. Slew-Rate Control Example No. 1

When V_{OUT} = 5 V, both CTL1 and CTL2 are in a high impedance state. When a 5 V to 12 V transition is requested, CTL2 goes low and turns off $Q_{(CTL2)}$. $Q_{(SL2)}$ gate starts to rise towards VCC at a rate determined by $R_{(SL2A)}$ + $R_{(SL2B)}$ and $C_{(SL2)}$. $Q_{(SL2)}$ gate continues to rise, until $Q_{(SL2)}$ is fully enhanced placing $R_{(FBL2)}$ in parallel with $R_{(FBL)}$. In similar fashion when $C_{(TL1)}$ goes low, $Q_{(CTL1)}$ turns off allowing $R_{(FBL1)}$ to slew in parallel with $R_{(FBL2)}$ and $R_{(FBL)}$.

The slewing resistors and capacitor can be chosen using the following equations. V_T is the VGS threshold voltage of $Q_{(SL1)}$ and $Q_{(SL2)}$. V_{REF} is the feedback regulator reference voltage. Choose the slewing resistance in the 100 kΩ range to reduce the loading on the bias voltage source (VCC) and then calculate $C_{(SL)}$. The falling transitions is shorter than the rising transitions in this topology.

Falling transitions:

- 20 V to 12 V

$$R_{(SL1B)} \times C_{(SL1)} = \frac{\Delta T_{20V-12V}}{\ln\left(\frac{V_T + V_{REF}}{V_{(VCC)}}\right) - \ln\left(\frac{V_T}{V_{(VCC)}}\right)} \quad (7)$$

- 12 V to 5 V

$$R_{(SL2B)} \times C_{(SL2)} = \frac{\Delta T_{12V-5V}}{\ln\left(\frac{V_T + V_{REF}}{V_{(VCC)}}\right) - \ln\left(\frac{V_T}{V_{(VCC)}}\right)} \quad (8)$$

Rising transitions:

- 5 V to 12 V

$$\left(R_{(SL2A)} + R_{(SL2B)}\right) \times C_{(SL2)} = \frac{\Delta T_{5V-12V}}{\ln\left(1 - \frac{V_T}{V_{(VCC)}}\right) - \ln\left(1 - \frac{V_T + V_{REF}}{V_{(VCC)}}\right)} \quad (9)$$

- 12 V to 20 V

$$\left(R_{(SL1A)} + R_{(SL1B)}\right) \times C_{(SL1)} = \frac{\Delta T_{12V-20V}}{\ln\left(1 - \frac{V_T}{V_{(VCC)}}\right) - \ln\left(1 - \frac{V_T + V_{REF}}{V_{(VCC)}}\right)} \quad (10)$$

Some converter regulators can tolerate a balance of capacitance on the feedback node without affecting loop stability. The LM5175 has been tested using Figure 42 to combine V_{OUT} slewing with a minimal amount of extra circuitry.

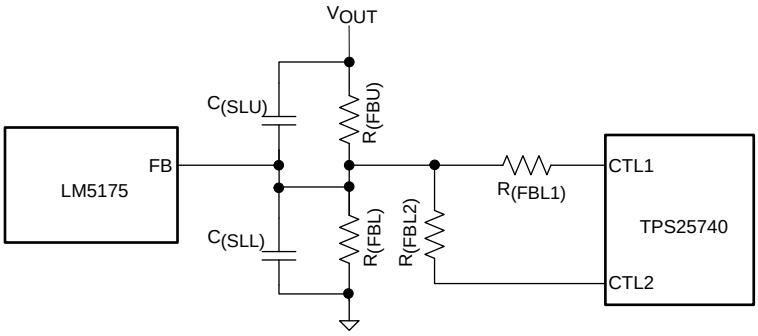


Figure 42. Slew-Rate Control Example No. 2

When a higher voltage is requested from TPS25740, CTL1 or CTL2 goes low changing the sensed voltage at the FB pin. The LM5175 compensates by increasing $C_{(SLU)}$. As V_{OUT} increases, $C_{(SLU)}$ is charged at a rate proportional to $R_{(FBU)}$. Three time constants yields a voltage change of approximately 95% and can be used to calculate the desired slew time. $C_{(SLU)}$ can be calculated using Equation 11 and Equation 12.

$$\Delta T_{(SLEW)} = 3 \times R_{(FBU)} \times C_{(SLU)} \tag{11}$$

$$C_{(SLU)} = \frac{\Delta T_{(SLEW)}}{3 \times R_{(FBU)}} \tag{12}$$

In order to minimize loop stability effects, a capacitor in parallel with $R_{(FBL)}$ is required. The ratio of $C_{(SLU)}/C_{(SLL)}$ should be chosen to match the ratio of $R_{(FBL)}/R_{(FBU)}$. Choose $C_{(SLL)}$ according to Equation 13.

$$C_{(SLL)} = C_{(SLU)} \times \frac{R_{(FBU)}}{R_{(FBL)}} \tag{13}$$

All slew rate control methods should be verified on the bench to ensure that the slew rate requirements are being met when the external VBUS capacitance is between 1 μF and 100 μF.

9.1.6 V_{BUS} Slew Control using GDNG $C_{(SLEW)}$

Care should be taken to control the slew rate of Q1 using $C_{(SLEW)}$; particularly in applications where C_{OUT} >> $C_{(SLEW)}$. The slew rate observed on VBUS when charging a purely capacitive load is the same as the slew rate of $V_{(GDNG)}$ and is dominated by the ratio $I_{(GDNON)}$ / $C_{(SLEW)}$. $R_{(SLEW)}$ helps block $C_{(SLEW)}$ from the GDNG pin enabling a faster transient response to OCP.

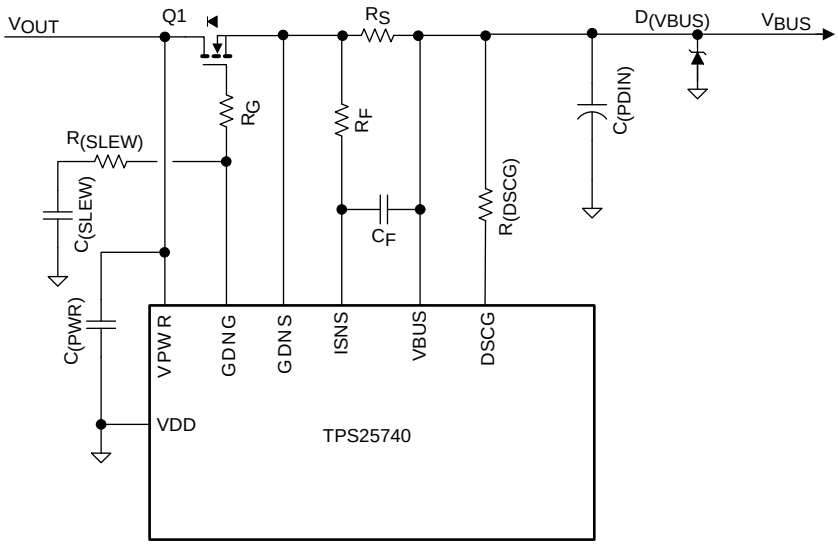


Figure 43. Slew-Rate control Using GDNG

There may be fault conditions where the voltage on VBUS triggers an OVP condition and then remains at a high voltage even after the TPS25740 configures the voltage source to output 5 V via CTL1 and CTL2. When this OVP occurs, the TPS25740 opens Q1 within t_{FOVP} + t_{FOVPDG}. The TPS25740 then issues a hard reset, discharge the power-path via the $R_{(DSCG)}$, and waits for 795 ms before enabling Q1 again. Due to the fault condition the voltage again triggers an OVP event when the voltage on VBUS exceeds $V_{(FOVP)}$. This retry process would continue as long as the fault condition persists, periodically pulsing up to $V_{(FOVP)}$ + $V_{SrcSlewPos}$ x (t_{FOVP} + t_{FOVPDG}) onto the VBUS of the Type-C receptacle. It is recommended to use a slew rate less than the maximum of $V_{SrcSlewPos}$ (30 mV / µs) allowed by USB (refer to 文档支持), the slew rate should instead be set in order to meet the requirement to have the voltage reach the target voltage within $t_{SrcSettle}$ (275 ms). This also limits the out-rush current from the C_{OUT} capacitor into the $C_{(PDIN)}$ capacitor and help protect Q1 and R_S.

9.1.7 Tuning OCP Using R_F and C_F

In applications where there are load transients or moderate ripple on V_{OUT}, the OCP performance of TPS25740 or TPS25740A may be impacted. Adding the R_F/C_F filter network as shown in Figure 44 helps mitigate the impact of the ripple and load transients on OCP performance.

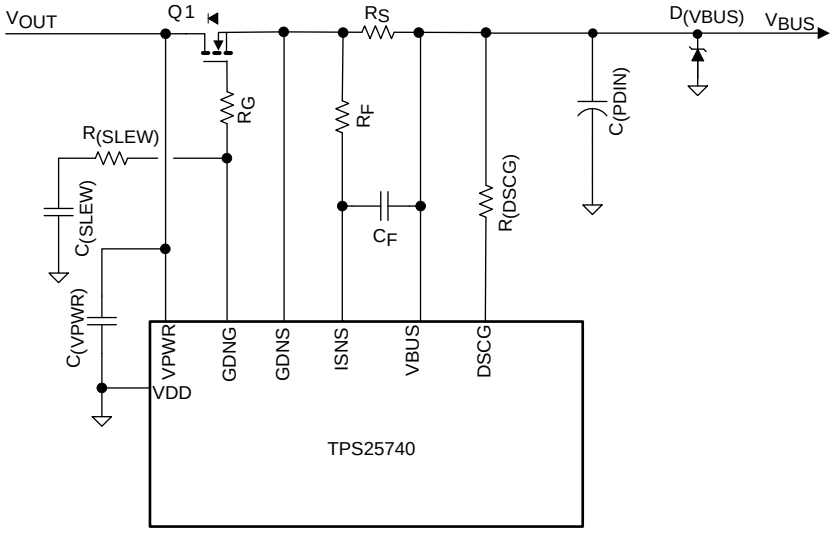


Figure 44. ISNS Filtering Example

R_F/C_F can be tailored to the amount of ripple on V_{OUT} as shown in Table 8.

Table 8. Ripple on V_{OUT}

Frequency x Ripple (kHz x V)	Suggested Filter Time Constant (µs)
< 5 (Ex: 50 mV ripple at 100 kHz)	None
5 to 15	2.2 µs (R_F = 10 Ω, C_F = 220 nF)
15 to 35	4.7 µs (R_F = 10 Ω, C_F = 470 nF)
35 to 105	10 µs (R_F = 10 Ω, C_F = 1 µF)

9.2 Typical Application , A/C Power Source (Wall Adapter)

In this design example, PSEL pin is configured so that $P_{(SEL)}$ = 65 W (see Table 9). Voltages offered are 5 V, 12 V, and 20 V at a maximum of 3 A. The overcurrent protection (OCP) trip point is set just above 3 A and VDD on the TPS25740 is grounded. The following example is based on PMP11451 and PMP11455, see www.ti.com/tool/PMP11451. In this design, the TPS25740 and some associated discretes are located on the paddle card (PMP11455) which plugs into the power supply card (PMP11451). This allows different paddle cards with different power and voltage advertisements to be used with a common power supply design.

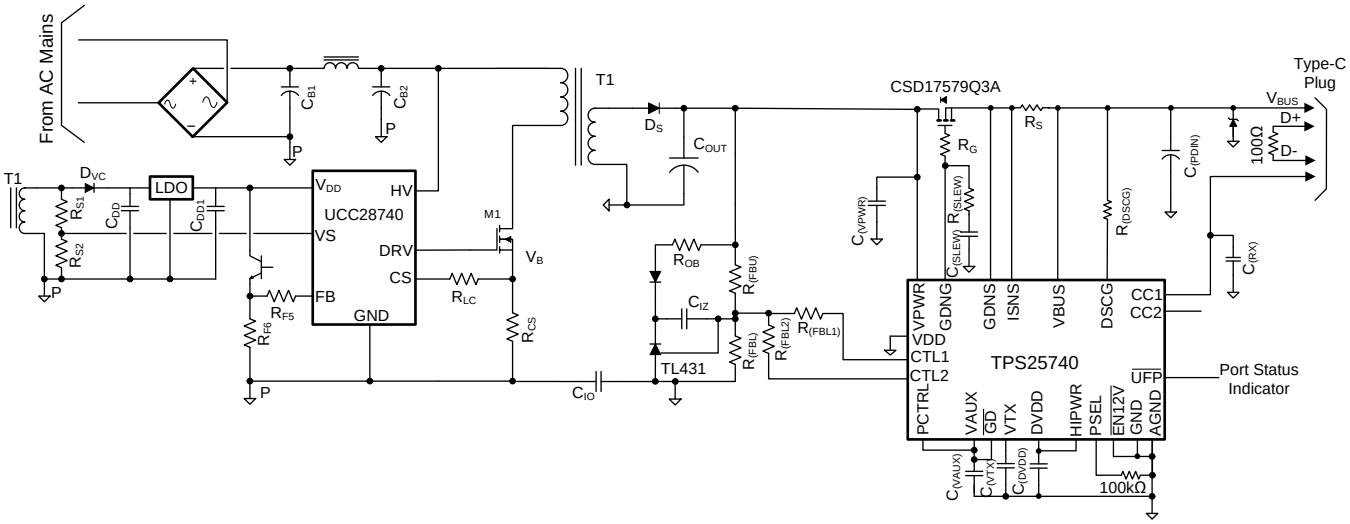


Figure 45. Captive Cable Adapter Provider Conceptual Schematic

9.2.1 Design Requirements

Table 9. Design Parameters

Design Parameter	Value
Configured Power Limit, $P_{(SEL)}$	65 W
Advertised Voltages	5 V, 12 V, 20 V
Advertised Current Limit	3 A
Over Current Protection Set point	4.2 A

9.2.2 Detailed Design Procedure

9.2.2.1 Power Pin Bypass Capacitors

- $C_{(VPWR)}$: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 20 (VPWR)
- $C_{(VDD)}$: 0.1 µF, 50 V, X7R ceramic at pin 17 (VDD). If VDD is not used in the application, then tie VDD to GND.
- $C_{(DVDD)}$: 0.22 µF, 10 V, ±10%, X5R ceramic at pin 13 (DVDD)
- $C_{(VAUX)}$: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 16 (VAUX)
- $C_{(VTX)}$: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 1 (VTX)

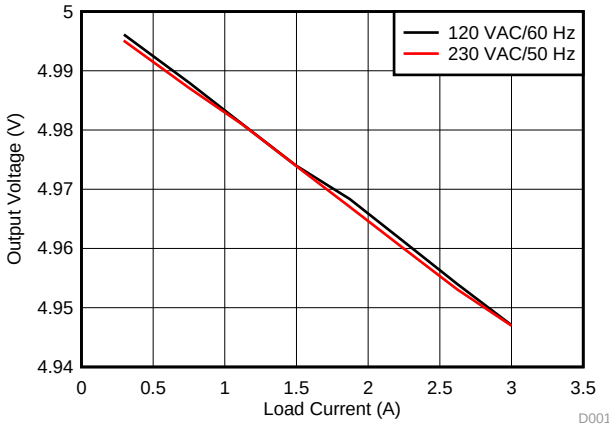
9.2.2.2 Non-Configurable Components

- $R_{(SEL)}$: When the application requires advertisement using $R_{(SEL)}$, use a 100 kΩ, ±1% resistor.
- $R_{(PCTRL)}$: If PCTRL will be pulled low with an external device then it can be connected to VAUX using a 220 kΩ, ±1% resistor. If PCTRL is always high, then it can be directly connected to VAUX.
- $R_{(SLEW)}$: Use a 1 kΩ, ±1% resistor
- R_G: Use a 10 Ω, ±1% resistor

9.2.2.3 Configurable Components

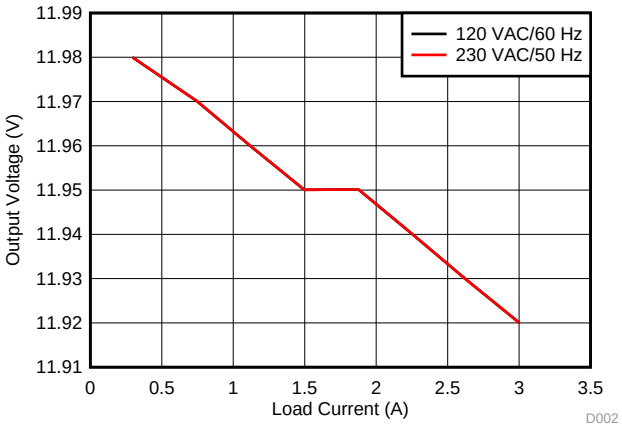
- $C_{(RX)}$: Choose $C_{(RX)}$ between 200 pF and 600 pF. A 560 pF, 50 V, ±5% COG/NPO ceramic is recommended for both CC1 and CC2 pins.
- Q_1: For a 3 A application, an N-Channel MOSFET with $R_{DS(on)}$ in the 10 mΩ range is sufficient. $BV_{(DSS)}$ should be rated for 30 V for applications delivering 20 V, and 25 V for 12 V applications. For this application, the TI CSD17579Q3A (SLPS527) NexFET™ is suitable.
- R_S: TPS25740 or TPS25740A OCP set point thresholds are targeted towards a 5 mΩ, ±1% sense resistor. Power dissipation for R_S at 3 A load is approximately 45 mW.
- $R_{(DSCG)}$: The minimum value of $R_{(DSCG)}$ is chosen based on the application VBUS (max) and $I_{(DSCGT)}$. For VBUS (max) = 12 V and $I_{(DSCGT)}$ = 350 mA, $R_{(DSCG(min))}$ = 34.3 Ω. The size of the external resistor can then be chosen based on the capacitive load that needs to be discharged and the maximum allowed discharge time of 265 ms. Typically, a 120 Ω, 0.5 W resistor provides suitable performance.
- R_F/C_F: Not used
- $C_{(PDIN)}$: The requirement for $C_{(PDIN)}$ is 10 µF maximum. A 6.8 µF, 25 V, ±10% X5R or X7R ceramic capacitor is suitable for most applications.
- $D_{(VBUS)}$: $D_{(VBUS)}$ provides reverse transient protection during large transient conditions when inductive loads are present. A Schottky diode with a $V_{(RRM)}$ rating of 30 V in a SMA package such as the B340A-13-F provideds suitable reverse voltage clamping performance.
- $C_{(SLEW)}$: To achieve a slew rate from zero to 5 V of less than 30 mV / µs using the typical GDNG current of 20 µA then $C_{(SLEW)}$ > 20 µA / 30 mV / µs = 0.67 nF be used. Choosing $C_{(SLEW)}$ = 10 nF yields a ramp rate of 2 mV / µs.
- $R_{(FBL1)}/R_{(FBL2)}$: In this design example, $R_{(FBU)}$ = 20 kΩ and $R_{(FBL)}$ = 20 kΩ. The feedback error amplifier is TL431AI which is rated for up to 36 V operation and V_{REF} = 2.495 V. Using the equations for $R_{(FBL2)}$ above yields a calculated value of 7.1 kΩ and a selected value of 7.15 kΩ. In similar fashion for $R_{(FBL1)}$, the equations yield a calculated value of 6.35 kΩ and a selected value of 6.34 kΩ.

9.2.3 Application Curves



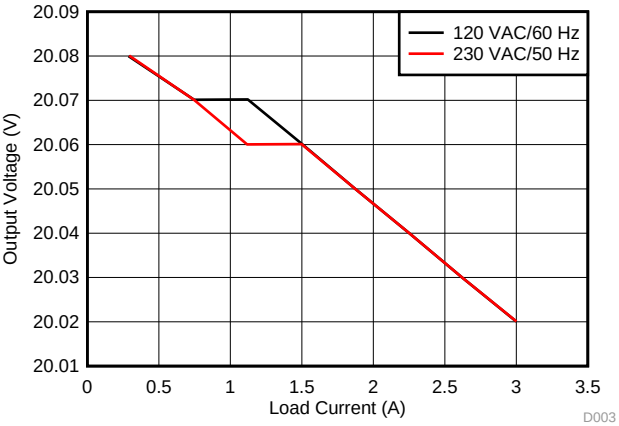
DFP End - VBUS = 5 V

Figure 46. Load Regulation



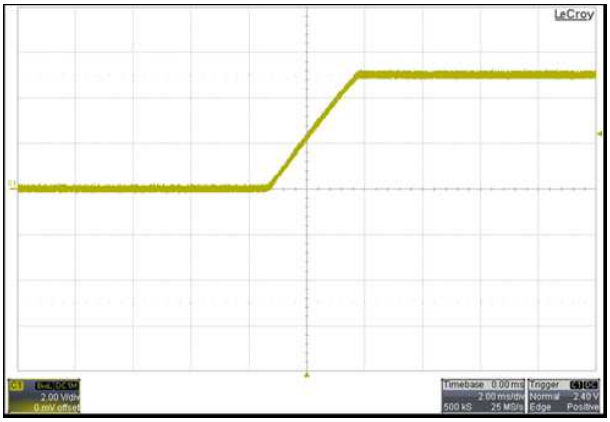
DFP End - VBUS = 12 V

Figure 47. Load Regulation



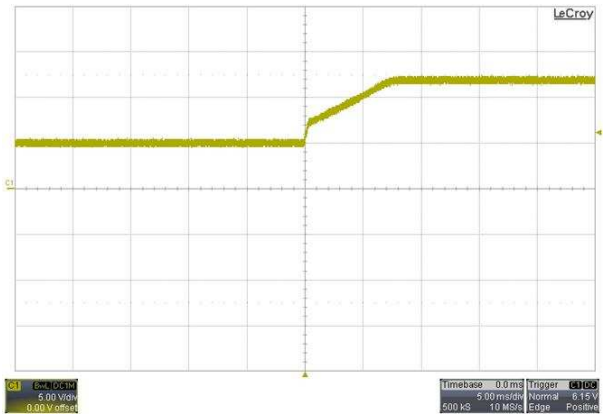
DFP End - VBUS = 20 V

Figure 48. Load Regulation



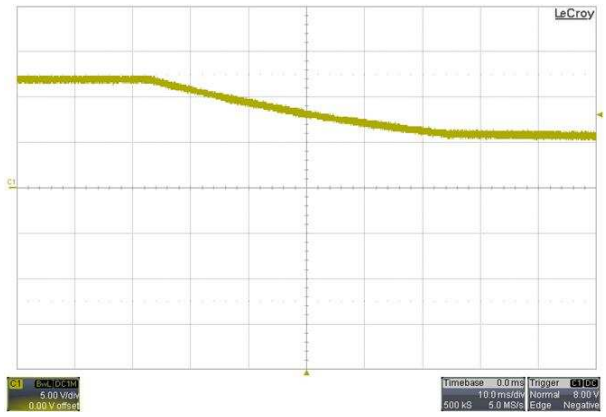
No Load

Figure 49. VBUS Startup



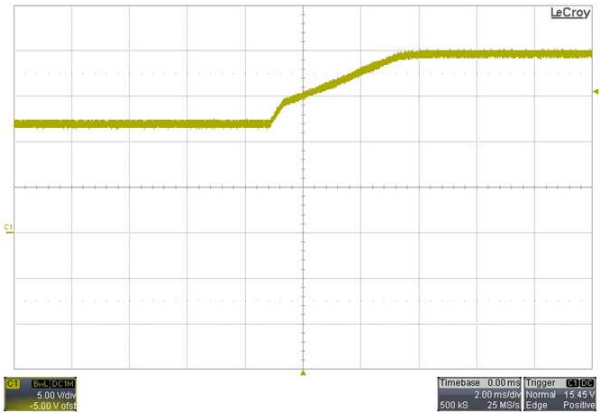
No Load

Figure 50. VBUS 5 V – 12 V Transition



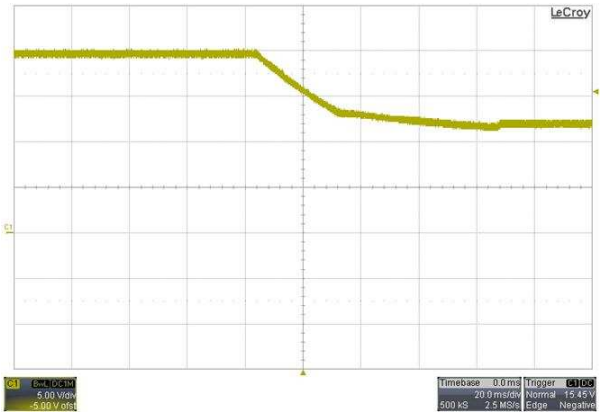
No Load

Figure 51. VBUS 12 V – 5 V Transition



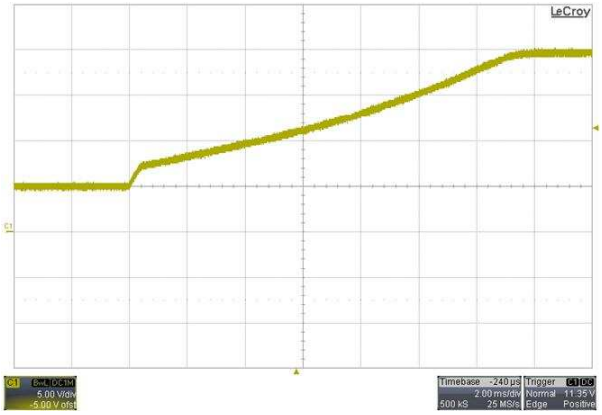
No Load

Figure 52. VBUS 12 V – 20 V Transition



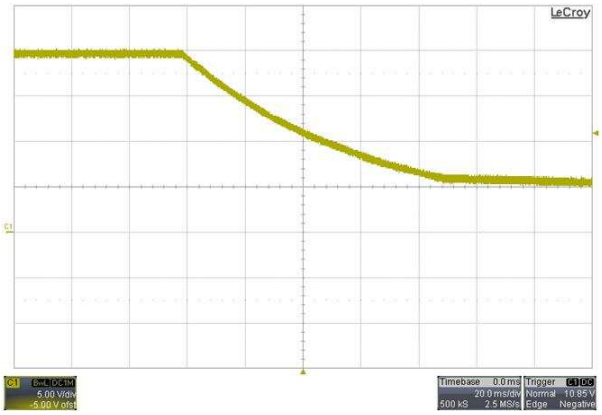
No Load

Figure 53. VBUS 20 V – 12 V Transition



No Load

Figure 54. VBUS 5 V – 20 V Transition



No Load

Figure 55. VBUS 20 V – 5 V Transition

9.2.4 Typical Application, D/C Power Source

In this design example the PSEL pin is configured such that $P_{(SEL)}$ = 65 W (see Table 10). Voltages offered are 5 V, 9 V, and 15 V at a maximum of 3 A. The overcurrent protection (OCP) trip point is set just above 3 A and VDD on the TPS25740A is grounded. The following example is based on TPS25740AEVM-741 (refer to 文档支持).

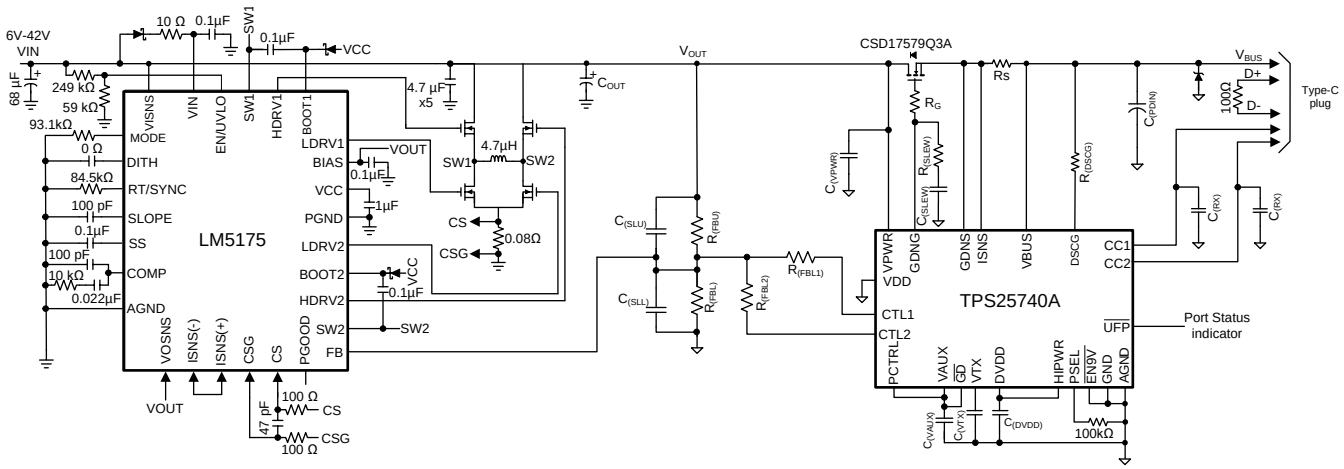


Figure 56. DC Power Source

9.2.4.1 Design Requirements

Table 10. Design Parameters

Design Parameter	Value
Configured Power Limit, $P_{(SEL)}$	65 W
Advertised Voltages	5 V, 9 V, 15 V
Advertised Current Limit	3 A
Over Current Protection Set point	4.2 A

9.2.4.2 Detailed Design Procedure

9.2.4.2.1 Power Pin Bypass Capacitors

- $C_{(VPWR)}$: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 20 (VPWR)
- $C_{(VDD)}$: 0.1 µF, 50 V, X7R ceramic at pin 17 (VDD). If VDD is not used in the application, then tie VDD to GND.
- $C_{(DVDD)}$: 0.22 µF, 10 V, ±10%, X5R ceramic at pin 13 (DVDD)
- $C_{(VAUX)}$: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 16 (VAUX)
- $C_{(VTX)}$: 0.1 µF, 50 V, ±10%, X7R ceramic at pin 1 (VTX)

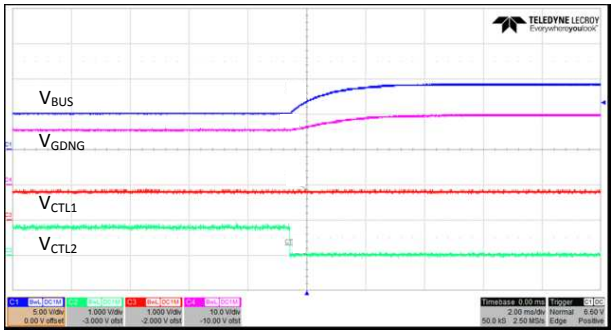
9.2.4.2.2 Non-Configurable Components

- $R_{(SEL)}$: When the application requires advertisement using $R_{(SEL)}$, use a 100 kΩ, ±1% resistor.
- $R_{(PCTRL)}$: If PCTRL will be pulled low with an external device then it can be connected to VAUX using a 220 kΩ, ±1% resistor. If PCTRL will always be high then it can be directly connected to VAUX.
- $R_{(SLEW)}$: Use a 1 kΩ, ±1% resistor
- R_G: Use a 10 Ω, ±1% resistor

9.2.4.2.3 Configurable Components

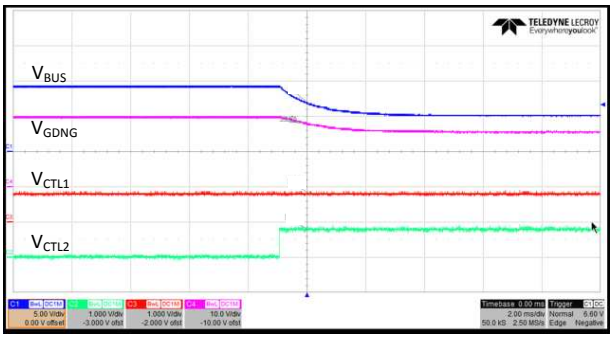
- $C_{(RX)}$: Choose $C_{(RX)}$ between 200 pF and 600 pF. A 560 pF, 50 V, ±5% COG/NPO ceramic is recommended for both CC1 and CC2 pins.
- Q_1: For a 3 A application, an N-Channel MOSFET with $R_{DS(on)}$ in the 10 mΩ range is sufficient. $BV_{(DSS)}$ should be rated for 30 V for applications delivering 20 V, and 25 V for 12 V applications. For this application, the TI CSD17579Q3A (SLPS527) NexFET™ is suitable.
- R_S: TPS25740 or TPS25740A OCP set point thresholds are targeted towards a 5 mΩ, ±1% sense resistor. Power dissipation for R_S at 3 A load is approximately 45 mW.
- $R_{(DSCG)}$: The minimum value of $R_{(DSCG)}$ is chosen based on the application VBUS (max) and $I_{(DSCGT)}$. For VBUS (max) = 12 V and $I_{(DSCGT)}$ = 350 mA, $R_{DS(CG(min))}$ = 34.3 Ω. The size of the external resistor can then be chosen based on the capacitive load that needs to be discharged and the maximum allowed discharge time of 265 ms. Typically, a 120 Ω, 0.5 W resistor provides suitable performance.
- R_F/C_F: Not used
- $C_{(PDIN)}$: The requirement for $C_{(PDIN)}$ is 10 µF maximum. A 6.8 µF, 25 V, ±10% X5R or X7R ceramic capacitor is suitable for most applications.
- $D_{(VBUS)}$: $D_{(VBUS)}$ provides reverse transient protection during large transient conditions when inductive loads are present. A Schottky diode with a $V_{(RRM)}$ rating of 30 V in a SMA package such as the B340A-13-F provideds suitable reverse voltage clamping performance.
- $C_{(SLEW)}$: To achieve a slew rate from zero to 5 V of less than 30 mV / µs using the typical GDNG current of 20 µA then $C_{(SLEW)}$ (nF) > 20 µA / 30 mV / µs = 0.67 nF be used. Choosing $C_{(SLEW)}$ = 10 nF yields a ramp rate of 2 mV / µs.
- $R_{(FBL1)}/R_{(FBL2)}$: In this design example, $R_{(FBU)}$ = 49.9 kΩ and $R_{(FBL)}$ = 9.53 kΩ. The feedback error amplifier V_{REF} = 0.8 V. Using the equations for $R_{(FBL2)}$ (Equation 5 and Equation 6) provide a calculated value of 9.9 kΩ and a selected value of 9.76 kΩ. In similar fashion for $R_{(FBL1)}$, a calculated value of 6.74 kΩ and a selected value of 6.65 kΩ is provided.
- $C_{(SLU)}/C_{(SLL)}$: The value of $C_{(SLU)}$ is calculated based on the desired 95% slew rate using Equation 12 and Equation 13. Choose a 22 nF capacitor for $C_{(SLU)}$. Choose a 100 nF capacitor for $C_{(SLL)}$.

9.2.4.3 Application Curves



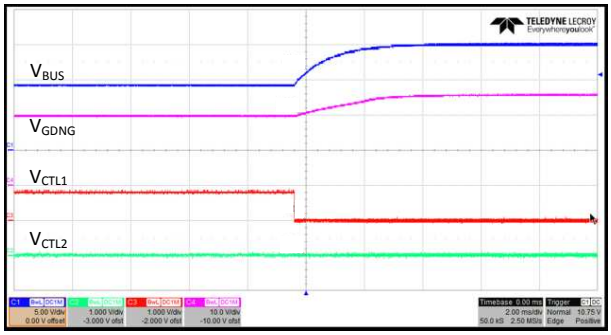
No Load

Figure 57. VBUS 5 V – 9 V Transition



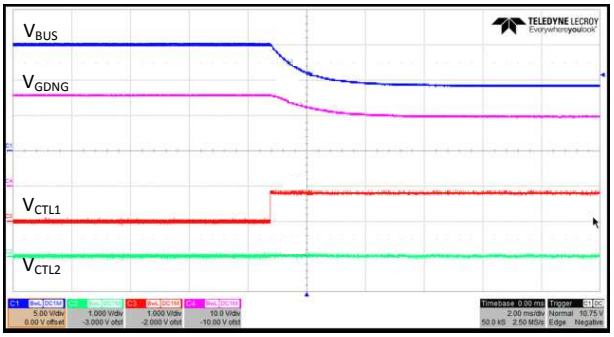
No Load

Figure 58. VBUS 9 V – 5 V Transition



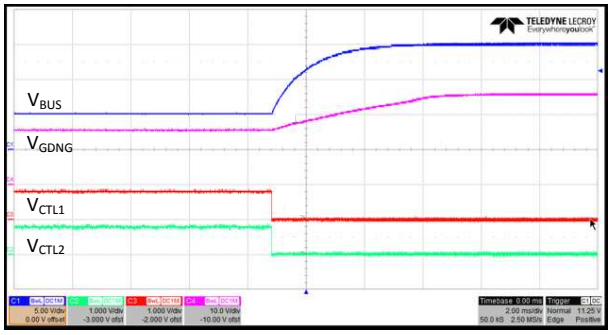
No Load

Figure 59. VBUS 9 V – 15 V Transition



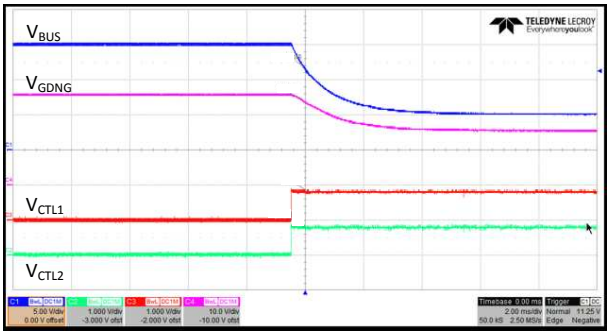
No Load

Figure 60. VBUS 15 V – 9 V Transition



No Load

Figure 61. VBUS 5 V – 15 V Transition



No Load

Figure 62. VBUS 15 V – 5 V Transition

9.3 System Examples

9.3.1 D/C Power Source (Power Hub)

In this system design example, the $P_{(SEL)}$ is configured such that $P_{(SEL)}$ = 93 W and 5 V, 12 V or 20 V are offered at a maximum of 5 A. The over-current protection (OCP) trip point is set just above 5 A.

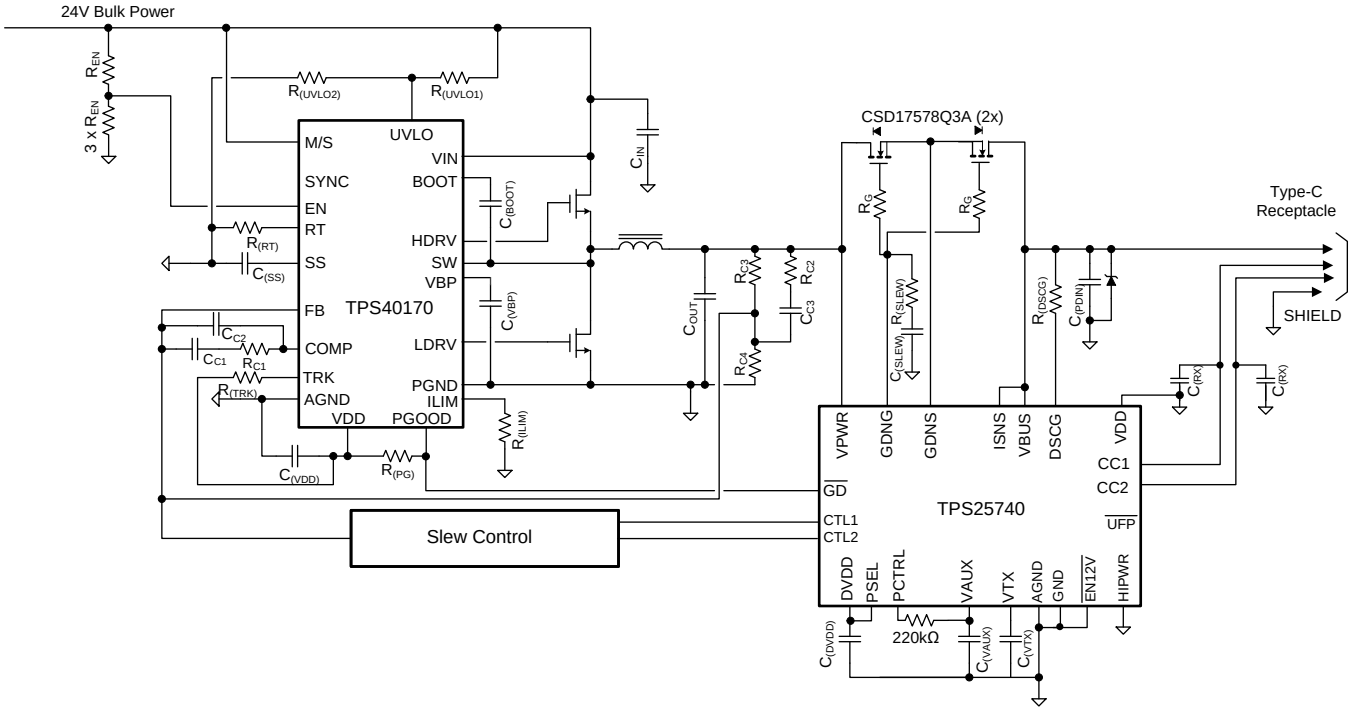


Figure 63. Power Hub Concept (Provider only)

This power hub circuit takes a 24 V input and produces a regulated output voltage. The over-current protection feature in the TPS25740 is not used; the ISNS and VBUS pins are connected directly. Instead $R_{(ILIM)}$ is chosen to set the current limit of the TPS40170 synchronous PWM buck controller. If the current limit trips, the $\overline{GD}$ pin of the TPS25740 is pulled low by the PGOOD pin of the TPS40170, which causes the power-path switch to be opened. Other fault conditions may also pull PGOOD low, but the slew rate of the voltage transition should be controlled as in one of the examples given above (Figure 41, Figure 42, or Figure 43).

VDD on the TPS25740 is grounded, if there is a suitable power supply available in the system the TPS25740 operates more efficiently if it is connected to VDD since $V_{(VPWR)} > V_{(VDD)}$. See Figure 66 for an example.

System Examples (continued)

9.3.2 A/C Power Source (Wall Adapter)

In this system design example, the PSEL pin is configured such that $P_{(SEL)}$ = 36 W, and only 5 V and 12 V are offered at a maximum of 3 A. The overcurrent protection (OCP) trip point is set just above 3 A. VDD on the TPS25740 is grounded, if there is a suitable power supply available in the system the TPS25740 operates more efficiently if it is connected to VDD since $V_{(VPWR)} > V_{(VDD)}$.

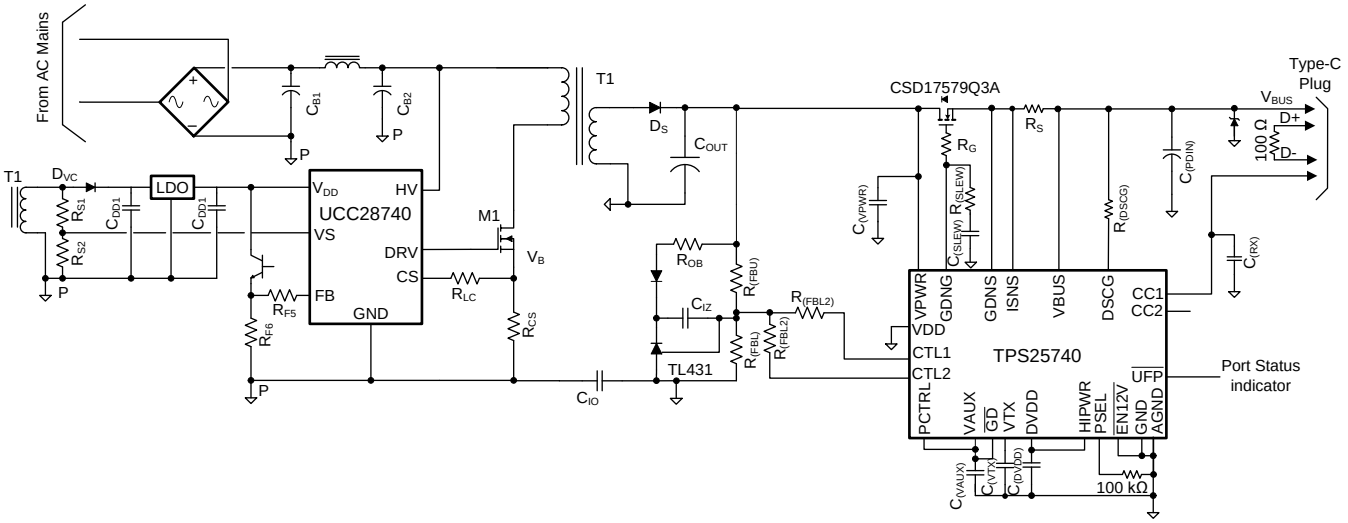


Figure 64. Adapter Provider Concept

System Examples (continued)

9.3.3 Dual-Port Power Managed A/C Power Source (Wall Adaptor)

In this system design example, the PSEL pin is configured such that $P_{(SEL)}$ = 36 W, and only 5 V and 12 V are offered at a maximum of 3 A. The over-current protection (OCP) trip point is set just above 3 A.

The $\overline{UFP}$ pin from one TPS25740 is attached to the PCTRL pin on the other TPS25740. When one port is not active (no UFP attached through the receptacle) its $\overline{UFP}$ pin is left high-z so the PCTRL pin on the other port is pulled high. This allows the adaptor to provide up to the full 36 W on a single port if a single UFP is attached. If two UFP's are attached (one to each port) then each port only offers current that would reach a maximum of 18 W. So each port is allocated half of the overall power when each port has a UFP attached.

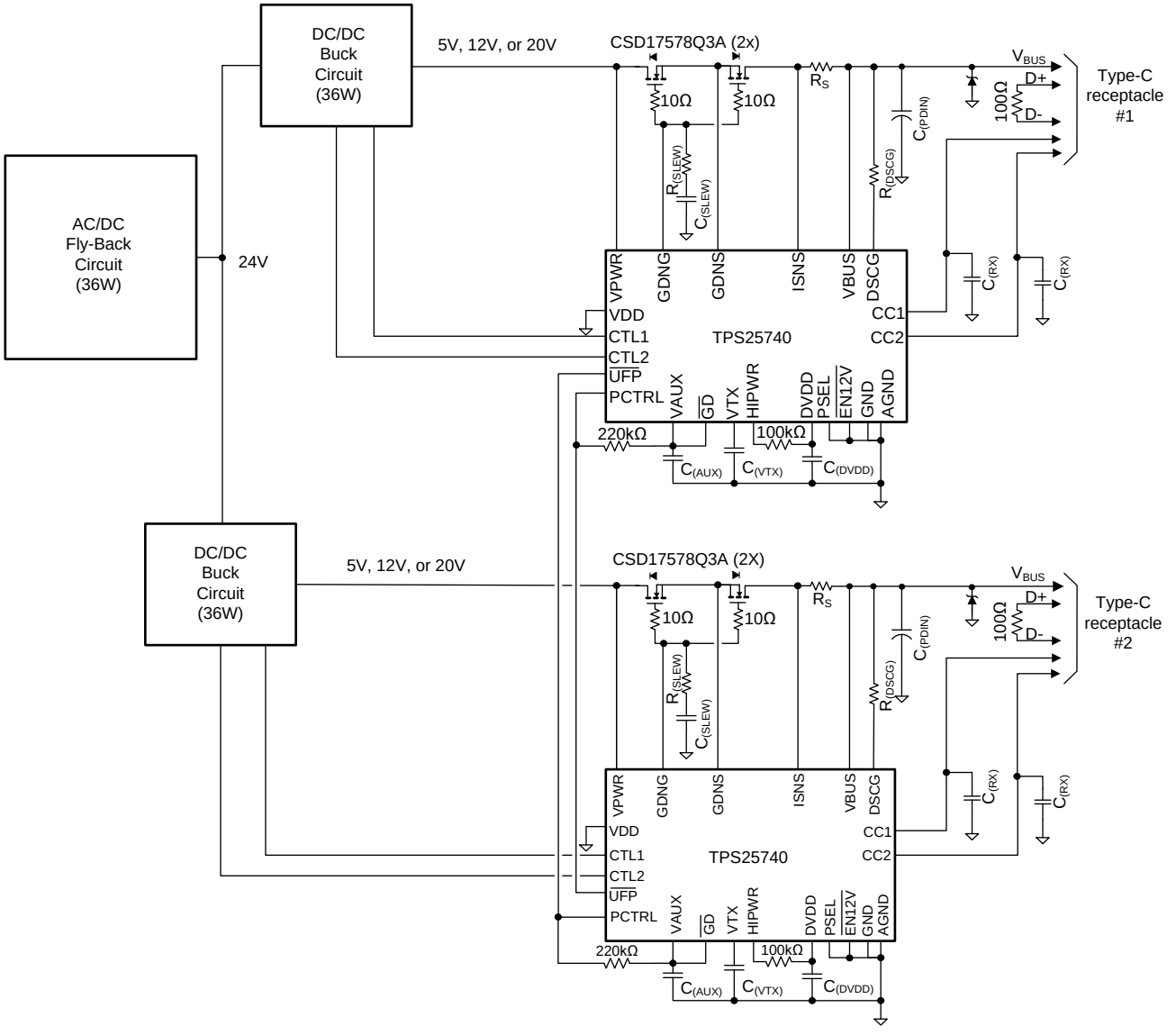


Figure 65. Dual-Port Adapter Provider Concept

System Examples (continued)

9.3.4 D/C Power Source (Power Hub with 3.3 V Rail)

In Figure 66, an LDO that outputs at least $I_{(SUPP)}$ at 3.3 V or 5 V is added to the power hub concept, and the DVDD pin is used to enable the buck regulator since it is active high. For an active low buck regulator, the $\overline{UFP}$ pin could be used. This implementation is more power efficient than the one in Figure 63.

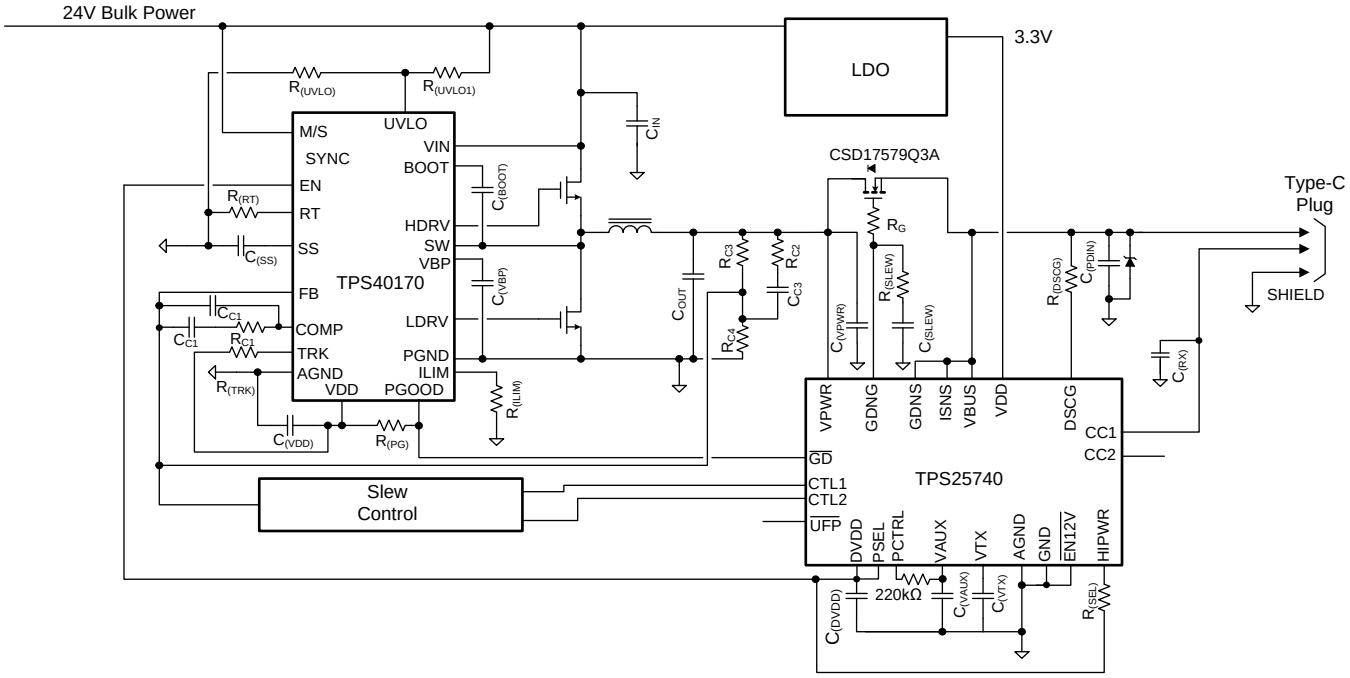


Figure 66. Power Hub Concept (Provider only)

10 Power Supply Recommendations

10.1 VDD

The recommended VDD supply voltage range is 3 V to 5.5 V. The device requires approximately 2 mA ($I_{(SUPP)}$) typical in normal operating mode and below 10 µA in sleep mode. If the VDD supply is not used, then it may be connected to AGND/GND.

10.2 VPWR

The recommended VPWR supply voltage range is 0 V to 25 V. The device requires approximately 2 mA ($I_{(SUPP)}$) typical in normal operating mode and below 10 µA in sleep mode.

11 Layout

11.1 Port Current Kelvin Sensing

Figure 67 provides a routing example for accurate current sensing for the overcurrent protection feature. The sense amplifier measurement occurs between the ISNS and VBUS pins of the device. Improper connection of these pins can result in poor OCP performance.

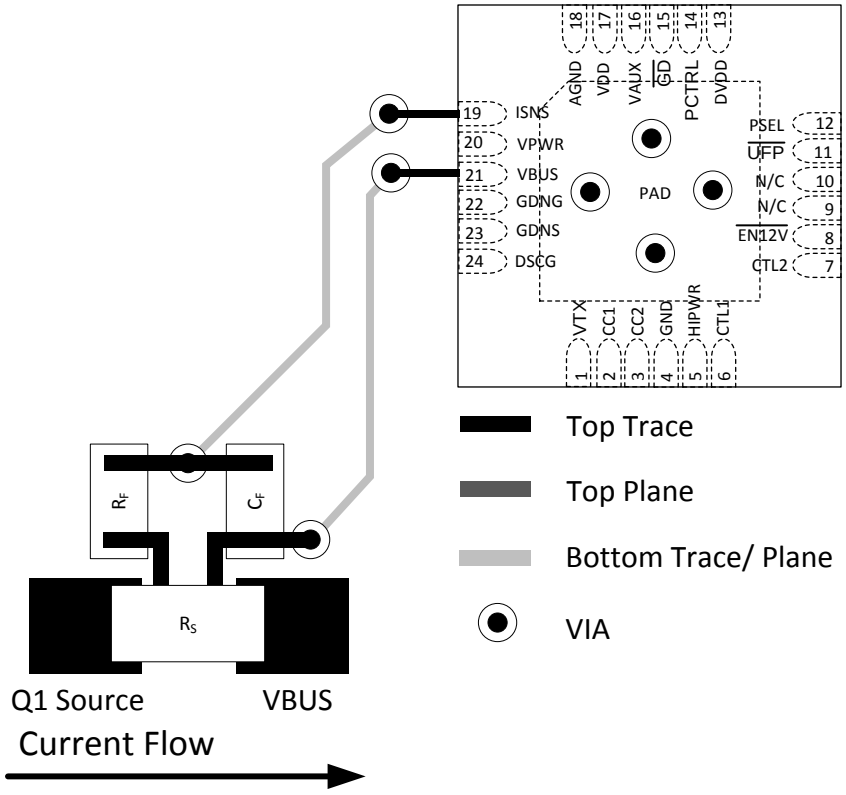


Figure 67. Kelvin Sense Layout Example

11.2 Layout Guidelines

11.2.1 Power Pin Bypass Capacitors

- $C_{(VPWR)}$: Place close to pin 20 (VPWR) and connect with low inductance traces and vias according to Figure 68.
- $C_{(VDD)}$: Place close to pin 17 (VDD) and connect with low inductance traces and vias according to Figure 68.
- $C_{(DVDD)}$: Place close to pin 13 (DVDD) and connect with low inductance traces and vias according to Figure 68.
- $C_{(VAUX)}$: Place close to pin 16 (VAUX) and connect with low inductance traces and vias according to Figure 68.
- $C_{(VTX)}$: Place close to pin 1 (VTX) and connect with low inductance traces and vias according to Figure 68.

11.2.2 Supporting Components

- $C_{(RX)}$: Place $C_{(RX1)}$ and $C_{(RX2)}$ in line with the CC1 and CC2 traces as shown in Figure 23. These should be placed within one inch from the Type C connector. Minimize stubs and tees from on the trace routes.
- Q_1: Place Q_1 in a manner such that power flows uninterrupted from Q_1 drain to the Type C connector VBUS connections. Provide adequate copper plane from Q_1 drain and source to the interconnecting circuits.
- R_S: Place R_S as shown in Figure 68 to facilitate uninterrupted power flow to the Type C connector. Orient R_S for optimal Kelvin sense connection/routing back to the TPS25740 or TPS25740A. In high current applications

Layout Guidelines (continued)

where the power dissipation is over 250 mW, provide an adequate copper feed to the pads of R_S.

- R_G: Place R_G near Q_1 as shown in Figure 68. Minimize stray leakage paths as the GDNG sourcing current could be affected.
- $R_{(SLEW)}/C_{(SLEW)}$: Place $R_{(SLEW)}$ and $C_{(SLEW)}$ near R_G as shown in Figure 68.
- $R_{(DSCG)}$: Place on top of the VBUS copper route and connect to the DSCG pin with a 15 mil trace.
- R_F/C_F: When required, place R_F and C_F as shown in Figure 68 to facilitate the Kelvin sense connection back to the device.
- $C_{(VBUS)}/D_{(VBUS)}$: Place $C_{(VBUS)}$ and $D_{(VBUS)}$ within one inch of the Type C connector and connect them to VBUS and GND using adequate copper shapes.
- $R_{(SEL)}/R_{(PCTRL)}$: Place $R_{(SEL)}$ and $R_{(PCTRL)}$ near the device.

11.3 Layout Example

The basic component placement and layout is provided in Figure 68. This layout represents the circuit shown in Figure 36. The layout for other power configurations will vary slightly from that shown below.

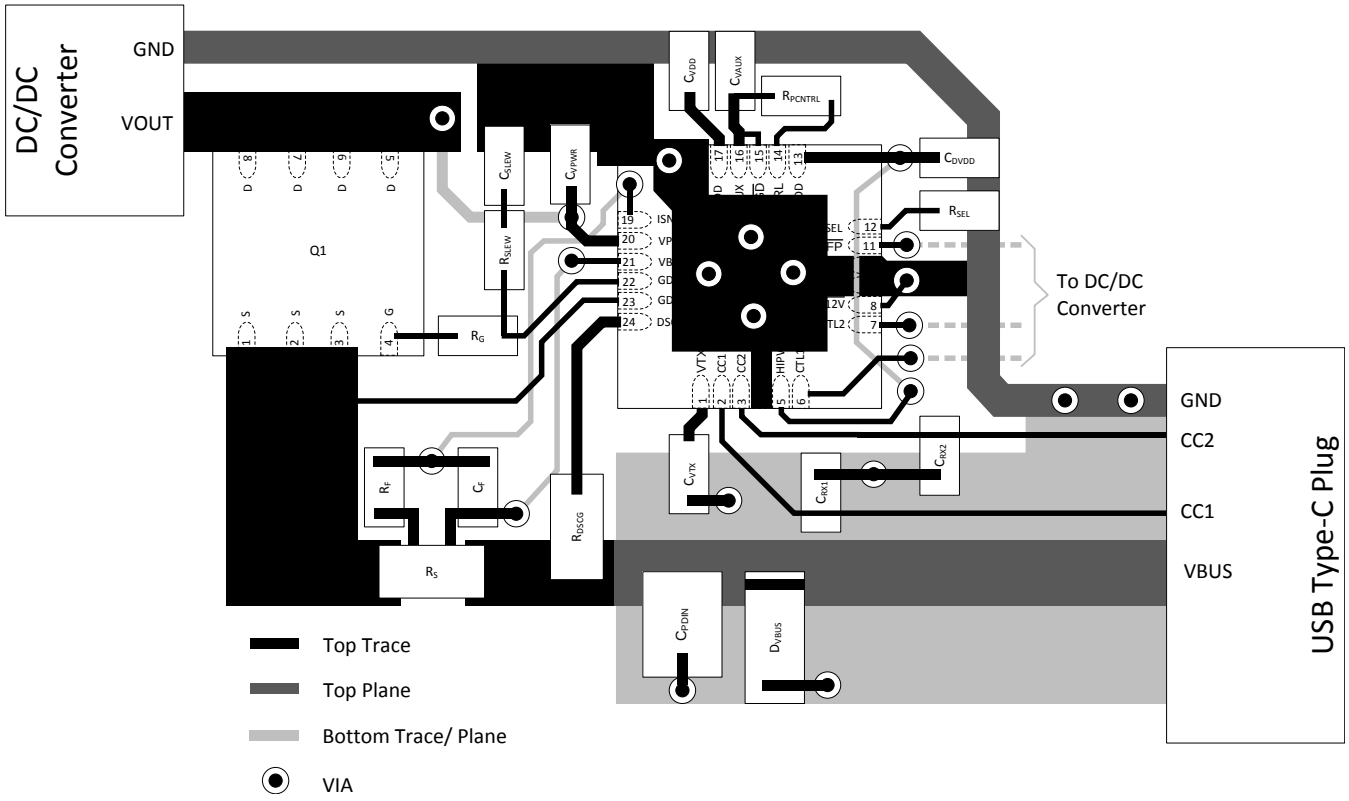


Figure 68. Example Layout

12 器件和文档支持

12.1 文档支持

有关 USB PD 和 USB Type-C 规范，请访问：http://www.usb.org/home

《TPS25740EVM-741 和 TPS25740AEVM-741 EVM 用户指南》

《TPS25740/TPS25740A 设计计算器工具》

12.2 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 11. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TPS25740	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS25740A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

E2E is a trademark of Texas Instruments.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25740ARGER	NRND	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25740A	
TPS25740ARGET	NRND	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25740A	
TPS25740RGER	NRND	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25740	
TPS25740RGET	NRND	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 25740	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

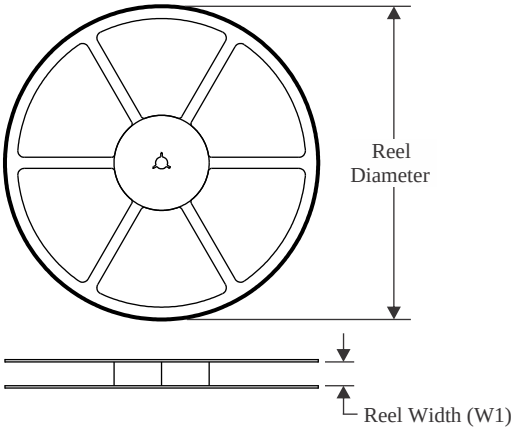
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

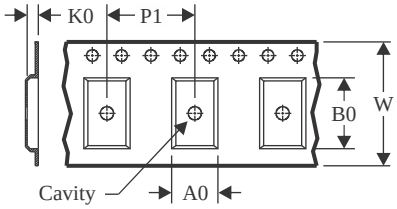
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

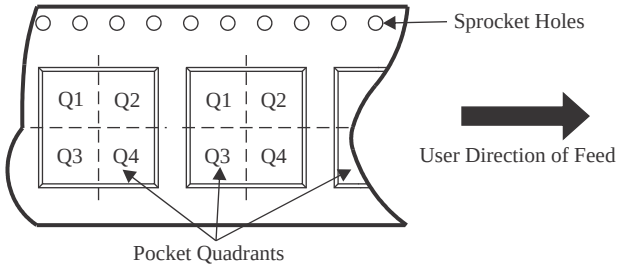


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

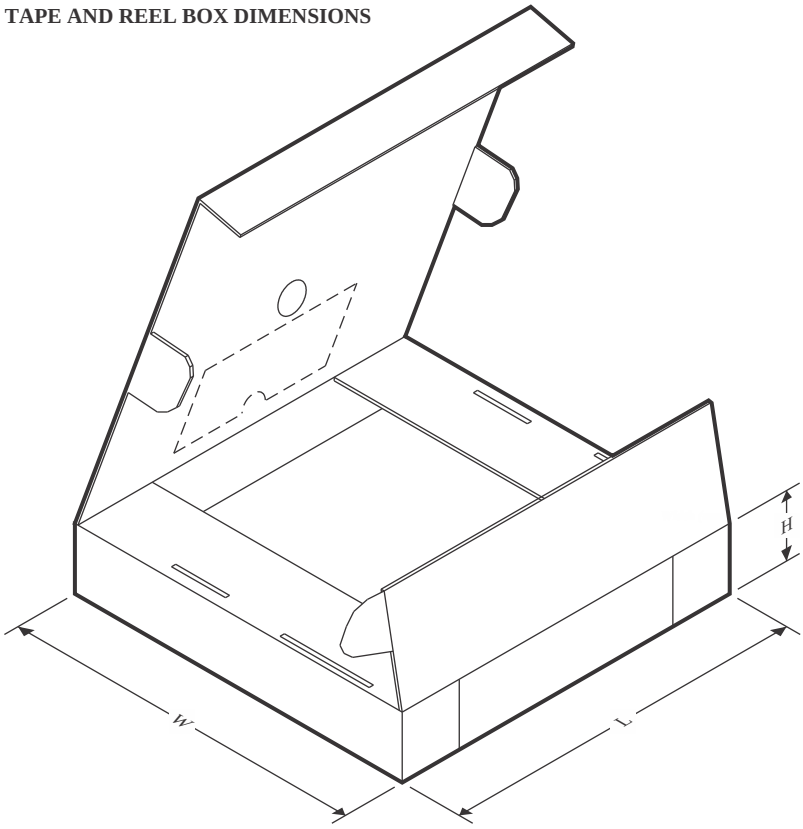
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25740ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS25740ARGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS25740RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS25740RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



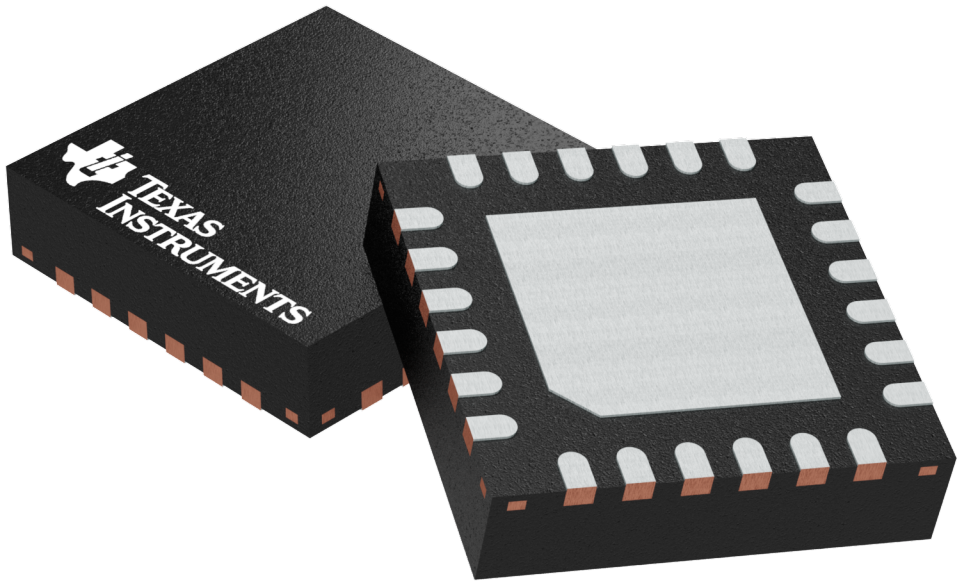
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25740ARGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS25740ARGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS25740RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS25740RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

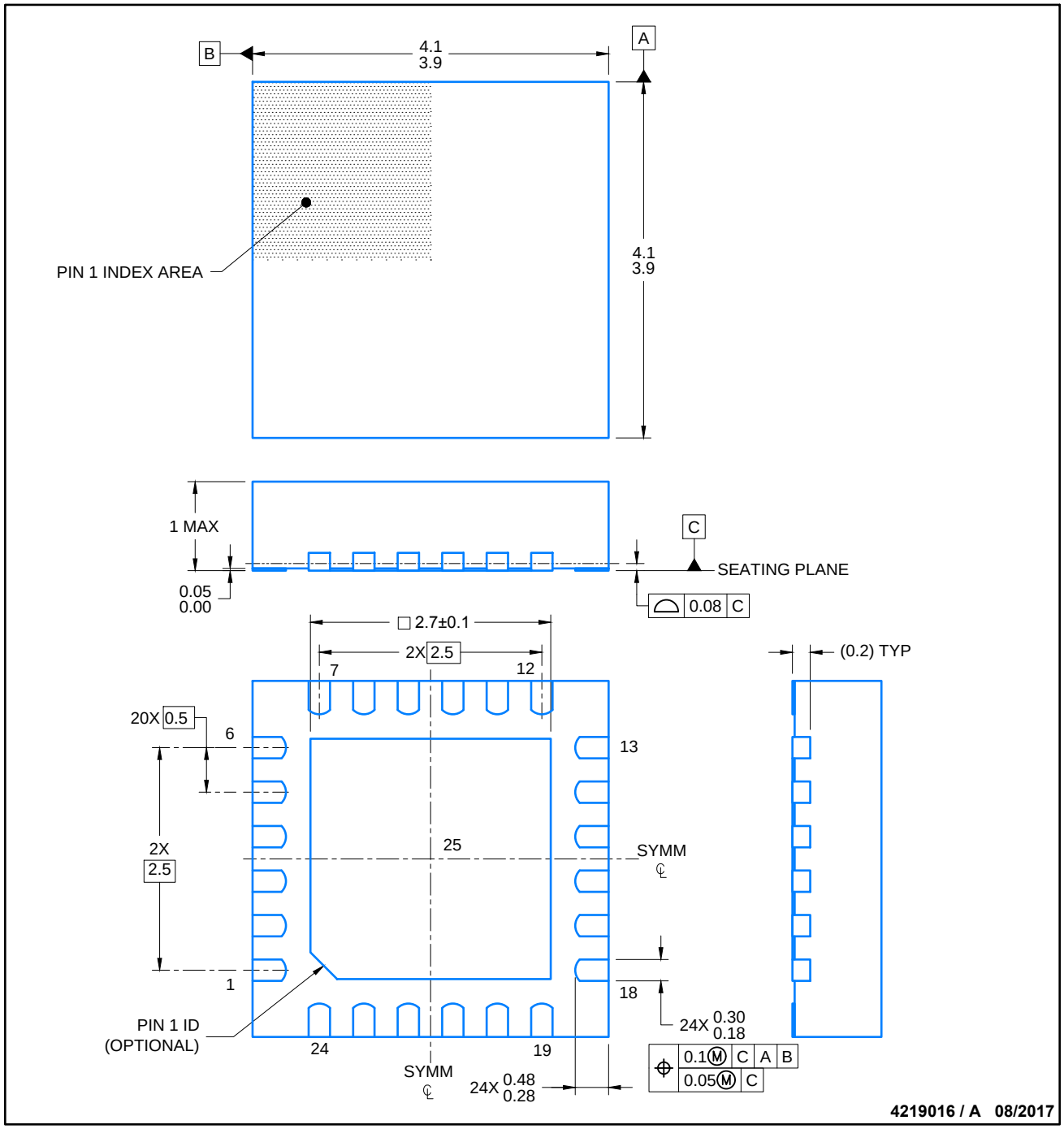
4204104/H

PACKAGE OUTLINE

RGE0024H

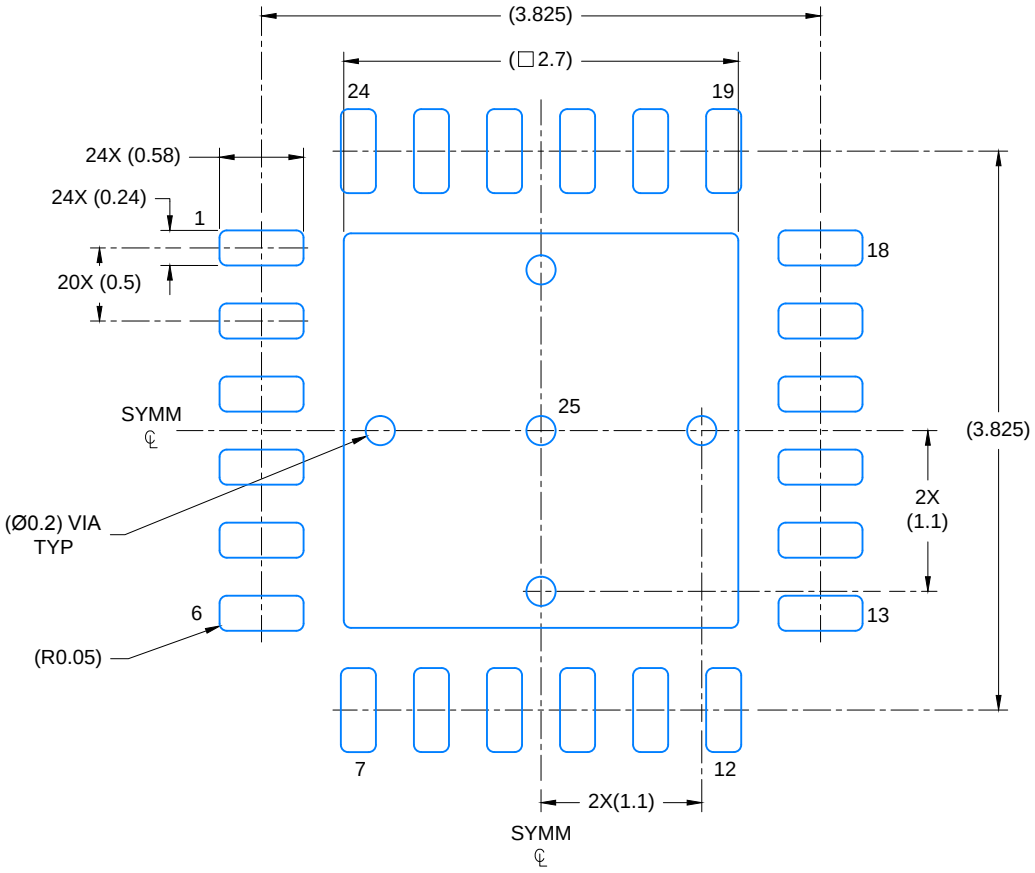
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



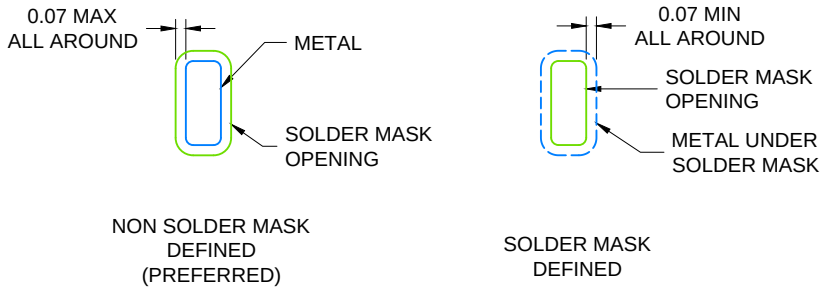
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

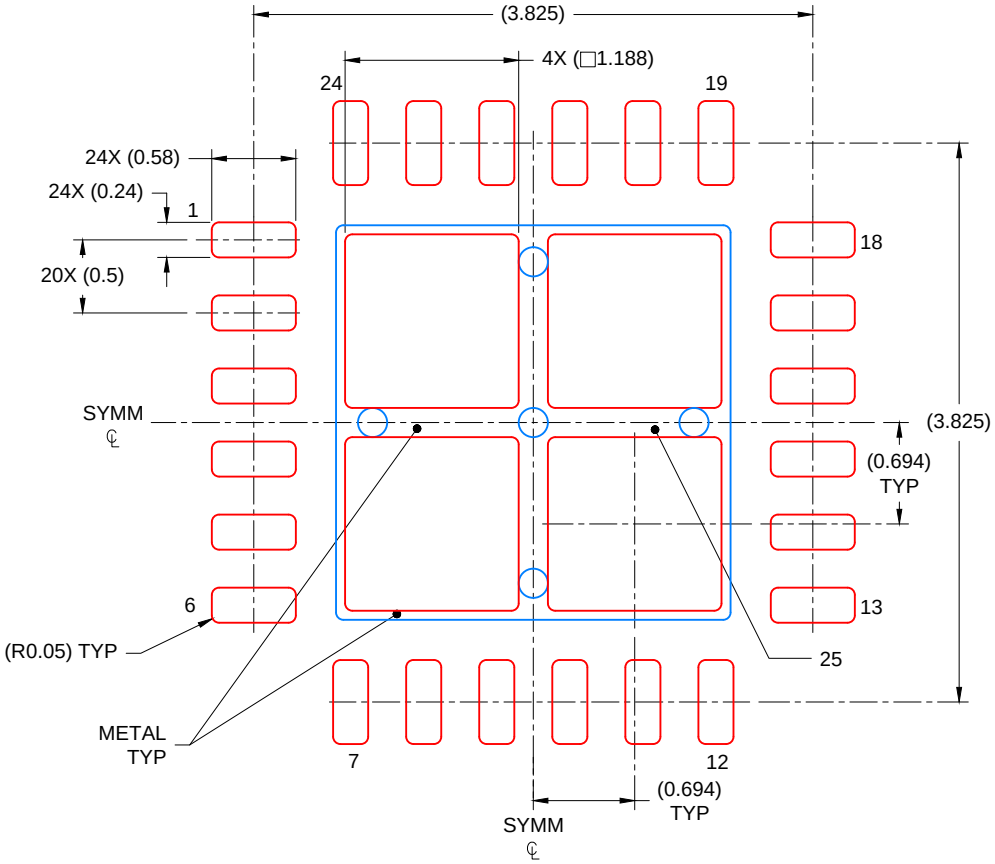


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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