单通道、超低电阻负载开关

查询样品: TPS22967

特性

- 集成的单通道负载开关
- 输入电压范围：**0.8V** 至 **5.5V**
- 超低 **$R_{导通}$** 电阻
  - **$V_{输入}$ = 5V**（**$V_{偏置}$ = 5V**）时，**$R_{导通}$ = 22mΩ**
  - **$V_{输入}$ = 3.6V**（**$V_{偏置}$ = 5V**）时，**$R_{导通}$ = 22mΩ**
  - **$V_{输入}$ = 1.8V**（**$V_{偏置}$ = 5V**）时，**$R_{导通}$ = 22mΩ**
- **4A** 最大持续开关电流
- 低静态电流 **(50μA)**
- 低控制输入阀值支持使用 **1.2V/1.8V/2.5V/3.3V** 逻辑电路
- 可配置的上升时间
- 快速输出放电 **(QOD)**
- 带有散热垫的小外形尺寸无引线 **(SON) 8** 引脚封装
- 根据 **JESD 22** 测试得出的静电放电 **(ESD)** 性能
  - **2KV** 人体模型 **(HBM)** 和 **1KV** 器件充电模型 **(CDM)**

应用范围

- **Ultrabook™**
- 笔记本电脑**/**上网本
- 平板电脑
- 消费类电子产品
- 机顶盒**/**家庭网关
- 电信系统
- 固态硬盘 **(SSD)**

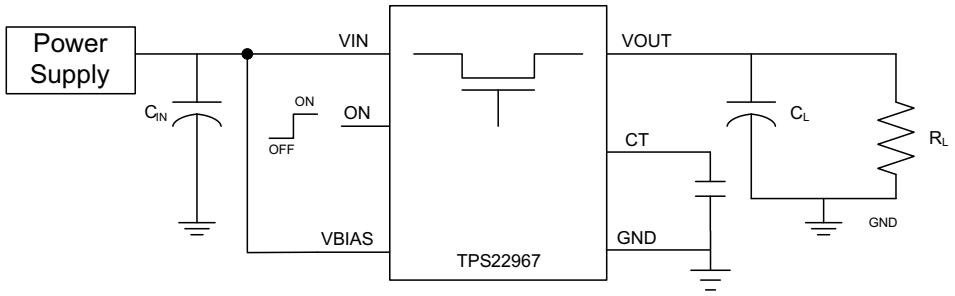
说明

TPS22967 是一款小型，超低 $R_{导通}$ 电阻，单通道负载开关，此开关具有受控开启功能。 此器件包含一个可在 0.8V 至 5.5V 输入电压范围内运行的 N 通道金属氧化物半导体场效应晶体管 (MOSFET)，并且每通道支持最大 4A 的持续电流。 此开关可由一个打开/关闭输入 (ON) 控制，此输入可与低压控制信号直接对接。 在 TPS22967 中，为了实现开关关闭时的快速输出放电，增加了一个 225Ω 的上拉电阻器。

TPS22967 采用小型，节省空间的 2mm x 2mm 8 引脚 SON 封装 (DSG)，此类封装具有可实现高功率耗散的集成散热垫。 器件在自然通风环境下的额定运行温度范围为 -40°C 至 85°C。

特性列表

3.6V（$V_{偏置}$ = 5V）时，$R_{导通}$ 的典型值	22mΩ
上升时间(1)	可调节
快速输出放电	支持
最大输出电流	4A
通用输入输出接口 (GPIO) 启用	高电平有效
工作温度	-40°C 至 85°C
(1) CT 电容值与上升时间之间的关系请参见应用信息部分。 (2) 这个特性通过一个 225Ω 电阻器将开关的输出放电至接地 (GND)，从而防止输出悬空。	



典型应用

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)(2)

			VALUE	UNIT(2)
V_{IN}	Input voltage range		–0.3 to 6	V
V_{OUT}	Output voltage range		–0.3 to 6	V
V_{BIAS}	Bias voltage range		–0.3 to 6	V
V_{ON}	ON voltage range		–0.3 to 6	V
I_{MAX}	Maximum continuous switch current		4	A
I_{PLS}	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle		6	A
T_A	Operating free-air temperature range(3)		–40 to 85	°C
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range		–65 to 150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	2000	V
		Charged-Device Model (CDM)	1000	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $TA_{(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

THERMAL INFORMATION

THERMAL METRIC(1)		TPS22967 DSG (8 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	65.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	74.2	
θ_{JB}	Junction-to-board thermal resistance	35.4	
ψ_{JT}	Junction-to-top characterization parameter	2.2	
ψ_{JB}	Junction-to-board characterization parameter	36.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	12.8	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：ZHCA543）。

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage range		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
C_{IN}	Input capacitor		1 (1)		µF

(1) Refer to Application Information section.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature **–40°C ≤ T_A ≤ 85°C** (Full) and **V_{BIAS} = 5.0 V**. Typical values are for T_A = 25°C.

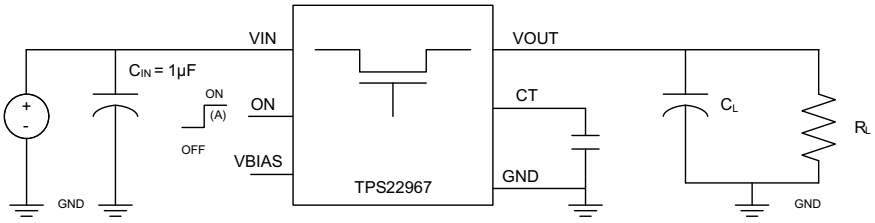
PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 5.0 V		Full		50	75	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 5.0 V	Full		0.2	8	µA
			V_{IN} = 3.3 V			0.02	3	
			V_{IN} = 1.8 V			0.01	2	
			V_{IN} = 0.8 V			0.005	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5.0 V	V_{IN} = 5.0 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 3.3 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 1.8 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 1.5 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 1.2 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 0.8 V	25°C		22	33	mΩ
				Full			35	
R_{PD}	Output pulldown resistance	V_{IN} = 5.0 V, V_{ON} = 0V, I_{OUT} = 15 mA		Full		225	300	Ω

ELECTRICAL CHARACTERISTICS

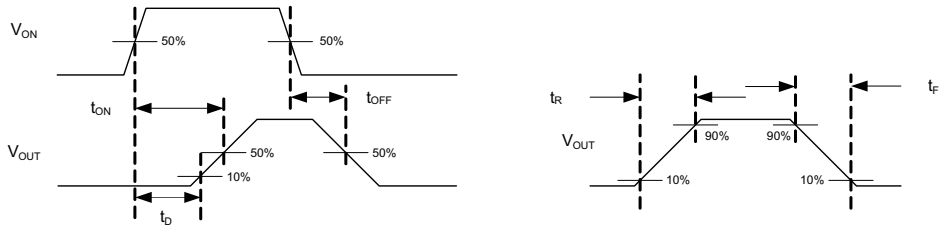
Unless otherwise noted, the specification in the following table applies over the operating ambient temperature **–40°C ≤ T_A ≤ 85°C** (Full) and **V_{BIAS} = 2.5 V**. Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		Full		20	30	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 2.5 V	Full		0.01	3	µA
			V_{IN} = 1.8 V			0.01	2	
			V_{IN} = 1.2 V			0.005	2	
			V_{IN} = 0.8 V			0.003	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		26	38	mΩ
				Full			40	
			V_{IN} = 1.8 V	25°C		26	38	mΩ
				Full			40	
			V_{IN} = 1.5 V	25°C		25	38	mΩ
				Full			40	
			V_{IN} = 1.2 V	25°C		24	38	mΩ
				Full			40	
			V_{IN} = 0.8 V	25°C		24	38	mΩ
				Full			40	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0V, I_{OUT} = 1 mA		Full		275	325	Ω

SWITCHING CHARACTERISTIC MEASUREMENT INFORMATION



TEST CIRCUIT



tON/tOFF WAVEFORMS

(A) Rise and fall times of the control signal is 100ns.

Figure 1. Test Circuit and Timing Waveforms

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10-Ω, C_L = 0.1 µF, C_T = 1000 pF		1325		µs
t_{OFF}	Turn-off time			10		
t_R	V_{OUT} rise time			1625		
t_F	V_{OUT} fall time			3.5		
t_D	ON delay time			500		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10-Ω, C_L = 0.1 µF, C_T = 1000 pF		600		µs
t_{OFF}	Turn-off time			80		
t_R	V_{OUT} rise time			300		
t_F	V_{OUT} fall time			5.5		
t_D	ON delay time			460		
V_{IN} = 2.5V, V_{ON} = 5 V, V_{BIAS} = 2.5V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10-Ω, C_L = 0.1 µF, C_T = 1000 pF		2200		µs
t_{OFF}	Turn-off time			9		
t_R	V_{OUT} rise time			2275		
t_F	V_{OUT} fall time			3.1		
t_D	ON delay time			1075		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10-Ω, C_L = 0.1 µF, C_T = 1000 pF		1450		µs
t_{OFF}	Turn-off time			60		
t_R	V_{OUT} rise time			875		
t_F	V_{OUT} fall time			5.5		
t_D	ON delay time			1010		

FUNCTIONAL BLOCK DIAGRAM

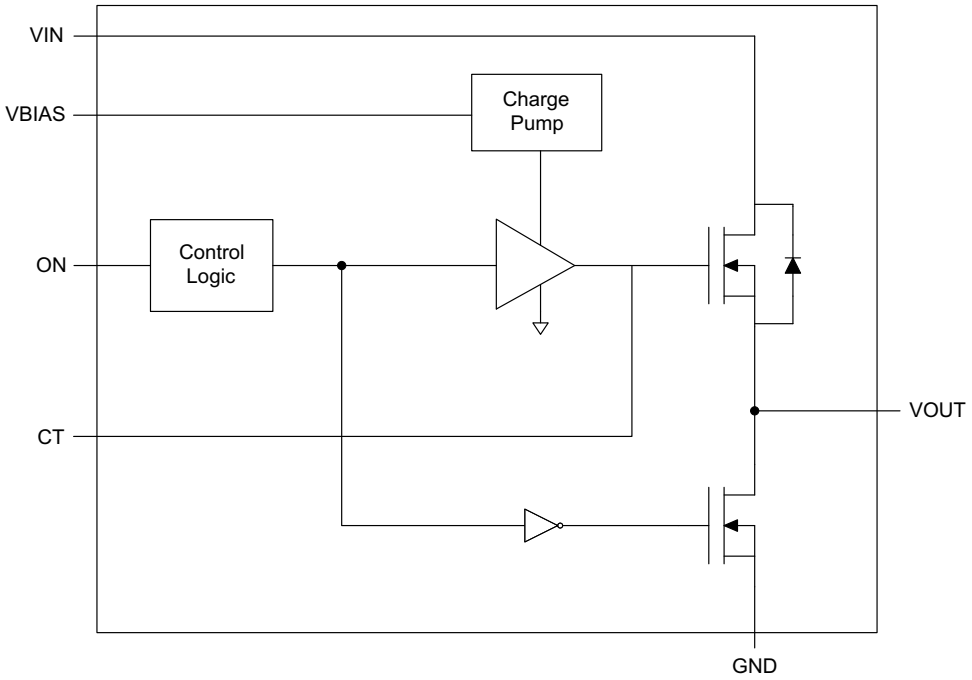
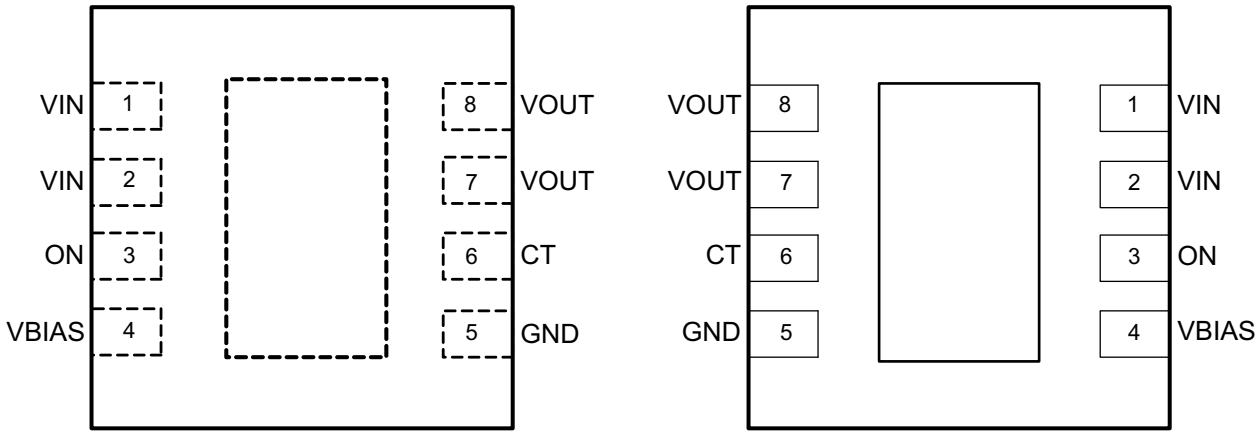


Figure 2. Functional Block Diagram

Table 1. FUNCTIONAL TABLE

ON	VIN to VOUT	VOUT to GND
L	Off	On
H	On	Off

DSG PACKAGE



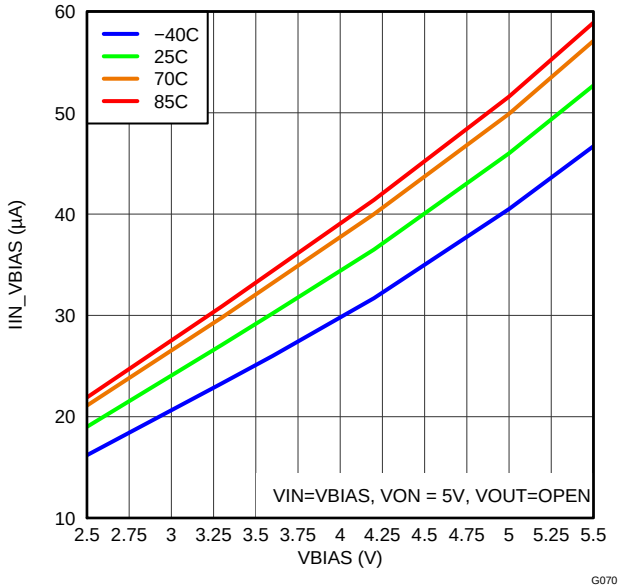
TOP VIEW BOTTOM VIEW

PIN DESCRIPTIONS

TPS22967 DSG	PIN NAME	I/O	DESCRIPTION
1	VIN	I	Switch input. Input capacitor recommended for minimizing V_{IN} dip. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{BIAS}.
2	VIN	I	Switch input. Input capacitor recommended for minimizing V_{IN} dip. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{BIAS}.
3	ON	I	Active high switch control input. Do not leave floating.
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V. See Application Information section for more information.
5	GND	-	Device ground.
6	CT	O	Switch slew rate control. Can be left floating. See Application Information section for more information.
7	VOUT	O	Switch output.
8	VOUT	O	Switch output.
	Thermal Pad	-	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See Application Information for layout guidelines.

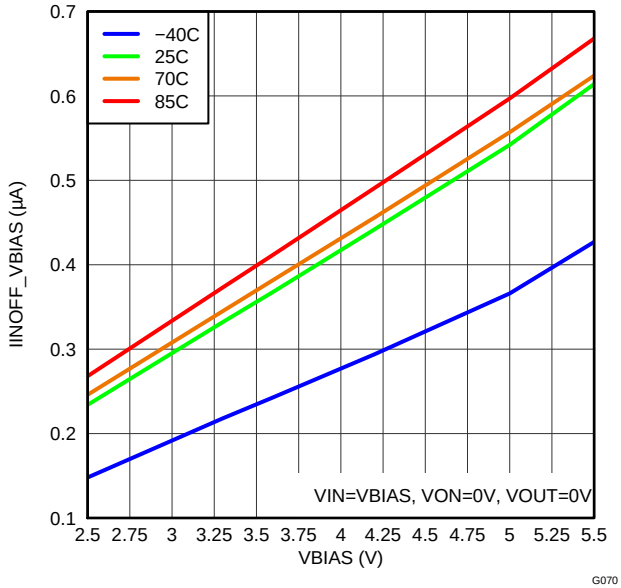
TYPICAL CHARACTERISTICS

V_{BIAS} vs. QUIESCENT CURRENT



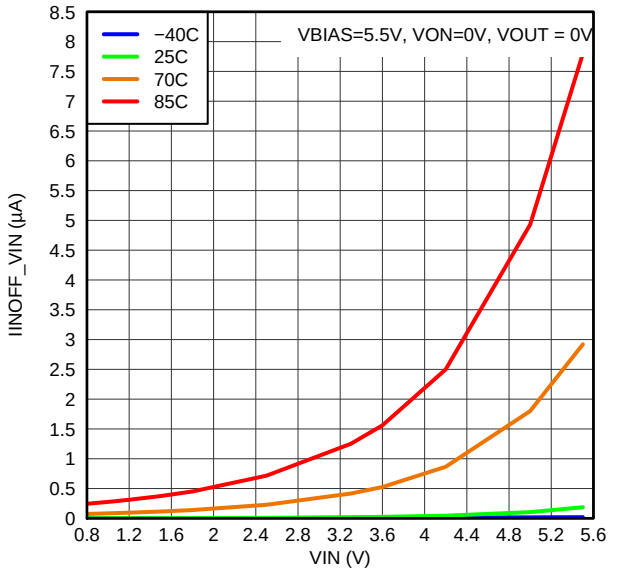
G070

V_{BIAS} vs. SHUTDOWN CURRENT



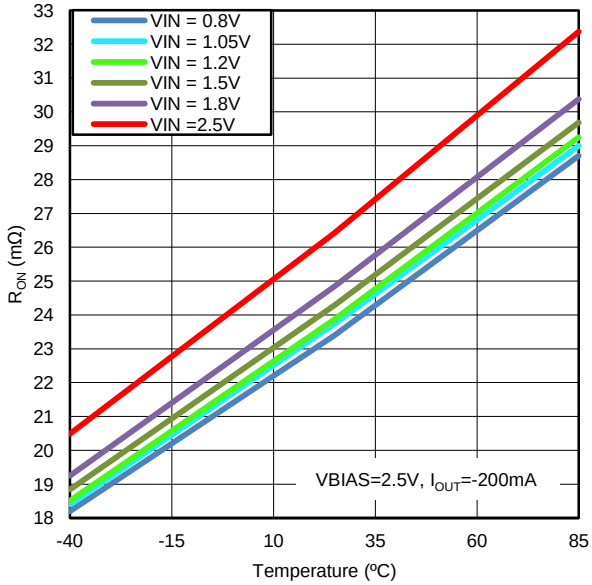
G070

V_{IN} vs. OFF-STATE VIN CURRENT



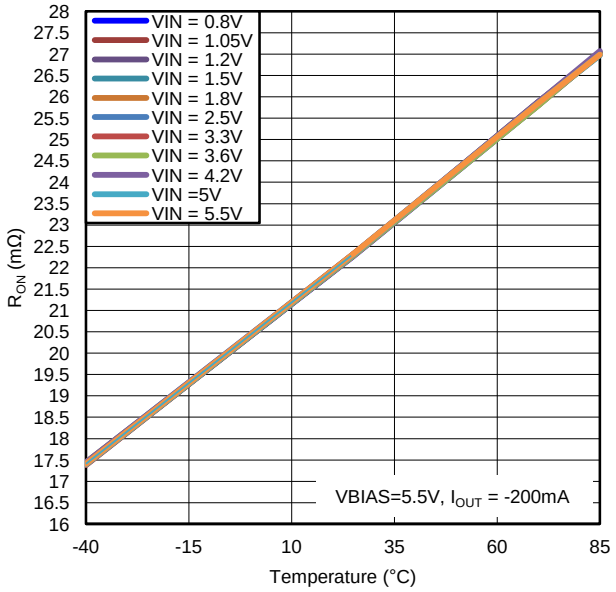
G067

TEMPERATURE vs. R_{ON} (V_{BIAS} = 2.5V)

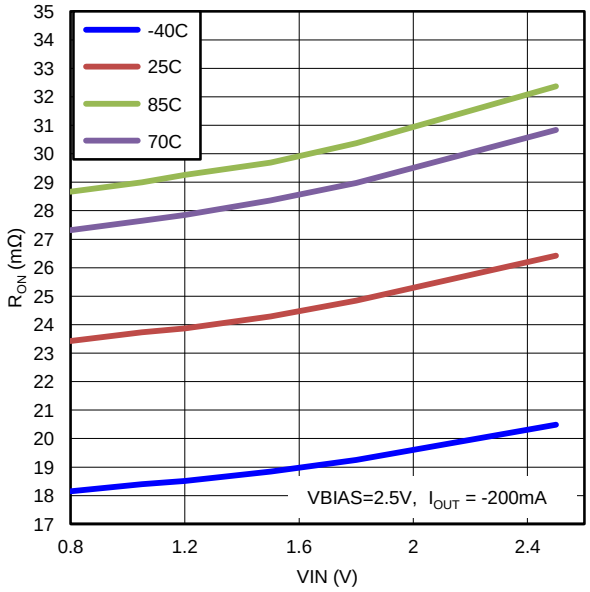


TYPICAL CHARACTERISTICS (continued)

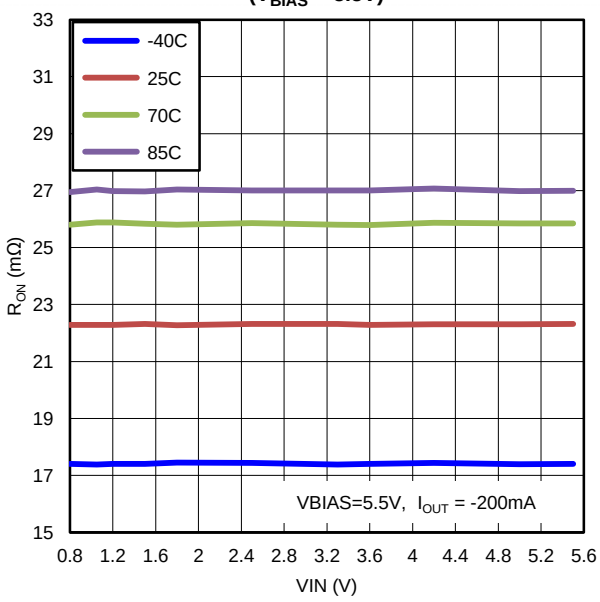
TEMPERATURE vs. R_{ON} (V_{BIAS} = 5.5V)



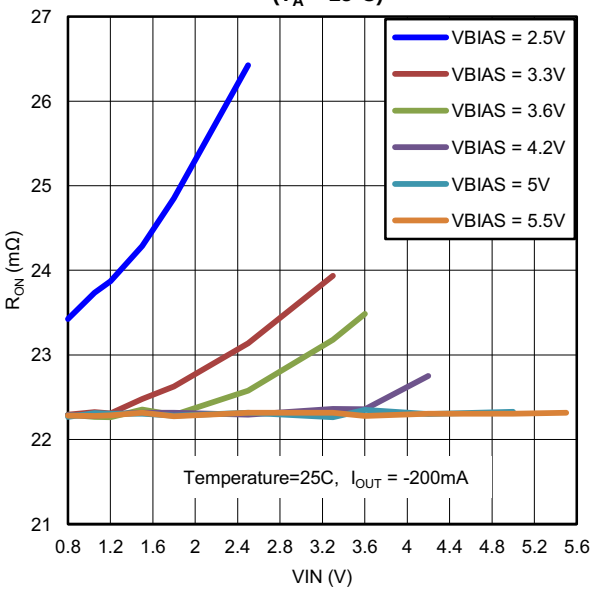
V_{IN} vs. R_{ON} (V_{BIAS} = 2.5V)



V_{IN} vs. R_{ON} (V_{BIAS} = 5.5V)

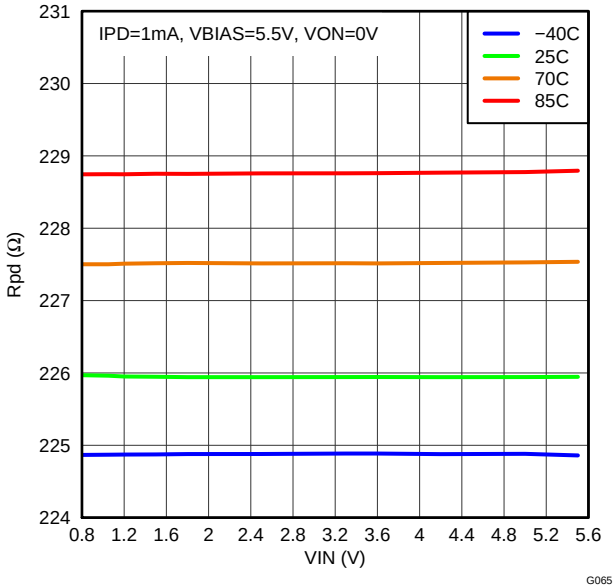


V_{IN} vs. R_{ON} (T_A = 25°C)

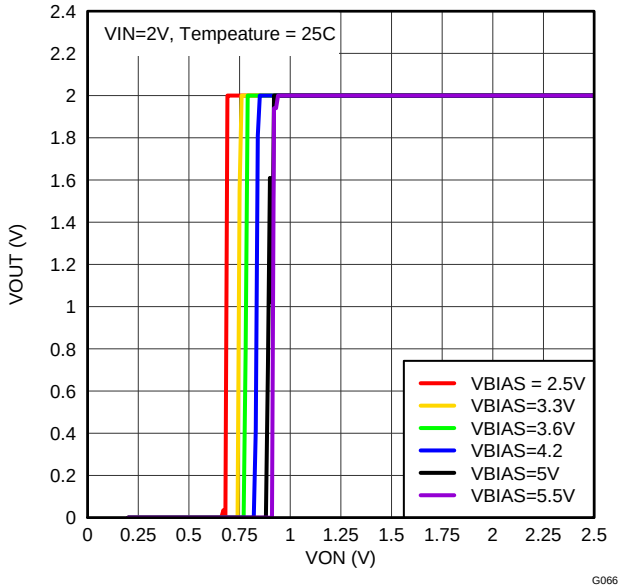


TYPICAL CHARACTERISTICS (continued)

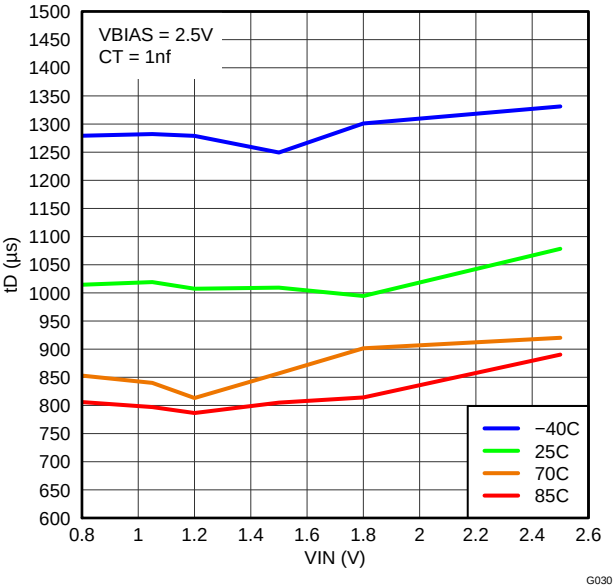
VIN vs. R_{PD} (V_{BIAS} = 5.5V)



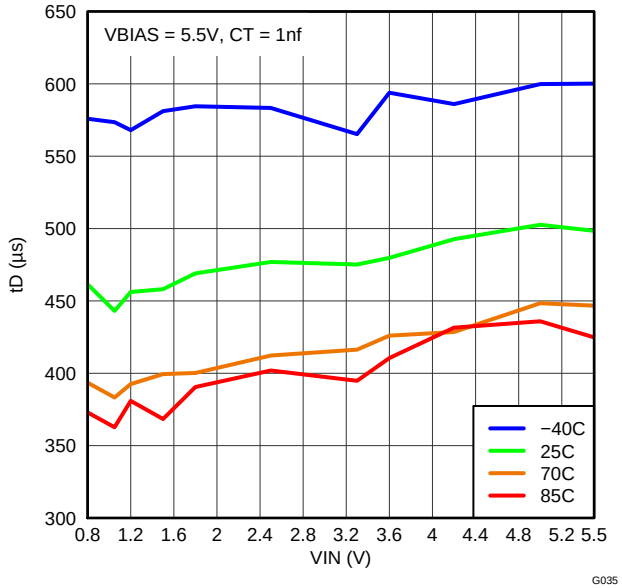
V_{ON} vs. V_{OUT} (T_A = 25°C)



V_{IN} vs. t_D (V_{BIAS} = 2.5V, CT = 1nF)

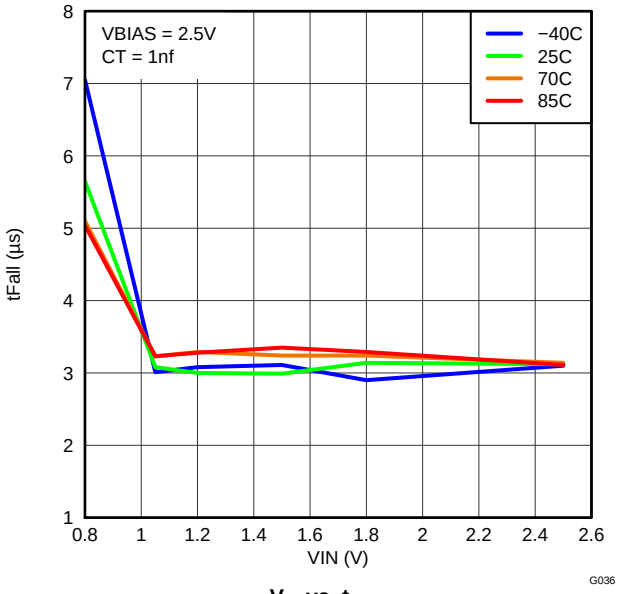


V_{IN} vs. t_D (V_{BIAS} = 5.5V, CT = 1nF)

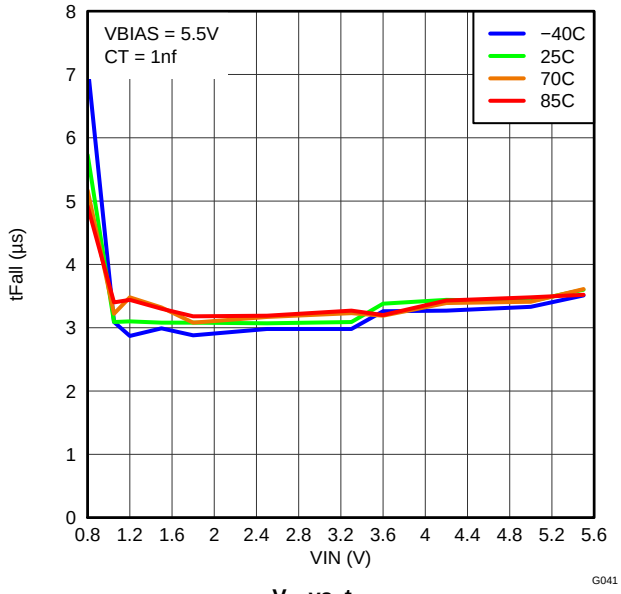


TYPICAL CHARACTERISTICS (continued)

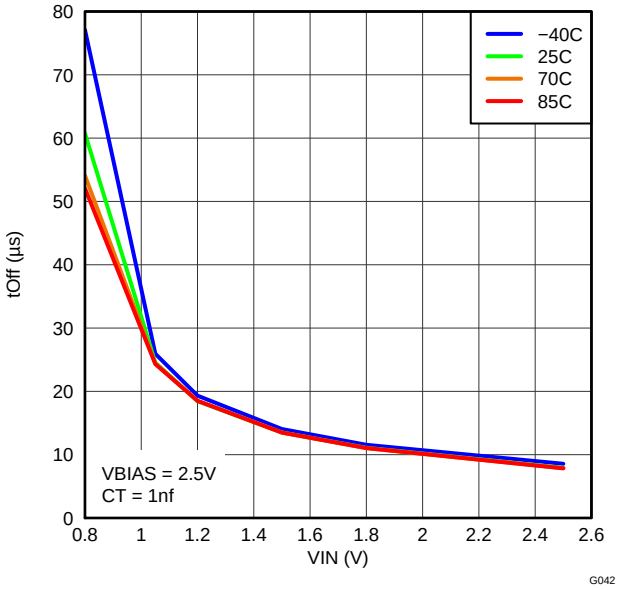
V_{IN} vs. t_F (V_{BIAS} = 2.5V, CT = 1nF)



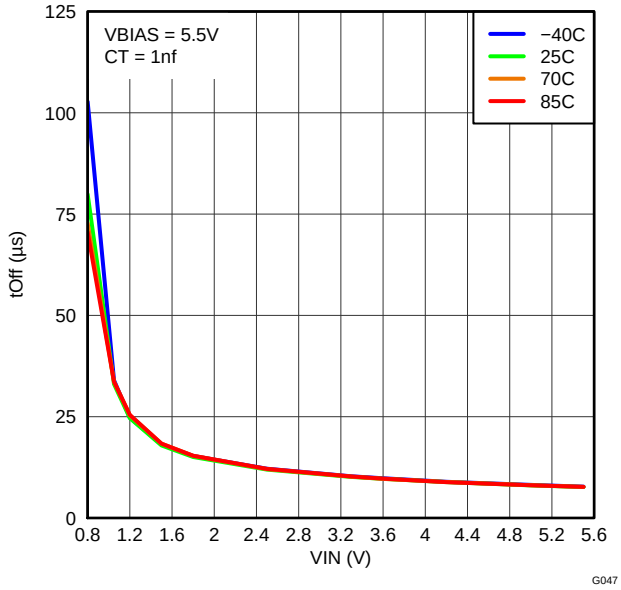
V_{IN} vs. t_F (V_{BIAS} = 5.5V, CT = 1nF)



V_{IN} vs. t_{OFF} (V_{BIAS} = 2.5V, CT = 1nF)

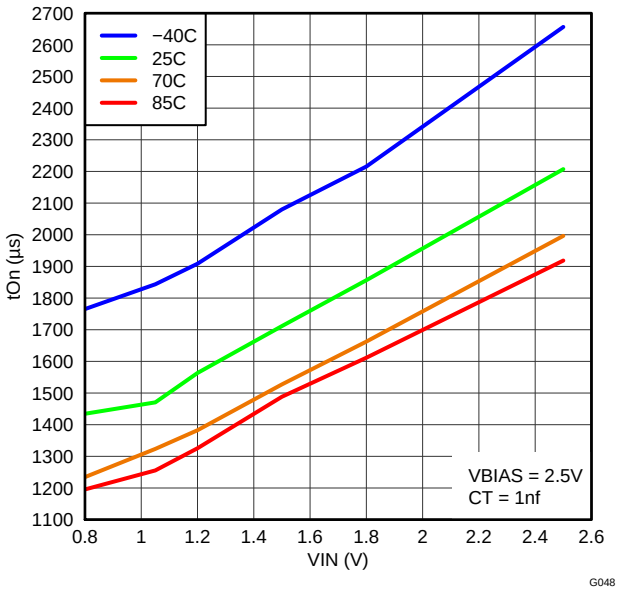


V_{IN} vs. t_{OFF} (V_{BIAS} = 5.5V, CT = 1nF)

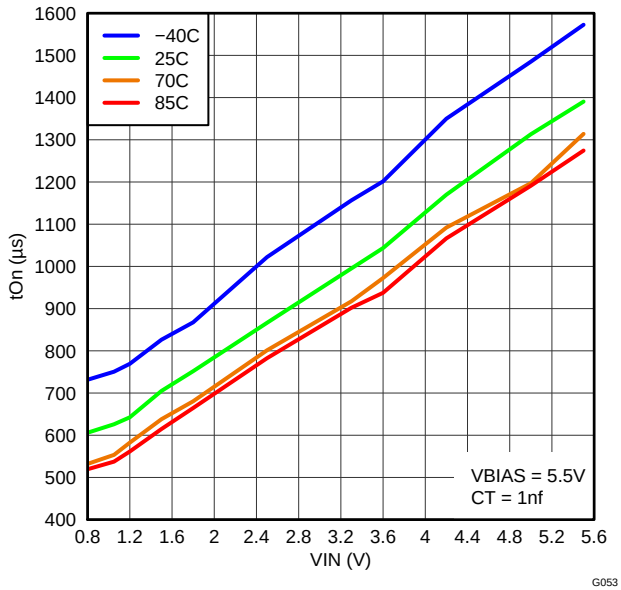


TYPICAL CHARACTERISTICS (continued)

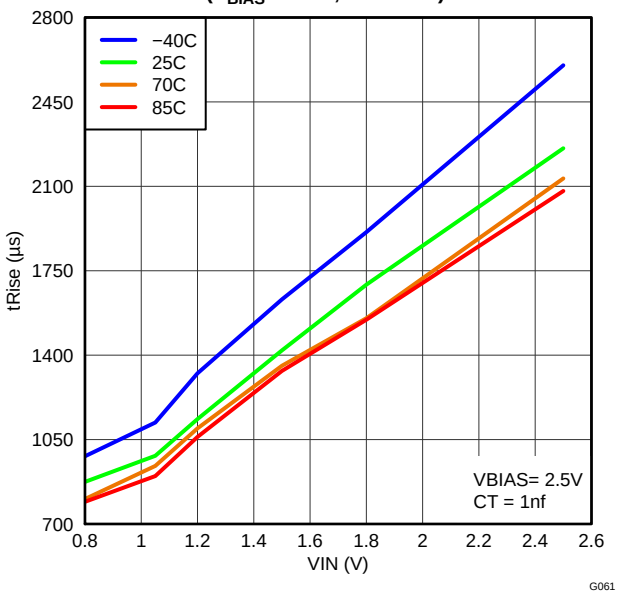
V_{IN} vs. t_{ON} (V_{BIAS} = 2.5V, CT = 1nF)



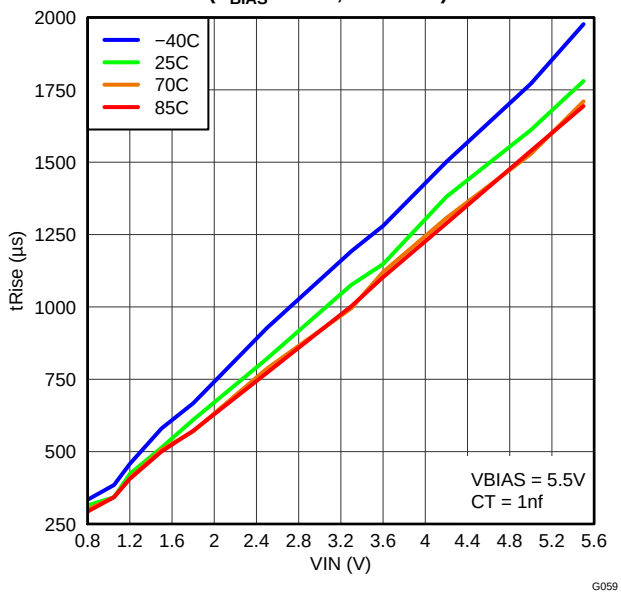
V_{IN} vs. t_{ON} (V_{BIAS} = 5.5V, CT = 1nF)



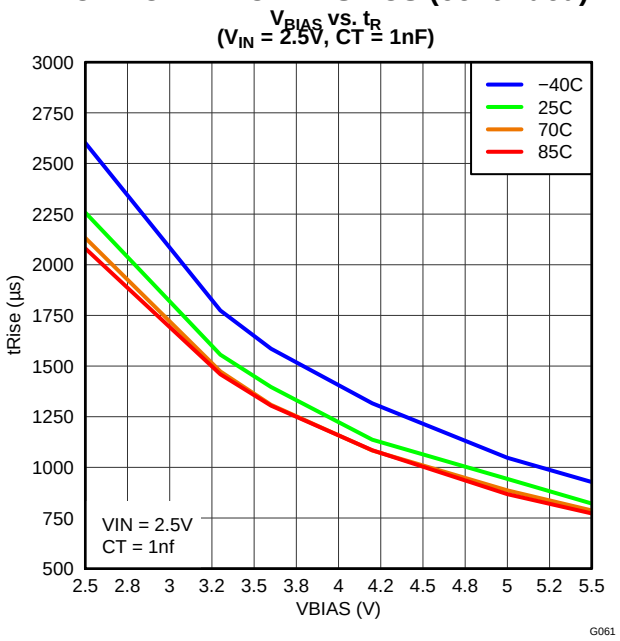
V_{IN} vs. t_R (V_{BIAS} = 2.5V, CT = 1nF)



V_{IN} vs. t_R (V_{BIAS} = 5.5V, CT = 1nF)

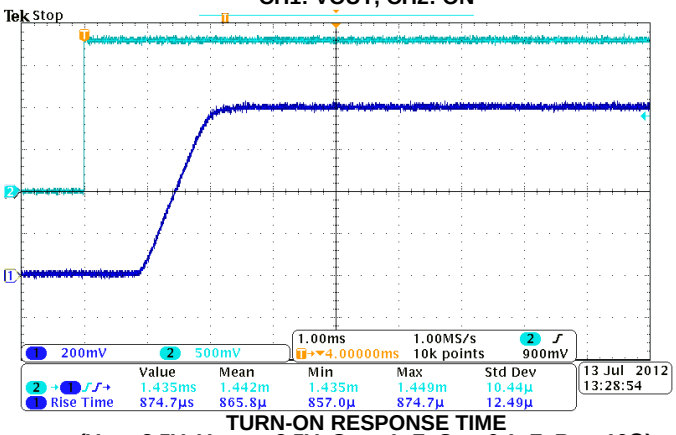


TYPICAL CHARACTERISTICS (continued)

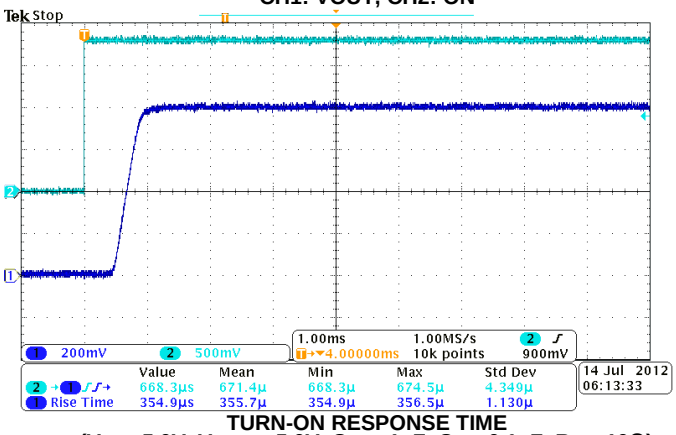


TYPICAL AC SCOPE CAPTURES at T_A = 25ºC, CT = 1nF

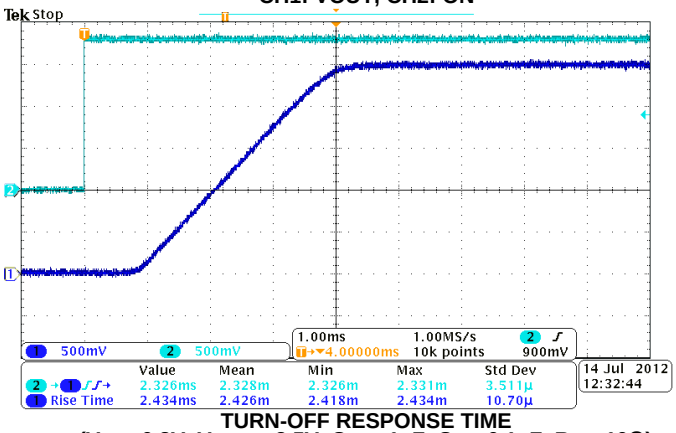
TURN-ON RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



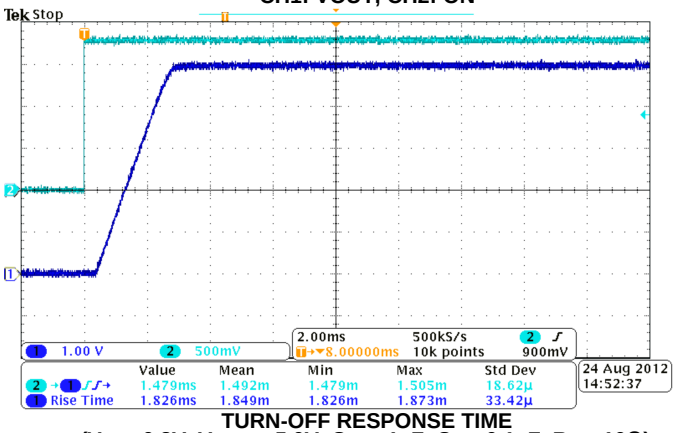
TURN-ON RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



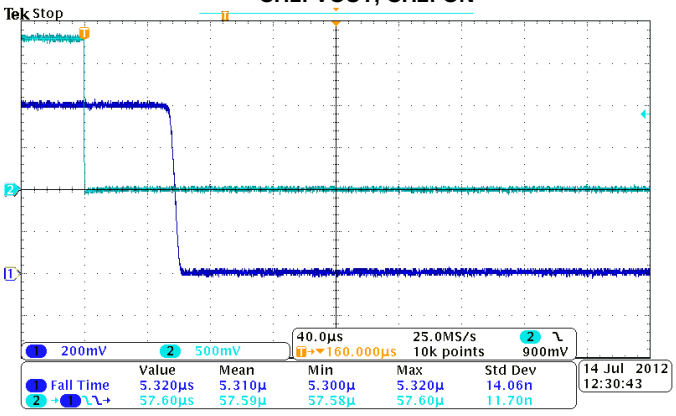
TURN-ON RESPONSE TIME
(V_{IN} = 2.5V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



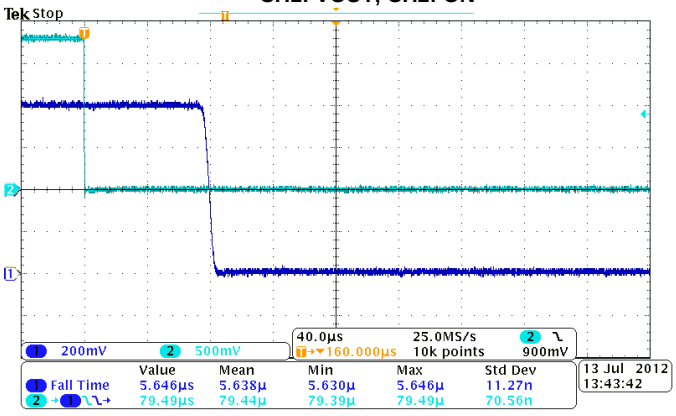
TURN-ON RESPONSE TIME
(V_{IN} = 5.0V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



TURN-OFF RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON

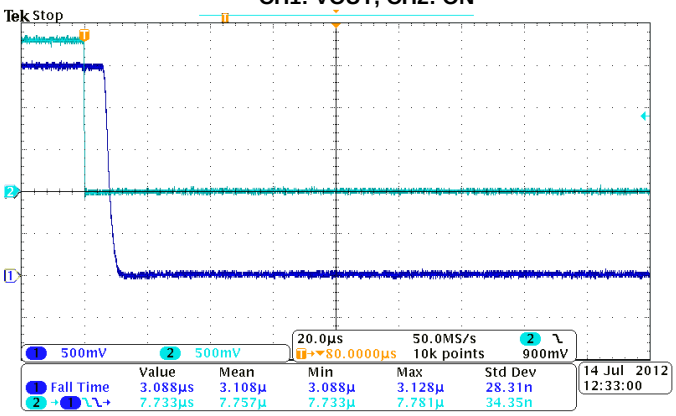


TURN-OFF RESPONSE TIME
(V_{IN} = 0.8V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON

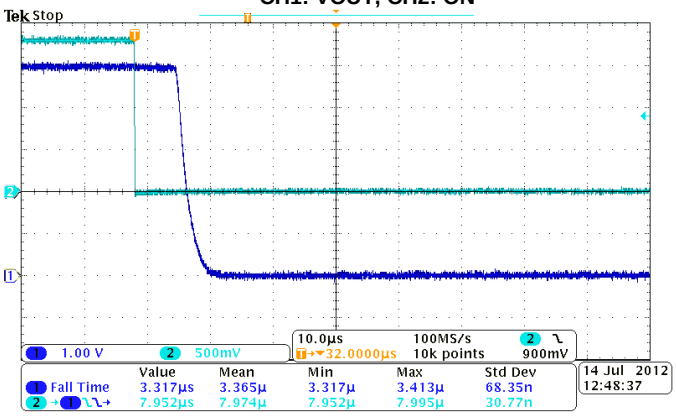


TYPICAL AC SCOPE CAPTURES at T_A = 25°C, CT = 1nF (continued)

TURN-OFF RESPONSE TIME
(V_{IN} = 2.5V, V_{BIAS} = 2.5V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



TURN-OFF RESPONSE TIME
(V_{IN} = 5.0V, V_{BIAS} = 5.0V, C_{IN} = 1µF, C_L = 0.1µF, R_L = 10Ω)
CH1: VOUT, CH2: ON



APPLICATION INFORMATION

ON/OFF CONTROL

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

INPUT CAPACITOR (OPTIONAL)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

OUTPUT CAPACITOR (OPTIONAL)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see below).

V_{IN} and V_{BIAS} VOLTAGE RANGE

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the ELECTRICAL CHARACTERISTICS table. See Figure 3 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for VIN and VBIAS.

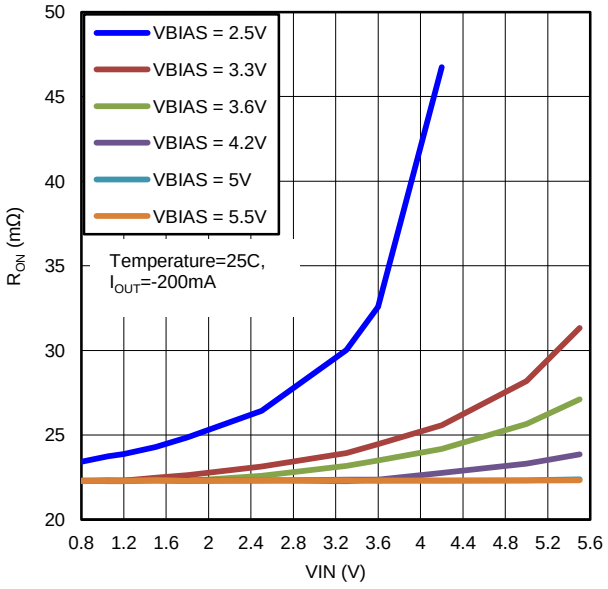


Figure 3. R_{ON} vs. V_{IN} ($V_{IN} > V_{BIAS}$)

ADJUSTABLE RISE TIME

A capacitor to GND on the CT pin sets the VOUT slew rate. The voltage on the CT pin can be as high as 12V. Therefore, the minimum voltage rating for the CT cap should be 25V for optimal performance. An approximate formula for the relationship between CT and slew rate is (the equation below accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CT = 0pF. Use table below to determine rise times for when CT = 0pF):

$$SR = 0.39 \times CT + 13.4 \quad (1)$$

Where,

SR = slew rate (in µs/V)

CT = the capacitance value on the CT pin (in pF)

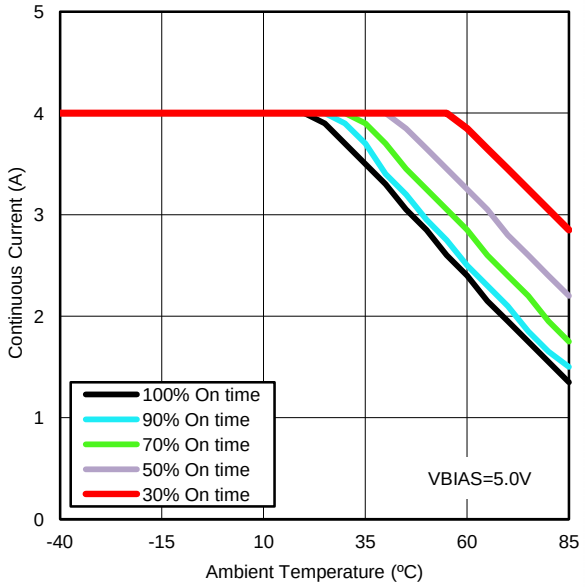
The units for the constant 13.4 is in µs/V. The units for the constant 0.39 are in µs/(V*pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the ON pin is asserted high.

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1µF, C_{IN} = 1µF, R_L = 10Ω TYPICAL VALUES at 25°C, 25V X7R 10% CERAMIC CAP						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	127	93	62	55	51	46	42
220	475	314	188	162	141	125	103
470	939	637	359	304	255	218	188
1000	1869	1229	684	567	476	414	344
2200	4020	2614	1469	1211	1024	876	681
4700	8690	5746	3167	2703	2139	1877	1568
10000	18360	12550	6849	5836	4782	4089	3449

SAFE OPERATING AREA (SOA)

The SOA curves show the continuous current carrying capability of the device versus ambient temperature (T_A) to ensure reliable operation over 70,000 hours of device lifetime. The different curves represent the *percentage On time* over device lifetime and can be used as a reference to understand the current carrying capability of TPS22967 under different use cases. It is recommended to maintain continuous current at or below the SOA curves shown in Figure 4.



"On time" is the duration of time that the device is enabled (ON ≥ V_{IH}) over 70,000 hour lifetime.

Figure 4. Safe Operating Area

BOARD LAYOUT AND THERMAL CONSIDERATIONS

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

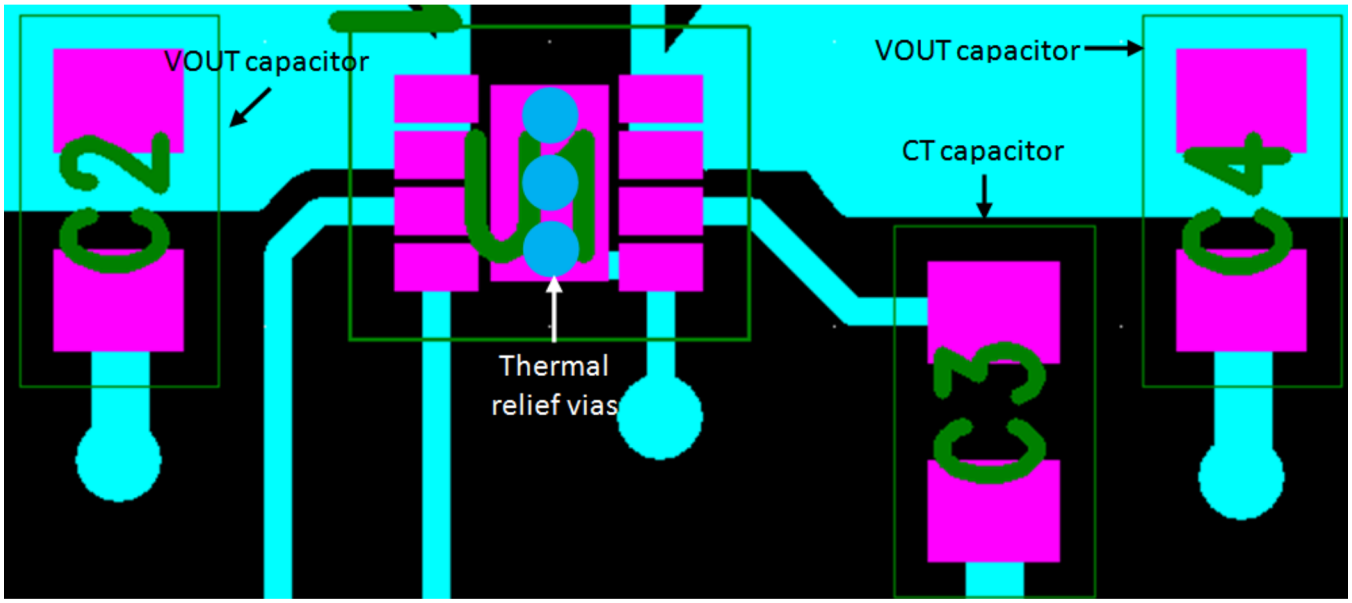
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\Theta_{JA}} \quad (2)$$

Where:

$P_{D(max)}$ = maximum allowable power dissipation
$T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22967)
T_A = ambient temperature of the device
Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

The figure below shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22967DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTU	Samples
TPS22967DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

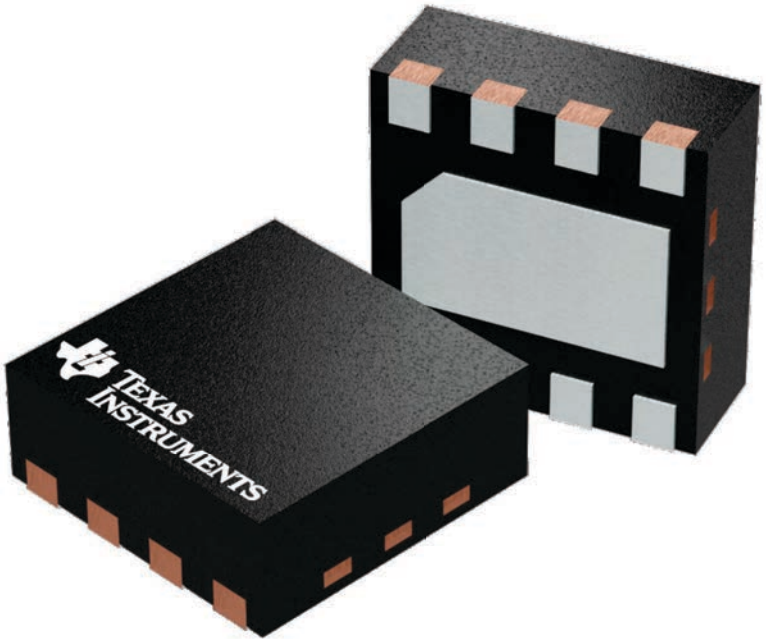
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



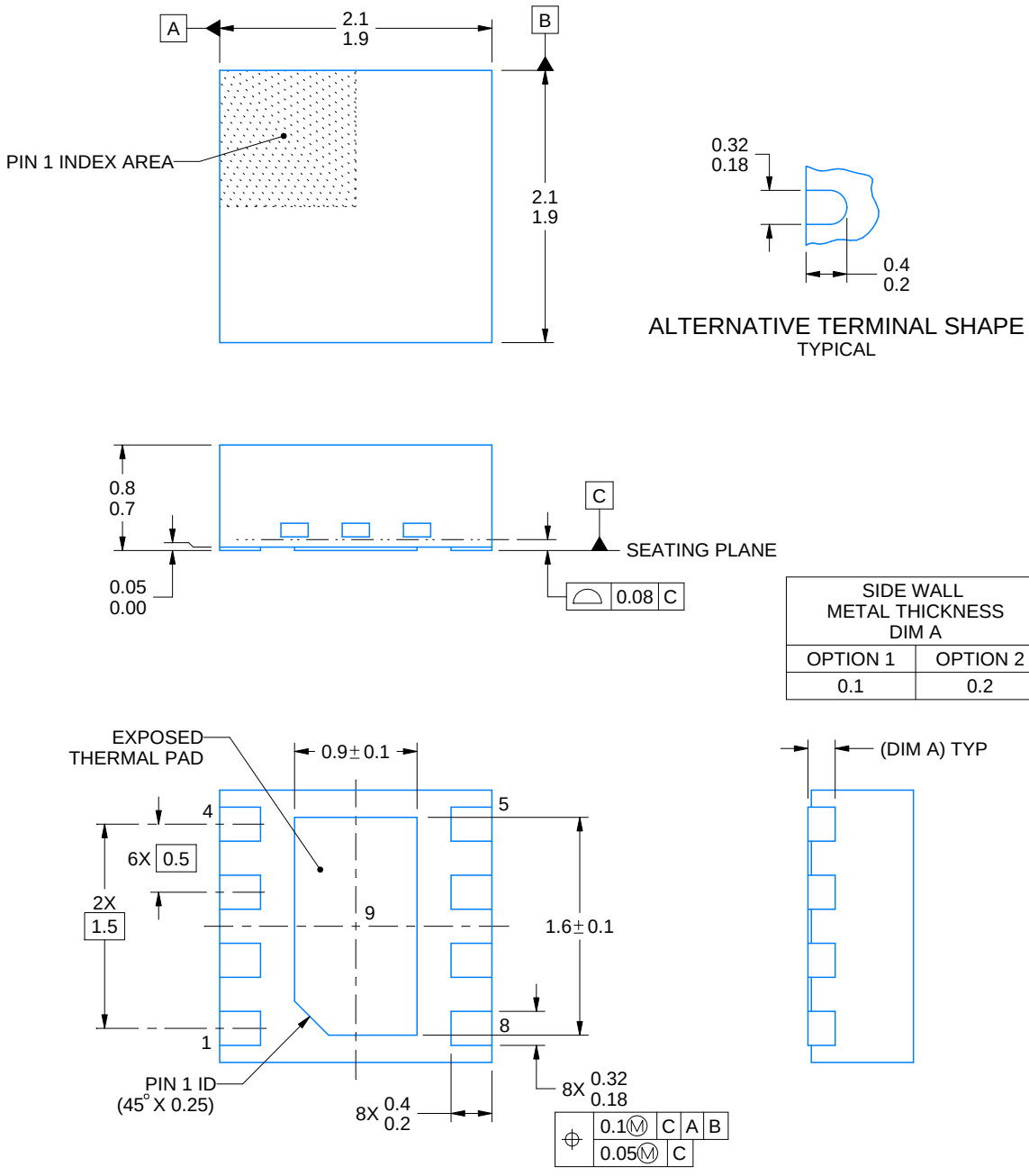
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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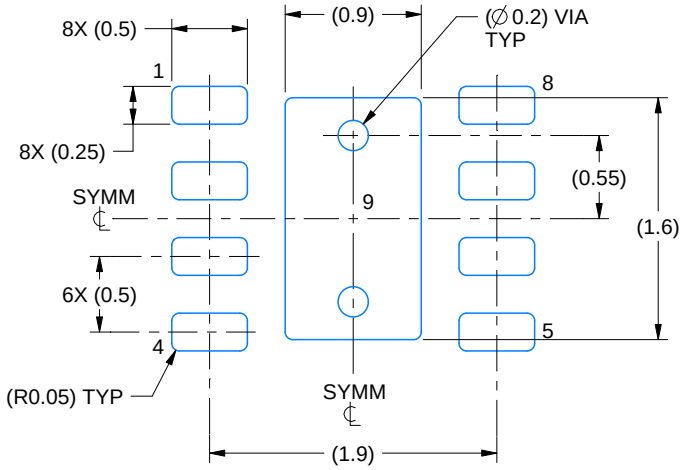
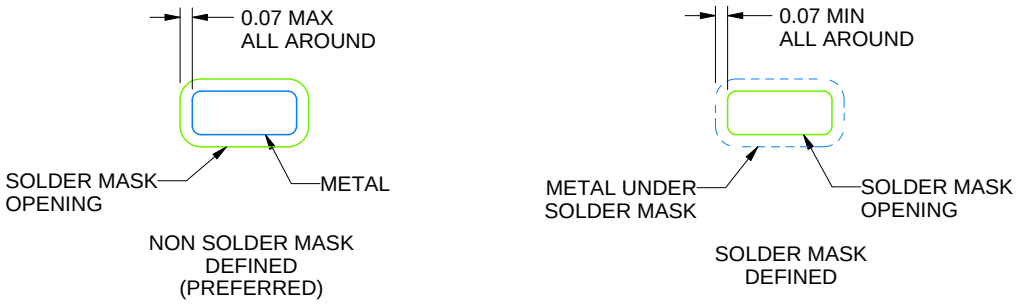
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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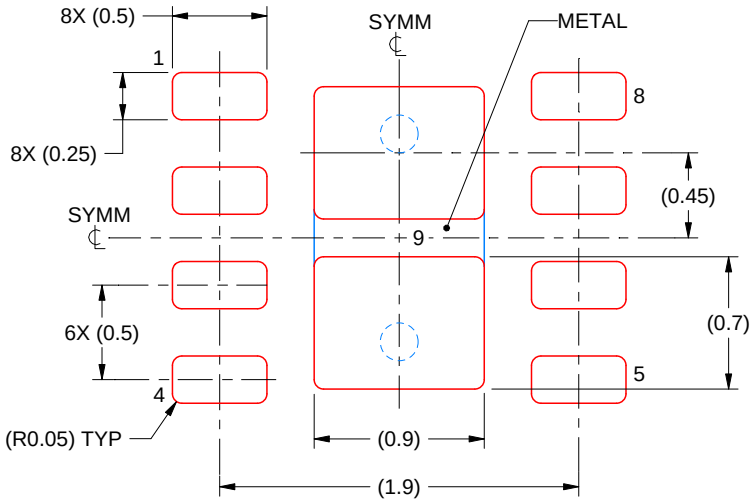
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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