# TPD4S311、TPD4S311A USB Type-C™ 端口保护器：$V_{BUS}$ 短路过压和 IEC ESD 保护

## 1 特性

- 4 通道 $V_{BUS}$ 短路过压保护（CC1、CC2、SBU1、SBU2）：可耐受 $24V_{DC}$ 电压
- 4 通道 IEC 61000-4-2 ESD 保护（CC1、CC2、SBU1、SBU2）
- CC1 和 CC2 过压保护 FET 可支持 $V_{CONN}$ 通过电流
  - 400mA $V_{CONN}$ 电流 (TPD4S311)
  - 600mA $V_{CONN}$ 电流 (TPD4S311A)
- CC 引脚上提供 ±35V 浪涌保护 (TPD4S311A)
- SBU 引脚上提供 ±30V 浪涌保护 (TPD4S311A)
- 集成 CC 无电电池电阻器，可用于处理移动设备中的无电电池用例
- 1.69mm × 1.69mm DSBGA 封装

## 2 应用

- 台式计算机/主板
- 标准笔记本电脑
- Chromebook 和 WOA
- 集线站
- 端口/线缆适配器和加密狗
- 智能手机

## 3 说明

TPD4S311 是一款单芯片 USB Type-C 端口保护器件，可提供 20V $V_{BUS}$ 短路过压保护和 IEC ESD 保护。

自从 USB Type-C 连接器发布以来，市场上已经发布了很多不符合 USB Type-C 规格的 USB Type-C 产品和配件。其中的一个示例就是仅在 $V_{BUS}$ 线路上布设 20V 电压的 USB Type-C 电力输送适配器。USB Type-C 的另一个问题是，由于此小型连接器中的各引脚极为靠近，因此连接器的机械扭转和滑动可能使引脚短路。这可能导致 20V $V_{BUS}$ 与 CC 和 SBU 引脚短路。此外，由于 Type-C 连接器中的各引脚极为靠近，所以存在碎屑和水气导致 20V $V_{BUS}$ 引脚与 CC 和 SBU 引脚短路的严重问题。

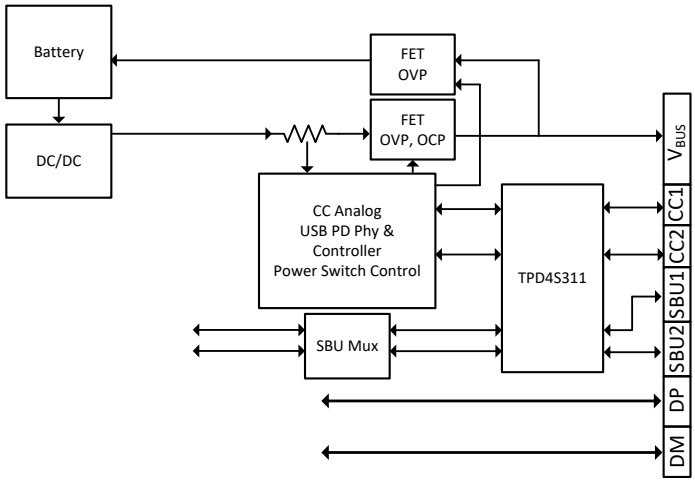
这些非理想的设备和机械事件使得 CC 和 SBU 引脚必须能够承受 20V 的电压，即使这些引脚仅在 5V 或更低电压下工作。通过在 CC 和 SBU 引脚上提供过压保护，TPD4S311 可以使 CC 和 SBU 引脚耐受 20V 的电压，同时不会干扰正常运行。该器件将高压 FET 串联放置在 SBU 和 CC 线路上。当在这些线路上检测到高于 OVP 阈值的电压时，高压开关被打开，并且将系统的其余部分与连接器上存在的高压状态隔离。

最后，大多数系统都需要为其外部引脚应用 IEC 61000-4-2 系统级 ESD 保护。TPD4S311 为 CC1、CC2、SBU1 和 SBU2 引脚集成了 IEC 61000-4-2 ESD 保护，无需再在连接器上（外部）放置高电压 TVS 二极管。

**器件信息**(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPD4S311 | DSBGA (16) | 1.69 mm × 1.69 mm |
| TPD4S311A | DSBGA (16) | 1.69 mm × 1.69 mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




**CC 和 SBU 过压保护**

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision B (August 2020) to Revision C (February 2021) | Page |
|---|---|
| • 添加了 A 版本器件 | 1 |
| • Added A version of the device | 3 |
| • Added A version of the device to Absolute Maximum Ratings table | 5 |
| • Added A version to ESD Ratings—IEC Specification table | 5 |
| • Added A version to Recommended Operating Conditions table | 5 |
| • Added A version to Electrical Characteristics table | 6 |
| • Added A version of the device to Detailed Description section | 16 |

| Changes from Revision A (April 2020) to Revision B (August 2020) | Page |
|---|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式 | 1 |
| • Added $I_O$ row in Absolute Maximum Ratings table | 5 |
| • Deleted 1.2 A spec from Recommended Operating Conditions table | 5 |
| • Updated $I_{VCONN}$ max current to 400 mA in Recommended Operating Conditions table | 5 |
| • Added table note to Recommended Operating Conditions table | 5 |
| • Updated 图 7-3 caption to 24 V | 9 |
| • Updated 图 7-4 caption to 24 V | 9 |
| • Updated 图 7-17 caption to 24 V | 9 |
| • Updated 图 7-18 caption to 24 V | 9 |
| • Updated 图 7-17 | 9 |
| • Updated 图 7-18 | 9 |

| Changes from Revision * (December 2019) to Revision A (September 2020) | Page |
|---|---|
| • 更新了附带链接的应用 部分 | 1 |
| • 将封装类型名称从 WCSP 更改为 DSBGA；全局更改 | 1 |


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## 5 Device Comparison Table

| Part Number | Channels and Protection | Vconn Current | CC On Resistance |
|---|---|---|---|
| TPD4S311 | 4-Ch (CC1, CC2, SBU1, SBU2 ) overvoltage protection.<br>4-Ch (CC1, CC2, SBU1, SBU2) IEC 61000-4-2 ESD protection. | 400 mA | 378 mΩ |
| TPD4S311A | 4-Ch (CC1, CC2, SBU1, SBU2 ) overvoltage protection.<br>4-Ch (CC1, CC2, SBU1, SBU2) IEC 61000-4-2 ESD protection.<br>4-Ch (CC1, CC2, SBU1, SBU2) IEC 61000-4-5 Surge Protection. | 600 mA | 232 mΩ |

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# 6 Pin Configuration and Functions

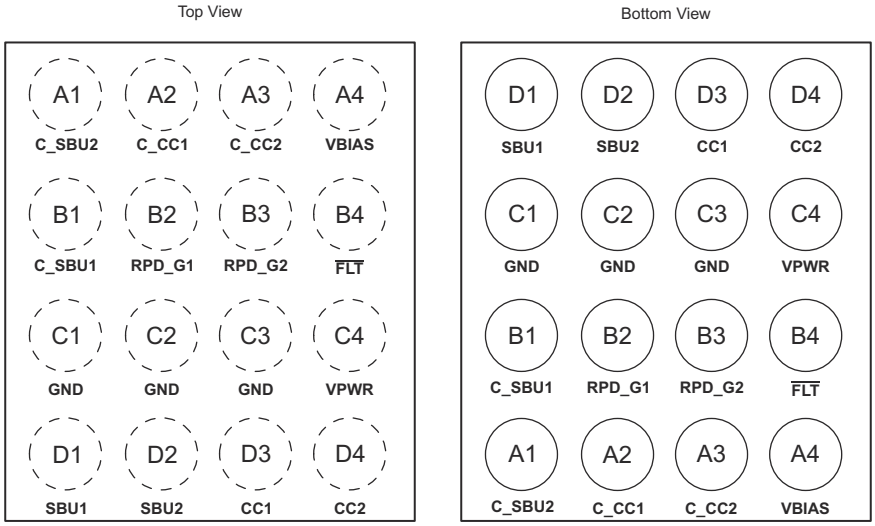


**图 6-1. YBF Package 16-Pin DSBGA**

**表 6-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| A1 | C_SBU2 | I/O | Connector side of the SBU2 OVP FET. Connect to either SBU pin of the USB Type-C connector. |
| A2 | C_CC1 | I/O | Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector. |
| A3 | C_CC2 | I/O | Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector. |
| A4 | VBIAS | P | Pin for ESD support capacitor. Place a 0.1-µF capacitor on this pin to ground. |
| B1 | C_SBU1 | I/O | Connector side of the SBU1 OVP FET. Connect to either SBU pin of the USB Type-C connector. |
| B2 | RPD_G1 | I/O | Short to C_CC1 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND. |
| B3 | RPD_G2 | I/O | Short to C_CC2 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND. |
| B4 | $\overline{\text{FLT}}$ | O | Open drain for fault reporting. |
| C1, C2, C3 | GND | GND | Ground |
| C4 | VPWR | P | 2.7-V to 4.5-V power supply. |
| D1 | SBU1 | I/O | System side of the SBU1 OVP FET. Connect to either SBU pin of the SBU MUX. |
| D2 | SBU2 | I/O | System side of the SBU2 OVP FET. Connect to either SBU pin of the SBU MUX. |
| D3 | CC1 | I/O | System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller. |
| D4 | CC2 | I/O | System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller. |

(1) I = input, O = output, I/O = input and output, GND = ground, P = power


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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage | VPWR | –0.3 | 5 | V |
| | | RPD_G1, RPD_G2 | –0.3 | 24 | V |
| $V_O$ | Output voltage | $\overline{FLT}$ | –0.3 | 6 | V |
| | | VBIAS | –0.3 | 24 | V |
| $V_{IO}$ | I/O voltage | CC1, CC2, SBU1, SBU2 | –0.3 | 6 | V |
| | | C_CC1, C_CC2, C_SBU1, C_SBU2 | –0.3 | 24 | V |
| $I_O$ | Output Current | C_CC1, C_CC2 (TPD4S311) | | 950 | mA |
| | | C_CC1, C_CC2 (TPD4S311A) | | 1.2 | A |
| $T_A$ | Operating free air temperature | | –40 | 85 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings—JEDEC Specification

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

## 7.3 ESD Ratings—IEC Specification

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge(1) | IEC 61000-4-2, C_CC1, C_CC2 | Contact discharge | ±8000 | V |
| $V_{(ESD)}$ | Electrostatic discharge(1) | IEC 61000-4-2, C_CC1, C_CC2 | Air-gap discharge | ±15000 | V |
| $V_{(ESD)}$ | Electrostatic discharge(1) | IEC 61000-4-2, C_SBU1, C_SBU2 | Contact discharge | ±6000 | V |
| $V_{(ESD)}$ | Electrostatic discharge(1) | IEC 61000-4-2, C_SBU1, C_SBU2 | Air-gap discharge | ±15000 | V |
| $V_{(Surge)}$ | Lightning and Surge | IEC 61000-4-5, C_CC1, C_CC2 (TPD4S311A) | | ±35 | V |
| | | IEC 61000-4-5, C_SBU1, C_SBU2 (TPD4S311A) | | ±30 | V |

(1) Tested with connection to the TPS65982 EVM.

## 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_I$ | Input voltage | VPWR | 2.7 | 3.3 | 4.5 | V |
| | | RPD_G1, RPD_G2 | 0 | | 5.5 | V |
| $V_O$ | Output voltage | $\overline{FLT}$ Pull-up resistor power rail | 2.7 | | 5.5 | V |
| $V_{IO}$ | I/O voltage | CC1, CC2, C_CC1, C_CC2 | 0 | | 5.5 | V |
| | | SBU1, SBU2, C_SBU1, C_SBU2 | 0 | | 4.3 | V |

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## 7.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{VCONN}$ | $V_{CONN}$ Current | Current flowing into CC1/2 and flowing out of C_CC1/2, 4.5 ⩽ CCx ⩽ 5.5, $T_J$ ⩽ 85 ℃ (TPD4S311) | | | 400(1) | mA |
| | | Current flowing into CC1/2 and flowing out of C_CC1/2, 4.5 ⩽ CCx ⩽ 5.5, $T_J$ ⩽ 105 ℃ (TPD4S311A) | | | 600 | mA |
| | | Current flowing into CC1/2 and flowing out of C_CC1/2, 4.5 ⩽ CCx ⩽ 5.5, $T_J$ ⩽ 70 ℃ (TPD4S311A) | | | 1.2 | A |
| External Components(2) | | $\overline{FLT}$ Pull-up resistance | 1.7 | | 300 | kΩ |
| | | VBIAS capacitance(3) | | 0.1 | | µF |
| | | VPWR Capacitance | 0.3 | 1 | | µF |

(1) $V_{conn}$ current loading beyond the values listed in *Recommended Operating Conditions* may degrade the operating lifetime of the device.
(2) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented should be within the minimum and maximums listed in the table.
(3) The VBIAS pin requires a minimum 35-VDC rated capacitor. A 50-VDC rated capacitor is recommended to reduce capacitance derating.
See the VBIAS Capacitor Selection section for more information on selecting the VBIAS capacitor.

## 7.5 Thermal Information

| THERMAL METRIC(1) | | TPD4S311 YBF DSBGA 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 84.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 21.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 21.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CC OVP Switches** | | | | | | |
| $R_{ON}$ | On Resistance of CC OVP FETs | CCx = 5.5 V, $T_J$ ⩽ 85 ℃ (TPD4S311) | | 378 | 550 | mΩ |
| | | CCx = 5.5 V, $T_J$ ⩽ 85 ℃ (TPD4S311A) | | 232 | 405 | mΩ |
| $C_{ON_CC}$ | Equivalent on Capacitance | Capacitance from CCx or C_CCx to GND when device is powered. Measure at $V_{C_CCx}/V_{CCx}$ = 0 V to 1.2 V, f = 400 kHz. | 45 | 74 | 120 | pF |
| RD_DB | Dead Battery Pull-Down Resistors (only present when device is unpowered) | $V_{C_CCx}$ = 2.6 V | 4.1 | 5.1 | 6.1 | kΩ |
| VTH_DB | Threshold voltage of the pull-down FET in series with RD during dead battery | $I_{C_CCx}$ = 80 µA | 0.5 | 0.9 | 1.2 | V |
| $V_{OVPCC}$ | OVP Threshold on CC Pins | Place 5.5 V on C_CCx. Step up C_CCx until $\overline{FLT}$ pin is asserted. Put 100-mA load through the CC FET and see the FET shuts off. | 5.75 | 6.0 | 6.2 | V |
| $V_{OVPCC_HYS}$ | Hysteresis on CC OVP | Place 6.5 V on C_CCx. Step down the voltage on C_CCx until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C_CCx. | | 50 | | mV |


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## 7.6 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $BW_{ON}$ | On Bandwidth Single Ended (-3dB) | Measure the -3 dB bandwidth from C_CCx to CCx. Single ended measurement, 50-Ω system. Vcm = 0.1 V to 1.2 V. | | 100 | | MHz |
| $V_{STBUS_CC}$ | Short-to-VBUS tolerance on the CC pins | Hot-Plug C_CCx with a 1 meter USB Type C Cable, place a 30-Ω load on CCx | | | 24 | V |
| $V_{STBUS_CC_CLAMP}$ | Short-to-VBUS System-Side Clamping Voltage on the CC pins (CCx) | Hot-Plug C_CCx with a 1 meter USB Type C Cable. Hot-Plug voltage C_CCx = 24 V. VPWR = 3.3 V. Place a 30-Ω load on CCx. | | 8 | | V |
| **SBU OVP Switches** | | | | | | |
| $R_{ON}$ | On Resistance of SBU OVP FETs | SBUx = 3.6 V. –40°C ≤ TJ ≤ +85°C | | 4 | 6.5 | Ω |
| $C_{ON_SBU}$ | Equivalent on Capacitance | Capacitance from SBUx or C_SBUx to GND when device is powered. Measure at $V_{C_SBUx}/V_{SBUx}$ = 0.3 V to 4.2 V. | | 6 | | pF |
| $V_{OVPSBU}$ | OVP Threshold on SBU Pins | Place 3.6 V on C_SBUx. Step up C_SBUx until $\overline{FLT}$ pin is asserted. | 4.35 | 4.5 | 4.7 | V |
| $V_{OVPSBU_HYS}$ | Hysteresis on SBU OVP | Place 5 V on C_CCx. Step down the voltage on C_CCx until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C_SBUx. | | 50 | | mV |
| $BW_{ON}$ | On Bandwidth Single Ended (-3dB) | Measure the –3 dB bandwidth from C_SBUx to SBUx. Single ended measurement, 50-Ω system. Vcm = 0.1 V to 3.6 V. | | 900 | | MHz |
| $X_{TALK}$ | Crosstalk | Measure crosstalk at f = 1 MHz from SBU1 to C_SBU2 or SBU2 to C_SBU1. Vcm1 = 3.6 V, Vcm2 = 0.3 V. Terminate open sides to 50 Ω. | | -70 | | dB |
| $V_{STBUS_SBU}$ | Short-to-VBUS tolerance on the SBU pins | Hot-Plug C_SBUx with a 1 meter USB Type C Cable. Put a 100-nF capacitor in series with a 40-Ω resistor to GND on SBUx. | | | 24 | V |
| $V_{STBUS_SBU_CLAMP}$ | Short-to-VBUS System-Side Clamping Voltage on the SBU pins (SBUx) | Hot-Plug C_SBUx with a 1 meter USB Type C Cable. Hot-Plug voltage C_SBUx = 24 V. VPWR = 3.3 V. Put a 150-nF capacitor in series with a 40-Ω resistor to GND on SBUx. | | 8 | | V |
| **Power Supply and Leakage Currents** | | | | | | |
| $V_{PWR_UVLO}$ | $V_{PWR}$ Under Voltage Lockout | Place 1 V on VPWR and raise voltage until SBU or CC FETs turn-on. | 2.1 | 2.3 | 2.5 | V |
| $V_{PWR_UVLO_HYS}$ | $V_{PWR}$ UVLO Hysteresis | Place 3 V on VPWR and lower voltage until SBU or CC FETs turnoff; measure difference between rising and falling UVLO to calculate hysteresis. | 100 | 150 | 200 | mV |
| $I_{VPWR}$ | $V_{PWR}$ supply current | VPWR = 3.3 V (typical), VPWR = 4.5 V (maximum). –40°C ≤ $T_J$ ≤ +85°C. | | 90 | 135 | µA |
| $I_{C_CC_LEAK}$ | Leakage current for C_CCx pins when device is powered | VPWR = 3.3 V, $V_{C_CCx}$ = 3.6 V, CCx pins are floating, measure leakage current into C_CCx pins. | | | 5 | µA |
| $I_{C_SBU_LEAK}$ | Leakage current for C_SBUx pins when device is powered | VPWR = 3.3 V, VC_SBUx = 3.6 V, SBUx pins are floating, measure leakage current into C_SBUx pins. Result should be same if SBUx side is biased and C_SBUx is left floating.-40°C ≤ $T_J$ ≤ +85°C | | | 3 | µA |
| $I_{C_CC_LEAK_OVP}$ | Leakage current for C_CCx pins when device is in OVP | VPWR = 0 V or 3.3 V, $V_{C_CCx}$ = 24 V, CCx pins are set to 0 V, measure leakage current into C_CCx pins. | | | 1200 | µA |

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## 7.6 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{C_SBU_LEAK_OVP}$ | Leakage current for C_SBUx pins when device is in OVP | VPWR = 0 V or 3.3 V, $V_{C_SBUx}$ = 24 V, SBUx pins are set to 0 V, measure leakage current into C_SBUx pins. | | | 400 | µA |
| $I_{CC_LEAK_OVP}$ | Leakage current for CC pins when device is in OVP | VPWR = 0 V or 3.3 V, $V_{C_CCx}$ = 24 V, CCx pins are set to 0 V, measure leakage current out of CCx pins. | | | 30 | µA |
| $I_{SBU_LEAK_OVP}$ | Leakage current for SBU pins when device is in OVP | VPWR = 0 V, $V_{C_SBUx}$ = 24 V, SBUx pins are set to 0 V, measure leakage current into SBUx pins. | -1 | | 1 | µA |
| **/FLT Pin** | | | | | | |
| $V_{OL}$ | Low-level output voltage | IOL = 3 mA. Measure voltage at $\overline{FLT}$ pin. | | | 0.4 | V |
| **Over Temperature Protection** | | | | | | |
| $T_{SD_RISING}$ | The rising over-temperature protection shutdown threshold | | 150 | 175 | | °C |
| $T_{SD_FALLING}$ | The falling over-temperature protection shutdown threshold | | 130 | 140 | | °C |
| $T_{SD_HYST}$ | The over-temperature protection shutdown threshold hysteresis | | | 35 | | °C |

## 7.7 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Power-On and Off Timings** | | | | | |
| $t_{ON_FET}$ | Time from Crossing Rising VPWR UVLO until CC and SBU OVP FETs are on. | | 1.3 | 3.5 | ms |
| $t_{ON_FET_DB}$ | Time from Crossing Rising VPWR UVLO until CC and SBU OVP FETs are on and the dead battery resistors are off. | | 5.7 | 9.5 | ms |
| $dV_{PWR_OFF}/dt$ | Minimum slew rate allowed to guarantee CC and FETs turn off during a power off. | -0.5 | | | V/µs |
| **Over Voltage Protection** | | | | | |
| $t_{OVP_RESPONSE_CC}$ | OVP response time on the CCx pins. Time from OVP asserted until OVP FETs turn off. | | 70 | | ns |
| $t_{OVP_RESPONSE_SBU}$ | OVP response time on the SBUx pins. Time from OVP asserted until OVP FETs turn off. | | 80 | | ns |
| $t_{OVP_RECOVERY_CC}$ | OVP recovery time on the CCx pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on. OVP must be removed for CC FETs to turn back on. | | 0.93 | | ms |
| $t_{OVP_RECOVERY_CC_DB}$ | OVP recovery time on the CCx pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on and the dead battery resistors turn off. OVP must be removed for CC FETs to turn back on. | | 5 | | ms |
| $t_{OVP_RECOVERY_SBU}$ | OVP recovery time on the SBUx pins. Once an OVP has occurred, the minimum time duration until the SBU FETs turn back on. OVP must be removed for SBU FETs to turn back on. | | 0.62 | | ms |
| $t_{OVP_FLT_ASSERTION}$ | Time from OVP Asserted to /FLT assertion. $\overline{FLT}$ assertion is 10% of the maxmimum value. Set C_CCx or C_SBUx above the maxmimum OVP threshold. Start the time where it passes the typical OVP threshold value. | | 20 | | µs |
| $t_{OVP_FLT_DEASSERTION}$ | Time from CC FET turn on after an OVP to $\overline{FLT}$ deassertion. | | 5 | | ms |


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## 7.8 Typical Characteristics

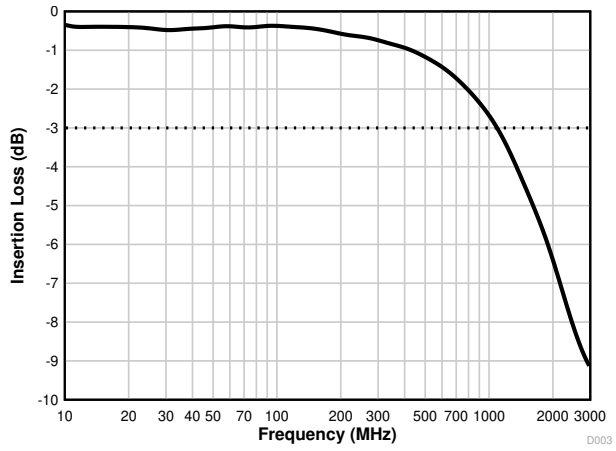


图 7-1. SBU Bandwidth

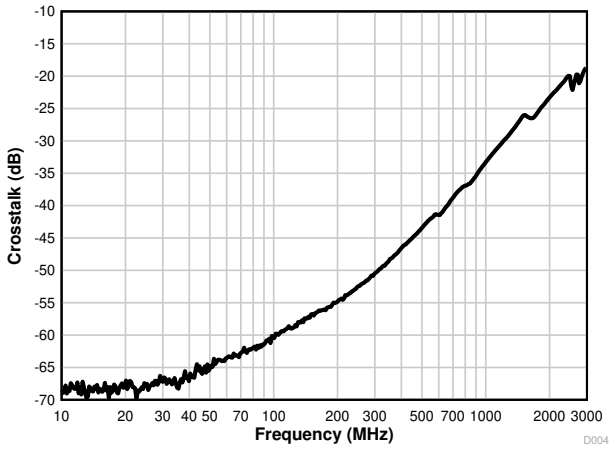


图 7-2. SBU Crosstalk

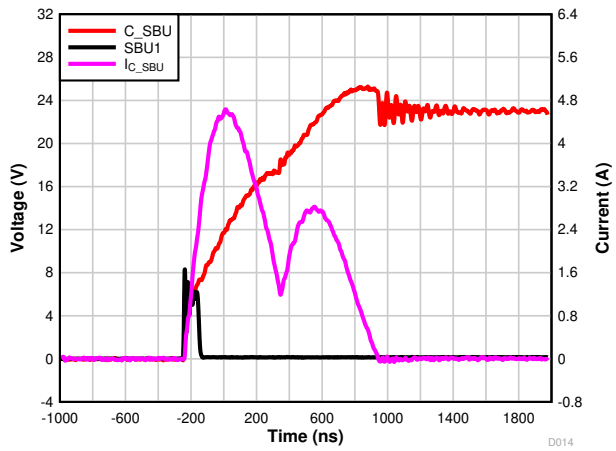


图 7-3. SBU Short-to-$V_{BUS}$ 24 V Zoomed In

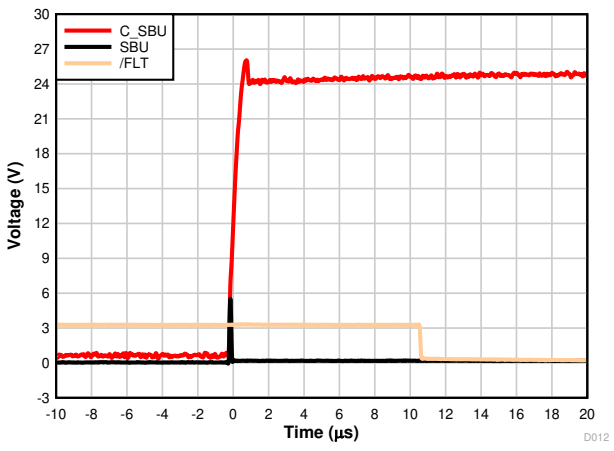


图 7-4. SBU Short-to-$V_{BUS}$ 24 V Zoomed Out

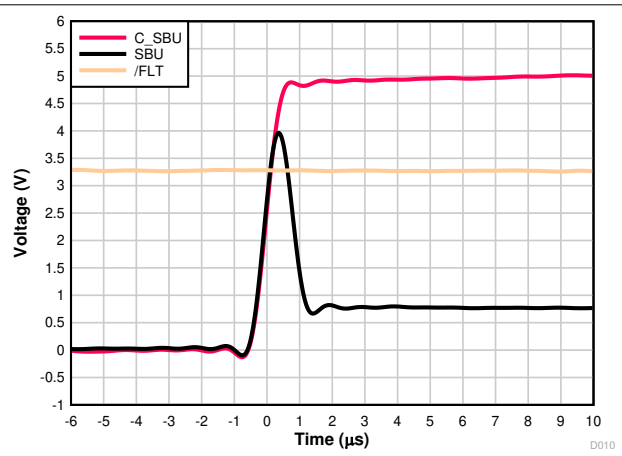


图 7-5. SBU Short-to-$V_{BUS}$ 5 V Zoomed In

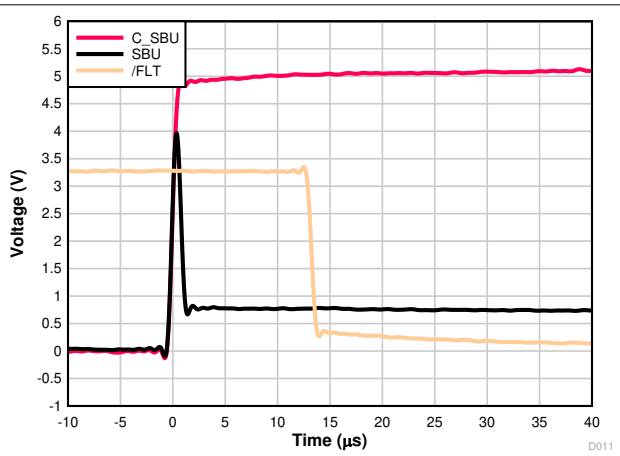


图 7-6. SBU Short-to-$V_{BUS}$ 5 V Zoomed Out

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## 7.8 Typical Characteristics (continued)

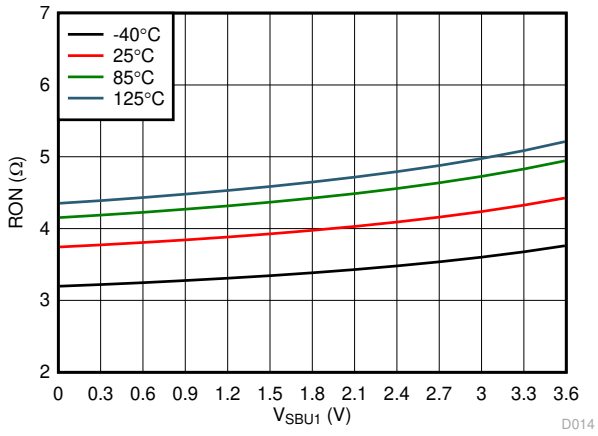


图 7-7. SBU $R_{ON}$ Flatness

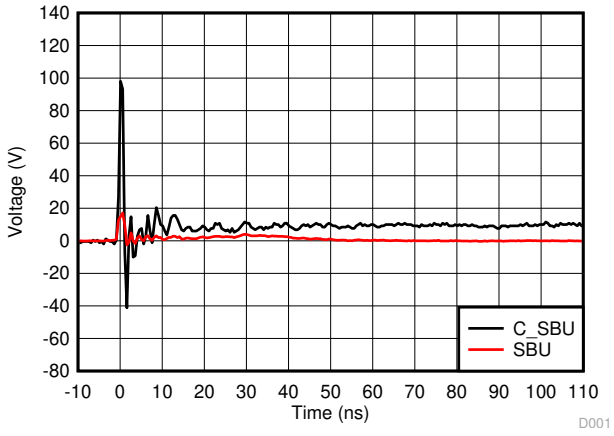


图 7-8. SBU IEC 61000-4-2 4-kV Response Waveform

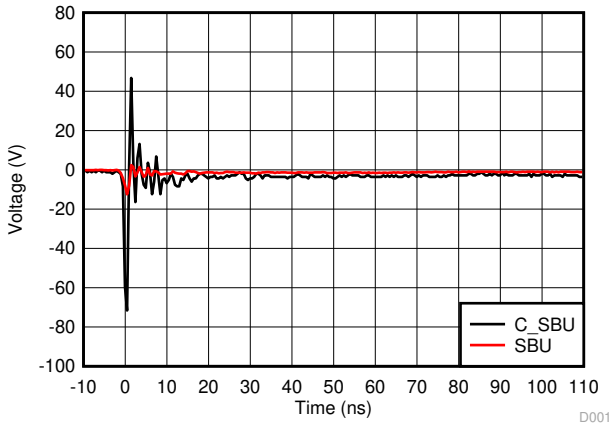


图 7-9. SBU IEC 61000-4-2 –4-kV Response Waveform

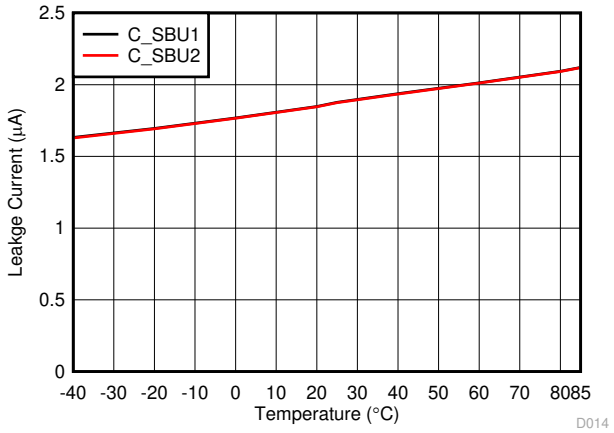


图 7-10. SBU Path Leakage Current vs Ambient Temperature at 3.6 V

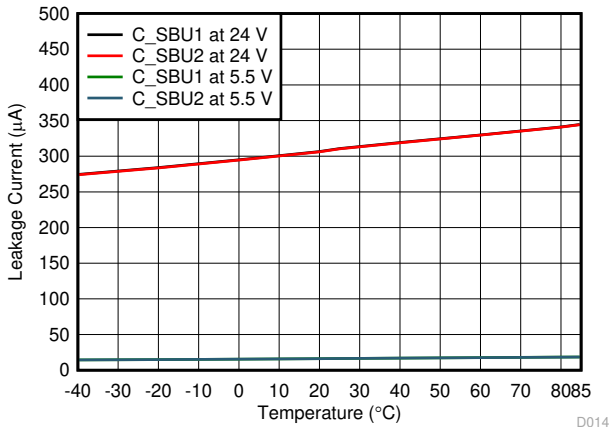


图 7-11. C_SBU OVP Leakage Current vs Ambient Temperature at 5.5 V and 24 V

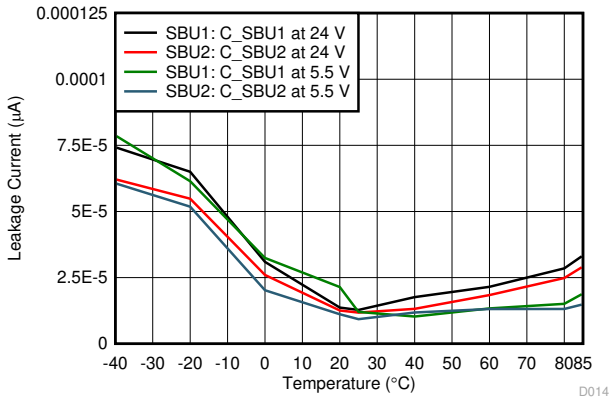


图 7-12. SBU OVP Leakage Current vs Ambient Temperature at 5.5 V and 24 V


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## 7.8 Typical Characteristics (continued)

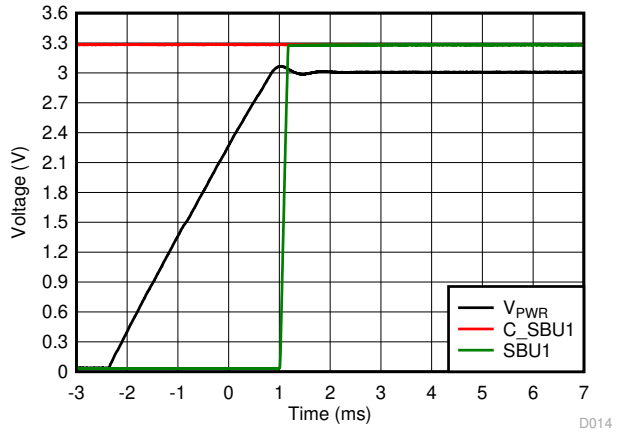


图 7-13. SBU FET Turnon Timing

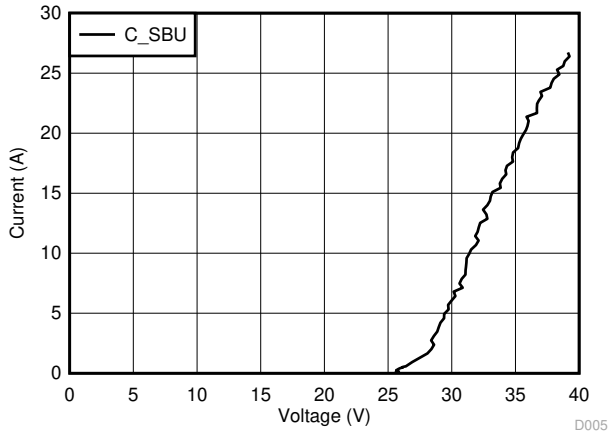


图 7-14. C_SBU TLP Curve Unpowered

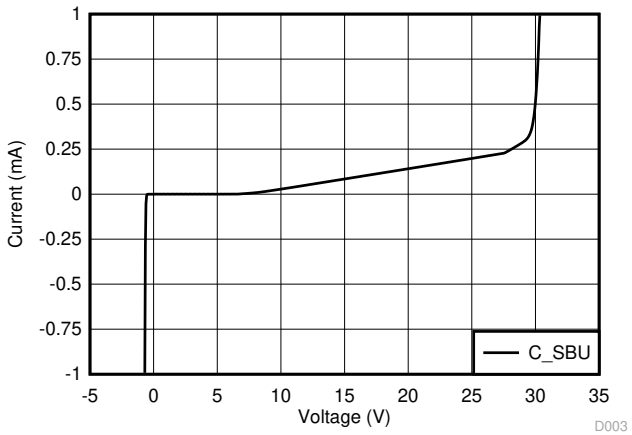


图 7-15. SBU IV Curve

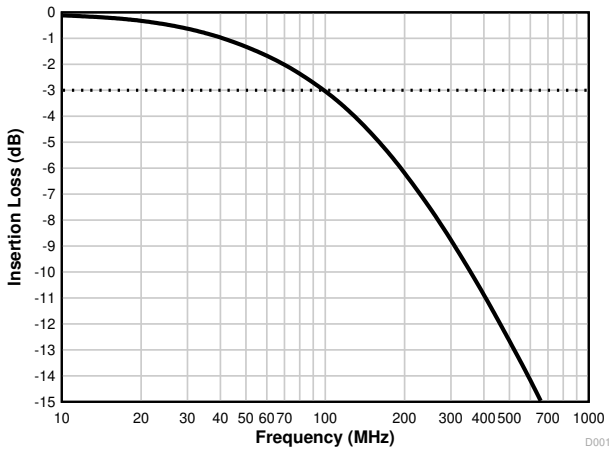


图 7-16. CC Bandwidth

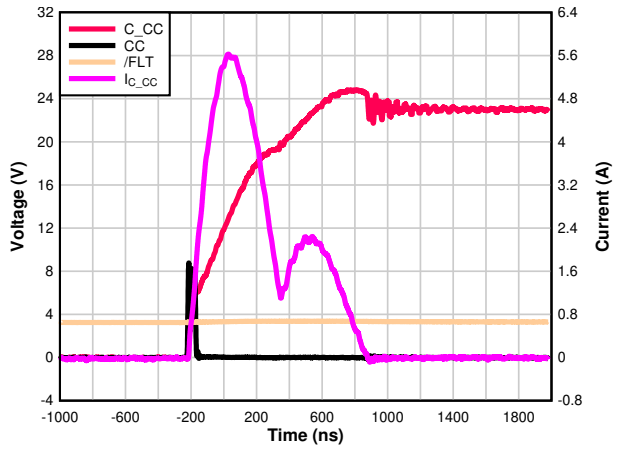


图 7-17. CC Short-to-$V_{BUS}$ 24 V Zoomed In

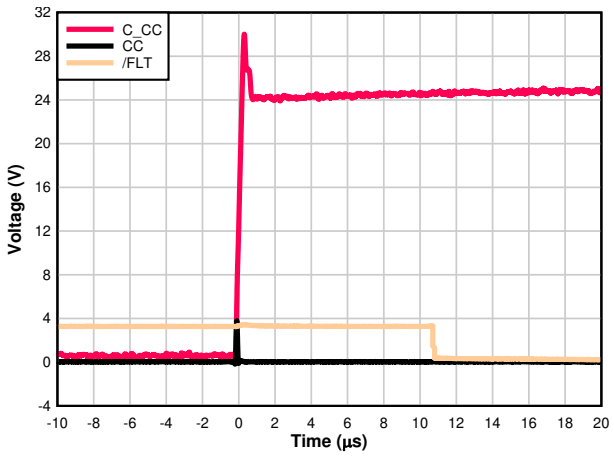


图 7-18. CC Short-to-$V_{BUS}$ 24 V Zoomed Out

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## 7.8 Typical Characteristics (continued)

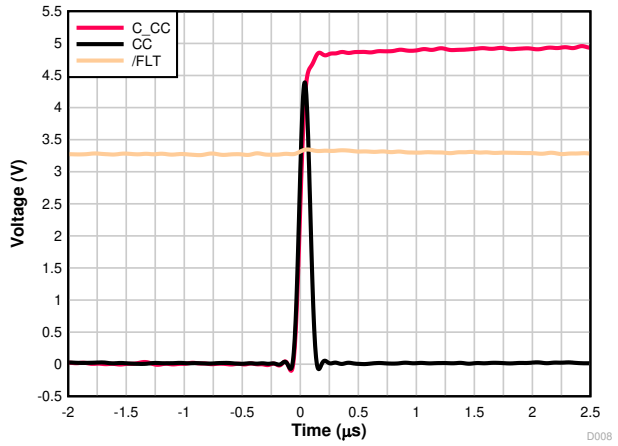


图 7-19. CC Short-to-$V_{BUS}$ 5 V Zoomed In

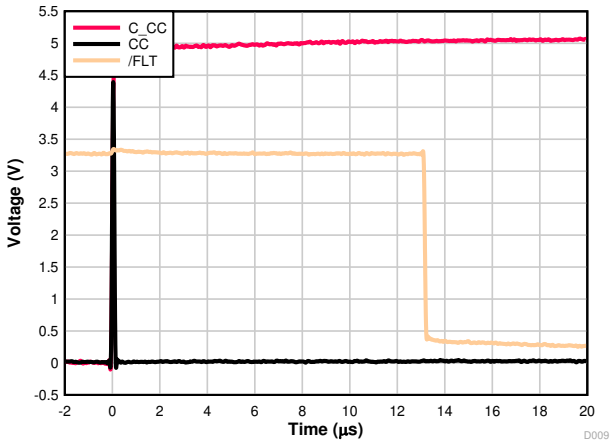


图 7-20. CC Short-to-$V_{BUS}$ 5 V Zoomed Out

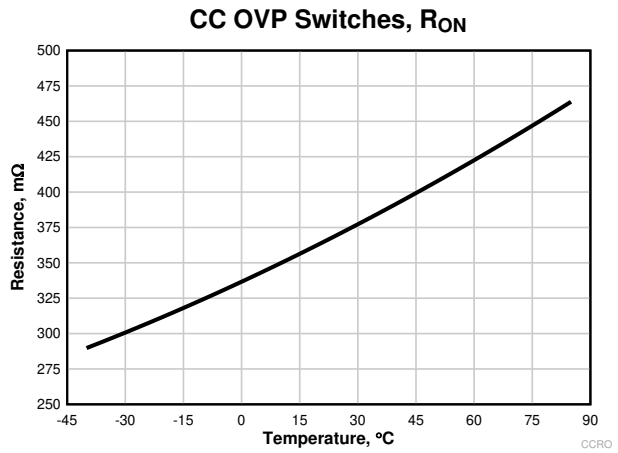


图 7-21. CC $R_{ON}$ Versus Temperature

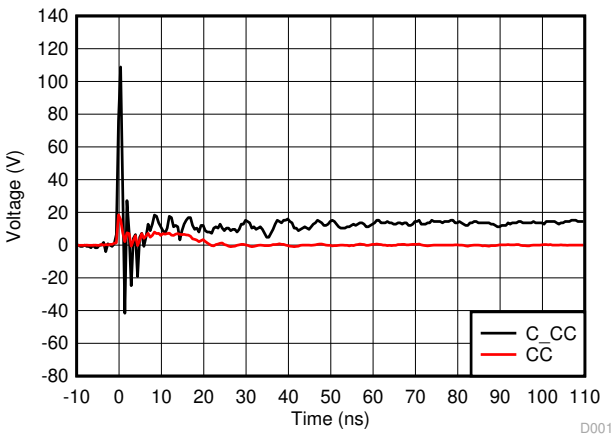


图 7-22. CC IEC 61000-4-2 8-kV Response Waveform

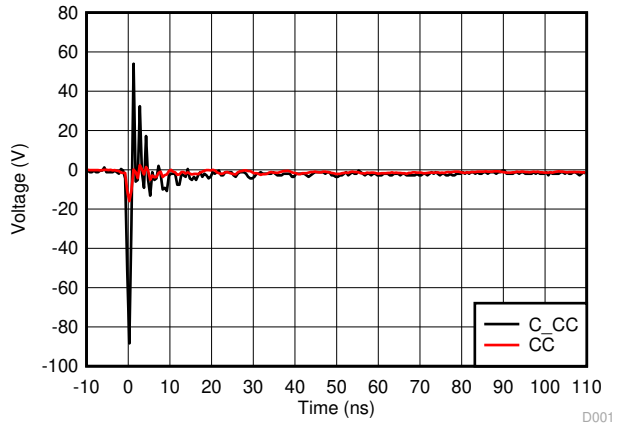


图 7-23. CC IEC 61000-4-2 –8-kV Response Waveform

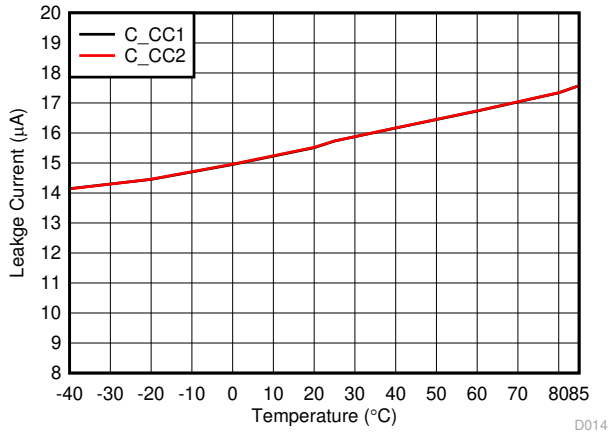


图 7-24. C_CC Path Leakage Current vs Ambient Temperature at C_CC = 5.5 V


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## 7.8 Typical Characteristics (continued)

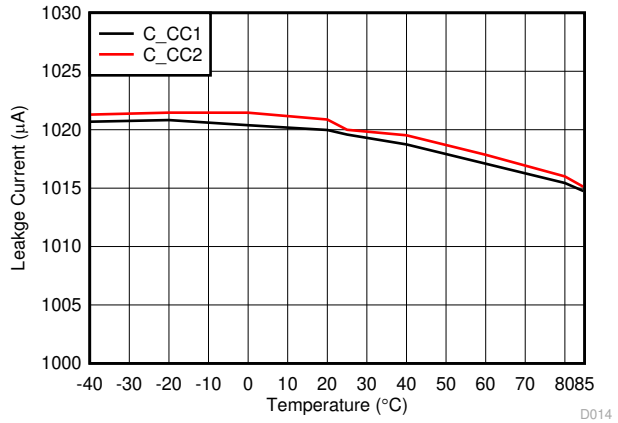



图 7-25. C_CC OVP Leakage Current vs Ambient Temperature at C_CC = 24 V

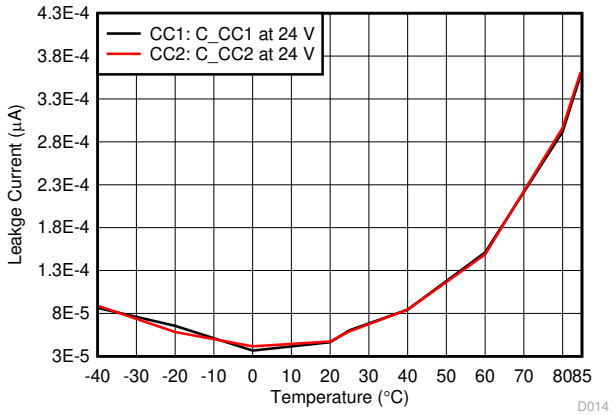



图 7-26. CC OVP Leakage Current vs Ambient Temperature at C_CC = 24 V

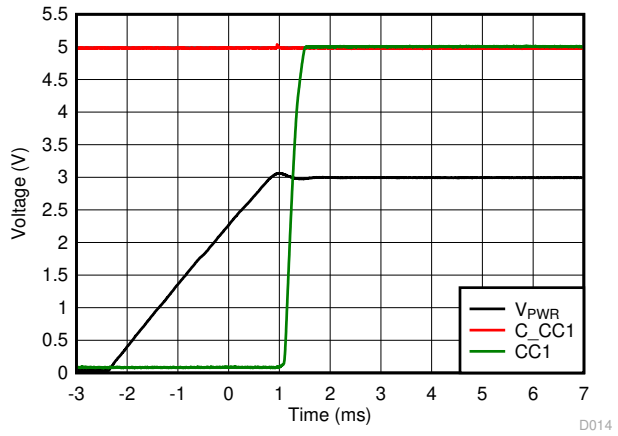



图 7-27. CC FET Turnon Timing

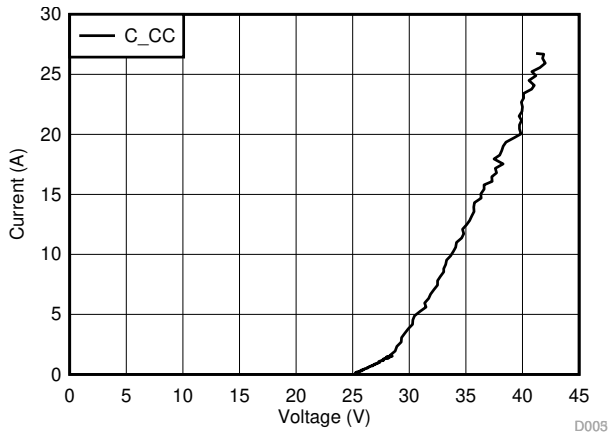



图 7-28. C_CC TLP Curve Unpowered

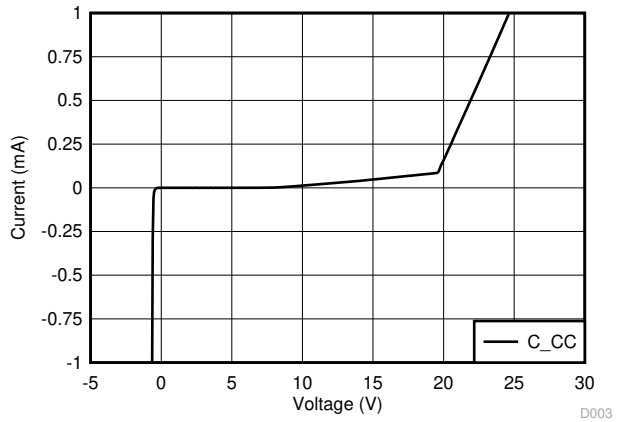



图 7-29. C_CC IV Curve

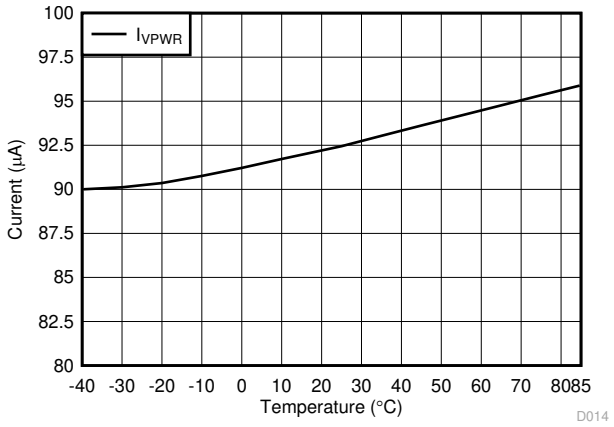



图 7-30. $V_{PWR}$ Supply Leakage vs Ambient Temperature at 3.6 V

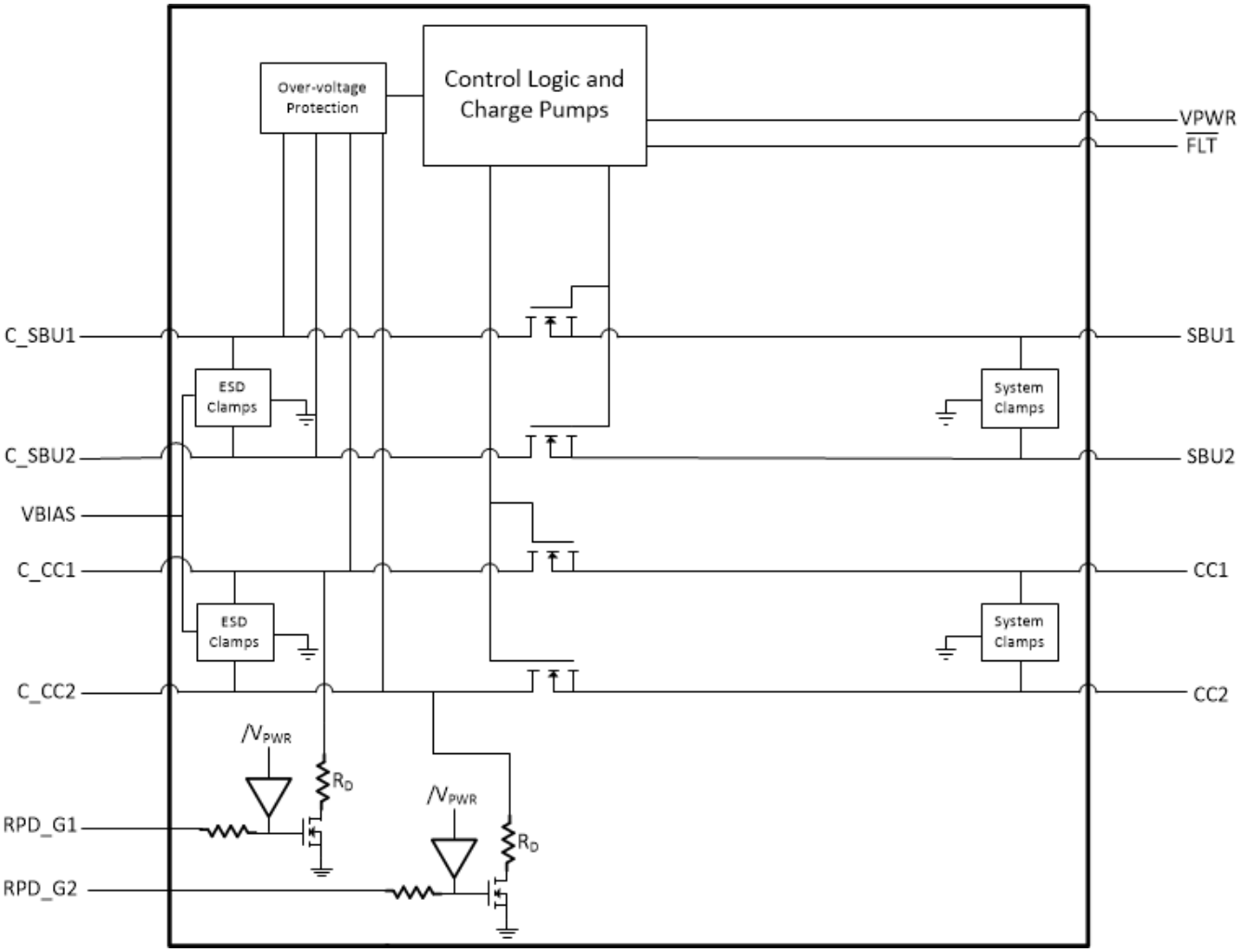
# 8 Detailed Description

## 8.1 Overview

The TPD4S311 is a single chip USB Type-C port protection solution that provides 20-V Short-to-$V_{BUS}$ overvoltage and IEC ESD protection. Due to the small pin pitch of the USB Type-C connector and non-compliant USB Type-C cables and accessories, the $V_{BUS}$ pins can get shorted to the CC and SBU pins inside the USB Type-C connector. Because of this short-to-$V_{BUS}$ event, the CC and SBU pins need to be 20-V tolerant, to support protection on the full USB PD voltage range. Even if a device does not support 20-V operation on $V_{BUS}$, non complaint adaptors can start out with 20-V $V_{BUS}$ condition, making it necessary for any USB Type-C device to support 20 V protection. The TPD4S311 integrates four channels of 20-V Short-to-$V_{BUS}$ overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector.

Additionally, IEC 61000-4-2 system level ESD protection is required in order to protect a USB Type-C port from ESD strikes generated by end product users. The TPD4S311 integrates four channels of IEC61000-4-2 ESD protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector. This means IEC ESD protection is provided for all of the low-speed pins on the USB Type-C connector in a single chip in the TPD4S311. Additionally, high-voltage IEC ESD protection that is 22-V DC tolerant is required for the CC and SBU lines in order to simultaneously support IEC ESD and Short-to-$V_{BUS}$ protection; there are not many discrete market solutions that can provide this kind of protection. This high-voltage IEC ESD diode is what the TPD4S311 integrates, specifically designed to guarantee it works in conjunction with the overvoltage protection FETs inside the device. This sort of solution is very hard to generate with discrete components.

## 8.2 Functional Block Diagram





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## 8.3 Feature Description

### 8.3.1 4-Channels of Short-to-$V_{BUS}$ Overvoltage Protection (CC1, CC2, SBU1, SBU2 Pins ): 24-$V_{DC}$ Tolerant

The TPD4S311 provides 4-channels of Short-to-$V_{BUS}$ Overvoltage Protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector. The TPD4S311 is able to handle 24-$V_{DC}$ on its C_CC1, C_CC2, C_SBU1, and C_SBU2 pins. This is necessary because according to the USB PD specification, with $V_{BUS}$ set for 20-V operation, the $V_{BUS}$ voltage is allowed to legally swing up to 21 V and 21.5 V on voltage transitions from a different USB PD $V_{BUS}$ voltage. The TPD4S311 builds in tolerance up to 24-$V_{BUS}$ to provide margin above this 21.5-V specification to be able to support USB PD adaptors that may break the USB PD specification.

When a short-to-$V_{BUS}$ event occurs, ringing happens due to the RLC elements in the hot-plug event. With very low resistance in this RLC circuit, ringing up to twice the settling voltage can appear on the connector. More than 2x ringing can be generated if any capacitor on the line derates in capacitance value during the short-to-$V_{BUS}$ event. This means that more than 44 V could be seen on a USB Type-C pin during a Short-to-$V_{BUS}$ event. The TPD4S311 has built in circuit protection to handle this ringing. The diode clamps used for IEC ESD protection also clamp the ringing voltage during the short-to-$V_{BUS}$ event to limit the peak ringing to approximately 30 V. Additionally, the overvoltage protection FETs integrated inside the TPD4S311 are 30-V tolerant, therefore being capable of supporting the high-voltage ringing waveform that is experienced during the short-to-$V_{BUS}$ event. The well designed combination of voltage clamps and 30-V tolerant OVP FETs insures the TPD4S311 can handle Short-to-$V_{BUS}$ hot-plug events with hot-plug voltages as high as 24-$V_{DC}$.

The TPD4S311 has an extremely fast turnoff time of 70 ns typical. Furthermore, additional voltage clamps are placed after the OVP FET on the system side (CC1, CC2, SBU1, SBU2) pins of the TPD4S311, to further limit the voltage and current that are exposed to the USB Type-C CC/PD controller during the 70 ns interval while the OVP FET is turning off. The combination of connector side voltage clamps, OVP FETs with extremely fast turnoff time, and system side voltage clamps all work together to insure the level of stress seen on a CC1, CC2, SBU1, or SBU2 pin during a short-to-$V_{BUS}$ event is less than or equal to an HBM event. This is done by design, as any USB Type-C CC/PD controller will have built in HBM ESD protection.

图 8-1 is an example of the TPD4S311 successfully protecting the TPS65982, the world's first fully integrated, full-featured USB Type-C and PD controller.

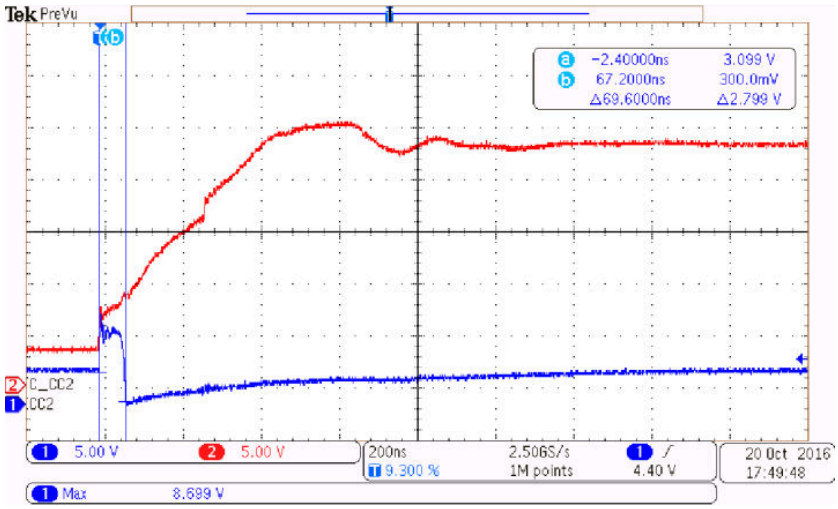


**图 8-1. TPD4S311 Protecting the TPS65982 During a Short-to-$V_{BUS}$ Event**

### 8.3.2 4-Channels of IEC 61000-4-2 ESD Protection (CC1, CC2, SBU1, SBU2 Pins)

The TPD4S311 integrates 4-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, and SBU2 pins. USB Type-C ports on end-products need system level IEC ESD protection in order to provide adequate protection for the ESD events that the connector can be exposed to from end users. The TPD4S311 integrates IEC ESD protection for all of the low-speed pins on the USB Type-C connector in a single chip. Also note, that while the RPD_Gx pins are not individually rated for IEC ESD, when they are shorted to the C_CCx

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pins, the C_CCx pins provide protection for both the C_CCx pins and the RPD_Gx pins. Additionally, high-voltage IEC ESD protection that is 24-V DC tolerant is required for the CC and SBU lines in order to simultaneously support IEC ESD and Short-to-$V_{BUS}$ protection; there are not many discrete market solutions that can provide this kind of protection. The TPD4S311 integrates this type of high-voltage ESD protection so a system designer can meet both IEC ESD and Short-to-$V_{BUS}$ protection requirements in a single device.

### 8.3.3 CC1, CC2 Overvoltage Protection FETs 400-mA or 600-mA Capable for Passing VCONN Power

The CC pins on the USB Type-C connector serve many functions; one of the functions is to be a provider of power to active cables. Active cables are required when desiring to pass greater than 3 A of current on the $V_{BUS}$ line or when the USB Type-C port uses the super-speed lines (TX1+, TX2 – , RX1+, RX1 – , TX2+, TX2 – , RX2+, RX2 – ). When CC is configured to provide power, it is called VCONN. VCONN is a DC voltage source in the range of 3 V to 5.5 V. If supporting VCONN, a VCONN provider must be able to provide 1 W of power to a cable; this translates into a current range of 200 mA to 333 mA (depending on your VCONN voltage level). Additionally, if operating in a USB PD alternate mode, greater power levels are allowed on the VCONN line.

When a USB Type-C port is configured for VCONN and using the TPD4S311, this VCONN current flows through the OVP FETs of the TPD4S311. Therefore, the TPD4S311 has been designed to handle these currents and have an RON low enough to provide a specification compliant VCONN voltage to the active cable. The TPD4S311 is designed to handle up to 400 mA, while the TPD4S311A is designed to handle up to 600 mA of DC current to allow for alternate mode support in addition to the standard 1 W required by the USB Type-C specification.

### 8.3.4 CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices

An important feature of USB Type-C and USB PD is the ability for this connector to serve as the sole power source to mobile devices. With support up to 100 W, the USB Type-C connector supporting USB PD can be used to power a whole new range of mobile devices not previously possible with legacy USB connectors.

When the USB Type-C connector is the sole power supply for a battery powered device, the device must be able to charge from the USB Type-C connector even when its battery is dead. In order for a USB Type-C power adapter to supply power on $V_{BUS}$, RD pulldown resistors must be exposed on the CC pins. These RD resistors are typically included inside a USB Type-C CC/PD controller. However, when the TPD4S311 is used to protect the USB Type-C port, the OVP FETs inside the device isolate these RD resistors in the CC/PD controller when the mobile device has no power. This is because when the TPD4S311 has no power, the OVP FETs are turned off to guarantee overvoltage protection in a dead battery condition. Therefore, the TPD4S311 integrates high-voltage, dead battery RD pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection.

If dead battery support is required, short the RPD_G1 pin to the C_CC1 pin, and short the RPD_G2 pin to the C_CC2 pin. This connects the dead battery resistors to the connector CC pins. When the TPD4S311 is unpowered, and the RP pull-up resistor is connected from a power adaptor, this RP pull-up resistor activates the RD resistor inside the TPD4S311. This enables $V_{BUS}$ to be applied from the power adaptor even in a dead battery condition. Once power is restored back to the system and back to the TPD4S311 on its VPWR pin, the TPD4S311 turns ON its OVP FETs in 3.5 ms and then turns OFF its dead battery RD. The TPD4S311 first turns ON its CC OVP FETs fully, and then removes its dead battery RDs. This is to make sure the PD controller RD is fully exposed before removing the RD of the TPD4S311. This is to help ensure the USB Type-C source remains attached because a USB Type-C sink must have an RD present on CC at all times to guarantee according to the USB Type-C spec that the USB Type-C source remains attached.

If desiring to power the CC/PD controller during dead battery mode and if the CC/PD Controller is configured as a DRP, it is critical that the TPD4S311 be powered before or at the same time that the CC/PD controller is powered. It is also critical that when unpowered, the CC/PD controller also expose its dead battery resistors. When the TPD4S311 gets powered, it exposes the CC pins of the CC/PD controller within 3.5 ms, and then removes its own RD dead battery resistors. Once the TPD4S311 turns on, the RD pull-down resistors of the CC/PD controller must be present immediately, in order to guarantee the power adaptor connected to power the dead battery device keeps its $V_{BUS}$ turned on. If the power adaptor does not see RD present, it can disconnect $V_{BUS}$. This removes power from the device with its battery still not sufficiently charged, which consequently removes power from the CC/PD controller and the TPD4S311. Then the RD resistors of the TPD4S311 are


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exposed again, and connects the power adaptor's $V_{BUS}$ to start the cycle over. This creates an infinite loop, never or very slowly charging the mobile device.

If the CC/PD Controller is configured for DRP and has started its DRP toggle before the TPD4S311 turns on, this DRP toggle is unable to guarantee that the power adaptor does not disconnect from the port. Therefore, it is recommended if the CC/PD controller is configured for DRP, that its dead battery resistors be exposed as well, and that they remain exposed until the TPD4S311 turns on. This is typically accomplished by powering the TPD4S311 at the same time as the CC/PD controller when powering the CC/PD controller in dead battery operation. When protecting the TPS6598x family of PD controllers with TPD4S311, this is accomplished by powering TPD4S311 from TPS6598x's LDO_3V3 pin (connect TPS6598x's LDO_3V3 pin to TPD4S311's $V_{PWR}$ pin).

If dead battery charging is not required in your application, connect the RPD_G1 and RPD_G2 pins to ground.

### 8.3.5 1.69-mm × 1.69-mm DSBGA Package

The TPD4S311 comes in a tiny, 1.69-mm × 1.69-mm DSBGA package, greatly reducing the size of implementing a similar protection solution discretely. The DSBGA package supports a wide range of PCB designs.

## 8.4 Device Functional Modes

表 8-1 describes all of the functional modes for the TPD4S311. The "X" in the below table are "do not care" conditions, meaning any value can be present within the absolute maximum ratings of the datasheet and maintain that functional mode.

**表 8-1. Device Mode Table**

| Device Mode Table | | Inputs | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| MODE | | VPWR | C_CCx | C_SBUx | RPD_Gx | $T_J$ | $\overline{FLT}$ | CC FETs | SBU FETs |
| Normal Operating Conditions | Unpowered, no dead battery support | <UVLO | X | X | Grounded | X | High-Z | OFF | OFF |
| | Unpowered, dead battery support | <UVLO | X | X | Shorted to C_CCx | X | High-Z | OFF | OFF |
| | Powered on | >UVLO | <OVP | <OVP | X, forced OFF | <TSD | High-Z | ON | ON |
| Fault Conditions | Thermal shutdown | >UVLO | X | X | X, forced OFF | >TSD | Low (Fault Asserted) | OFF | OFF |
| | CC over voltage condition | >UVLO | >OVP | X | X, forced OFF | <TSD | Low (Fault Asserted) | OFF | OFF |
| | SBU over voltage condition | >UVLO | X | >OVP | X, forced OFF | <TSD | Low (Fault Asserted) | OFF | OFF |
| | IEC ESD generated over voltage condition(1) | >UVLO | X | X | $R_D$ ON if RPD_Gx is shorted to C_CCx | <TSD | Low (Fault Asserted) | OFF | OFF |

(1) This row describes the state of the device while still in OVP after the IEC ESD strike which put the device into OVP is over, and the voltages on the C_CCx and C_SBUx pins have returned to their normal voltage levels.

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# 9 Application and Implementation

**Note**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 9.1 Application Information

The TPD4S311 provides 4-channels of Short-to-$V_{BUS}$ overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector, and 4-channels of IEC ESD protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector. Care must be taken to insure that the TPD4S311 provides adequate system protection as well as insuring that proper system operation is maintained. The following application example explains how to properly design the TPD4S311 into a USB Type-C system.

## 9.2 Typical Application

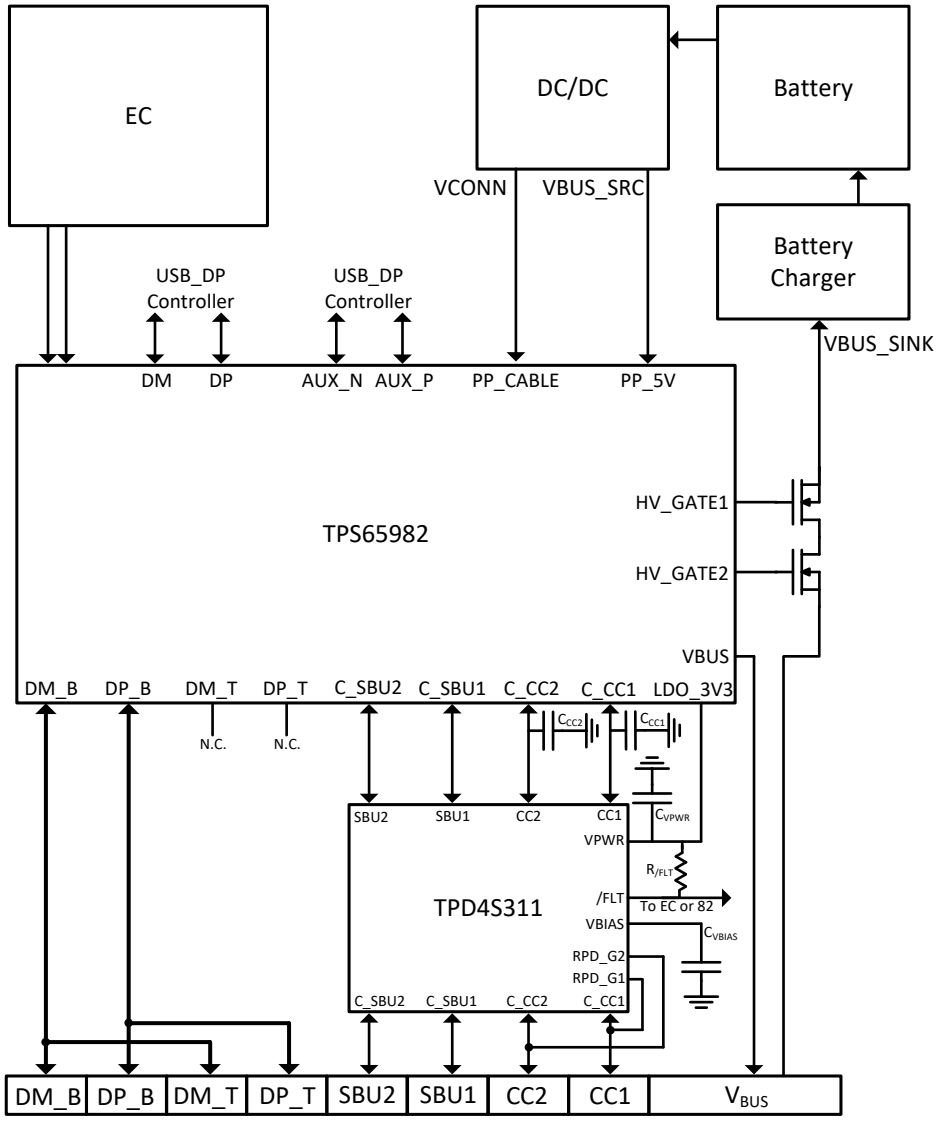


**图 9-1. TPD4S311 Typical Application Diagram**


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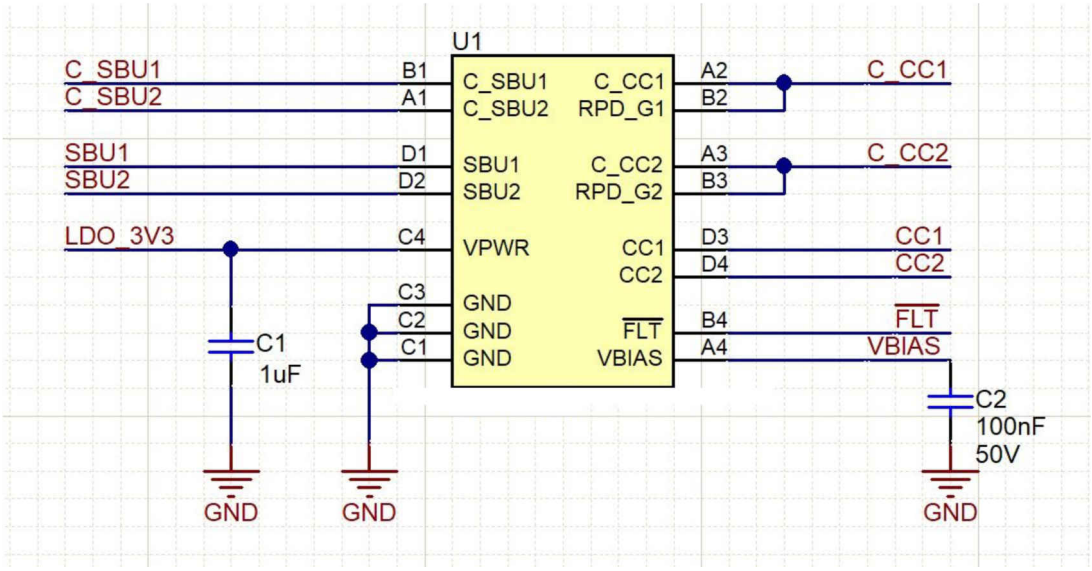


图 9-2. TPD4S311 Reference Schematic

### 9.2.1 Design Requirements

In this application example we study the protection requirements for a full-featured USB Type-C DRP Port, fully equipped with USB-PD, USB2.0, USB3.0, Display Port, and 100 W charging. The TPS65982 is used to easily enable a full-featured port with a single chip solution. In this application, all the pins of the USB Type-C connector are used. Both the CC and SBU pins are susceptible to shorting to the $V_{BUS}$ pin. With 100 W charging, $V_{BUS}$ operates at 20 V, requiring the CC and SBU pins to tolerate 20-$V_{DC}$. With these protection requirements present for the USB Type-C connector, the TPD4S311 is used. The TPD4S311 is a single chip solution that provides all the required protection for the SBU and CC pins in the USB Type-C connector.

表 9-1 lists the TPD4S311 design parameters.

表 9-1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| $V_{BUS}$ nominal operating voltage | 20 V |
| Short-to-$V_{BUS}$ tolerance for the CC and SBU pins | 24 V |
| VBIAS nominal capacitance | 0.1 µF |
| Dead battery charging | 100 W |
| Maximum ambient temperature requirement | 85°C |

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### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 VBIAS Capacitor Selection*

As noted in the *Recommended Operating Conditions* table, a minimum of 35-$V_{BUS}$ rated capacitor is required for the VBIAS pin, and a 50-$V_{BUS}$ capacitor is recommended. The VBIAS capacitor is in parallel with the central diode clamp integrated inside the TPD4S311. A forward biased hiding diode connects the VBIAS pin to the C_CCx and C_SBUx pins. Therefore, when a Short-to-$V_{BUS}$ event occurs at 20 V, 20-$V_{BUS}$ minus a forward biased diode drop is exposed to the VBIAS pin. Additionally, during the short-to-$V_{BUS}$ event, ringing can occur almost double the settling voltage of 20 V, allowing a potential 40 V to be exposed to the C_CCx and C_SBUx pins. However, the internal diode clamps limit the voltage exposed to the C_CCx and C_SBUx pins to around 30 V. Therefore, at least 35-$V_{BUS}$ capacitor is required to insure the VBIAS capacitor does not get destroyed during Short-to-$V_{BUS}$ events.

A 50-V, X7R capacitor is recommended to further improve the derating performance of the capacitors. When the voltage across a real capacitor is increased, its capacitance value derates. The more the capacitor derates, the greater than 2x ringing can occur in the short-to-$V_{BUS}$ RLC circuit. The 50-V X7R capacitors have great derating performance, allowing for the best short-to-$V_{BUS}$ performance of the TPD4S311.

Additionally, the VBIAS capacitor helps pass IEC 61000-4-2 ESD strikes. The more capacitance present, the better the IEC performance. So the less the VBIAS capacitor derates, the better the IEC performance. 表 9-2 shows real capacitors recommended to achieve the best performance with the TPD4S311.

**表 9-2. Design Parameters**

| CAPACITOR SIZE | PART NUMBER |
|---|---|
| 0402 | CC0402KRX7R9BB104 |
| 0603 | GRM188R71H104KA93D |

#### *9.2.2.2 Dead Battery Operation*

For this application, we want to support 100-W dead battery operation; when the laptop is out of battery, we still want to charge the laptop at 20 V and 5 A. This means that the USB PD Controller must receive power in dead battery mode. The TPS65982 has its own built in LDO in order to supply the TPS65982 power from $V_{BUS}$ in a dead battery condition. The TPS65982 can also provide power to its flash during this condition through its LDO_3V3 pin.

The OVP FETs of the TPD4S311 remain OFF when it is unpowered in order to insure in a dead battery situation proper protection is still provided to the PD controller in the system, in this case the TPS65982. However, when the OVP FETs are OFF, this isolates the TPS65982s dead battery resistors from the USB Type-C ports CC pins. A USB Type-C power adaptor must see the RD pull-down dead battery resistors on the CC pins or it does not provide power on $V_{BUS}$. Since the TPS65982s dead battery resistors are isolated from the USB Type-C connector's CC pins, the built-in, dead battery resistors of the TPD4S311 must be connected. Short the RPD_G1 pin to the C_CC1 pin, and short the RPD_G2 pin to the C_CC2 pin.

Once the power adaptor sees the dead battery resistors of the TPD4S311, it applies 5 V on the $V_{BUS}$ pin. This provides power to the TPS65982, turning the PD controller on, and allowing the battery to begin to charge. However, this application requires 100 W charging in dead battery mode, so $V_{BUS}$ at 20 V and 5 A is required. USB PD negotiation is required to accomplish this, so the TPS65982 needs to be able to communicate on the CC pins. This means the TPD4S311 needs to be turned on in dead battery mode as well so the TPS65982s PD controller can be exposed to the CC lines. To accomplish this, it is critical that the TPD4S311 is powered by the TPS65982s internal LDO, the LDO_3V3 pin. This way, when the TPS65982 receives power on $V_{BUS}$, the TPD4S311 is turned on simultaneously.

It is critical that the TPS65982's dead battery resistors are also connected to its CC pins for dead battery operation. Short the TPS65982s RPD_G1 pin to its C_CC1 pin, and its RPD_G2 pin to its C_CC2 pin. It is critical that the TPS65982s dead battery resistors are present; once the TPD4S311 receives power, turns on its OVP FETs and then removes its dead battery RD resistor, TPS65982's RD pull-down resistors must be present on the CC line in order to guarantee the power adaptor stays connected. If RD is not present the power adaptor will eventually interpret this as a disconnect and remove $V_{BUS}$.


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Also, it is important that the TPS65982's dead battery resistors are present so it properly boots up in dead battery operation with the correct voltages on its CC pins.

Once this process has occurred, the TPS65982 can start negotiating with the power adaptor through USB PD for higher power levels, allowing 100-W operation in dead battery mode.

For more information on the TPD4S311 dead battery operation, see the *CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices* section of the datasheet.

#### 9.2.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the *USB PD Specification* is given below in 表 9-3.

**表 9-3. USB PD cReceiver Specification**

| NAME | DESCRIPTION | MIN | MAX | UNIT | COMMENT |
|---|---|---|---|---|---|
| cReceiver | CC receiver capacitance | 200 | 600 | pF | The DFP or UFP system shall have capacitance within this range when not transmitting on the line |

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TPS65982, the TPD4S311, and any external capacitor must fall within these limits. 表 9-4 shows the analysis involved in choosing the correct external CC capacitor for this system, and shows that an external CC capacitor is required.

**表 9-4. CC Line Capacitor Calculation**

| CC CAPACITANCE | MIN | MAX | UNIT | COMMENT |
|---|---|---|---|---|
| CC line target capacitance | 200 | 600 | pF | From the *USB PD Specification* section |
| TPS65982 capacitance | 70 | 120 | pF | From the *TPS65982* data sheet |
| TPD4S311 capacitance | 45 | 120 | pF | From the *Electrical Characteristics* table |
| Proposed capacitor GRM033R71E221KA01D | 110 | 330 | pF | CAP, CERM, 220 pF, 25 V, ±10%, X7R, 0201 (for min and max, assume ±50% capacitance change with temperature and voltage derating to be overly conservative) |
| TPS65982 + TPD4S311 + GRM033R71E221KA01D | 225 | 570 | pF | Meets USB PD cReceiver specification |

#### 9.2.2.4 Additional ESD Protection on CC and SBU Lines

If additional IEC ESD protection is desired to be placed on either the CC or SBU lines, it is important that high-voltage ESD protection diodes be used. The maximum DC voltage that can be seen in USB PD is 21-$V_{BUS}$, with 21.5 V allowed during voltage transitions. Therefore, an ESD protection diode must have a reverse stand off voltage higher than 21.5 V in order to guarantee the diode does not breakdown during a short-to-$V_{BUS}$ event and have large amounts of current flowing through it indefinitely, destroying the diode. A reverse stand off voltage of 24 V is recommended to give margin above 21.5 V in case USB Type-C power adaptors are released in the market which break the USB Type-C specification.

Furthermore, due to the fact that the Short-to-$V_{BUS}$ event applies a DC voltage to the CC and SBU pins, a deep-snap-back diode cannot be used unless its minimum trigger voltage is above 42 V. During a Short-to-$V_{BUS}$ event, RLC ringing of up to 2x the settling voltage can be exposed to CC and SBU, allowing for up to 42 V to be exposed. Furthermore, if any capacitor derates on the CC or SBU line, greater than 2x ringing can occur. Since this ringing is hard to bound, it is recommended to not use deep-snap-back diodes. If the deep-snap-back diode triggers during the short-to-$V_{BUS}$ hot-plug event, it begins to operate in its conduction region. With a 20-$V_{BUS}$ source present on the CC or SBU line, this allows the diode to conduct indefinitely, destroying the diode.

#### 9.2.2.5 $\overline{FLT}$ Pin Operation

Once a Short-to-$V_{BUS}$ occurs on the C_CCx or C_SBUx pins, the $\overline{FLT}$ pin is asserted in 20 µs (typical) so the PD controller can be notified quickly. If $V_{BUS}$ is being shorted to CC or SBU, it is recommended to respond to the

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event by forcing a detach in the USB PD controller to remove $V_{BUS}$ from the port. Although the USB Type-C port using the TPD4S311 is not damaged, as the TPD4S311 provides protection from these events, the other device connected through the USB Type-C Cable or any active circuitry in the cable can be damaged. Although shutting the $V_{BUS}$ off through a detach does not guarantee it stops the other device or cable from being damaged, it can mitigate any high current paths from causing further damage after the initial damage takes place. Additionally, even if the active cable or other device does have proper protection, the short-to-$V_{BUS}$ event may corrupt a configuration in an active cable or in the other PD controller, so it is best to detach and reconfigure the port.

#### *9.2.2.6 How to Connect Unused Pins*

If either the RPD_Gx pins are unused in a design, they must be connected to GND.

### 9.2.3 Application Curves

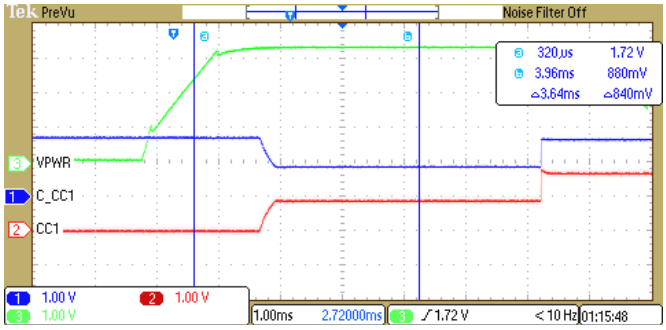


**图 9-3. TPD4S311 Turning On in Dead Battery Mode with $R_D$ on CC1**

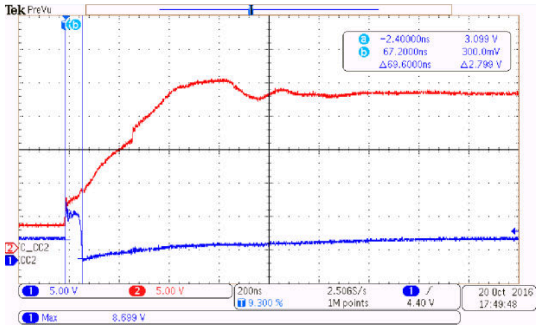


**图 9-4. TPD4S311 Protecting the TPS65982 During a Short-to-$V_{BUS}$ Event**


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## 10 Power Supply Recommendations

The $V_{PWR}$ pin provides power to all the circuitry in the TPD4S311. It is recommended a 1-µF decoupling capacitor is placed as close as possible to the VPWR pin. If USB PD is desired to be operated in dead battery conditions, it is critical that the TPD4S311 share the same power supply as the PD controller in dead battery boot-up (such as sharing the same dead battery LDO). See the *CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices* section for more details.

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# 11 Layout

## 11.1 Layout Guidelines

Proper routing and placement is important to maintain the signal integrity the SBU and CC line signals. The following guidelines apply to the TPD4S311:

- Place the bypass capacitors as close as possible to the $V_{PWR}$ pin, and ESD protection capacitor as close as possible to the $V_{BIAS}$ pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to-$V_{BUS}$ and ESD strikes.
- The SBU lines must be routed as straight as possible and any sharp bends must be minimized.

Standard ESD recommendations apply to the C_CC1, C_CC2, C_SBU1, C_SBU2:

- The optimum placement for the device is as close to the connector as possible:
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TPD4S311 and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

## 11.2 Layout Example

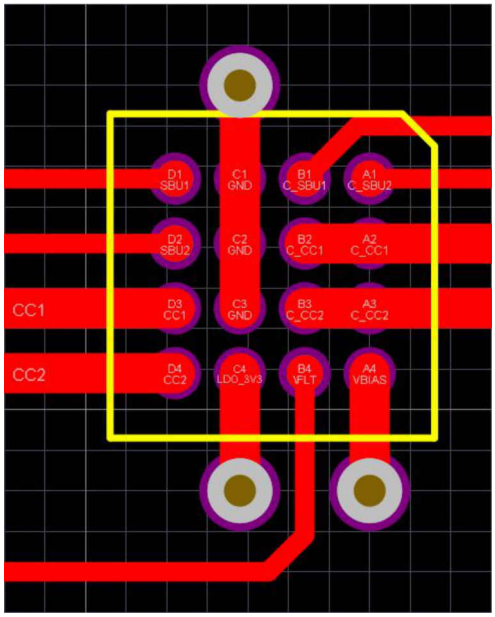


图 11-1. TPD4S311 Top Layer Routing

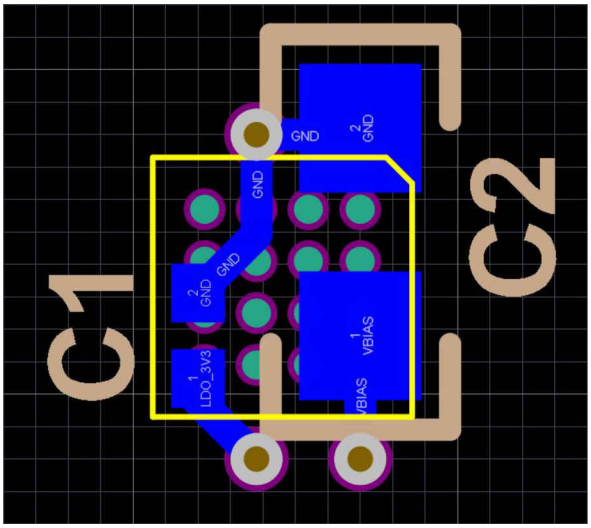


图 11-2. TPD4S311 Bottom Layer Routing


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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*TPD6S300 Evaluation Module User's Guide*

*TPS65982 USB Type-C and USB PD Controller, Power Switch, and High-Speed Multiplexer*

## 12.2 接收文档更新通知

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD4S311AYBFR | ACTIVE | DSBGA | YBF | 16 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 4S311<br>A1 | Samples |
| TPD4S311YBFR | ACTIVE | DSBGA | YBF | 16 | 3000 | RoHS & Green | SAC396 | Level-1-260C-UNLIM | -40 to 85 | 4S311<br>A0 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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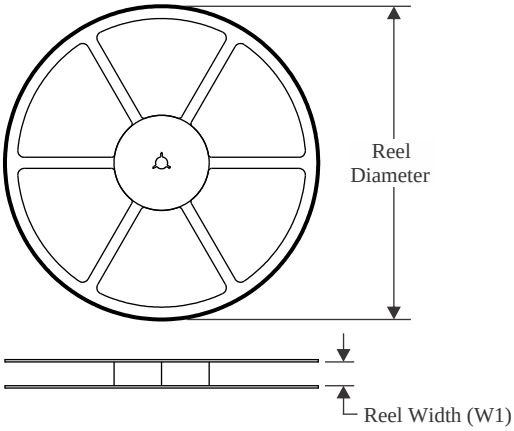
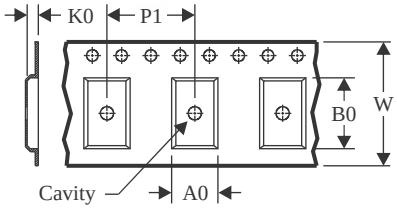
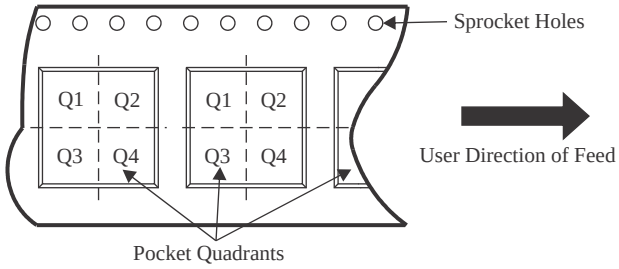



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

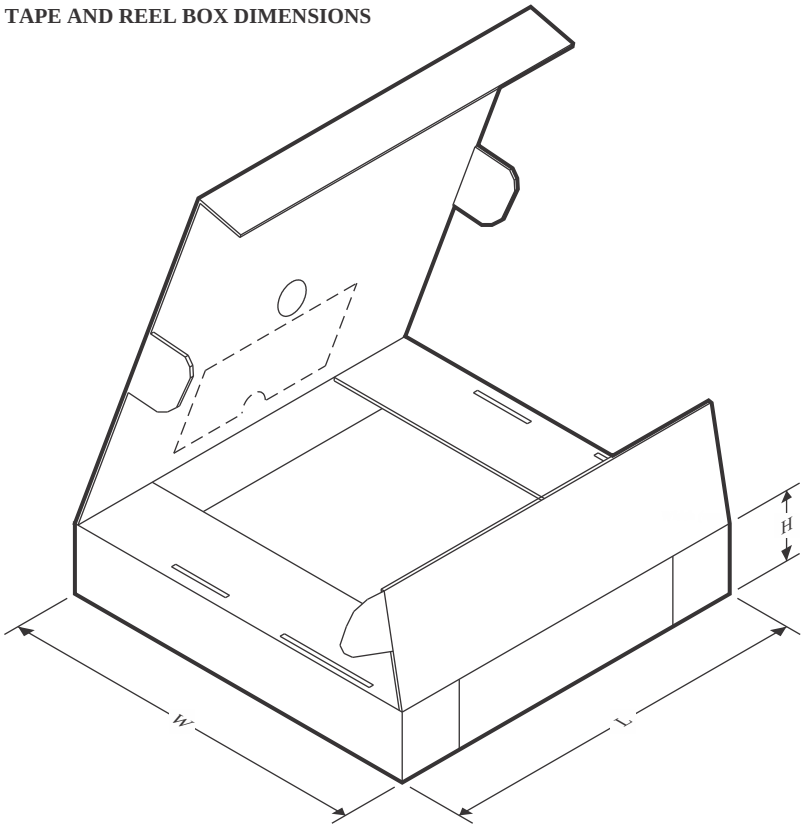
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD4S311AYBFR | DSBGA | YBF | 16 | 3000 | 180.0 | 8.4 | 1.86 | 1.86 | 0.62 | 4.0 | 8.0 | Q1 |
| TPD4S311YBFR | DSBGA | YBF | 16 | 3000 | 180.0 | 8.4 | 1.86 | 1.86 | 0.62 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

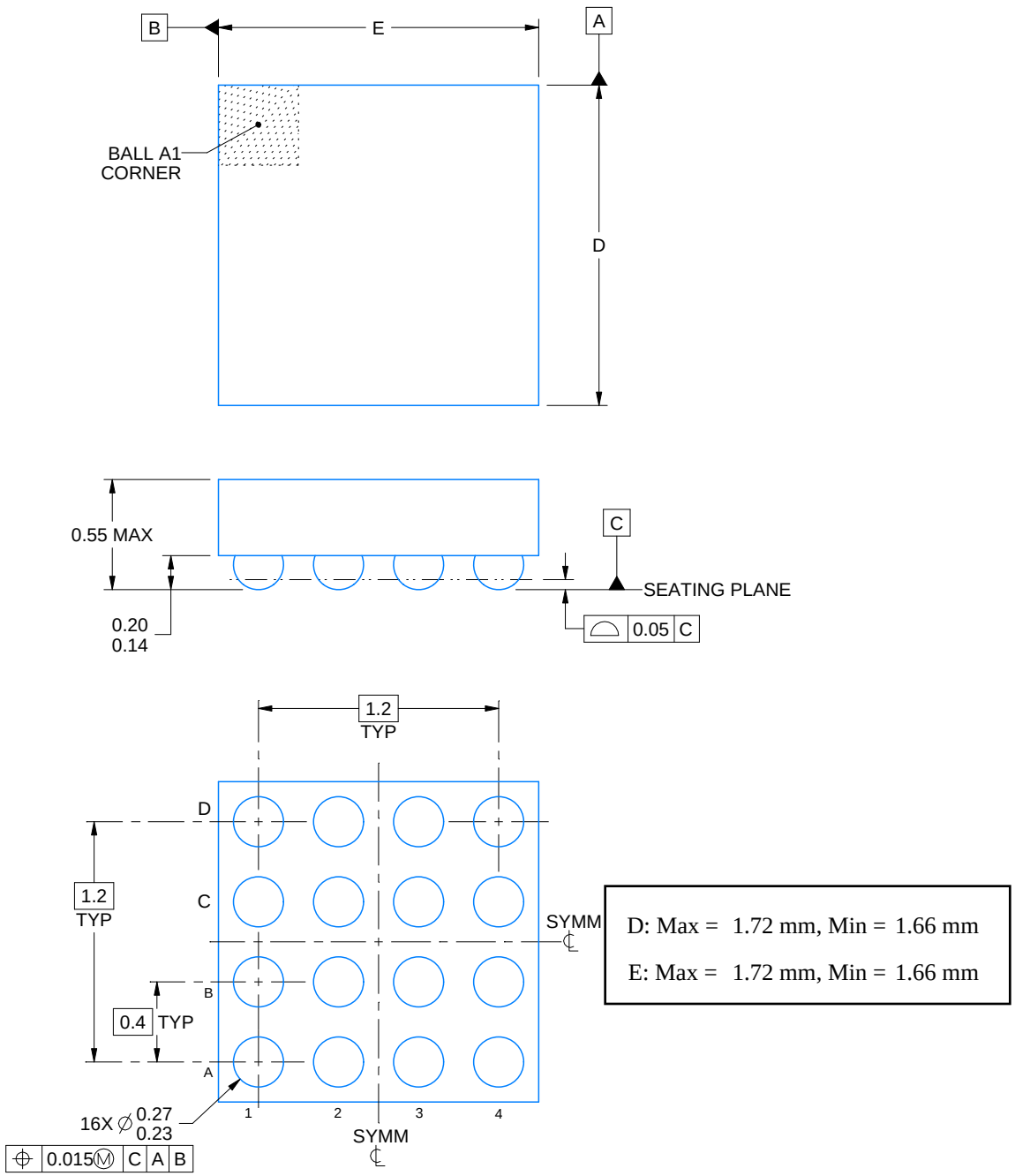
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD4S311AYBFR | DSBGA | YBF | 16 | 3000 | 182.0 | 182.0 | 20.0 |
| TPD4S311YBFR | DSBGA | YBF | 16 | 3000 | 182.0 | 182.0 | 20.0 |

# YBF0016

# PACKAGE OUTLINE

## DSBGA - 0.55 mm max height

DIE SIZE BALL GRID ARRAY

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NOTES:

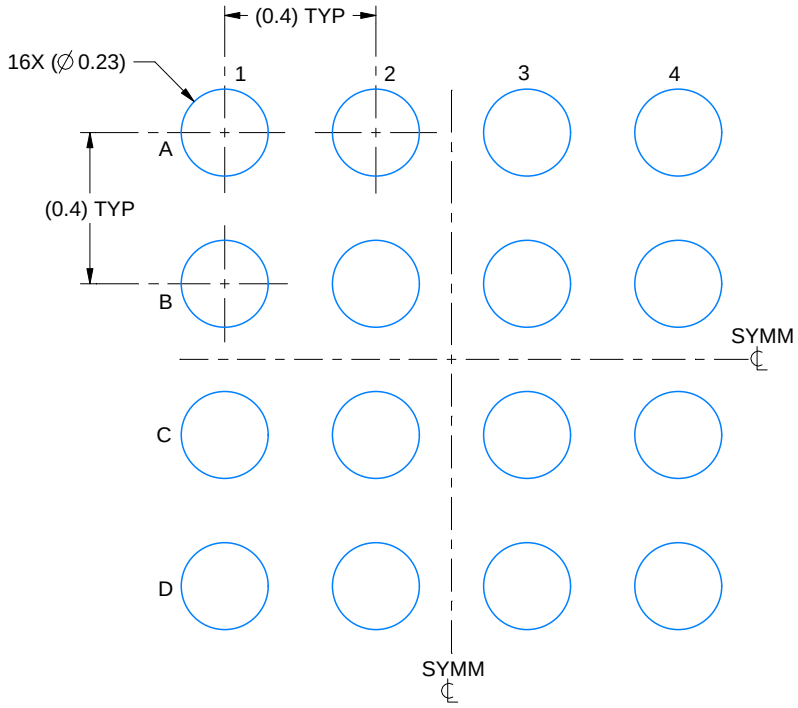
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

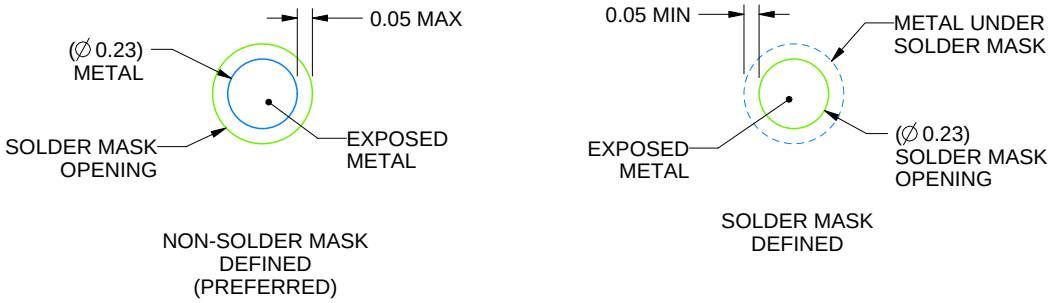
## YBF0016

## DSBGA - 0.55 mm max height

DIE SIZE BALL GRID ARRAY




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X




SOLDER MASK DETAILS
NOT TO SCALE

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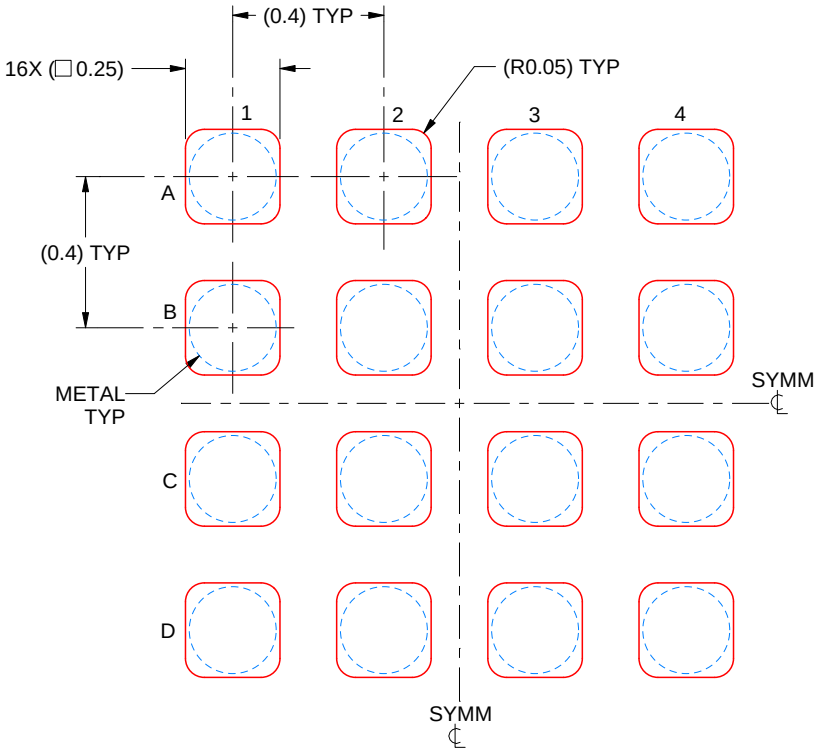
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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