

# 具有动态范围压缩和 **AGC** 功能、每通道可提供 **2.8W** 输出驱动功率的立体声 **D** 类音频放大器

查询样品: [TPA2016D2](#)

## 特性

- 无滤波器 **D** 类架构
- 在 **5V** 电压条件下, 每个通道可为 **8Ω** 负载提供 **1.7W** 的输出驱动功率 (**10% THD + N**)
- 在 **3.6V** 电压条件下, 每个通道可为 **8Ω** 负载时提供 **750mW** 的输出驱动功率 (**10% THD + N**)
- 在 **5V** 电压条件下, 每个通道可为 **4Ω** 负载提供 **2.8W** 的输出驱动功率 (**10% THD + N**)
- 在 **3.6V** 电压条件下, 每个通道可为 **4Ω** 负载提供 **1.5W** 的输出驱动功率 (**10% THD + N**)
- 电源范围: **2.5V** 至 **5.5V**
- 灵活操作 (带/不带 **I<sup>2</sup>C**)
- 可编程 **DRC/AGC** 参数
- 数字 **I<sup>2</sup>C** 音量控制
- 可选增益范围从 **-28dB** 至 **30dB** (**1dB** 步进) (当使用压缩功能时)
- 可选攻击、释放和保持时间
- **4** 种可选压缩比率
- 低电源电流: **3.5mA**
- 低停机电流: **0.2 μA**
- 高 **PSRR**: **80dB**
- 快速启动时间: **5ms**
- **AGC** 启用/禁用功能
- 限制器启用/禁用功能
- 短路和热保护
- 节省空间的封装
  - **2,2 mm × 2,2 mm Nano-Free™ WCSP (YZH)**

## 应用

- 无线或蜂窝手机及 **PDA**
- 便携式导航设备
- 便携式 **DVD** 播放器
- 笔记本 **PC**
- 便携式收音机
- 便携式游戏机
- 教育玩具
- **USB** 扬声器

## 说明

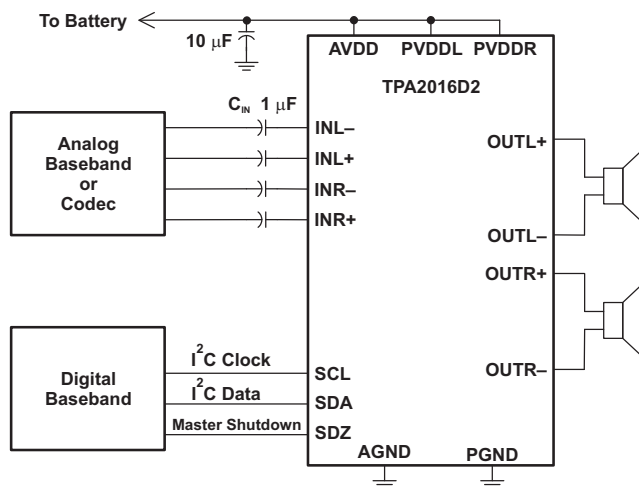
**TPS2016D2** 是一款立体声、无滤波器的 **D** 类音频功率放大器, 具有音量控制、动态范围压缩 (**DRC**) 和自动增益控制 (**AGC**) 功能。该器件采用 **2.2mm x 2.2mm WCSP** 封装和 **20** 引脚 **QFN** 封装。

**TPS2016D2** 中的 **DRC / AGC** 功能可通过一个数字 **I<sup>2</sup>C** 接口来编程。**DRC / AGC** 功能可通过配置自动地防止音频信号的失真, 并对一般听不到的寂静声音片段进行提升。另外, 还可以通过配置来使 **DRC / AGC** 功能保护扬声器在高功率电平下不受损坏, 并压缩音乐的动态范围以令其处于扬声器的动态范围内。增益的可选范围从 **-28dB** 至 **+30dB** (**1dB** 步进)。

**TPS2016D2** 能为 **8Ω** 负载提供每通道 **1.7W** (在 **5V** 电压下) 或 **750mW** (在 **3.3V** 电压下) 的驱动功率; 或者为 **4Ω** 负载提供每通道 **2.8W** (在 **5V** 电压下) 或 **1.5W** (在 **3.3V** 电压下) 的驱动功率。该器件具有用于每个通道的独立软件停机控制功能, 而且还提供了热保护和短路保护。

除了上述特性之外, 快速启动时间和小巧的封装尺寸还使 **TPS2016D2** 成为蜂窝手机、**PDA** 和其他便携式应用的理想选择。

## 简化的应用示意图



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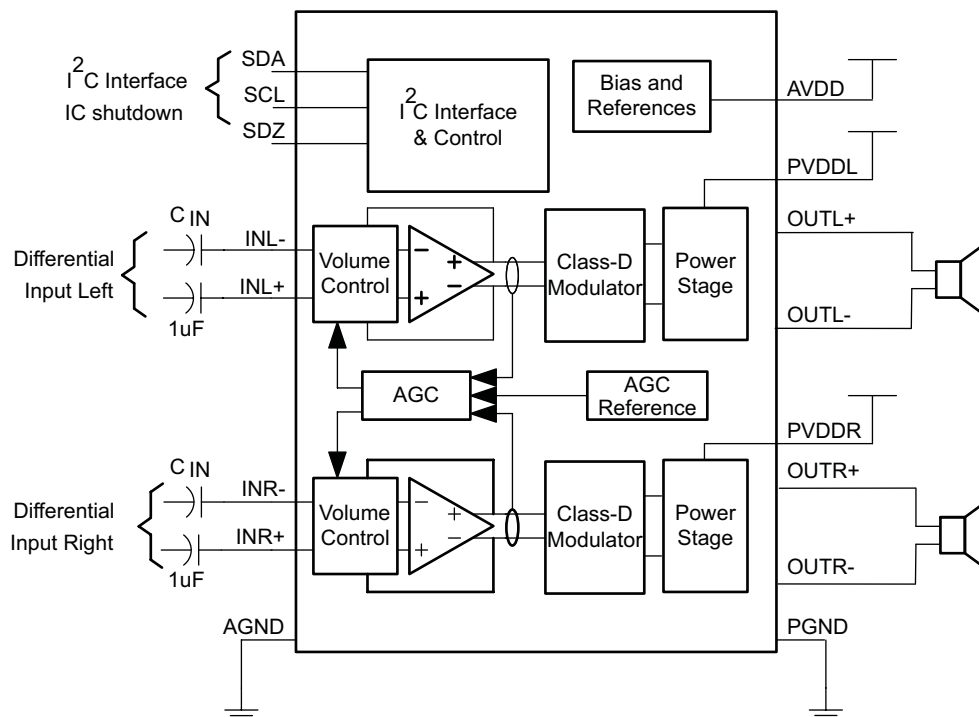
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English Data Sheet: [SLOS524D](#)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

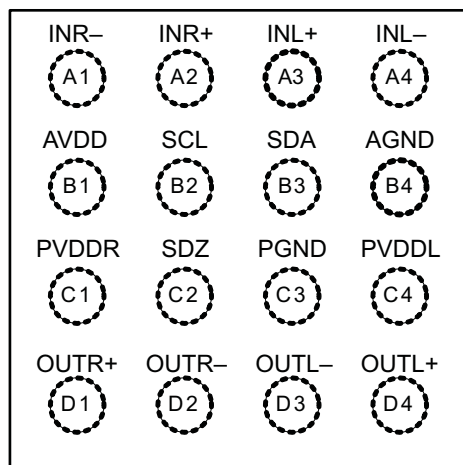
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### FUNCTIONAL BLOCK DIAGRAM

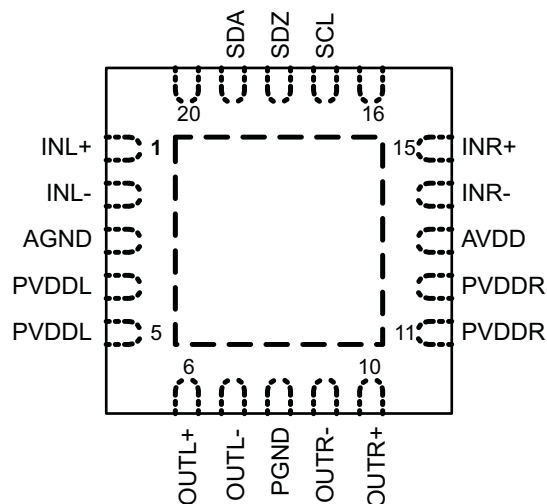


### DEVICE PINOUT

**YZH (WCSP) PACKAGE  
(Top View)**



**RTJ (QFN) PACKAGE  
(Top View)**



## PIN FUNCTIONS

| PIN   |      |        | I/O/P | DESCRIPTION   |
|-------|------|--------|-------|---|
| NAME  | WCSP | RTJ    |       |   |
| INR+  | A2   | 15     | I     | Right channel positive audio input                              |
| INR–  | A1   | 14     | I     | Right channel negative audio input                              |
| INL+  | A3   | 1      | I     | Left channel positive audio input                               |
| INL–  | A4   | 2      | I     | Left channel negative audio input                               |
| SDZ   | C2   | 18     | I     | Shutdown terminal (active low)                                  |
| SDA   | B3   | 19     | I/O   | I <sup>2</sup> C data interface                                 |
| SCL   | B2   | 17     | I     | I <sup>2</sup> C clock interface                                |
| OUTR+ | D1   | 10     | O     | Right channel positive differential output                      |
| OUTR– | D2   | 9      | O     | Right channel negative differential output                      |
| OUTL+ | D4   | 6      | O     | Left channel positive differential output                       |
| OUTL– | D3   | 7      | O     | Left channel negative differential output                       |
| AVDD  | B1   | 13     | P     | Analog supply (must be the same as PVDDR and PVDDL)             |
| AGND  | B4   | 3      | P     | Analog ground (all GND pins need to be connected)               |
| PVDDR | C1   | 11, 12 | P     | Right channel power supply (must be the same as AVDD and PVDDL) |
| PGND  | C3   | 8      | P     | Power ground (all GND pins need to be connected)                |
| PVDDL | C4   | 4, 5   | P     | Left channel power supply (must be the same as AVDD and PVDDR)  |
|       |      | 16, 20 |       | Not connected   |

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted).

|                   |  |                             | VALUE / UNIT                     |
|-------------------|--|-----------------------------|----------------------------------|
| V <sub>DD</sub>   | Supply voltage                               | AVDD, PVDDR, PVDDL          | –0.3 V to 6 V                    |
|                   | Input voltage                                | SDZ, INR+, INR–, INL+, INL– | –0.3 V to V <sub>DD</sub> +0.3 V |
|                   |  | SDA, SCL                    | –0.3 V to 6 V                    |
|                   | Continuous total power dissipation           |                             | See Dissipation Ratings Table    |
| T <sub>A</sub>    | Operating free-air temperature range         |                             | –40°C to +85°C                   |
| T <sub>J</sub>    | Operating junction temperature range         |                             | –40°C to 150°C                   |
| T <sub>stg</sub>  | Storage temperature range                    |                             | –65°C to 150°C                   |
| ESD               | Electro-Static Discharge Tolerance, all pins | Human Body Model (HBM)      | 2 KV                             |
|                   |  | Charged Device Model (CDM)  | 500 V                            |
| R <sub>LOAD</sub> | Minimum load resistance                      |                             | 3.2 Ω                            |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS TABLE<sup>(1)</sup>

| PACKAGE      | T <sub>A</sub> ≤ 25°C | DERATING FACTOR | T <sub>A</sub> = 70°C | T <sub>A</sub> = 85°C |
|--------------|-----------------------|-----------------|-----------------------|-----------------------|
| 16-ball WCSP | 1.25 W                | 10 mW/°C        | 0.8 W                 | 0.65 W                |
| 20-pin QFN   | 5.2 W                 | 41.6 mW/°C      | 3.12 W                | 2.7 W                 |

- (1) Dissipations ratings are for a 2-side, 2-plane PCB.

**AVAILABLE OPTIONS<sup>(1)</sup>**

| T <sub>A</sub> | PACKAGED DEVICES <sup>(2)</sup>                                 | PART NUMBER   | SYMBOL |
|----------------|---|---------------|--------|
| –40°C to 85°C  | 16-ball, 2,2 mm × 2,2 mm WCSP (+0.01 mm/<br>–0.09 mm tolerance) | TPA2016D2YZHR | CCJ    |
|                |   | TPA2016D2YZHT | CCJ    |
| –40°C to 85°C  | 20-pin, 4 mm × 4 mm QFN (RTJ)                                   | TPA2016D2RTJR | –      |
|                |   | TPA2016D2RTJT | –      |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com)
- (2) The YZH packages are only available taped and reeled. The suffix R indicates a reel of 3000; the suffix T indicates a reel of 250.

**RECOMMENDED OPERATING CONDITIONS**

|                 |                                |                    | MIN | MAX | UNIT |
|-----------------|--------------------------------|--------------------|-----|-----|------|
| V <sub>DD</sub> | Supply voltage                 | AVDD, PVDDR, PVDDL | 2.5 | 5.5 | V    |
| V <sub>IH</sub> | High-level input voltage       | SDZ, SDA, SCL      | 1.3 |     | V    |
| V <sub>IL</sub> | Low-level input voltage        | SDZ, SDA, SCL      |     | 0.6 | V    |
| T <sub>A</sub>  | Operating free-air temperature |                    | −40 | +85 | °C   |

**ELECTRICAL CHARACTERISTICS**

at T<sub>A</sub> = 25°C, V<sub>DD</sub> = 3.6 V, SDZ = 1.3 V, and R<sub>L</sub> = 8 Ω + 33 μH (unless otherwise noted).

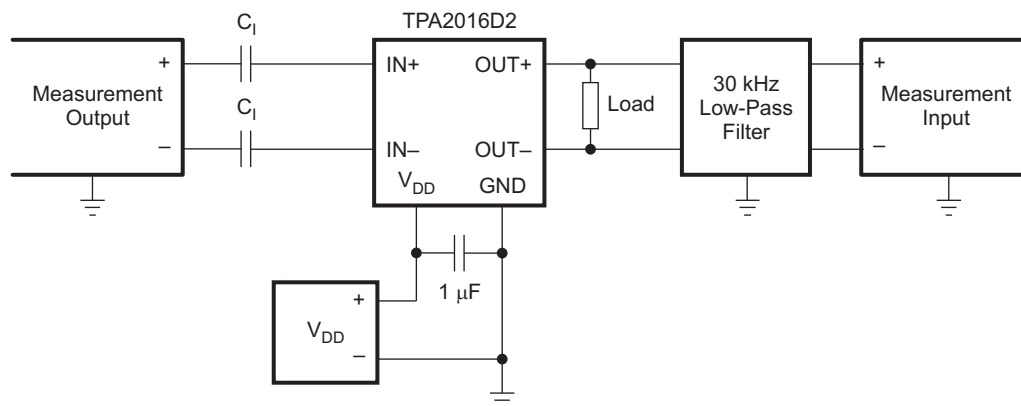
| PARAMETER          | TEST CONDITIONS                       | MIN  | TYP | MAX | UNIT |
|--------------------|---------------------------------------|------|-----|-----|------|
| V <sub>DD</sub>    | Supply voltage range                  | 2.5  | 3.6 | 5.5 | V    |
| I <sub>SDZ</sub>   | SDZ = 0.35 V, V <sub>DD</sub> = 2.5 V |      | 0.1 | 1   | μA   |
|                    | SDZ = 0.35 V, V <sub>DD</sub> = 3.6 V |      | 0.2 | 1   |      |
|                    | SDZ = 0.35 V, V <sub>DD</sub> = 5.5 V |      | 0.3 | 1   |      |
| I <sub>SWS</sub>   | SDZ = 1.3 V, V <sub>DD</sub> = 2.5 V  |      | 35  | 50  | μA   |
|                    | SDZ = 1.3 V, V <sub>DD</sub> = 3.6 V  |      | 50  | 70  |      |
|                    | SDZ = 1.3 V, V <sub>DD</sub> = 5.5 V  |      | 75  | 110 |      |
| I <sub>DD</sub>    | V <sub>DD</sub> = 2.5 V               |      | 3.5 | 4.5 | mA   |
|                    | V <sub>DD</sub> = 3.6 V               |      | 3.7 | 4.7 |      |
|                    | V <sub>DD</sub> = 5.5 V               |      | 4.5 | 5.5 |      |
| f <sub>SW</sub>    | Class D Switching Frequency           | 275  | 300 | 325 | kHz  |
| I <sub>IH</sub>    | High-level input current              |      |     | 1   | μA   |
| I <sub>IL</sub>    | Low-level input current               | –1   |     |     | μA   |
| t <sub>START</sub> | Start-up time                         |      | 5   |     | ms   |
| POR                | Power on reset ON threshold           |      | 2   | 2.3 | V    |
| POR                | Power on reset hysteresis             |      | 0.2 |     | V    |
| CMRR               | Input common mode rejection           |      | –70 |     | dB   |
| V <sub>oo</sub>    | Output offset voltage                 | –10  | 2   | 10  | mV   |
| Z <sub>OUT</sub>   | Output Impedance in shutdown mode     |      | 2   |     | kΩ   |
|                    | Gain accuracy                         | –0.5 |     | 0.5 | dB   |
| PSRR               | Power supply rejection ratio          |      | –80 |     | dB   |

## OPERATING CHARACTERISTICS

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.6\text{V}$ ,  $SDZ = 1.3\text{ V}$ ,  $R_L = 8\ \Omega + 33\ \mu\text{H}$ , and  $A_v = 6\text{ dB}$  (unless otherwise noted).

| PARAMETER                                     | TEST CONDITIONS   | MIN | TYP  | MAX   | UNIT          |
|---|---|-----|------|-------|---------------|
| $k_{SVR}$ power-supply ripple rejection ratio | $V_{DD} = 3.6\text{ Vdc}$ with ac of $200\text{ mV}_{PP}$ at $217\text{ Hz}$    |     | -68  |       | dB            |
| THD+N Total harmonic distortion + noise       | $f_{aud\_in} = 1\text{ kHz}$ ; $P_O = 550\text{ mW}$ ; $V_{DD} = 3.6\text{ V}$  |     | 0.1% |       |               |
|   | $f_{aud\_in} = 1\text{ kHz}$ ; $P_O = 1\text{ W}$ ; $V_{DD} = 5\text{ V}$       |     | 0.1% |       |               |
|   | $f_{aud\_in} = 1\text{ kHz}$ ; $P_O = 630\text{ mW}$ ; $V_{DD} = 3.6\text{ V}$  |     | 1%   |       |               |
|   | $f_{aud\_in} = 1\text{ kHz}$ ; $P_O = 1.4\text{ W}$ ; $V_{DD} = 5\text{ V}$     |     | 1%   |       |               |
| $N_{fo_{nF}}$ Output integrated noise         | $A_v = 6\text{ dB}$   |     | 44   |       | $\mu\text{V}$ |
| $N_{fo_A}$ Output integrated noise            | $A_v = 6\text{ dB floor}$ , A-weighted  |     | 33   |       | $\mu\text{V}$ |
| FR Frequency response                         | $A_v = 6\text{ dB}$   | 20  |      | 20000 | Hz            |
| $P_{O_{max}}$ Maximum output power            | THD+N = 10%, $V_{DD} = 5\text{ V}$ , $R_L = 8\ \Omega$                          |     | 1.72 |       | W             |
|   | THD+N = 10%, $V_{DD} = 3.6\text{ V}$ , $R_L = 8\ \Omega$                        |     | 750  |       | mW            |
|   | THD+N = 10%, $V_{DD} = 5\text{ V}$ , $R_L = 4\ \Omega$                          |     | 2.8  |       | W             |
|   | THD+N = 10%, $V_{DD} = 3.6\text{ V}$ , $R_L = 4\ \Omega$                        |     | 1.5  |       | mW            |
| $\eta$ Efficiency                             | THD+N = 1%, $V_{DD} = 3.6\text{ V}$ , $R_L = 8\ \Omega$ , $P_O = 0.63\text{ W}$ |     | 90%  |       |               |
|   | THD+N = 1%, $V_{DD} = 5\text{ V}$ , $R_L = 8\ \Omega$ , $P_O = 1.4\text{ W}$    |     | 90%  |       |               |

**Figure 1. TEST SET-UP FOR GRAPHS**



- (1) All measurements were taken with a  $1\text{-}\mu\text{F}$   $C_1$  (unless otherwise noted.)
- (2) A  $33\text{-}\mu\text{H}$  inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.
- (3) The  $30\text{-kHz}$  low-pass filter is required, even if the analyzer has an internal low-pass filter. An RC low-pass filter ( $1\text{ k}\Omega$   $4.7\text{ nF}$ ) is used on each output for the data sheet graphs.
- (4) All THD + N graphs are taken with outputs out of phase (unless otherwise noted). All data is taken on left channel.
- (5) All data is taken on the WCSP package unless otherwise noted.

## I<sup>2</sup>C TIMING CHARACTERISTICS

For I<sup>2</sup>C Interface Signals Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS | MIN | TYP | MAX | UNIT    |
|--|-----------------|-----|-----|-----|---------|
| $f_{SCL}$ Frequency, SCL                                   | No wait states  |     |     | 400 | kHz     |
| $t_{W(H)}$ Pulse duration, SCL high                        |                 | 0.6 |     |     | $\mu$ s |
| $t_{W(L)}$ Pulse duration, SCL low                         |                 | 1.3 |     |     | $\mu$ s |
| $t_{SU(1)}$ Setup time, SDA to SCL                         |                 | 100 |     |     | ns      |
| $t_{H1}$ Hold time, SCL to SDA                             |                 | 10  |     |     | ns      |
| $t_{(buf)}$ Bus free time between stop and start condition |                 | 1.3 |     |     | $\mu$ s |
| $t_{SU2}$ Setup time, SCL to start condition               |                 | 0.6 |     |     | $\mu$ s |
| $t_{H2}$ Hold time, start condition to SCL                 |                 | 0.6 |     |     | $\mu$ s |
| $t_{SU3}$ Setup time, SCL to stop condition                |                 | 0.6 |     |     | $\mu$ s |

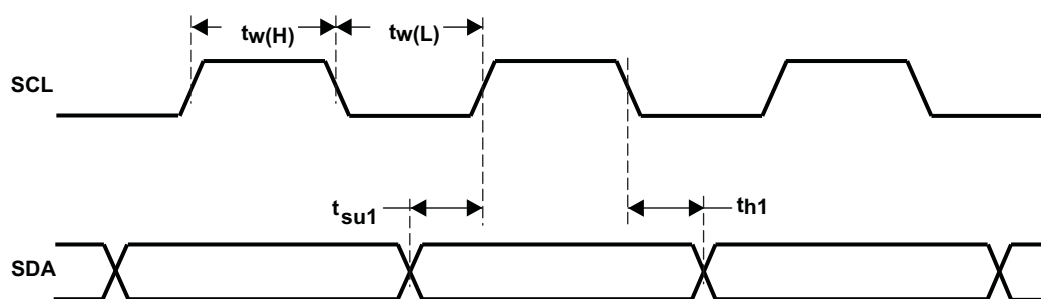


Figure 2. SCL and SDA Timing

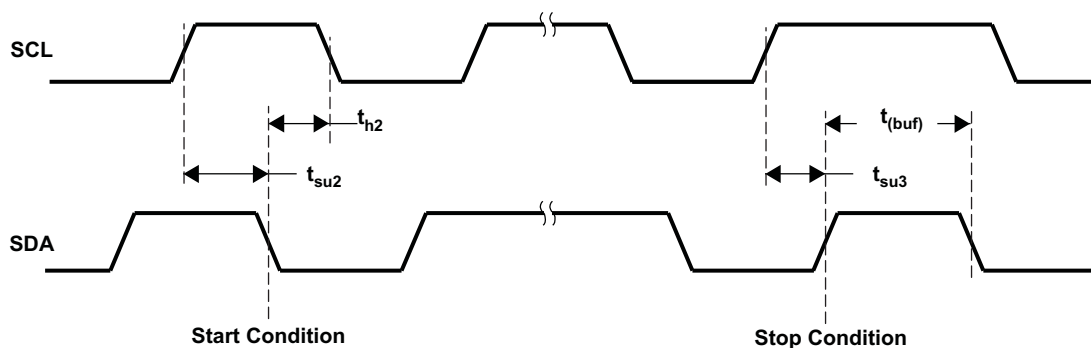


Figure 3. Start and Stop Conditions Timing

## TYPICAL CHARACTERISTICS

with  $C_{(DECOUPLE)} = 1 \mu\text{F}$ ,  $C_I = 1 \mu\text{F}$ .

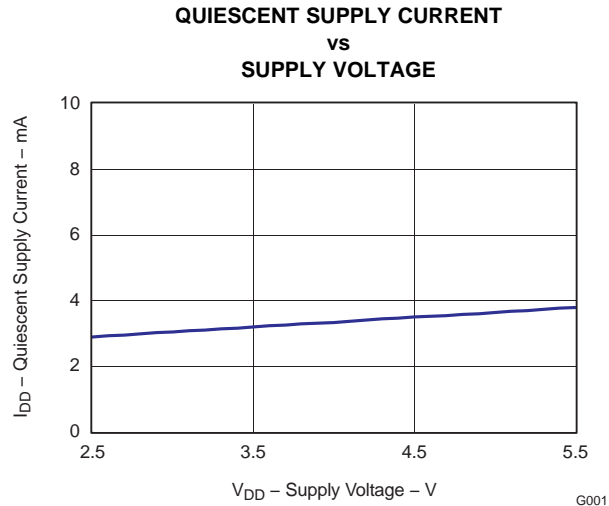


Figure 4.

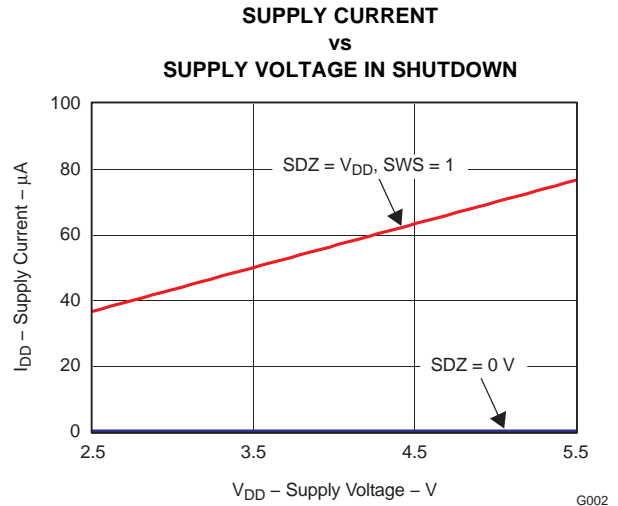


Figure 5.

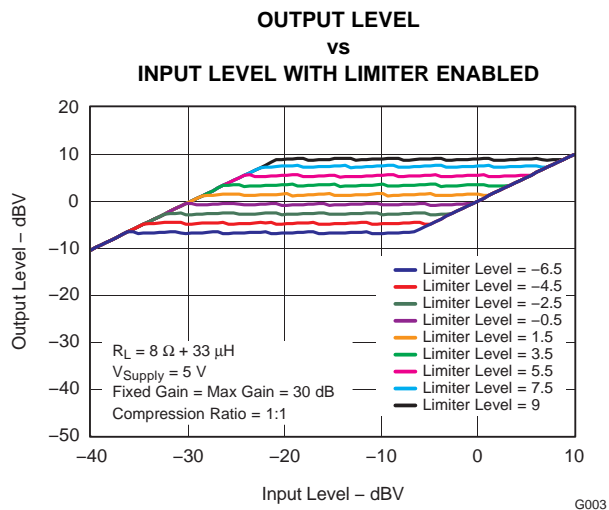


Figure 6.

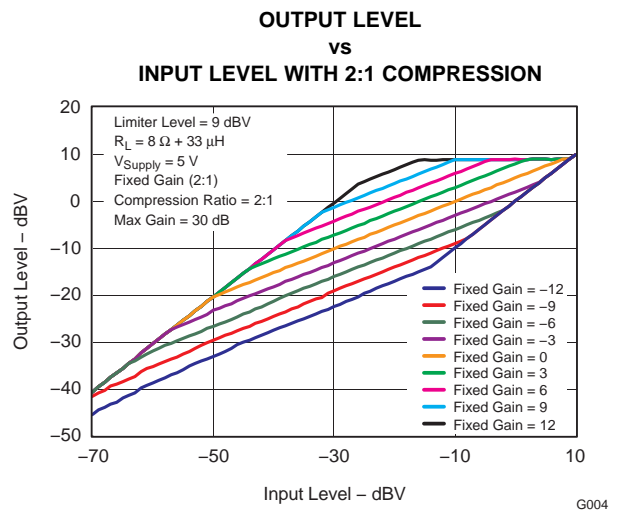


Figure 7.

## TYPICAL CHARACTERISTICS (continued)

with  $C_{(\text{DECOUPLE})} = 1 \mu\text{F}$ ,  $C_I = 1 \mu\text{F}$ .

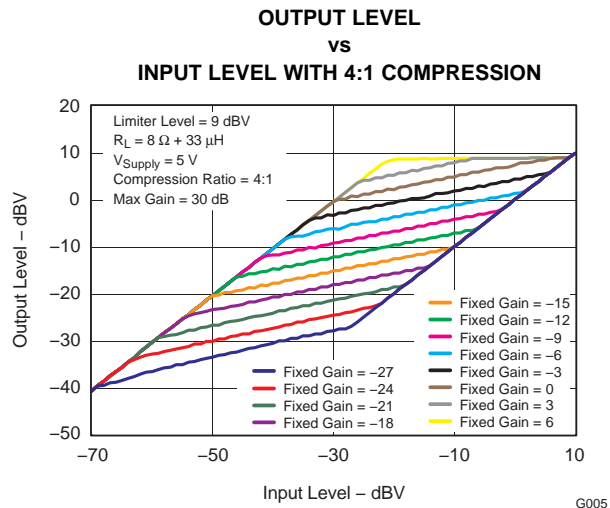


Figure 8.

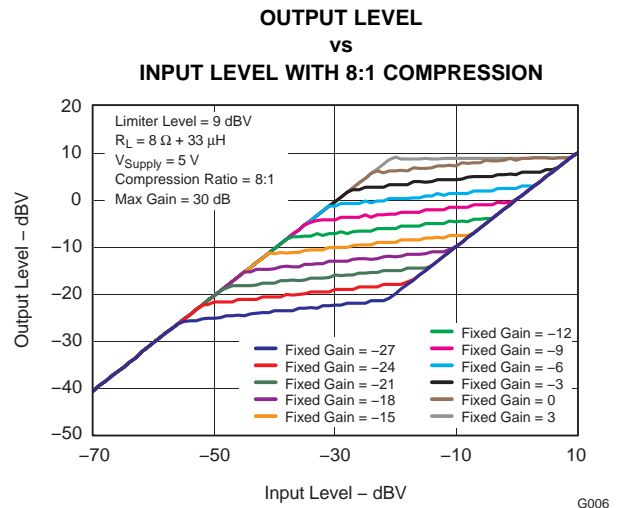


Figure 9.

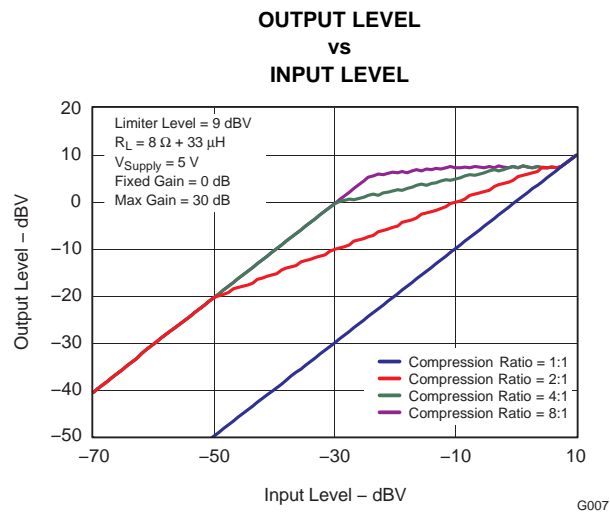


Figure 10.

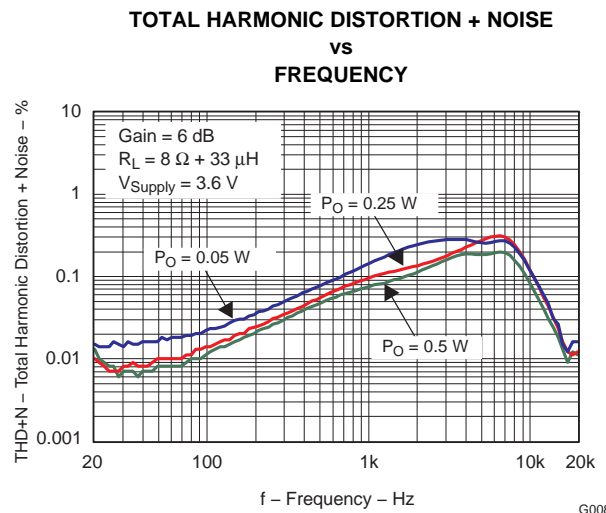


Figure 11.



## TYPICAL CHARACTERISTICS (continued)

with  $C_{(DECOUPLE)} = 1 \mu\text{F}$ ,  $C_I = 1 \mu\text{F}$ .

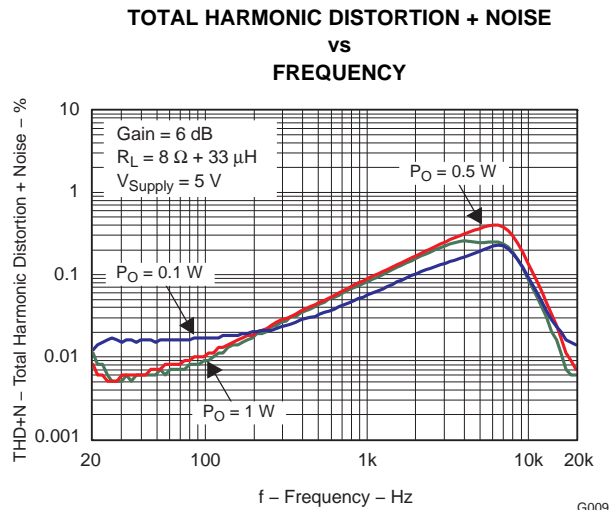


Figure 12.

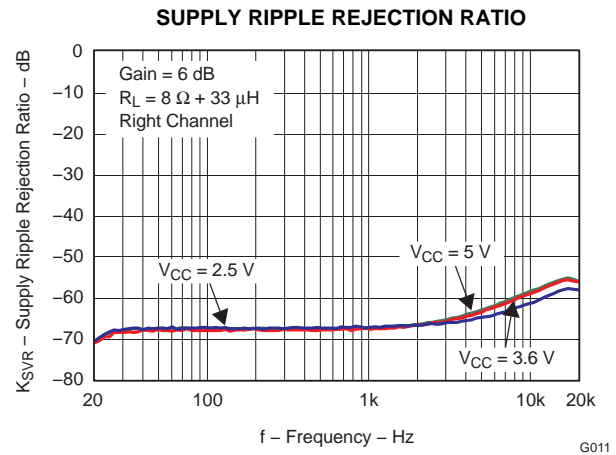


Figure 13.

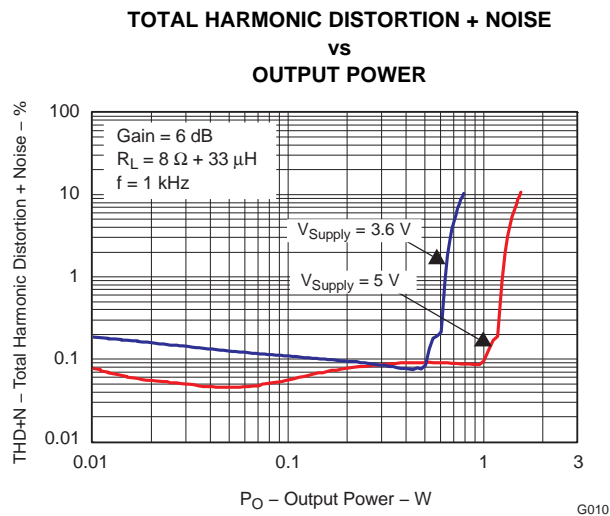


Figure 14.

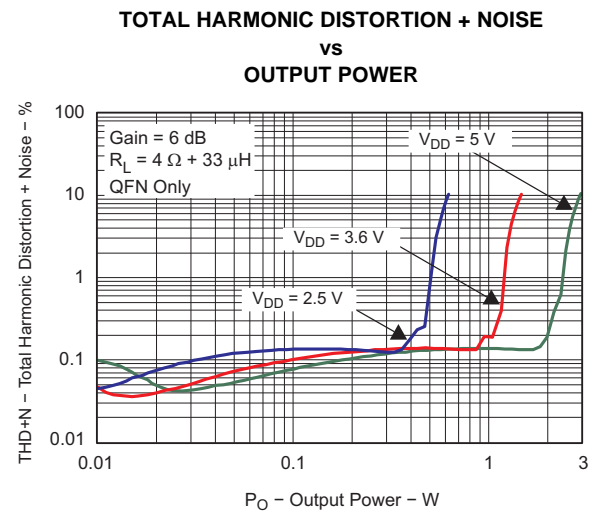


Figure 15.

## TYPICAL CHARACTERISTICS (continued)

with  $C_{\text{DECOUPLE}} = 1 \mu\text{F}$ ,  $C_I = 1 \mu\text{F}$ .

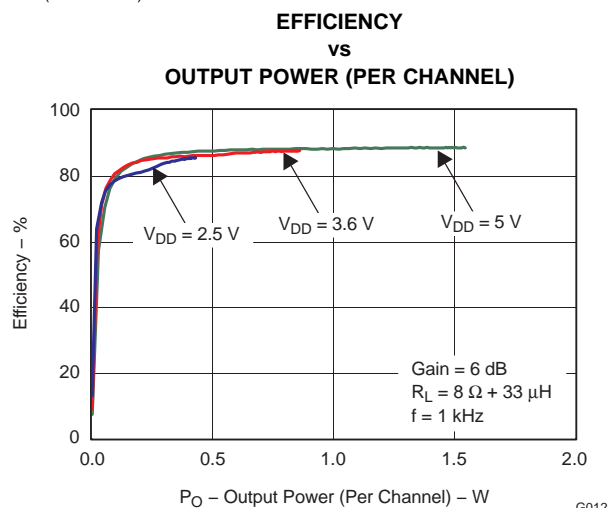


Figure 16.

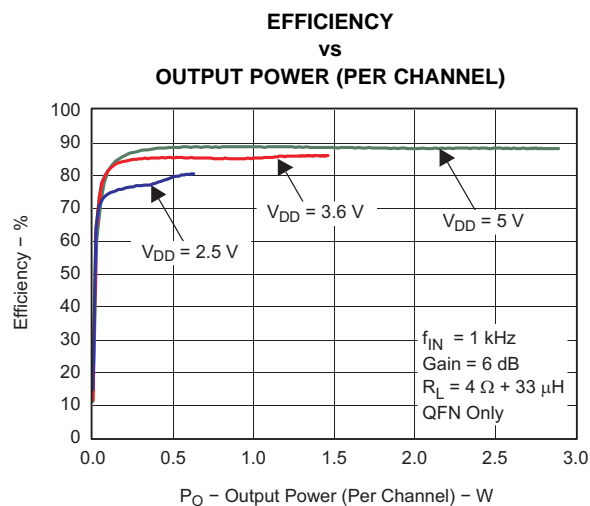


Figure 17.

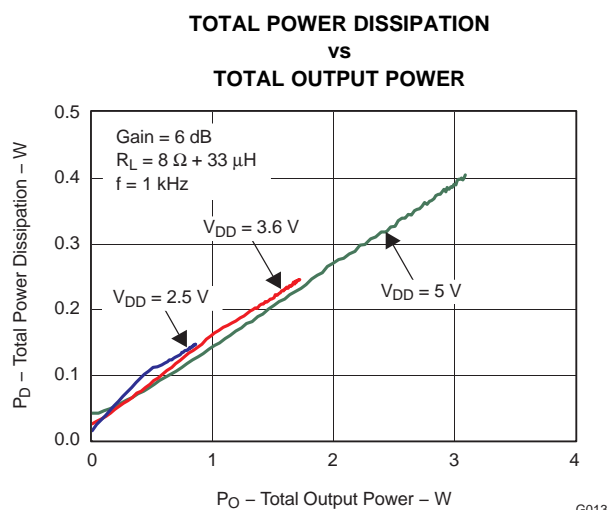


Figure 18.

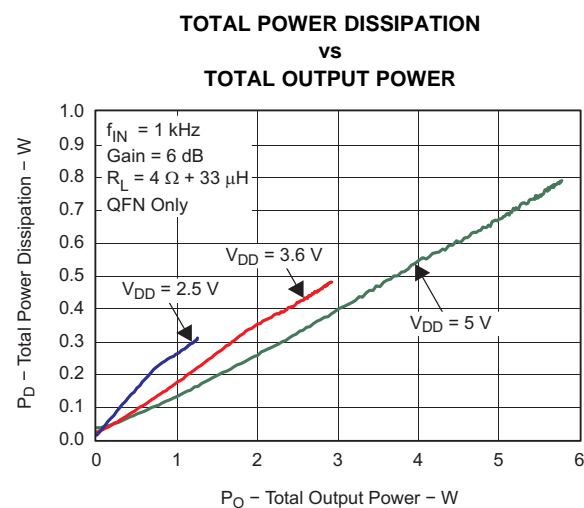


Figure 19.

## TYPICAL CHARACTERISTICS (continued)

with  $C_{\text{DECOUPLE}} = 1 \mu\text{F}$ ,  $C_1 = 1 \mu\text{F}$ .

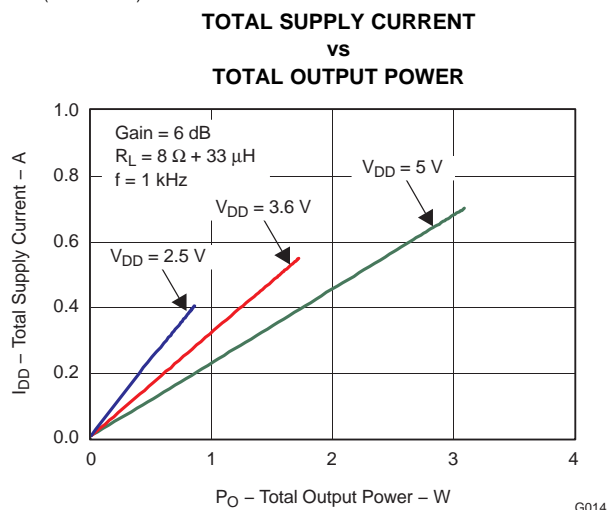


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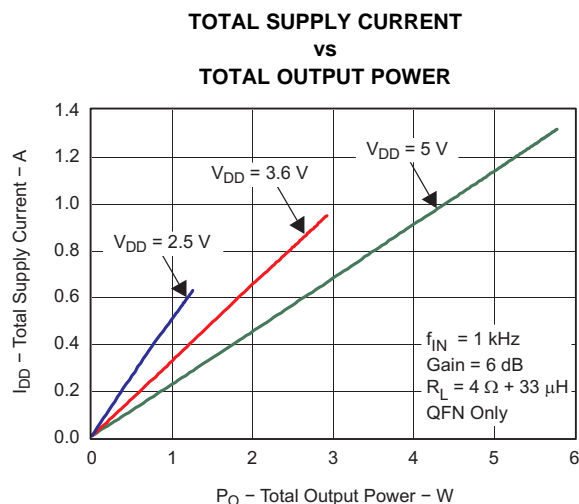


Figure 21.

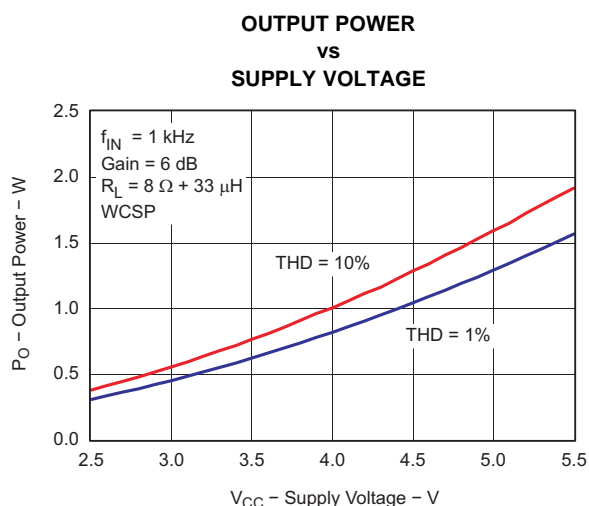


Figure 22.

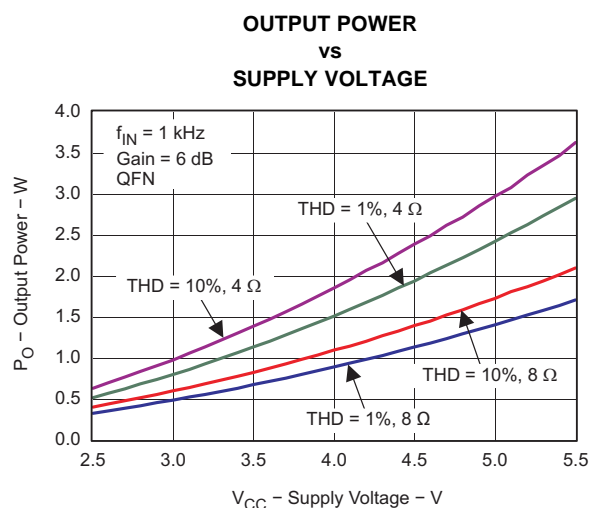


Figure 23.

## APPLICATION INFORMATION

### AUTOMATIC GAIN CONTROL

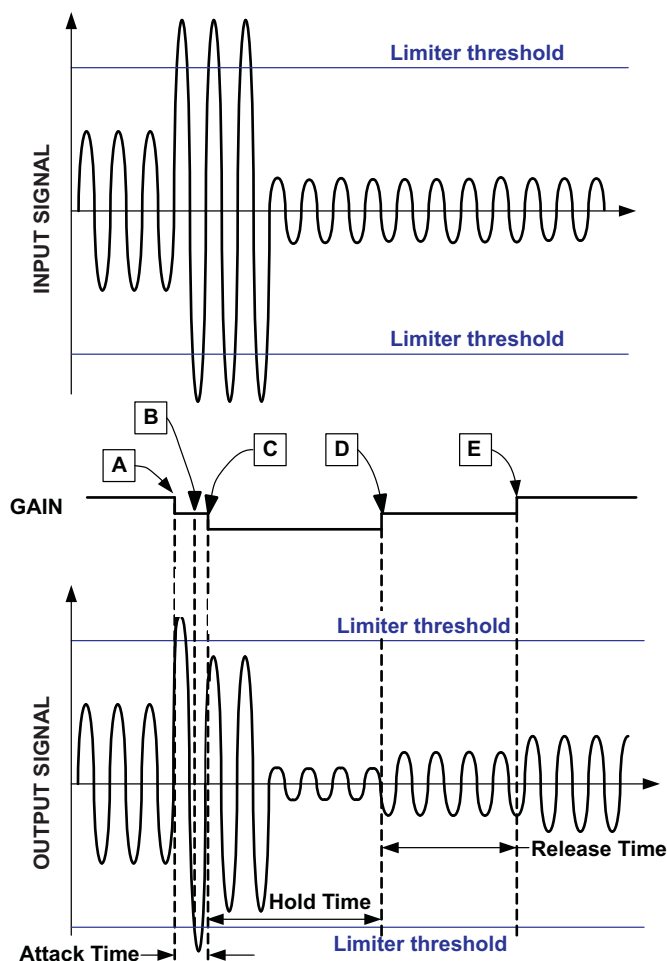
The Automatic Gain Control (AGC) feature provides continuous automatic gain adjustment to the amplifier through an internal PGA. This feature enhances the perceived audio loudness and at the same time prevents speaker damage from occurring (Limiter function).

The AGC function attempts to maintain the audio signal gain as selected by the user through the Fixed Gain, Limiter Level, and Compression Ratio variables. Other advanced features included are Maximum Gain and Noise Gate Threshold. [Table 1](#) describes the function of each variable in the AGC function.

**Table 1. TPA2016D2 AGC Variable Descriptions**

| VARIABLE             | DESCRIPTION  |
|----------------------|--|
| Maximum Gain         | The gain at the lower end of the compression region.   |
| Fixed Gain           | The normal gain of the device when the AGC is inactive.<br>The fixed gain is also the initial gain when the device comes out of shutdown mode or when the AGC is disabled. |
| Limiter Level        | The value that sets the maximum allowed output amplitude.  |
| Compression Ratio    | The relation between input and output voltage.   |
| Noise Gate Threshold | Below this value, the AGC holds the gain to prevent breathing effects.   |
| Attack Time          | The minimum time between two gain decrements.  |
| Release Time         | The minimum time between two gain increments.  |
| Hold Time            | The time it takes for the very first gain increment after the input signal amplitude decreases.  |

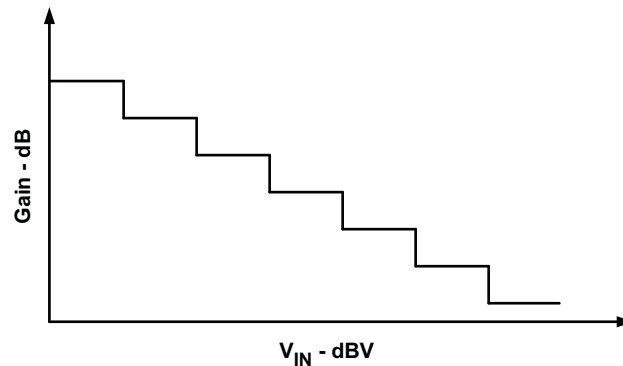
The AGC works by detecting the audio input envelope. The gain changes depending on the amplitude, the limiter level, the compression ratio, and the attack and release time. The gain changes constantly as the audio signal increases and/or decreases to create the compression effect. The gain step size for the AGC is 0.5 dB. If the audio signal has near-constant amplitude, the gain does not change. Figure 26 shows how the AGC works.



- A. Gain decreases with no delay; attack time is reset. Release time and hold time are reset.
- B. Signal amplitude above limiter level, but gain cannot change because attack time is not over.
- C. Attack time ends; gain is allowed to decrease from this point forward by one step. Gain decreases because the amplitude remains above limiter threshold. All times are reset
- D. Gain increases after release time finishes and signal amplitude remains below desired level. All times are reset after the gain increase.
- E. Gain increases after release time is finished again because signal amplitude remains below desired level. All times are reset after the gain increase.

**Figure 26. Input and Output Audio Signal vs Time**

Since the number of gain steps is limited the compression region is limited as well. The following figure shows how the gain changes vs. the input signal amplitude in the compression region.



**Figure 27. Input Signal Voltage vs Gain**

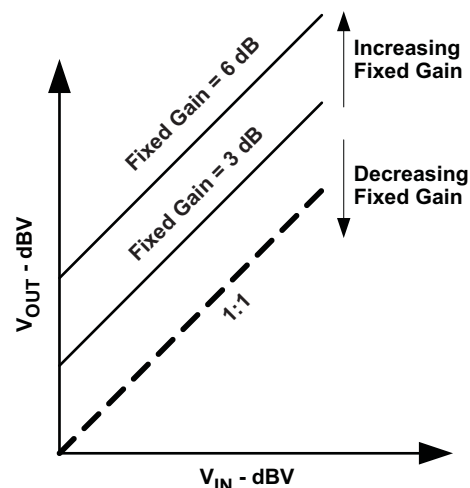
Thus the AGC performs a mapping of the input signal vs. the output signal amplitude. This mapping can be modified according to the variables from [Table 1](#).

The following graphs and explanations show the effect of each variable to the AGC independently and which considerations should be taken when choosing values.

**Fixed Gain:** The fixed gain determines the initial gain of the AGC. Set the gain using the following variables:

- Set the fixed gain to be equal to the gain when the AGC is disabled.
- Set the fixed gain to maximize SNR.
- Set the fixed gain such that it will not overdrive the speaker.

[Figure 28](#) shows how the fixed gain influences the input signal amplitude vs. the output signal amplitude state diagram. The dotted 1:1 line is displayed for reference. The 1:1 line means that for a 1dB increase in the input signal, the output increases by 1dB.



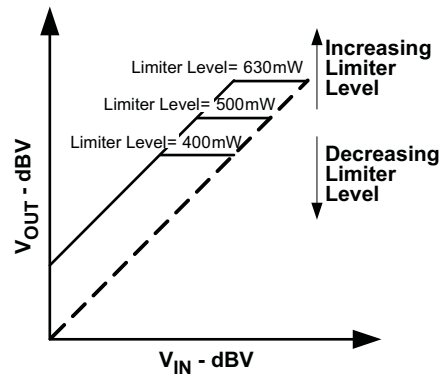
**Figure 28. Output Signal vs Input Signal State Diagram Showing Different Fixed Gain Configurations**

If the Compression function is enabled, the Fixed Gain is adjustable from –28dB to 30dB. If the Compression function is disabled, the Fixed gain is adjustable from 0dB to 30dB.

**Limiter Level:** The Limiter level sets the maximum amplitude allowed at the output of the amplifier. The limiter should be set with the following constraints in mind:

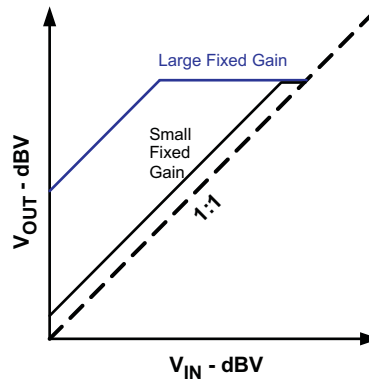
- Below or at the maximum power rating of the speaker
- Below the minimum supply voltage in order to avoid clipping

[Figure 29](#) shows how the limiter level influences the input signal amplitude vs. the output signal amplitude state diagram.



**Figure 29. Output Signal vs Input Signal State Diagram Showing Different Limiter Level Configurations**

The limiter level and the fixed gain influence each other. If the fixed gain is set high, the AGC has a large limiter range. The fixed gain is set low, the AGC has a short limiter range. Figure 30 illustrates the two examples:



**Figure 30. Output Signal vs. Input Signal State Diagram Showing Same Limiter Level Configurations with Different Fixed Gain Configurations**

**Compression Ratio:** The compression ratio sets the relation between input and output signal outside the limiter level region. The compression ratio compresses the dynamic range of the audio. For example if the audio source has a dynamic range of 60dB and compression ratio of 2:1 is selected, then the output has a dynamic range of 30dB. Most small form factor speakers have small dynamic range. Compression ratio allows audio with large dynamic range to fit into a speaker with small dynamic range.

The compression ratio also increases the loudness of the audio without increasing the peak voltage. The higher the compression ratio, the louder the perceived audio.

For example:

- A compression ratio of 4:1 is selected (meaning that a 4dB change in the input signal results in a 1dB signal change at the output)
- A fixed gain of 0dB is selected and the maximum audio level is at 0dBV.

When the input signal decreases to -32dBV, the amplifier increases the gain to 24dB in order to achieve an output of -8dBV. The output signal amplitude equation is:

$$\text{Output signal amplitude} = \frac{\text{Input signal initial amplitude} - |\text{Current input signal amplitude}|}{\text{Compression ratio}} \quad (1)$$

In this example:

$$-8\text{dBV} = \frac{0\text{dBV} - |-32\text{dBV}|}{4} \quad (2)$$

The gain change equation is:

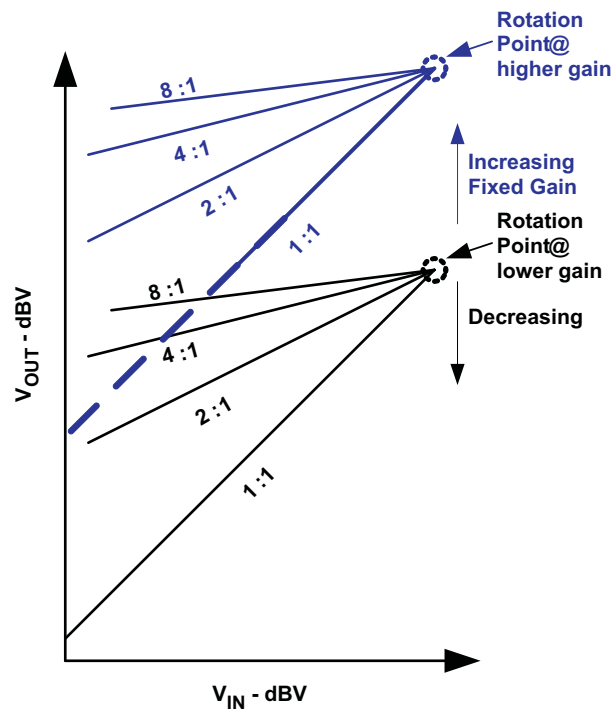
$$\text{Gain change} = \left( 1 - \frac{1}{\text{Compression ratio}} \right) \times \text{Input signal change} \quad (3)$$

$$24 \text{ dB} = \left( 1 - \frac{1}{4} \right) \times 32 \quad (4)$$

Consider the following when setting the compression ratio:

- Dynamic range of the speaker
- Fixed gain level
- Limiter Level
- Audio Loudness vs Output Dynamic Range.

Figure 31 shows different settings for dynamic range and different fixed gain selected but no limiter level.



**Figure 31. Output Signal vs Input Signal State Diagram Showing Different Compression Ratio Configurations with Different Fixed Gain Configurations**

The rotation point is always at  $V_{in} = 10\text{dBV}$ . The rotation point is not located at the intersection of the limiter region and the compression region. By changing the fixed gain the rotation point will move in the y-axis direction only, as shown in the previous graph.

**Interaction between compression ratio and limiter range:** The compression ratio can be limited by the limiter range. Note that the limiter range is selected by the limiter level and the fixed gain.

For a setting with large limiter range, the amount of gain steps in the AGC remaining to perform compression are limited. Figure 32 shows two examples, where the fixed gain was changed.

1. Small limiter range yielding a large compression region (small fixed gain).
2. Large limiter range yielding a small compression region (large fixed gain).



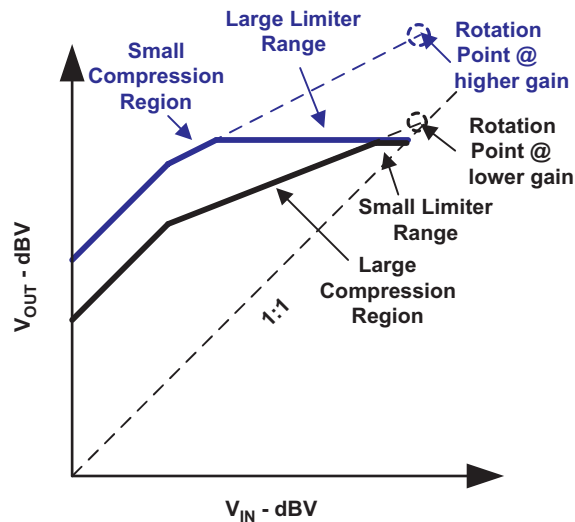


Figure 32. Output Signal vs Input Signal State Diagram Showing the Effects of the Limiter Range to the Compression Region

**Noise Gate Threshold:** The noise gate threshold prevents the AGC from changing the gain when there is no audio at the input of the amplifier. The noise gate threshold stops gain changes until the input signal is above the noise gate threshold. Select the noise gate threshold to be above the noise but below the minimum audio at the input of the amplifier signal. A filter is needed between delta-sigma CODEC/DAC and TPA2016D2 for effectiveness of the noise gate function. The filter eliminates the out-of-band noise from delta-sigma modulation and keeps the CODEC/DAC output noise lower than the noise gate threshold.

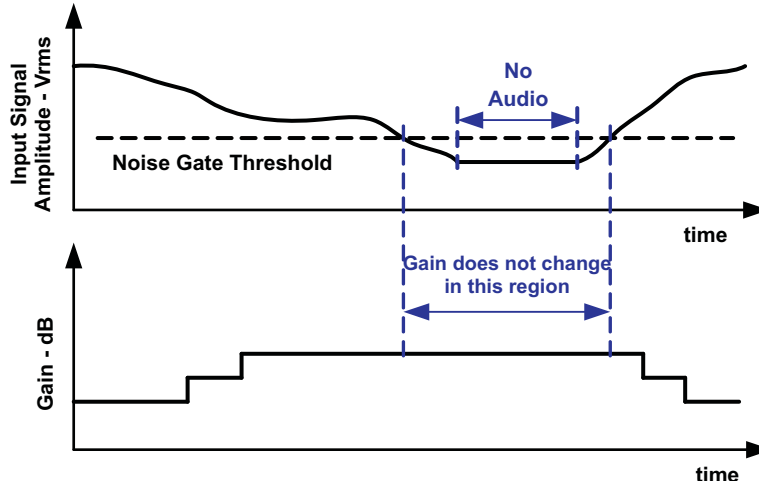
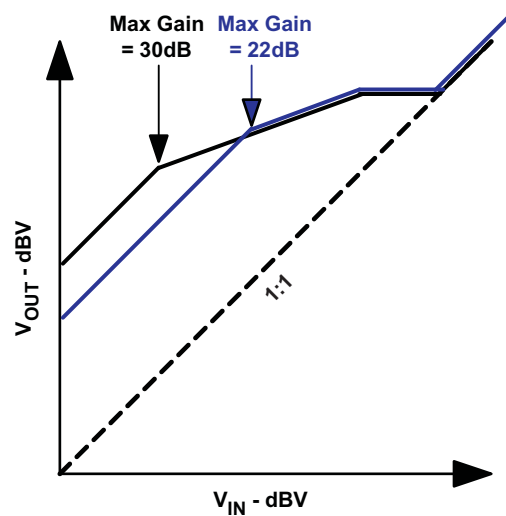


Figure 33. Time Diagram Showing the Relationship Between Input Signal Amplitude, Noise Gate Threshold and Gain Versus Time

**Maximum Gain:** This variable limits the number of gain steps in the AGC. This feature is useful in order to accomplish a more advanced output signal vs. input signal transfer characteristic.

For example, to prevent the gain from going above a certain value, reduce the maximum gain.

However, this variable will affect the limiter range and the compression region. If the maximum gain is decreased, the limiter range and/or compression region is reduced. Figure 34 illustrates the effects.



**Figure 34. Output Signal vs. Input Signal State Diagram Showing Different Maximum Gains**

A particular application requiring maximum gain of 22dB, for example. Thus, set the maximum gain at 22dB. The amplifier gain will never have a gain higher than 22dB; however, this will reduce the limiter range.

#### **Attack, Release, and Hold time:**

- The attack time is the minimum time between gain decreases.
- The release time is the minimum time between gain increases.
- The hold time is the minimum time between a gain decrease (attack) and a gain increase (release). The hold time can be deactivated. Hold time is only valid if greater than release time.

Successive gain decreases are never faster than the attack time. Successive gain increases are never faster than the release time.

All time variables (attack, release and hold) start counting after each gain change performed by the AGC. The AGC is allowed to decrease the gain (attack) only after the attack time finishes. The AGC is allowed to increase the gain (release) only after the release time finishes counting. However, if the preceding gain change was an attack (gain increase) and the hold time is enabled and longer than the release time, then the gain is only increased after the hold time.

The hold time is only enabled after a gain decrease (attack). The hold time replaces the release time after a gain decrease (attack). If the gain needs to be increased further, then the release time is used. The release time is used instead of the hold time if the hold time is disabled.

The attack time should be at least 100 times shorter than the release and hold time. The hold time should be the same or greater than the release time. It is important to select reasonable values for those variables in order to prevent the gain from changing too often or too slow.

Figure 35 illustrates the relationship between the three time variables.

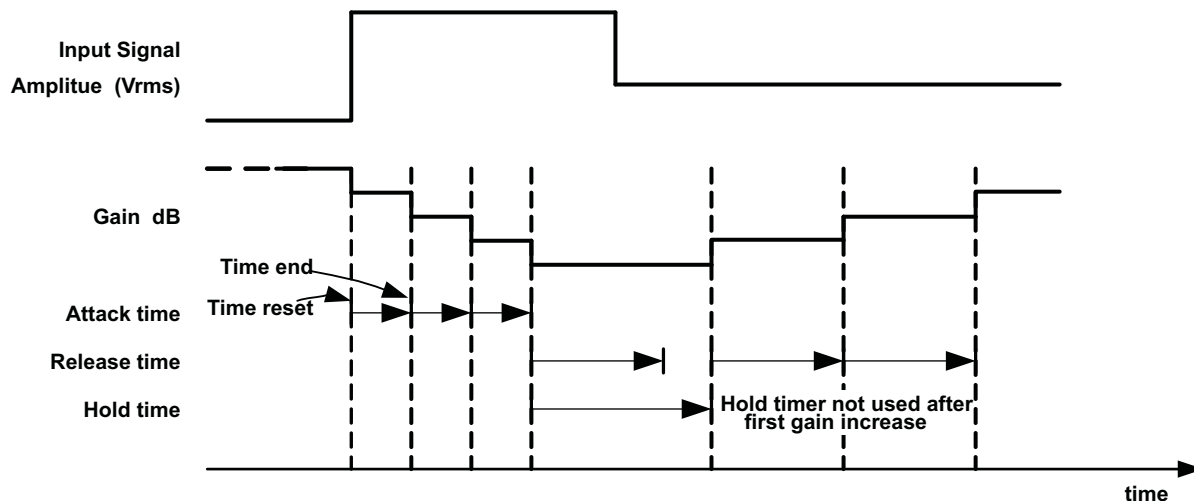


Figure 35. Time Diagram Showing the Relation Between the Attack, Release, and Hold Time vs Input Signal Amplitude and Gain

Figure 36 shows a state diagram of the input signal amplitude vs. the output signal amplitude and a summary of how the variables from table 1 described in the preceding pages affect them.

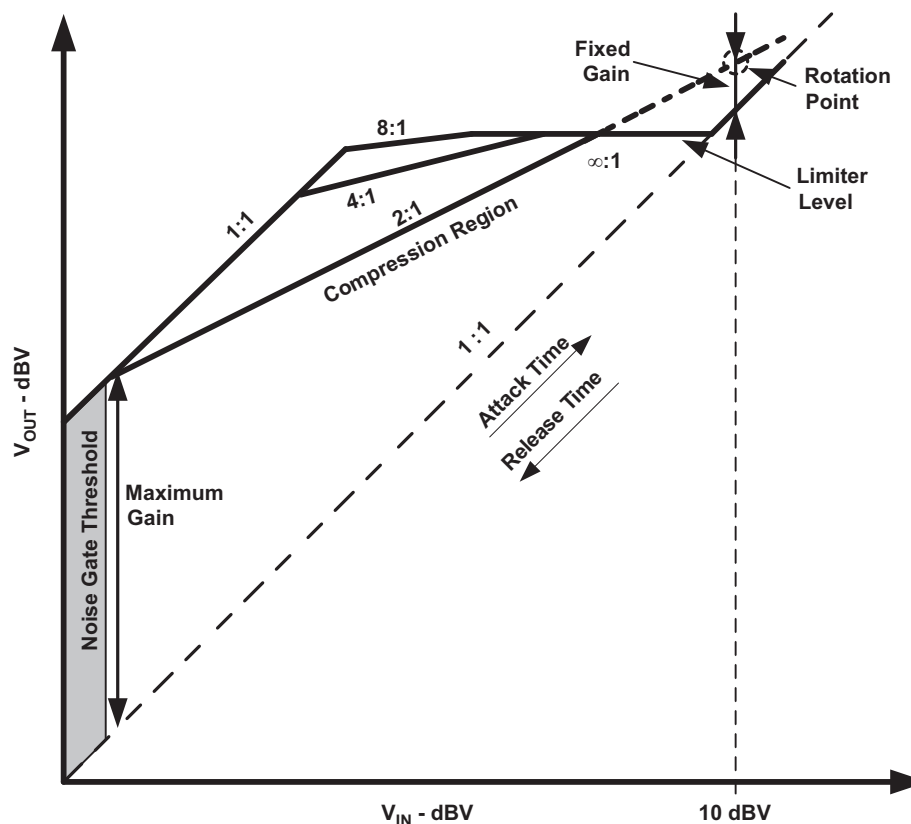


Figure 36. Output Signal vs. Input Signal State Diagram

## TPA2016D2 AGC OPERATION

The TPA2016D2 is controlled by the I<sup>2</sup>C interface. The correct start-up sequence is:

1. Apply the supply voltage to the AV<sub>DD</sub> and PV<sub>DD</sub> (L, R) pins.
2. Apply a voltage above V<sub>IH</sub> to the SDZ pin. The TPA2016D2 powers up the I<sup>2</sup>C interface and the control logic. By default, the device is in active mode (SWS = 0). After a few milliseconds the amplifier will enable the class-D output stage and become fully operational.
3. The amplifier starts at a gain of 0 dB and the AGC starts ramping the gain after the input signal exceeds the noise gate threshold.

### CAUTION

Do not interrupt the start-up sequence after changing SDZ from V<sub>IL</sub> to V<sub>IH</sub>.  
Do not interrupt the start-up sequence after changing SWS from 1 to 0.

The default conditions of TPA2016D2 allows audio playback without I2C control. Refer to [Table 4](#) for entire default conditions.

There are several options to disable the amplifier:

- Write SPK\_EN\_R = 0 and SPK\_EN\_L = 0 to the register (0x01, 6 and 0x01, 7). This write disables each speaker amplifier, but leaves all other circuits operating.
- Write SWS = 1 to the register (0x01, 5). This action disables most of the amplifier functions.
- Apply V<sub>IL</sub> to SDZ. This action shuts down all the circuits and has very low quiescent current consumption. This action resets the registers to its default values.

### CAUTION

Do not interrupt the shutdown sequence after changing SDZ from V<sub>IH</sub> to V<sub>IL</sub>.  
Do not interrupt the shutdown sequence after changing SWS from 0 to 1.

## TPA2016D2 AGC RECOMMENDED SETTINGS

**Table 2. Recommended AGC Settings for Different Types of Audio Source (V<sub>DD</sub> = 3.6V)**

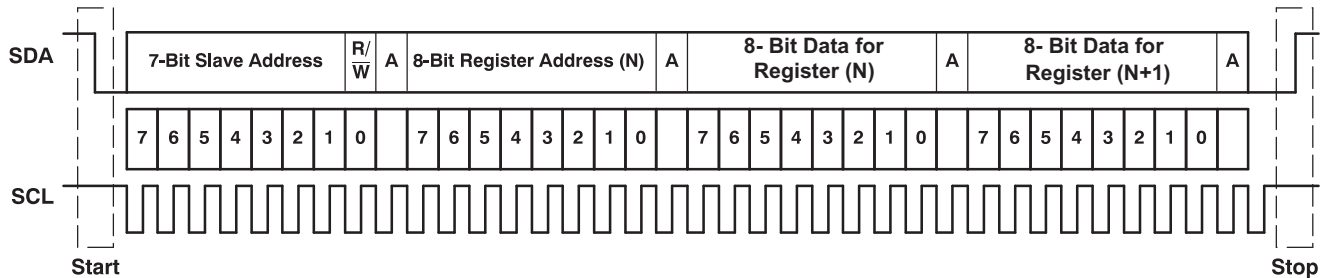
| AUDIO SOURCE | COMPRESSION RATIO | ATTACK TIME (ms/6 dB) | RELEASE TIME (ms/6 dB) | HOLD TIME (ms) | FIXED GAIN (dB) | LIMITER LEVEL (dBV) |
|--------------|-------------------|-----------------------|------------------------|----------------|-----------------|---------------------|
| Pop Music    | 4:1               | 1.28 to 3.84          | 986 to 1640            | 137            | 6               | 7.5                 |
| Classical    | 2:1               | 2.56                  | 1150                   | 137            | 6               | 8                   |
| Jazz         | 2:1               | 5.12 to 10.2          | 3288                   | —              | 6               | 8                   |
| Rap/ Hip Hop | 4:1               | 1.28 to 3.84          | 1640                   | —              | 6               | 7.5                 |
| Rock         | 2:1               | 3.84                  | 4110                   | —              | 6               | 8                   |
| Voice/ News  | 4:1               | 2.56                  | 1640                   | —              | 6               | 8.5                 |

## GENERAL I<sup>2</sup>C OPERATION

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially one bit at a time. The address and data 8-bit bytes are transferred most significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an *acknowledge* bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. [Figure 37](#) shows a typical sequence. The master generates the 7-bit slave

address and the read/write (R/W) bit to open communication with another device, and then waits for an acknowledge condition. The TPA2016D2 holds SDA low during the acknowledge clock period to indicate acknowledgment. When this acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

An external pull-up resistor must be used for the SDA and SCL signals to set the logic high level for the bus. When the bus level is 5 V, use pull-up resistors between 1 k $\Omega$  and 2 k $\Omega$ .



**Figure 37. Typical I²C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in [Figure 37](#).

## SINGLE-AND MULTIPLE-BYTE TRANSFERS

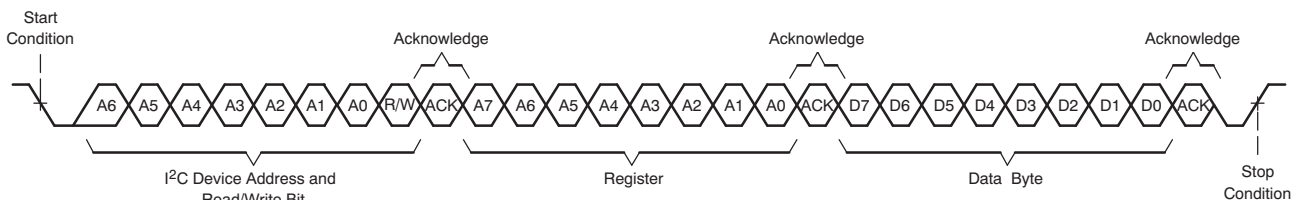
The serial control interface supports both single-byte and multi-byte read/write operations for all registers.

During multiple-byte read operations, the TPA2016D2 responds with data, one byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledgments.

The TPA2016D2 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has occurred. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines the number of registers written.

## SINGLE-BYTE WRITE

As [Figure 38](#) shows, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to '0'. After receiving the correct I²C device address and the read/write bit, the TPA2016D2 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TPA2016D2 internal memory address being accessed. After receiving the register byte, the TPA2016D2 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the register byte, the TPA2016D2 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.



**Figure 38. Single-Byte Write Transfer**

## MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TPA2016D2 as shown in Figure 39. After receiving each data byte, the TPA2016D2 responds with an acknowledge bit.

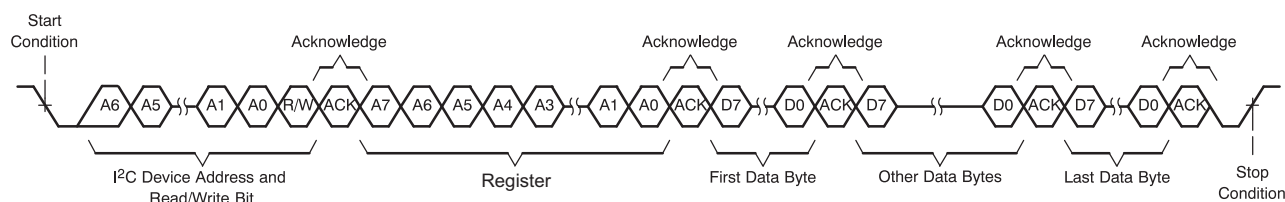


Figure 39. Multiple-Byte Write Transfer

## SINGLE-BYTE READ

As Figure 40 shows, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually executed. Initially, a write is executed to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a '0'.

After receiving the TPA2016D2 address and the read/write bit, the TPA2016D2 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TPA2016D2 issues an acknowledge bit. The master device transmits another start condition followed by the TPA2016D2 address and the read/write bit again. This time the read/write bit is set to '1', indicating a read transfer. Next, the TPA2016D2 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a *not-acknowledge* followed by a stop condition to complete the single-byte data read transfer.

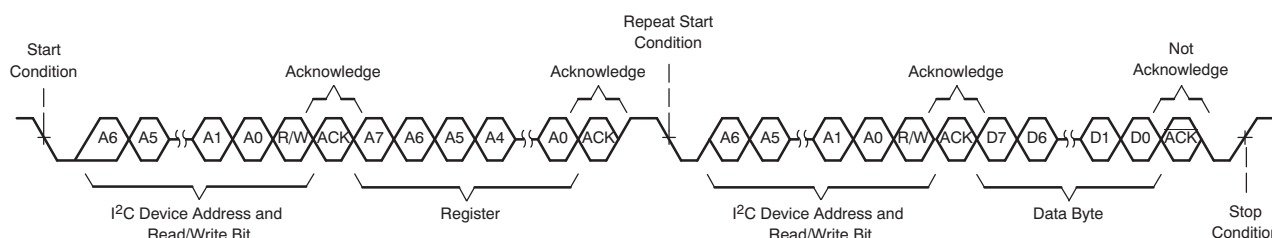


Figure 40. Single-Byte Read Transfer

## MULTIPLE-BYTE READ

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TPA2016D2 to the master device as shown in Figure 41. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

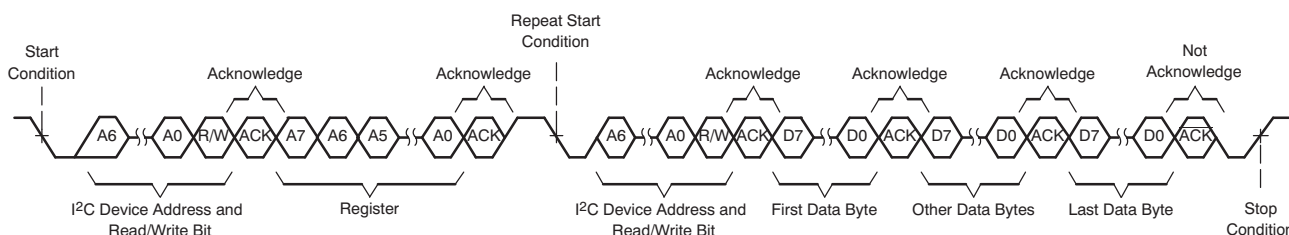


Figure 41. Multiple-Byte Read Transfer

## Register Map

**Table 3. TPA2016D2 Register Map**

| Register | Bit7                   | Bit6                    | Bit5                    | Bit4                     | Bit3                     | Bit2                     | Bit1                     | Bit0                     |
|----------|------------------------|-------------------------|-------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| 1        | SPK_EN_R               | SPL_EN_L                | SWS                     | FAULT_R                  | FAULT_L                  | Thermal                  | 1                        | NG_EN                    |
| 2        | 0                      | 0                       | ATK_time [5]            | ATK_time [4]             | ATK_time [3]             | ATK_time [2]             | ATK_time [1]             | ATK_time [0]             |
| 3        | 0                      | 0                       | REL_time [5]            | REL_time [4]             | REL_time [3]             | REL_time [2]             | REL_time [1]             | REL_time [0]             |
| 4        | 0                      | 0                       | Hold_time [5]           | Hold_time [4]            | Hold_tme [3]             | Hold_time [2]            | Hold_time [1]            | Hold_time [0]            |
| 5        | 0                      | 0                       | FixedGain [5]           | FixedGain [4]            | FixedGain [3]            | FixedGain [2]            | FixedGain [1]            | FixedGain [0]            |
| 6        | Output Limiter Disable | NoiseGate Threshold [1] | NoiseGate Threshold [2] | Output Limiter Level [4] | Output Limiter Level [3] | Output Limiter Level [2] | Output Limiter Level [1] | Output Limiter Level [0] |
| 7        | Max Gain [3]           | Max Gain [2]            | Max Gain [1]            | Max Gain [0]             | 0                        | 0                        | Compression Ratio [1]    | Compression Ratio [0]    |

The default register map values are given in [Table 4](#).

**Table 4. TPA2016D2 Default Register Values Table**

| Register | 0x01 | 0x02 | 0x03 | 0x04 | 0x05 | 0x06 | 0x07 |
|----------|------|------|------|------|------|------|------|
| Default  | C3h  | 05h  | 0Bh  | 00h  | 06h  | 3Ah  | C2h  |

Any register above address 0x08 is reserved for testing and should not be written to because it may change the function of the device. If read, these bits may assume any value.

Some of the default values can be reprogrammed through the I<sup>2</sup>C interface and written to the EEPROM. This function is useful to speed up the turn-on time of the device and minimizes the number of I<sup>2</sup>C writes. If this is required, contact your local TI representative.

The TPA2016D2 I<sup>2</sup>C address is 0xB0 (binary 10110000) for writing and 0xB1 (binary 10110001) for reading. If a different I<sup>2</sup>C address is required, please contact your local TI representative. See the General I2C operation section for more detail.

The following tables show the details of the registers, the default values, and the values that can be programmed through the I<sup>2</sup>C interface.

**IC FUNCTION CONTROL (Address: 1)**

| REGISTER ADDRESS                            | I <sup>2</sup> C BIT | LABEL    | DEFAULT     | DESCRIPTION  |
|---|----------------------|----------|-------------|--|
| 01 (01 <sub>H</sub> ) – IC Function Control | 7                    | SPK_EN_R | 1 (enabled) | Enables right amplifier  |
|   | 6                    | SPK_EN_L | 1 (enabled) | Enables left amplifier   |
|   | 5                    | SWS      | 0 (enabled) | Shutdown IC when bit = 1   |
|   | 4                    | FAULT_R  | 0           | Changes to a 1 when there is a short on the right channel. Reset by writing a 0. |
|   | 3                    | FAULT_L  | 0           | Changes to a 1 when there is a short on the left channel. Reset by writing a 0   |
|   | 2                    | Thermal  | 0           | Changes to a 1 when die temperature is above 150°C                               |
|   | 1                    | UNUSED   | 1           |  |
|   | 0                    | NG_EN    | 1 (enabled) | Enables Noise Gate function  |

**SPK\_EN\_R:** Enable bit for the right-channel amplifier. Amplifier is active when bit is high. This function is gated by thermal and returns once the IC is below the threshold temperature.

**SPK\_EN\_L:** Enable bit for the left-channel amplifier. Amplifier is active when bit is high. This function is gated by thermal and returns once the IC is below the threshold temperature

**SWS:** Software shutdown control. The device is in software shutdown when the bit is '1' (control, bias and oscillator are inactive). When the bit is '0' the control, bias and oscillator are enabled.

**Fault\_L:** This bit indicates that an over-current event has occurred on the left channel with a '1'. This bit is cleared by writing a '0' to it.

**Fault\_R:** This bit indicates that an over-current event has occurred on the right channel with a '1'. This bit is cleared by writing a '0' to it.

**Thermal:** This bit indicates a thermal shutdown that was initiated by the hardware with a '1'. This bit is deglitched and latched, and can be cleared by writing a '0' to it.

**NG\_EN:** Enable bit for the Noise Gate function. This function is enabled when this bit is high. This function can only be enabled when the Compression ratio is not 1:1.

**AGC ATTACK CONTROL (Address: 2)**

| REGISTER ADDRESS                    | I <sup>2</sup> C BIT | LABEL    | DEFAULT                 | DESCRIPTION                                   |           |          |           |
|-------------------------------------|----------------------|----------|-------------------------|---|-----------|----------|-----------|
| 02 (02 <sub>H</sub> ) – AGC Control | 7:6                  | Unused   | 00                      |   |           |          |           |
|                                     | 5:0                  | ATK_time | 000101<br>(6.4 ms/6 dB) | AGC Attack time (gain ramp down)              |           |          |           |
|                                     |                      |          |                         |   | Per Step  | Per 6 dB | 90% Range |
|                                     |                      |          |                         | 000001  | 0.1067 ms | 1.28 ms  | 5.76 ms   |
|                                     |                      |          |                         | 000010  | 0.2134 ms | 2.56 ms  | 11.52 ms  |
|                                     |                      |          |                         | 000011  | 0.3201 ms | 3.84 ms  | 17.19 ms  |
|                                     |                      |          |                         | 000100  | 0.4268 ms | 5.12 ms  | 23.04 ms  |
|                                     |                      |          |                         | (time increases by 0.1067 ms with every step) |           |          |           |
|                                     |                      |          |                         | 111111  | 6.722 ms  | 80.66 ms | 362.99 ms |

**ATK\_time** These bits set the attack time for the AGC function. The attack time is the minimum time between gain decreases.



**AGC RELEASE CONTROL (Address: 3)**

| REGISTER ADDRESS                            | I <sup>2</sup> C BIT | LABEL    | DEFAULT                   | DESCRIPTION                                  |          |          |           |
|---|----------------------|----------|---------------------------|--|----------|----------|-----------|
| 03 (03 <sub>H</sub> ) – AGC Release Control | 7:6                  | Unused   | 00                        |  |          |          |           |
|   | 5:0                  | REL_time | 001011<br>(1.81 sec/6 dB) | AGC Release time (gain ramp down)            |          |          |           |
|   |                      |          |                           |  | Per Step | Per 6 dB | 90% Range |
|   |                      |          |                           | 000001                                       | 0.0137 s | 0.1644 s | 0.7398 s  |
|   |                      |          |                           | 000010                                       | 0.0274 s | 0.3288 s | 1.4796 s  |
|   |                      |          |                           | 000011                                       | 0.0411 s | 0.4932 s | 2.2194 s  |
|   |                      |          |                           | 000100                                       | 0.0548 s | 0.6576 s | 2.9592 s  |
|   |                      |          |                           | (time increases by 0.0137 s with every step) |          |          |           |
|   |                      |          |                           | 111111                                       | 0.8631 s | 10.36 s  | 46.6 s    |

**REL\_time** These bits set the release time for the AGC function. The release time is the minimum time between gain increases.

**Table 5. AGC HOLD TIME CONTROL (Address: 4)**

| REGISTER ADDRESS                              | I <sup>2</sup> C BIT | LABEL     | DEFAULT           | DESCRIPTION                                  |                   |          |
|---|----------------------|-----------|-------------------|--|-------------------|----------|
| 04 (04 <sub>H</sub> ) – AGC Hold Time Control | 7:6                  | Unused    | 00                |  |                   |          |
|   | 5:0                  | Hold_time | 000000 (Disabled) | AGC Hold time                                |                   |          |
|   |                      |           |                   |  |                   | Per Step |
|   |                      |           |                   | 000000                                       | Hold Time Disable |          |
|   |                      |           |                   | 000001                                       | 0.0137 s          |          |
|   |                      |           |                   | 000010                                       | 0.0274 s          |          |
|   |                      |           |                   | 000011                                       | 0.0411 s          |          |
|   |                      |           |                   | 000100                                       | 0.0548 s          |          |
|   |                      |           |                   | (time increases by 0.0137 s with every step) |                   |          |
| 111111  | 0.8631 s             |           |                   |  |                   |          |

**Hold\_time** These bits set the hold time for the AGC function. The hold time is the minimum time between a gain decrease (attack) and a gain increase (release). The hold time can be deactivated.

**AGC FIXED GAIN CONTROL (Address: 5)**

| REGISTER ADDRESS                               | I <sup>2</sup> C BIT | LABEL      | DEFAULT     | DESCRIPTION  |        |  |
|--|----------------------|------------|-------------|--|--------|--|
| 05 (05 <sub>H</sub> ) – AGC Fixed Gain Control | 7:6                  | Unused     | 00          |  |        |  |
|  | 5:0                  | Fixed Gain | 00110 (6dB) | Sets the fixed gain of the amplifier: two's compliment |        |  |
|  |                      |            |             |  | Gain   |  |
|  |                      |            |             | 100100   | –28 dB |  |
|  |                      |            |             | 100101   | –27 dB |  |
|  |                      |            |             | 100110   | –26 dB |  |
|  |                      |            |             | (gain increases by 1 dB with every step)               |        |  |
|  |                      |            |             | 111101   | –3 dB  |  |
|  |                      |            |             | 111110   | –2 dB  |  |
|  |                      |            |             | 111111   | –1 dB  |  |
|  |                      |            |             | 000000   | 0 dB   |  |
|  |                      |            |             | 000001   | 1 dB   |  |
|  |                      |            |             | 000010   | 2 dB   |  |
|  |                      |            |             | 000011   | 3 dB   |  |
|  |                      |            |             | (gain increases by 1dB with every step)                |        |  |
|  |                      |            |             | 011100   | 28 dB  |  |
|  |                      |            |             | 011101   | 29 dB  |  |
|  |                      |            |             | 011110   | 30 dB  |  |

**Fixed Gain** These bits are used to select the fixed gain of the amplifier. If the Compression is enabled, fixed gain is adjustable from –28dB to 30dB. If the Compression is disabled, fixed gain is adjustable from 0dB to 30dB.

**AGC CONTROL (Address: 6)**

| REGISTER ADDRESS                    | I <sup>2</sup> C BIT | LABEL                  | DEFAULT                  | DESCRIPTION  |
|-------------------------------------|----------------------|------------------------|--------------------------|--|
| 06 (06 <sub>H</sub> ) – AGC Control | 7                    | Output Limiter Disable | 0 (enable)               | Disables the output limiter function. Can only be disabled when the AGC compression ratio is 1:1 (off) |
|                                     | 6:5                  | NoiseGate Threshold    | 01 (4mV <sub>rms</sub> ) | Select the threshold of the noise gate   |
|                                     |                      |                        |                          | Threshold  |
|                                     |                      |                        |                          | 00 1 mV <sub>rms</sub>   |
|                                     |                      |                        |                          | 01 4 mV <sub>rms</sub>   |
|                                     |                      |                        |                          | 10 10 mV <sub>rms</sub>  |
|                                     |                      |                        |                          | 11 20 mV <sub>rms</sub>  |
|                                     | 4:0                  | Output Limiter Level   | 11010 (6.5dBV)           | Selects the output limiter level   |
|                                     |                      |                        |                          | Output Power (Wrms) Peak Output Voltage (Vp) dBV   |
|                                     |                      |                        |                          | 00000 0.03 0.67 –6.5   |
|                                     |                      |                        |                          | 00001 0.03 0.71 –6   |
|                                     |                      |                        |                          | 00010 0.04 0.75 –5.5   |
|                                     |                      |                        |                          | (Limiter level increases by 0.5dB with every step)   |
|                                     |                      |                        |                          | 11101 0.79 3.55 8  |
|                                     |                      |                        |                          | 11110 0.88 3.76 8.5  |
|                                     |                      |                        |                          | 11111 0.99 3.99 9  |

**Output Limiter Disable** This bit disables the output limiter function when set to 1. Can only be disabled when the AGC compression ratio is 1:1

**NoiseGate Threshold** These bits set the threshold level of the noise gate. NoiseGate Threshold is only functional when the compression ratio is not 1:1

**Output Limiter Level** These bits select the output limiter level. Output Power numbers are for 8Ω load.

**AGC CONTROL (Address: 7)**

| REGISTER ADDRESS                    | I <sup>2</sup> C BIT | LABEL             | DEFAULT      | DESCRIPTION                                  |
|-------------------------------------|----------------------|-------------------|--------------|--|
| 07 (07 <sub>H</sub> ) – AGC Control | 7:4                  | Max Gain          | 1100 (30 dB) | Selects the maximum gain the AGC can achieve |
|                                     |                      |                   |              | Gain   |
|                                     |                      |                   |              | 0000 18 dB                                   |
|                                     |                      |                   |              | 0001 19 dB                                   |
|                                     |                      |                   |              | 0010 20 dB                                   |
|                                     |                      |                   |              | (gain increases by 1 dB with every step)     |
|                                     |                      |                   |              | 1100 30 dB                                   |
|                                     | 3:2                  | Unused            | 00           |  |
|                                     | 1:0                  | Compression Ratio | 10 (4:1)     | Selects the compression ratio of the AGC     |
|                                     |                      |                   |              | Ratio  |
|                                     |                      |                   |              | 00 1:1 (off)                                 |
|                                     |                      |                   |              | 01 2:1                                       |
|                                     |                      |                   |              | 10 4:1                                       |
|                                     |                      |                   |              | 11 8:1                                       |

**Compression Ratio** These bits select the compression ratio. Output Limiter is enabled by default when the compression ratio is not 1:1.

**Max Gain** These bits select the maximum gain of the amplifier. In order to maximize the use of the AGC, set the Max Gain to 30dB

## DECOUPLING CAPACITOR $\diamond_s$ )

The TPA2016D2 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) 1- $\mu$ F ceramic capacitor (typically) placed as close as possible to the device PVDD (L, R) lead works best. Placing this decoupling capacitor close to the TPA2016D2 is important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 4.7  $\mu$ F or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

## INPUT CAPACITORS $\diamond_i$ )

The input capacitors and input resistors form a high-pass filter with the corner frequency,  $f_c$ , determined in Equation 5.

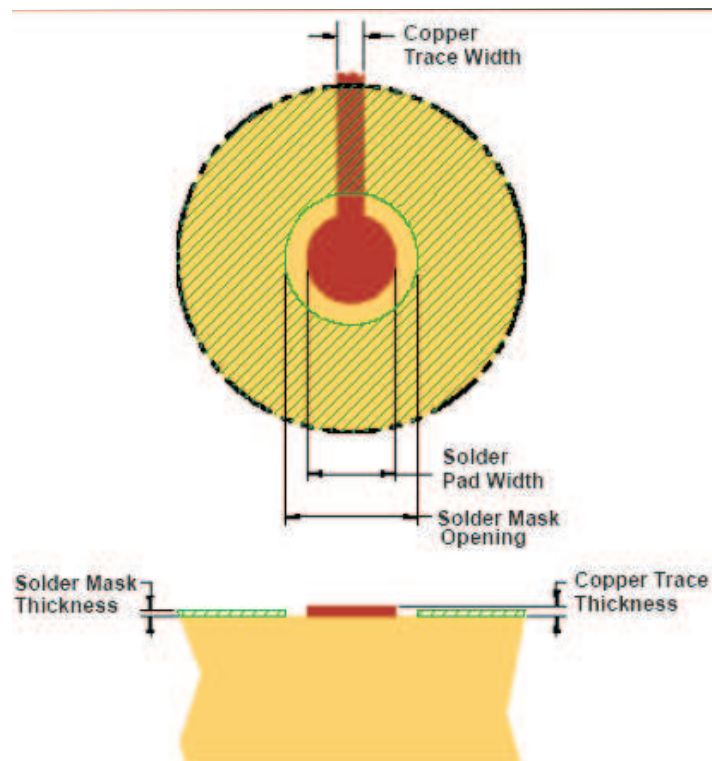
$$f_c = \frac{1}{(2\pi \times R_i \times C_i)} \quad (5)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Not using input capacitors can increase output offset. Equation 6 is used to solve for the input coupling capacitance. If the corner frequency is within the audio band, the capacitors should have a tolerance of  $\pm 10\%$  or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

$$C_i = \frac{1}{(2\pi \times R_i \times f_c)} \quad (6)$$

## BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use non solder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 42 and Table 6 shows the appropriate diameters for a WCSP layout. The TPA2016D2 evaluation module (EVM) layout is shown in the next section as a layout example.



**Figure 42. Land Pattern Dimensions**

**Table 6. Land Pattern Dimensions<sup>(1) (2) (3) (4)</sup>**

| SOLDER PAD DEFINITIONS         | COPPER PAD                                      | SOLDER MASK <sup>(5)</sup> OPENING              | COPPER THICKNESS             | STENCIL <sup>(6) (7)</sup> OPENING                                 | STENCIL THICKNESS       |
|--------------------------------|---|---|------------------------------|--|-------------------------|
| Non solder mask defined (NSMD) | 275 $\mu\text{m}$<br>(+0.0, -25 $\mu\text{m}$ ) | 375 $\mu\text{m}$<br>(+0.0, -25 $\mu\text{m}$ ) | 1 oz max (32 $\mu\text{m}$ ) | 275 $\mu\text{m}$ $\times$ 275 $\mu\text{m}$ Sq. (rounded corners) | 125 $\mu\text{m}$ thick |

- (1) Circuit traces from NSMD defined PWB lands should be 75  $\mu\text{m}$  to 100  $\mu\text{m}$  wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
- (2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
- (3) Recommend solder paste is Type 3 or Type 4.
- (4) For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5  $\mu\text{m}$  to avoid a reduction in thermal fatigue performance.
- (5) Solder mask thickness should be less than 20  $\mu\text{m}$  on top of the copper circuit pattern
- (6) Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
- (7) Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

## COMPONENT LOCATION

Place all the external components very close to the TPA2016D2. Placing the decoupling capacitor,  $C_S$ , close to the TPA2016D2 is important for the efficiency of the Class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

## TRACE WIDTH

Recommended trace width at the solder balls is 75  $\mu\text{m}$  to 100  $\mu\text{m}$  to prevent solder wicking onto wider PCB traces. For high current pins (PVDD (L, R), PGND, and audio output pins) of the TPA2016D2, use 100- $\mu\text{m}$  trace widths at the solder balls and at least 500- $\mu\text{m}$  PCB traces to ensure proper performance and output power for the device. For the remaining signals of the TPA2016D2, use 75- $\mu\text{m}$  to 100- $\mu\text{m}$  trace widths at the solder balls. The audio input pins (INR $\pm$  and INL $\pm$ ) must run side-by-side to maximize common-mode noise cancellation

## EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the packages are shown in the dissipation rating table. Converting this to  $\theta_{JA}$  for the WCSP package:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.01} = 100^{\circ}\text{C/W} \quad (7)$$

Given  $\theta_{JA}$  of  $100^{\circ}\text{C/W}$ , the maximum allowable junction temperature of  $150^{\circ}\text{C}$ , and the maximum internal dissipation of 0.4 W (0.2 W per channel) for 1.5 W per channel, 8- $\Omega$  load, 5-V supply, from [Figure 16](#), the maximum ambient temperature can be calculated with the following equation.

$$T_{A\text{Max}} = T_{J\text{Max}} - \theta_{JA} P_{D\text{MAX}} = 150 - 100 (0.4) = 110^{\circ}\text{C} \quad (8)$$

[Equation 8](#) shows that the calculated maximum ambient temperature is  $110^{\circ}\text{C}$  at maximum power dissipation with a 5-V supply and 8- $\Omega$  a load. The TPA2016D2 is designed with thermal protection that turns the device off when the junction temperature surpasses  $150^{\circ}\text{C}$  to prevent damage to the IC. Also, using speakers more resistive than 8- $\Omega$  dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

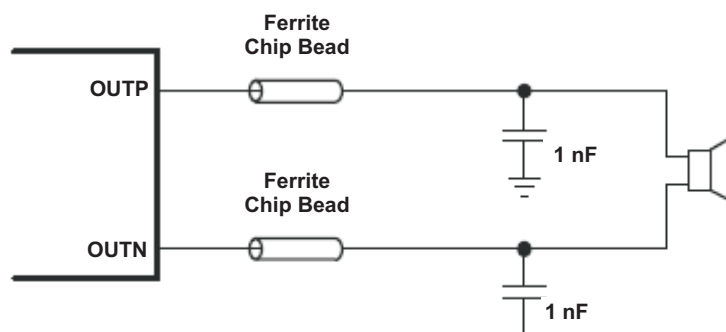
## OPERATION WITH DACS AND CODECS

In using Class-D amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when mixing of the output frequencies of the CODEC/DAC mix with the switching frequencies of the audio amplifier input stage. The noise increase can be solved by placing a low-pass filter between the CODEC/DAC and audio amplifier. This filters off the high frequencies that cause the problem and allow proper performance. See the functional block diagram.

## FILTER FREE OPERATION AND FERRITE BEAD FILTERS

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter and the frequency sensitive circuit is greater than 1 MHz. This filter functions well for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. When choosing a ferrite bead, choose one with high impedance at high frequencies, and low impedance at low frequencies. In addition, select a ferrite bead with adequate current rating to prevent distortion of the output signal.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker. [Figure 43](#) shows typical ferrite bead and LC output filters.



**Figure 43. Typical Ferrite Bead Filter (Chip bead example: TDK: MPZ1608S221A)**

## REVISION HISTORY

### Changes from Original (June 2008) to Revision A Page

- Changed From: 1.4 W/Ch Into 8  $\Omega$  at 5 V (10% THD+N) To: 1.7 W/Ch Into 8  $\Omega$  at 5 V (10% THD+N) ..... 1

### Changes from Revision A (June 2008) to Revision B Page

- Changed Feature High PSRR From: 75 dB at 217 Hz To: 80 dB ..... 1
- Added 00 to Default column ..... 24
- Added 00 to Default column ..... 25
- Added 00 to Default column ..... 25

### Changes from Revision B (June 2008) to Revision C Page

- Changed  $R_{LOAD}$  from 6.4  $\Omega$  to 3.2  $\Omega$  ..... 3

### Changes from Revision C (October 2008) to Revision D Page

- Added the RTJ (QFN) package. .... 1
- Added Feature: 2.8 W/Ch Into 4  $\Omega$  at 5 V (10% THD+N) ..... 1
- Added Feature: 1.5 W/Ch Into 4  $\Omega$  at 3.6 V (10% THD+N) ..... 1
- Added the RTJ (QFN) pin out package. .... 2
- Added the RTJ (QFN) package to the Dissipation Ratings Table. .... 3
- Changed the RTJ Package Options to the Available Options Table. .... 4
- Changed  $I_{SWS}$  Softwre shutdown 3.6V From: Max 60 To: 70  $\mu$ A ..... 4
- Changed  $I_{SWS}$  Softwre shutdown 5.5V From: Max 100 to 110  $\mu$ A ..... 4
- Changed Output offset TYP From 0 mV To: 2 mV ..... 4
- Added text notes 4 and 5 to the Test Set-Up for Graphs. .... 5
- Deleted Table of Graphs from the Typical Characteristics. .... 7
- Added 4 $\Omega$  Efficiency Graph ..... 10
- Added 4 $\Omega$  Total Power Dissipation Graph ..... 10
- Added 4 $\Omega$  Total Supply Current Graph ..... 11
- Added QFN Output Power Graph ..... 11

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPA2016D2RTJR    | ACTIVE        | QFN          | RTJ                | 20   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPA<br>2016D2           | <a href="#">Samples</a> |
| TPA2016D2RTJT    | ACTIVE        | QFN          | RTJ                | 20   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPA<br>2016D2           | <a href="#">Samples</a> |
| TPA2016D2YZHR    | ACTIVE        | DSBGA        | YZH                | 16   | 3000           | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | CCJ                     | <a href="#">Samples</a> |
| TPA2016D2YZHT    | ACTIVE        | DSBGA        | YZH                | 16   | 250            | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | CCJ                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPA2016D2RTJR | QFN          | RTJ             | 20   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPA2016D2RTJT | QFN          | RTJ             | 20   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPA2016D2RTJT | QFN          | RTJ             | 20   | 250  | 180.0              | 12.4               | 4.3     | 4.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPA2016D2YZHR | DSBGA        | YZH             | 16   | 3000 | 180.0              | 8.4                | 2.18    | 2.18    | 0.81    | 4.0     | 8.0    | Q1            |
| TPA2016D2YZHT | DSBGA        | YZH             | 16   | 250  | 180.0              | 8.4                | 2.18    | 2.18    | 0.81    | 4.0     | 8.0    | Q1            |

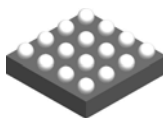
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPA2016D2RTJR | QFN          | RTJ             | 20   | 3000 | 356.0       | 356.0      | 35.0        |
| TPA2016D2RTJT | QFN          | RTJ             | 20   | 250  | 210.0       | 185.0      | 35.0        |
| TPA2016D2RTJT | QFN          | RTJ             | 20   | 250  | 195.0       | 200.0      | 45.0        |
| TPA2016D2YZHR | DSBGA        | YZH             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| TPA2016D2YZHT | DSBGA        | YZH             | 16   | 250  | 182.0       | 182.0      | 20.0        |

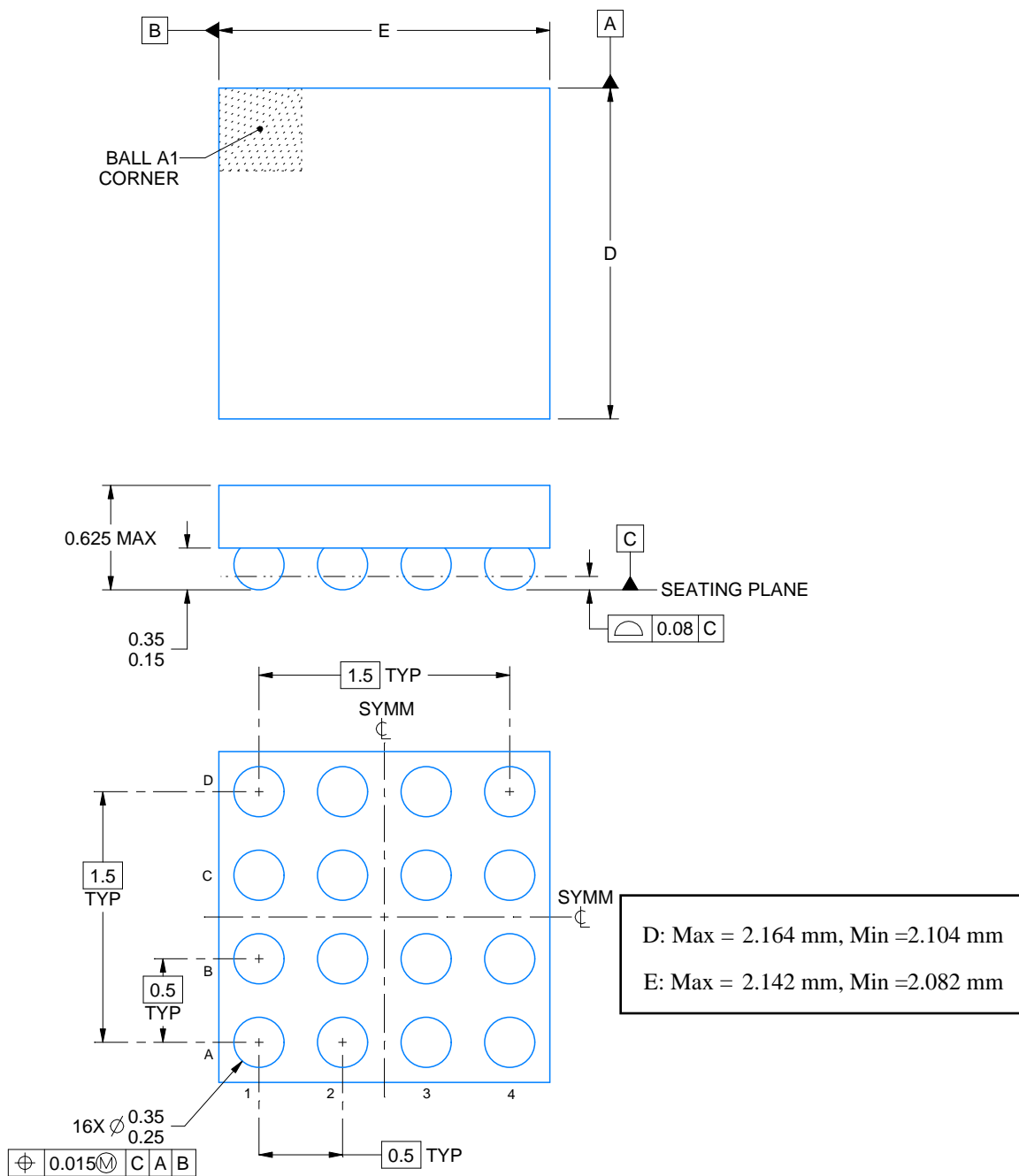
YZH0016



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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## NOTES:

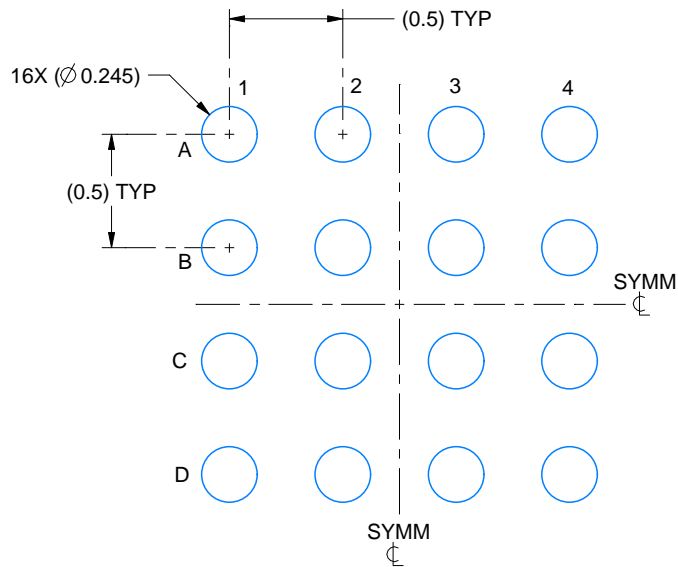
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

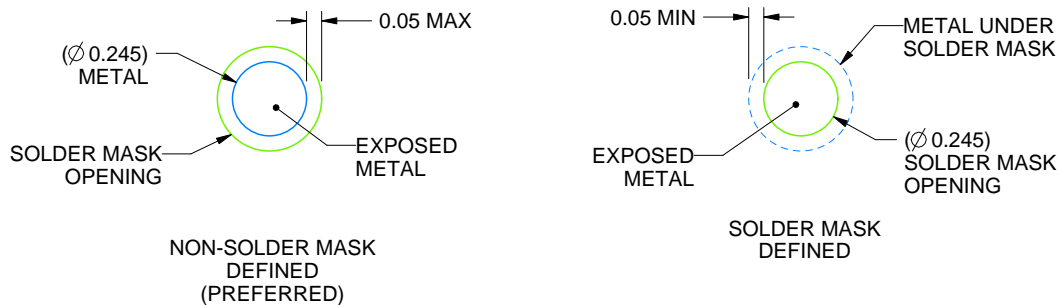
YZH0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 30X



SOLDER MASK DETAILS  
NOT TO SCALE

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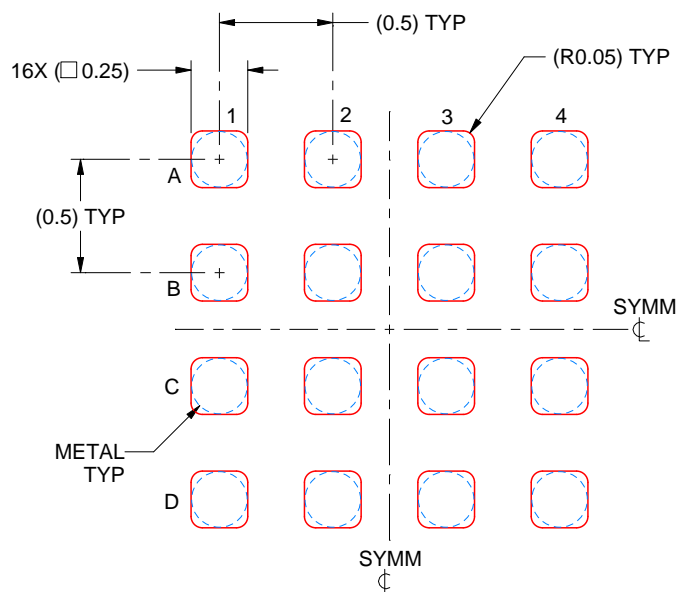
NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

**YZH0016**

## DSBGA - 0.625 mm max height

## DIE SIZE BALL GRID ARRAY



**SOLDER PASTE EXAMPLE**  
**BASED ON 0.075 mm THICK STENCIL**  
**SCALE: 30X**

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## GENERIC PACKAGE VIEW

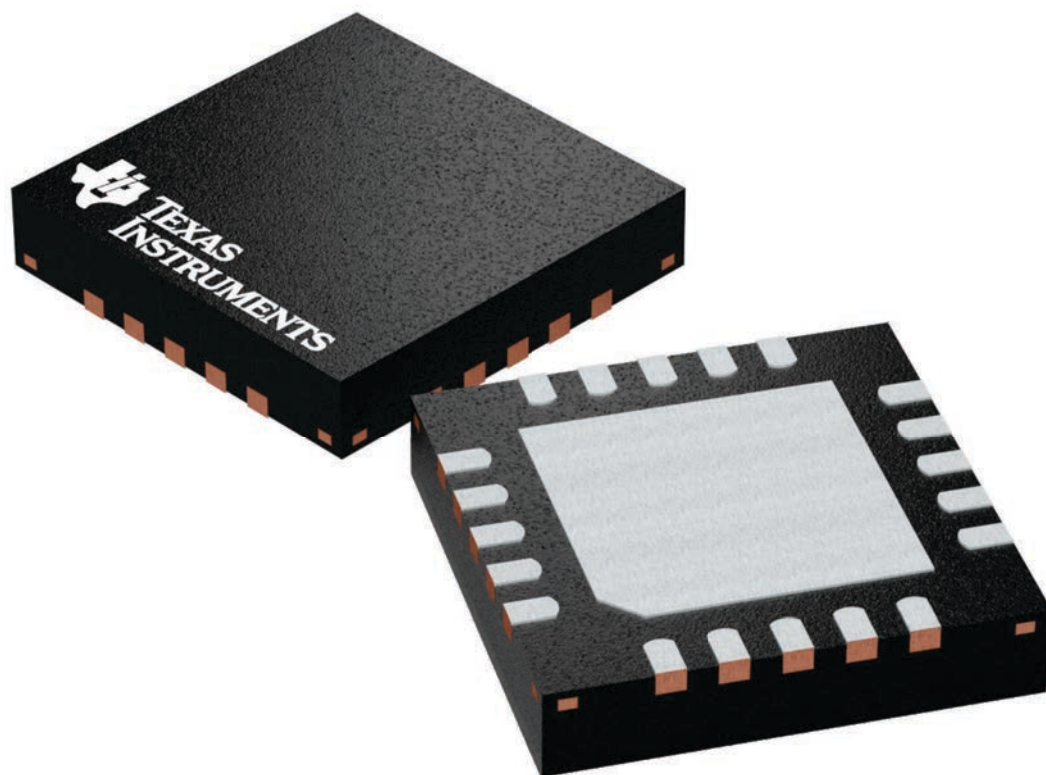
**RTJ 20**

**WQFN - 0.8 mm max height**

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD


This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



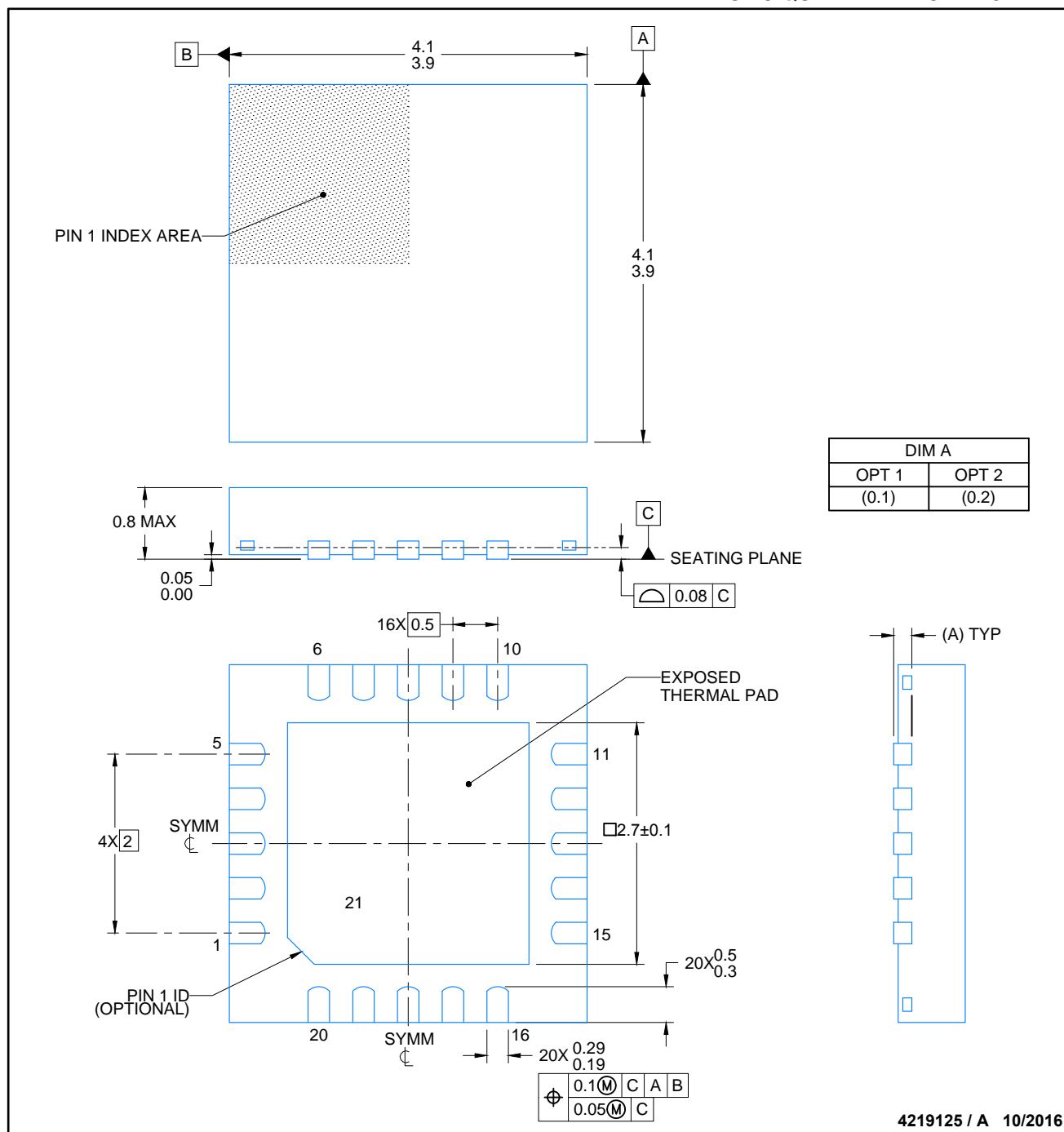
4224842/A

DATA BOOK  
PACKAGE OUTLINE

|                   |
|-------------------|
| LEADFRAME EXAMPLE |
| 4222370           |

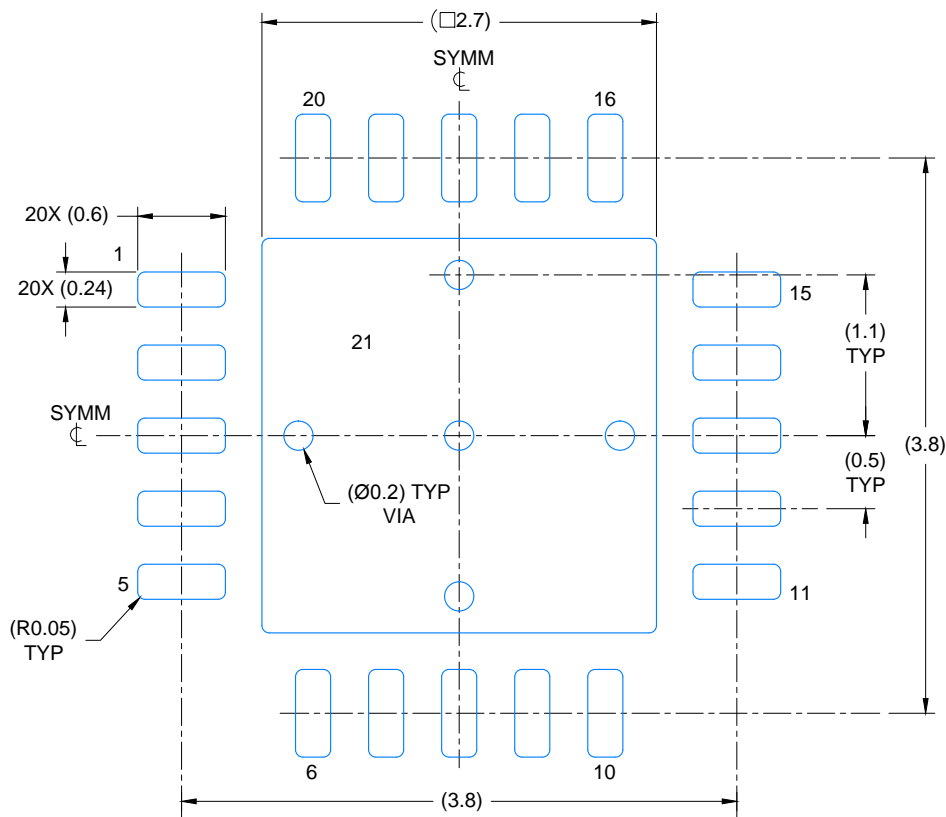
|                                  |  |                     |   |           |                           |          |                |
|----------------------------------|--|---------------------|---|-----------|---------------------------|----------|----------------|
| DRAFTSMAN:<br>H. DENG            |  | DATE:<br>09/12/2016 |   |           | DIMENSIONS IN MILLIMETERS |          |                |
| DESIGNER:<br>H. DENG             |  | DATE:<br>09/12/2016 | <div> <b>TEXAS INSTRUMENTS</b><br/>SEMICONDUCTOR OPERATIONS</div> <div>CODE IDENTITY<br/>NUMBER<br/>01295</div> <div>ePOD, RTJ0020D / WQFN,<br/>20 PIN, 0.5 MM PITCH</div> |           |                           |          |                |
| CHECKER:<br>V. PAKU & T. LEQUANG |  | DATE:<br>09/12/2016 |   |           |                           |          |                |
| ENGINEER:<br>T. TANG             |  | DATE:<br>09/12/2016 |   |           |                           |          |                |
| APPROVED:<br>E. REY & D. CHIN    |  | DATE:<br>10/06/2016 |   |           |                           |          |                |
| RELEASED:<br>WDM                 |  | DATE:<br>10/24/2016 |   |           |                           |          |                |
| TEMPLATE INFO:<br>EDGE# 4218519  |  | DATE:<br>04/07/2016 | SCALE<br>15X  | SIZE<br>A | 4219125                   | REV<br>A | PAGE<br>1 OF 5 |



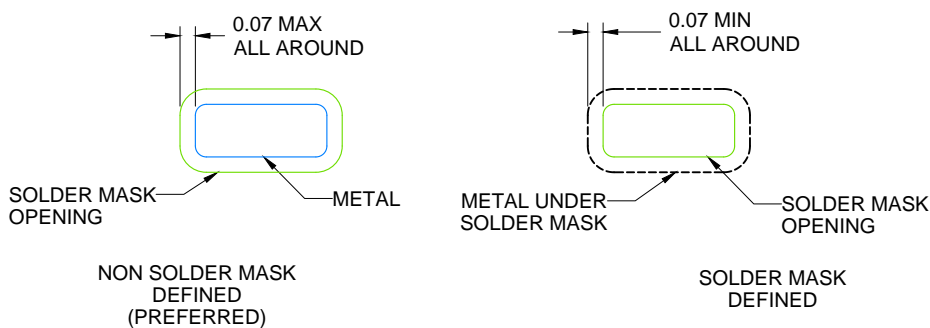


## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE  
SCALE: 20X

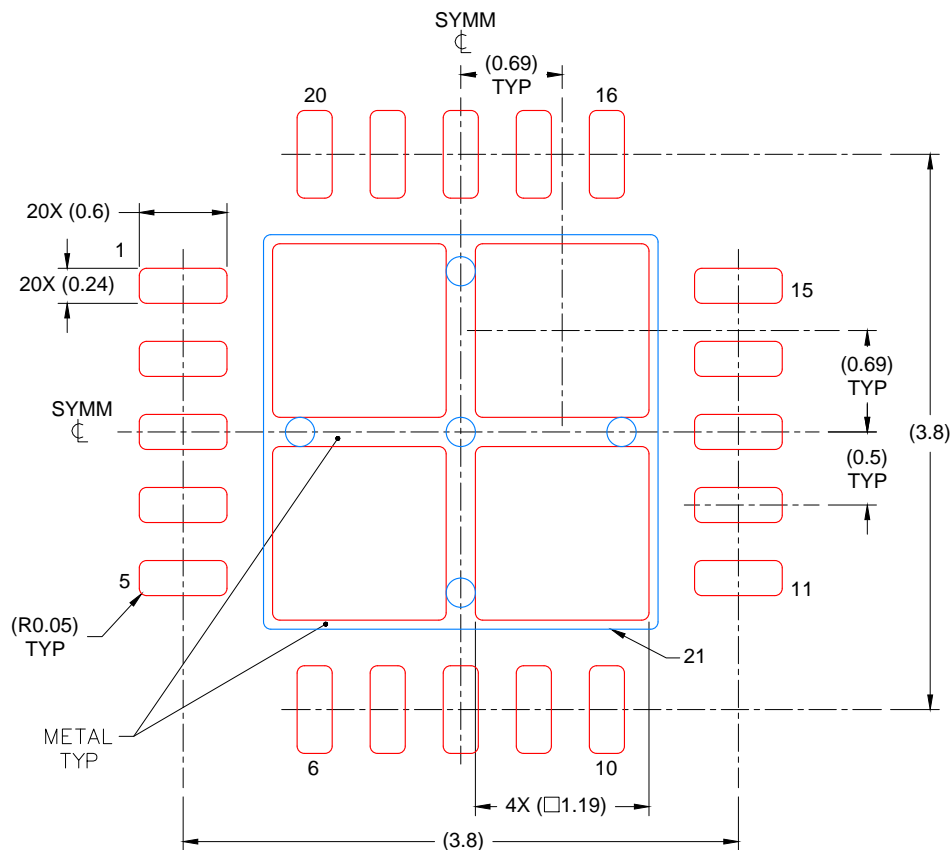


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 78% PRINTED COVERAGE BY AREA  
 SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

# REVISIONS

| REV | DESCRIPTION         | ECR     | DATE       | ENGINEER / DRAFTSMAN |
|-----|---------------------|---------|------------|----------------------|
| A   | RELEASE NEW DRAWING | 2160736 | 10/24/2016 | T. TANG / H. DENG    |

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