

TMUXHS221LV USB 2.0 480Mbps 2:1 或 1:2 多路复用器或多路信号分离器开关

1 特性

- 与 USB 2.0 以及 eUSB2 LS、FS 和 HS 物理层兼容
- 支持高达 3Gbps 差分信号的开关
- 可支持高达 3.3V 的大多数 CMOS 信号的模拟开关
- 数据引脚可承受 5V 电压
- $V_{IO} = 0\text{ V}$ 时, R_{ON} 低至 3Ω
- 高 -3dB 带宽为 3.3GHz
- 非常适合 240MHz 下的 USB 2.0 或 eUSB2 HS 信号 :
 - 插入损耗 = -0.4dB
 - 回损 = -22dB
 - 关断隔离或串扰 = -32dB
- 超低的垂直和水平 USB 2.0 HS 眼图衰减
- 1.8V 电源电压
- 1.2V 或 1.8V 控制逻辑输入
- 工业级工作温度范围 : -40°C 至 125°C
- 小型 10 引脚 1.8 mm × 1.4 mm UQFN 封装
- 具有多个源的引脚对引脚和 BOM 对 BOM

2 应用

- PC 和笔记本电脑
- 游戏、电视、家庭影院和娱乐系统
- 数据中心和企业级计算
- 医疗应用
- 测试和测量
- 工厂自动化和控制
- 手机和平板电脑

3 说明

TMUXHS221LV 是一款针对 USB 2.0 以及 eUSB2 LS、FS 和 HS 信号传输进行优化的高速双向 2:1 或 1:2 多路复用器或多路信号分离器。TMUXHS221LV 是一款适用于诸多数据速率高达 3Gbps 的高速接口的模拟无源开关。TMUXHS221LV 支持电压范围为 -0.3V 至 3.6V 的差分或单端 CMOS 信号传输。

TMUXHS221LV 的出色高速性能可将 USB 2.0 或 eUSB2 HS 信号眼图的衰减降至超低水平, 而且通道导通电阻、高带宽、低反射和低附加抖动也非常低。该器件经过优化, 可实现出色的高频响应, 因而可以更轻松地通过 USB 2.0 HS 电气合规性测试。该器件的数据路径也经过匹配, 可实现出色的差分对内延迟性能。

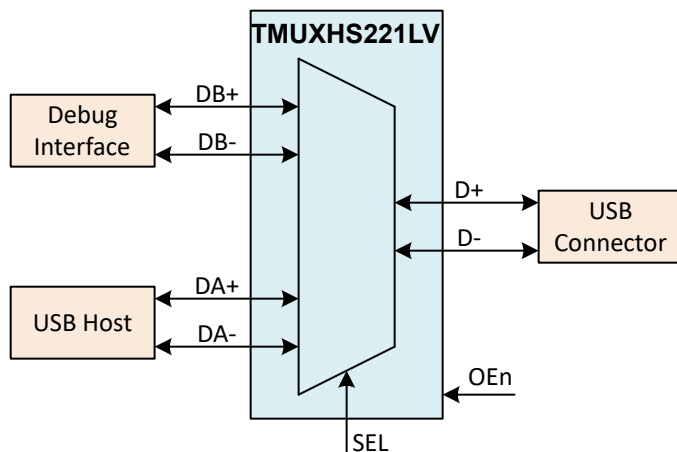
TMUXHS221LV 的工作温度范围适用于多种严苛应用, 包括工业和高可靠性用例。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
TMUXHS221LV	NKG (UQFN , 10)	1.8 mm x 1.4 mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



应用用例



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4 Revision History

DATE	REVISION	NOTES
July 2023	*	Initial Release

5 Pin Configuration and Functions

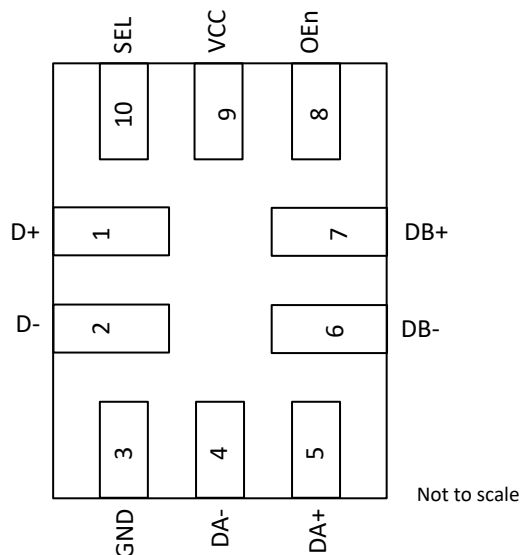


图 5-1. TMUXHS221LV NKG Package, 10-Pin UQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
D+	1	I/O	Data signals Common Port, positive
D-	2	I/O	Data signals Common Port, negative
DA+	5	I/O	Data signals Port A, positive
DA-	4	I/O	Data signals Port A, negative
DB+	7	I/O	Data signals Port B, positive
DB-	6	I/O	Data signals Port B, negative
SEL	10	IN	Switch control configuration signal as provided in 表 7-1 .
OEn	8	IN	
VCC	9	P	1.8 V power supply
GND	3	G	Ground

(1) IN = input, I/O = input or output, P = power, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC-ABSMAX}	Supply voltage	−0.5	2.4	V
V _{I/O-ABSMAX}	Voltage	−0.5	5.5	V
V _{IN-ABSMAX}	Voltage	−0.5	4	V
I _{I/O-ABSMAX}	ON-state switch current		100	mA
T _{J-ABSMAX}	Junction temperature	−40	125	°C
T _{STG}	Storage temperature	−65	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

		VALUE	UNIT
V _{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±5000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage	DC plus AC power should not exceed these limits	1.62	1.8	1.98	V
V _{CCRAMP}	Supply voltage ramp time		0.1		100	ms
V _{I/O}	Voltage range for data signals (V _{I/O})	D, DA, DB	−0.3		3.6	V
V _{IN}	Voltage range for control signals (V _{IN})	OEn, SEL	−0.3		3.6	V
T _J	Junction temperature				125	°C
T _A	Operating free-air/ambient temperature		−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUXHS221LV	UNIT
		NKG (UQFN)	
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance - High K	225.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	93.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	147.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	3.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	147.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{CC}	Device active current	OEn = L		10	17	μA
I _{STDN}	Device shutdown current	OEn = H		0.5	3	μA
C _{ON}	Output ON capacitance to GND	OEn = L		1.4		pF
R _{ON}	Channel ON resistance	V _{I/O} = 0 V, I _O = –8 mA		3	5.4	Ω
		V _{I/O} = 2.4 V, I _O = –8 mA		3.9	8	Ω
R _{ON,FLAT}	Channel ON resistance flatness defined as difference of R _{ON} over input voltage range	V _{I/O} = 0 V and V _{I/O} = 2.4 V; I _O = –8 mA		1		Ω
ΔR _{ON}	On-resistance match between pairs for the same channel at same V _{I/O} , V _{CC} and T _A	V _{I/O} = 0 V; I _O = –8 mA		0.2		Ω
		V _{I/O} = 2.4 V; I _O = –8 mA		0.2		Ω
V _{IH}	Input high voltage, control pins (OEn, SEL)		0.9		3.6	V
V _{IL}	Input low voltage, control pins (OEn, SEL)		–0.3		0.25	
I _{IH,IN}	Input high current, control pins (OEn, SEL)	V _{IN} = 3.6 V			8	μA
I _{IL,IN}	Input low current, control pins (OEn, SEL)	V _{IN} = 0 V			0.2	μA
I _{I/O,H}	Input high current, data pins (Dx, DAx, DBx)	V _{I/O} = 3.6 V			5	μA
I _{I/O,L}	Input low current, data pins (Dx, DAx, DBx)	V _{I/O} = 0 V			0.2	μA
I _{HIZ,I/O}	Leakage current through turned off switch	OEn = H; V _{I/O} = 3.6 V			8	μA
I _{OFF,IN}	Failsafe leakage current for control pins (IN)	V _{CC} = 0 V, V _{IN} = 1.98 V			12	μA
I _{OFF,I/O}	Failsafe leakage current for data pins (I/O)	V _{CC} = 0 V, V _{I/O} = 3.6 V			12	μA

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BW	–3-dB bandwidth	Relative to DC		3.3		GHz
I _L	Differential insertion loss	f = 10 MHz		–0.3		dB
		f = 240 MHz		–0.4		
R _L	Differential return loss	f = 10 MHz		–32		dB
		f = 240 MHz		–22		
O _{IRR}	Differential OFF isolation (D to DA/DB)	f = 10 MHz		–60		dB
		f = 240 MHz		–32		
XT	Single-Ended cross-talk (in between D+ and D- or DA+ and DA- or DB+ and DB-)	f = 10 MHz		–60		dB
		f = 240 MHz		–41		
XT _{diff}	Differential cross-talk (DA to DB or DB to DA)	f = 10 MHz		–64		dB
		f = 240 MHz		–32		

6.7 Switching Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
t _{PD}	Switch propagation delay			60	80	ps
t _{SW}	Switching time CTRL-to-Switch ON (SEL toggles in between H, L)	R _L = 50 Ω, C _L = 10 pF			1.5	μs
t _{OFF}	Time required for device ON-to-OFF transition (OEn = L to H)	R _L = 50 Ω, C _L = 10 pF			0.5	μs
t _{ON}	Time required for device OFF-to-ON transition (OEn = H to L)	R _L = 50 Ω, C _L = 10 pF			32	μs
t _{SK_INTRA}	Intra-pair output skew between positive and negative for same differential channel	For Dx to DAx or DBx channels		3	10	ps
t _{SK_INTER}	Inter-pair output skew between channels	For Dx to DAx or DBx channels		1	10	ps

6.8 Typical Characteristics – S-Parameters

图 6-1 和 图 6-2 显示典型 TMUXHS221LV 通道的差分插入损耗和回波损耗，分别。优异的 240 MHz 高速性能导致对 USB 2.0 或 eUSB2 HS 信号眼图的最小衰减。图 6-3 显示典型 TMUXHS221LV 通道的差分串扰。注意，提供的测量是在 TI 评估板上进行的，且板上和设备寄生参数已校准。

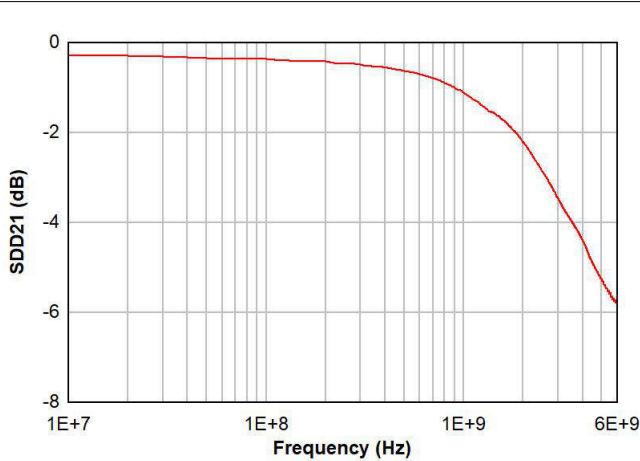


图 6-1. Typical Differential Insertion Loss vs Frequency

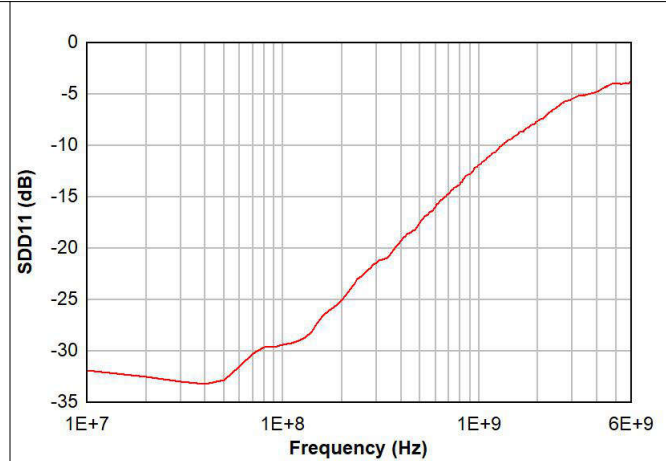


图 6-2. Typical Differential Return Loss vs Frequency

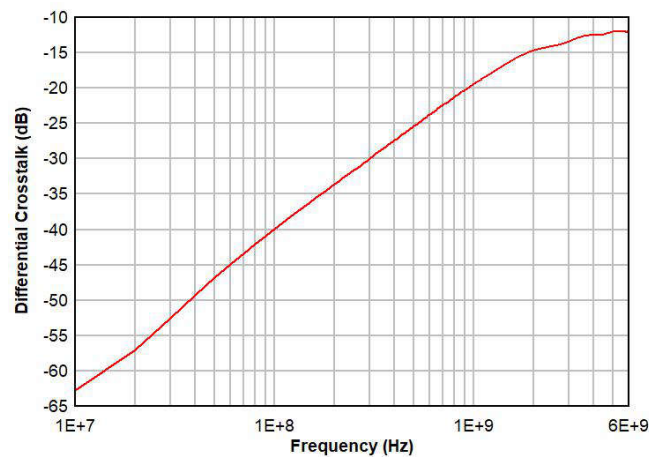


图 6-3. Typical Differential Crosstalk vs Frequency

6.9 Typical Characteristics – R_{ON}

图 6-4, 图 6-5, and 图 6-6 show switch ON resistance R_{ON} versus common mode voltage VCM, supply voltage VCC, and ambient temperature respectively. All curves are at nominal PVT conditions unless specified.

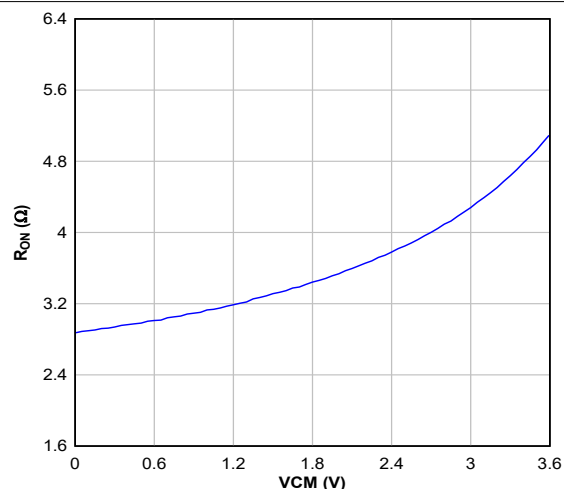


图 6-4. R_{ON} vs Common Mode Voltage VCM

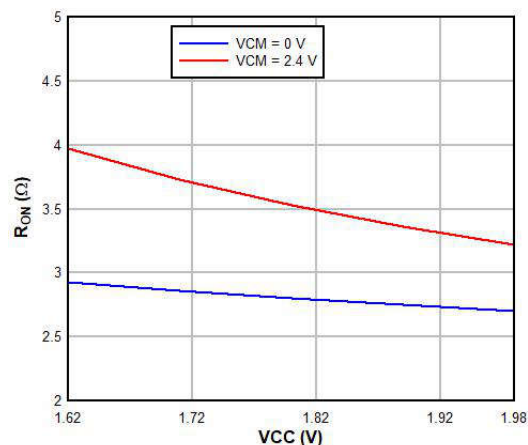


图 6-5. R_{ON} vs Supply Voltage VCC

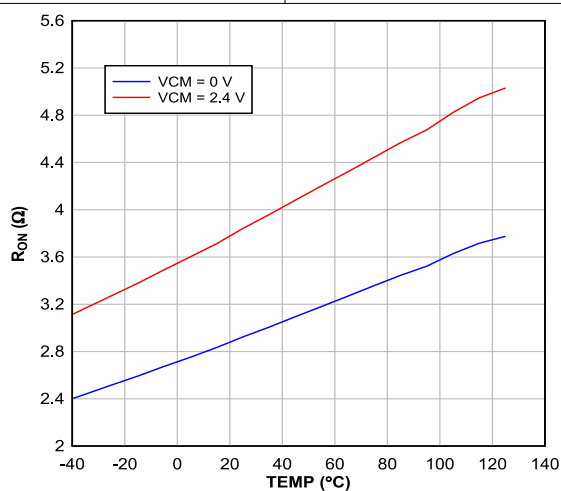


图 6-6. R_{ON} vs Ambient Temperature

6.10 Typical Characteristics – Eye Diagrams

图 6-7 和 图 6-8 显示 480Mbps USB 2.0 HS 信号通过校准迹（无设备）和典型 TMUXHS221LV 通道的侧-by-侧眼图比较。通过该设备的垂直和水平眼图衰减是微不足道的。此外，该复用设备向信号添加的抖动量可忽略不计。



图 6-7. Through Calibration Traces at 480Mbps



图 6-8. Through a Typical TMUXHS221LV Channel at 480Mbps

图 6-9 和 图 6-10 显示 3Gbps 信号通过校准迹（无设备）和典型 TMUXHS221LV 通道的侧-by-侧眼图比较。通过该设备的垂直和水平眼图衰减是微不足道的。该复用设备仅在 3Gbps 时添加少量抖动。



图 6-9. Through Calibration Traces at 3Gbps



图 6-10. Through a Typical TMUXHS221LV Channel at 3Gbps

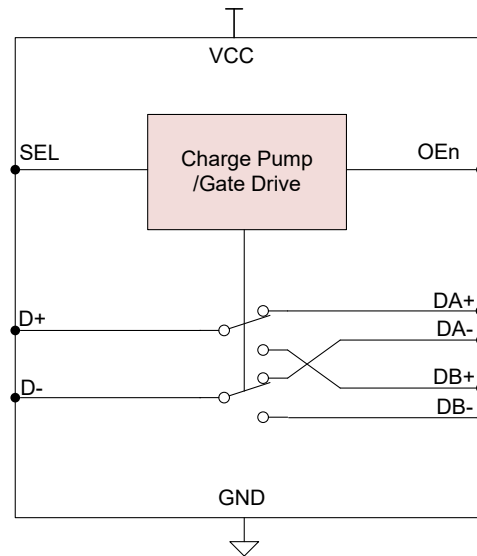
7 Detailed Description

7.1 Overview

The TMUXHS221LV is an analog passive mux with 2:1 or 1:2 multiplexer or demultiplexer that can work for any low-speed, high-speed, differential or single-ended signals. The signals must be within the allowable voltage range of -0.3 to 3.6 V. The device is optimized for eUSB2 and USB 2.0 LS, FS, and HS signaling.

The dynamic characteristics of the device allow high-speed switching with minimal attenuation to the signal eye diagram and little added jitter. While the device is recommended for the interfaces up to 3Gbps, actual data rates where the device can be used highly depends on the electrical channels. For low loss channels where adequate margin is maintained, the device can potentially be used for higher data rates.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Enable and Power Savings

The TMUXHS221LV has two power modes: active, or normal, operating mode and standby, or shutdown mode. During standby mode, the device consumes very little current to achieve ultra low power in systems where saving power is critical. To enter standby mode, OEn must be pulled high.

7.3.2 Data Line Biasing

The TMUXHS221LV does not contain any internal biasing. All channels of the device must be externally biased from either of the two sides to avoid floating channels.

7.4 Device Functional Modes

表 7-1. Mux Configuration Control Logic for TMUXHS221LV⁽¹⁾

SEL	OEn	Mux Configuration
L	L	D to DA
H	L	D to DB
X	H	All channels are disabled and Hi-Z

- (1) The TMUXHS221LV can tolerate polarity inversions. Ensure that the polarity consistency is maintained for all signals. However the device cannot change polarity from input to output.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TMUXHS221LV is an analog high-speed mux/demux that can be used for routing differential as well as single ended CMOS signals through it. The device can be used for many high speed and low speed interfaces up to 3Gbps including the following:

- Universal Serial Bus (USB) 2.0 HS, FS, and LS
- Embedded Universal Serial Bus (eUSB) 2.0 HS, FS, and LS
- Inter-Integrated Circuit (I²C) Bus
- System Management Bus (SMBus™)
- Universal Asynchronous Receiver-Transmitter (UART™)
- Debug interface signals
- Mipi® Camera Serial Interface (CSI-2), Display Serial Interface (DSI)
- PCIe® clock
- DisplayPort™ Auxiliary and Hot Plug Detect Signals
- Universal Serial Bus Type C Sideband Use (USB-C™ SBU) signals
- Low Voltage Differential Signaling (LVDS)

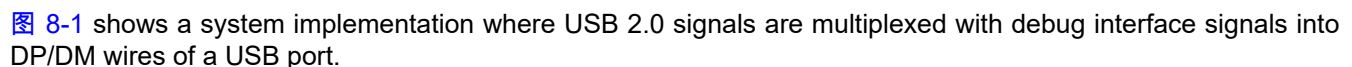
An available GPIO pin of a controller or hard tie to voltage level H or L can easily control the mux or demux selection pin (SEL) of the device as an application requires.

Many interfaces require AC coupling the capacitors between the transmitter and receiver. The 0201 or 0402 capacitors are the preferred option, but other capacitors may be used depending on interface speed and signal integrity needs. If AC coupling capacitors are used on both sides of the TMUXHS221LV, then ensure the device is biased from either side, as there is no internal biasing to the device.

8.2 Typical Applications

8.2.1 Routing Debug Signals to USB Port

Many electronic end-equipment such as PCs, media players, point of sales registers, printers, cameras, headphones, smartphones, tablets, and so forth use USB ports (such as USB Type-A, USB Type-B, or USB Type-C™) for in-field or factory debug interface. In such use cases debug signals are routed to USB 2.0 pins of a USB port through a mux or demux device. TMUXHS221LV is a good fit for such use cases with its flexible data handling capability. TMUXHS221LV can handle virtually any debug interface signals as long as they are limited to -0.3 V (minimum) to 3.6 V (maximum). The device also provides very low attenuation to both USB 2.0 and debug signals with its very low channel ON resistance, high bandwidth, and low reflection.

 8-1 shows a system implementation where USB 2.0 signals are multiplexed with debug interface signals into DP/DM wires of a USB port.

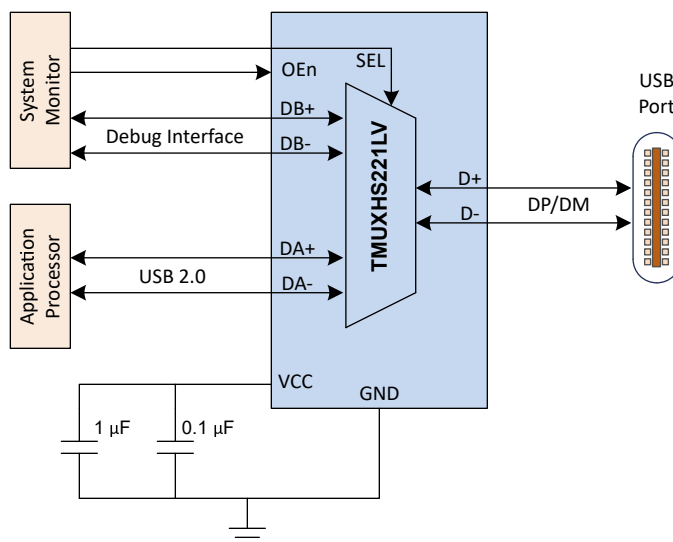


图 8-1. Routing Debug Signals to USB Port

8.2.1.1 Design Requirements

表 8-1 provides various parameters and their expected values to implement the routing debug signals into the USB port. Note that the recommendation is for illustration purpose only.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
DA+, DA-, DB+, and DB-	Direct connect to processors, -0.3 – 3.6 V
SEL/OEn pin maximum voltage for low	0.4 V
SEL/OEn pin minimum voltage for high	1.4 V
Decoupling capacitor for VCC	0.1 µF and 1 µF

8.2.1.2 Detailed Design Procedure

Signal integrity is important because as a passive switch, the device provides no signal conditioning capability.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Provide a control signal for the SEL and OEn pins.
- Provide good ground connection to the board ground plane.
- See the application schematics for the recommended decoupling capacitors from VCC pins to ground.

8.2.1.3 Application Curves

图 8-2 和 图 8-3 显示 USB 2.0 信号通过校准迹线（无设备）和 TMUXHS221LV 通道的眼图。A 组合 of 非常低的通道 ON 电阻、高带宽、非常低的反射（回损），和低添加的抖动来自设备允许 480Mbps USB 2.0 HS 信号保持未衰减。许多系统平台 struggle 通过 USB 2.0 合规性由于高损耗。TMUXHS221LV 允许插入一个模拟复用器设备在信号路径中而不创建任何额外的信号完整性问题。

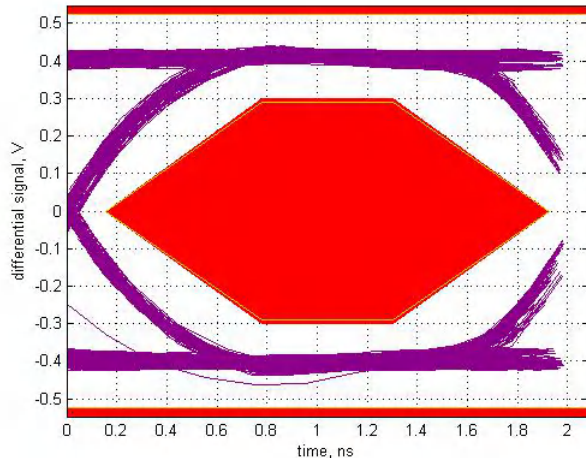


图 8-2. USB 2.0 HS Compliance Eye in TI Evaluation Board – Through Calibration Traces

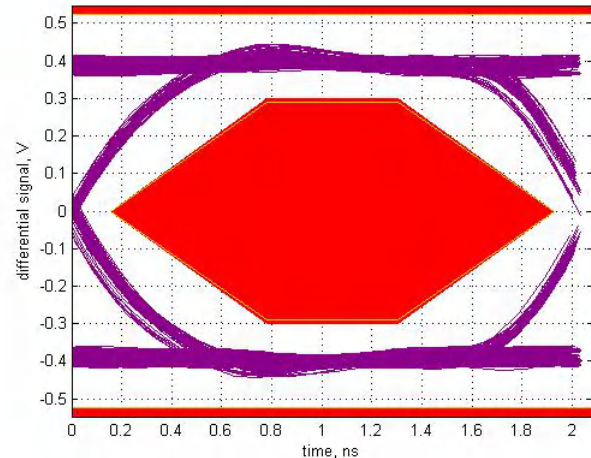


图 8-3. USB 2.0 HS Compliance Eye in TI Evaluation Board – Through TMUXHS221LV Channel

8.2.2 Systems Examples

8.2.2.1 PCIe Clock Muxing

图 8-4 显示一个应用，其中 TMUXHS221LV 用于切换 PCIe 时钟。该设备在 TI 评估板上进行测量，具有可用的时钟源，以显示添加的抖动小于 10 fs 用于所有 NOISE_FOLD 和 PCIe 5.0 CK 滤波器版本，这远低于 PCIe 5.0 时钟规格。

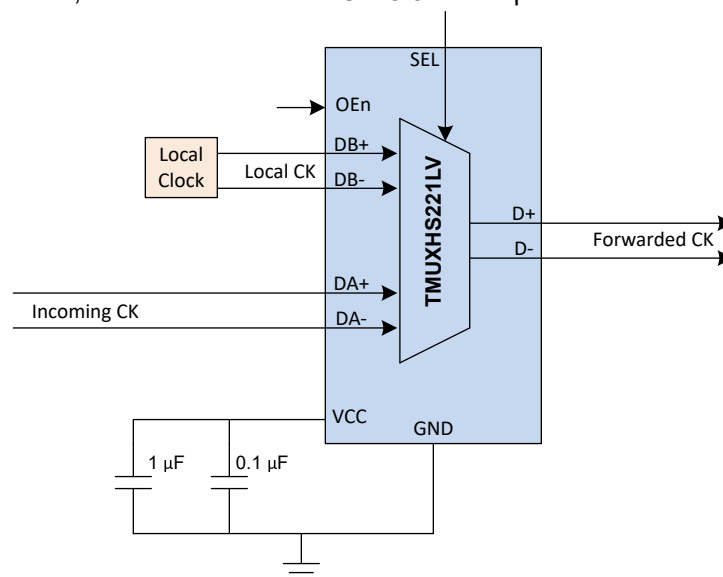


图 8-4. PCIe Clock Muxing

8.2.2.2 USB-C SBU Muxing

图 8-5 shows an application block diagram that implements SBU cross-muxing in a USB Type-C interface for implementing DisplayPort (DP) Alternate mode using the TMUXHS221LV. Note that the device has adequate bandwidth to support fast Auxiliary (AUX) signals. It is also capable of handling asymmetric biasing for DP AUX signals.

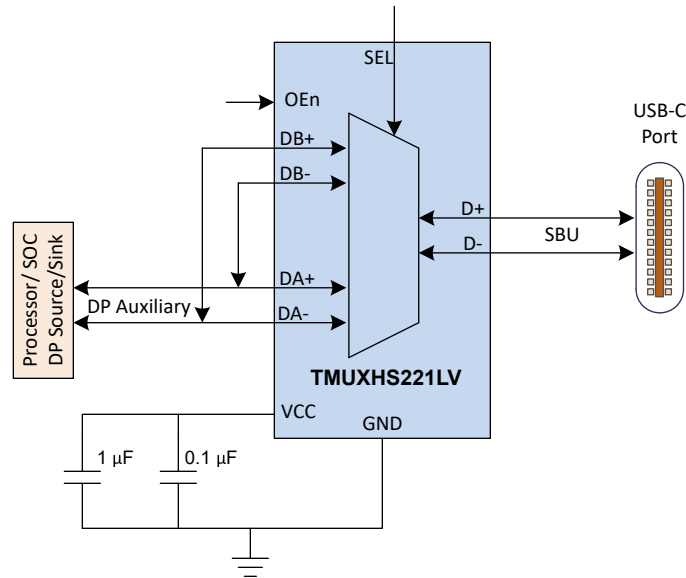


图 8-5. USB Type-C SBU Signals Muxing

8.2.2.3 Switching USB Port

图 8-6 shows an application block diagram where TMUXHS221LV is used to switch the USB port in between a hand-held portable device and its connected dock.

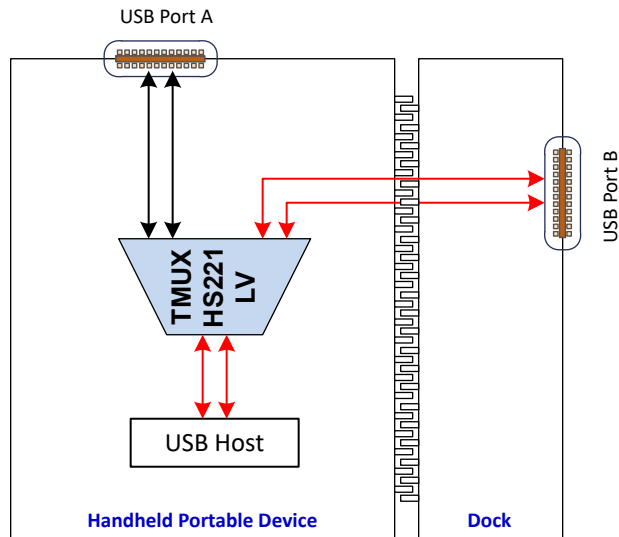


图 8-6. Switching USB Port

8.3 Power Supply Recommendations

The TMUXHS221LV does not require a power supply sequence. However, TI recommends to enable the device after VCC is stable and within specification. TI also recommends to place ample decoupling capacitors at the device VCC near the pin.

8.4 Layout

8.4.1 Layout Guidelines

A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In the layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance. The high-speed D+/D– traces should always be matched and must be no more than 4 inches, otherwise the eye diagram performance may be degraded.

- Place supply bypass capacitors as close to the VCC pin as possible.
- Avoid placing the bypass capacitors near the D+/D–traces.
- Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. When a via must be used, increase the clearance size around it to minimize its capacitance.
- Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.
- Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.
- Route all high-speed USB signal traces over continuous planes (VCC or GND) with no interruptions.
- Avoid crossing over anti-etch, commonly found with plane split.

For high speed layout guidelines, refer to [High-Speed Layout Guidelines for Signal Conditioners and USB Hubs application note](#).

8.4.2 Layout Example

图 8-7 shows a TMUXHS221LV layout example.

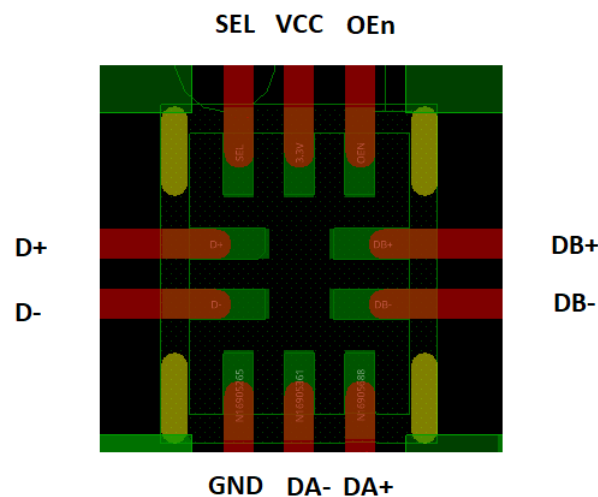


图 8-7. TMUXHS221LV Layout Example

9 Device and Documentation Support

9.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [High-Speed Layout Guidelines for Signal Conditioners and USB Hubs application note](#)

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

9.4 Trademarks

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9.5 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUXHS221LVNKGR	ACTIVE	UQFN	NKG	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	21L	Samples
TMUXHS221LVNKG	ACTIVE	UQFN	NKG	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	21L	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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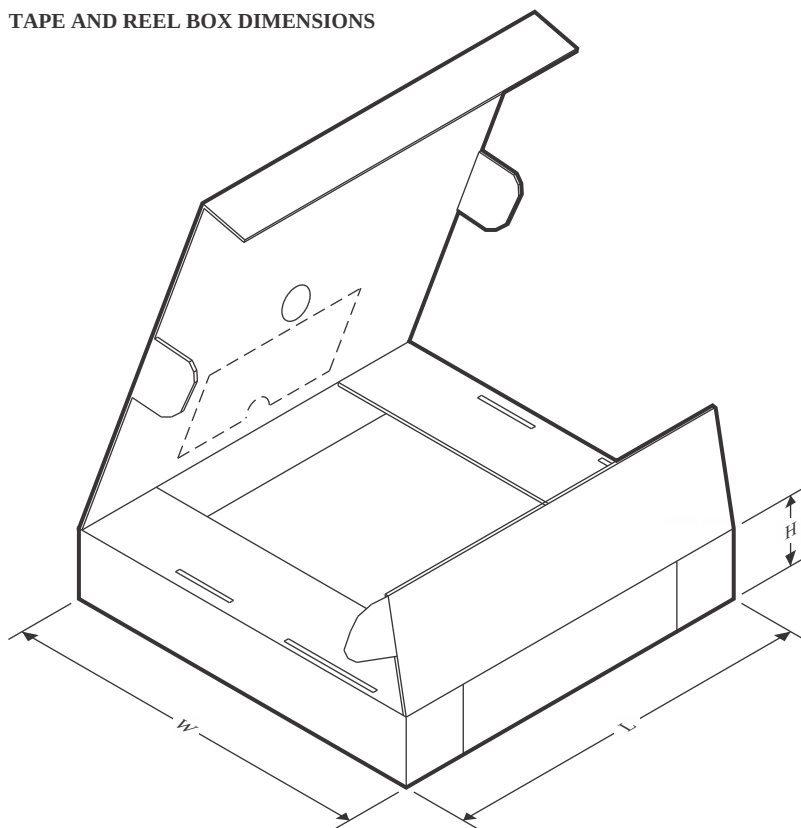
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXHS221LVNKGR	UQFN	NKG	10	3000	180.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
TMUXHS221LVNKGT	UQFN	NKG	10	250	180.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXHS221LVNKGR	UQFN	NKG	10	3000	210.0	185.0	35.0
TMUXHS221LVNKGT	UQFN	NKG	10	250	210.0	185.0	35.0

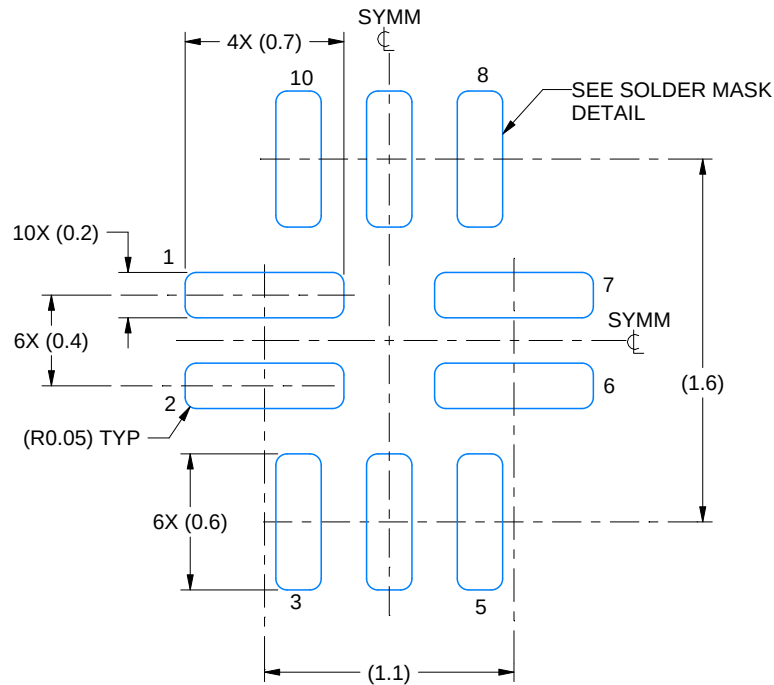


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

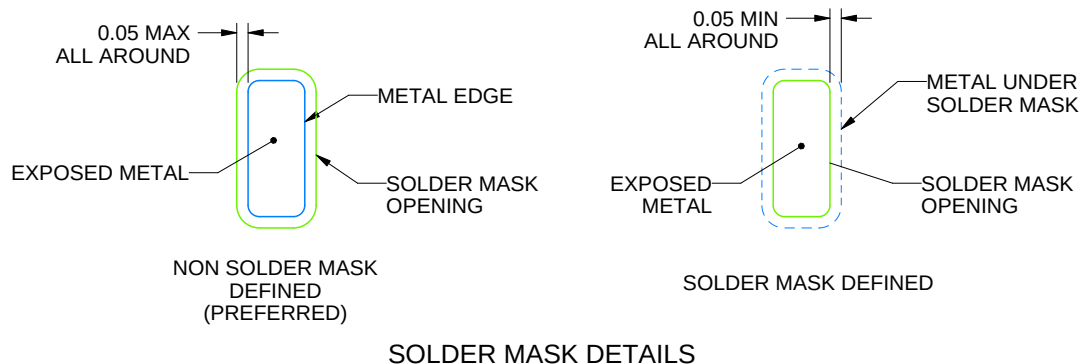
NKG0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



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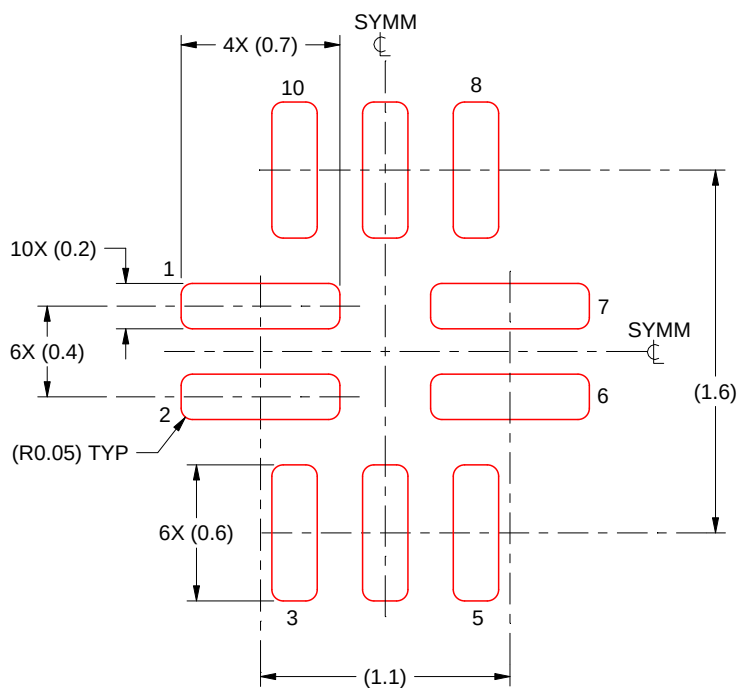
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

NKG0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 30X

4228479/A 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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