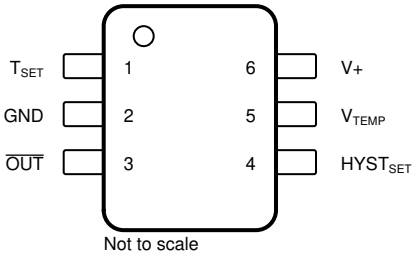
TMP300 采用 SC70 封装的 1.8V 电阻器可编程温度开关和模拟输出温度传感器

1 特性

- 精度：±1°C（+25°C 时的典型值）
- 可编程跳闸点
- 可编程迟滞：5°C/10°C
- 开漏输出
- 低功耗：110 µA（最大值）
- 宽电压范围：+1.8 V 至 +18 V
- 温度范围：–40°C 至 +125°C
- 模拟输出：10mV/°C
- SC70-6 和 SOT23-6 封装

2 应用

- 电源系统
- 直流/直流模块
- 过热监控
- 电子保护系统



引脚分配

3 说明

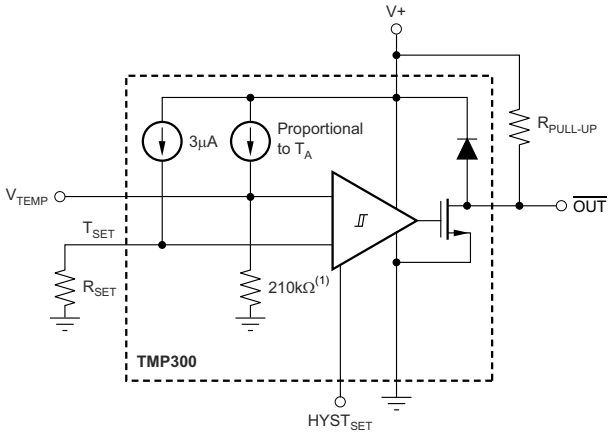
TMP300 是一款低功耗、电阻器可编程、数字输出温度开关。可通过添加外部电阻器设置器件阈值点。提供两种等级的迟滞。TMP300 有一个 V_{TEMP} 模拟输出，此输出可用作测试点或者用在温度补偿环路中。

TMP300 可采用两种微型封装并具有成熟的热特性、低电流消耗和低至 1.8V 的电源电压，专为需要简单可靠的热管理的功耗敏感型系统而设计。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
TMP300	SOT-23 (6)	2.90mm × 1.60mm
	SC70 (6)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



注：薄膜电阻器精度误差大约为 10%，但是该精度误差在出厂时已经过校准。

应用原理图

Table of Contents

4 Revision History

Changes from Revision E (December 2018) to Revision F (January 2023)	Page
• 更新了整个文档的表、图和交叉参考的编号格式	1
• 将*器件信息*表更改为*封装信息*	1
• Added parameter to the *Absolute Maximum Ratings* table: input current into any pin	4

Changes from Revision D (January 2016) to Revision E (December 2018)	Page
• Added *Pin Configuration and Functions* section	3

Changes from Revision C (January 2011) to Revision D (January 2016)	Page
• 添加了*器件信息*表、*ESD 等级*表、*特性说明*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1
• 更改了*温度范围*特性要点	1
• 向引脚排列部分添加了封装名称	1
• Deleted *Ordering Information* table	4
• Changed Temperature Range, *TA, Functional Range* parameter name in *Electrical Characteristics* table	5
• Added footnote 4 to *Electrical Characteristics* table	5

Changes from Revision B (November 2008) to Revision C (January 2011)	Page
• 删除了*说明*部分的第二句	1
• Added TMP300B grade device specifications to *Electrical Characteristics* table	5

5 Pin Configuration and Functions

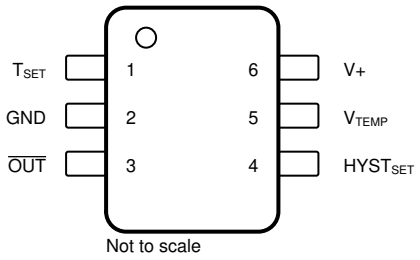


图 5-1. DCK and DBV Package 6-Pin SOT-23 and SC70 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
T_{SET}	1	I	Temperature set pin. Connects to a resistor to set the trip point
GND	2	—	Ground
$\overline{OUT}$	3	O	Trip output
$HYST_{SET}$	4	I	Hysteresis Set. Connect to Ground for 5°C hysteresis or connect to V+ for 10°C hysteresis
V_{TEMP}	5	I	Analog Temperature output
V+	6	O	Supply voltage: 1.8 V to 18 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V+	Supply voltage		+18	V
	Signal input pins, voltage(2)	–0.5	(V+) + 0.5	V
	Signal input pins, current(2)	–10	10	mA
	Input current into any pin		10	mA
I_{SC}	Output short-circuit(3)	Continuous		
	Open-drain output		(V+) + 0.5	V
T_A	Functional temperature	–40	+150	°C
T_{stg}	Storage temperature	–55	+150	°C
T_J	Junction temperature		+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±4000	V
		Charged-device model (CDM)	±1000	

6.3 Electrical Characteristics

At V_S = 3.3 V and T_A = –40°C to +125°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	TMP300			TMP300B			UNIT
				MIN(1)	TYP(1)	MAX(1)	MIN	TYP	MAX	
TEMPERATURE MEASUREMENT										
	Measurement range		V_S = 2.35 V to 18 V	–40		+125	–40		+125	°C
			V_S = 1.8 V to 2.35 V	–40		100 × (V_S – 0.95)	–40		100 × (V_S – 0.95)	
TRIP POINT										
	Total accuracy		T_A = –40°C to +125°C		±2	±4(3)		±2	±6	°C
	R_{SET} equation		T_C is in °C		R_{SET} = 10 (50 + T_C)/3			R_{SET} = 10 (50 + T_C)/3		kΩ
HYSTERESIS SET INPUT										
	LOW threshold					0.4			0.4	V
	HIGH threshold			V_S – 0.4			V_S – 0.4			V
	Threshold hysteresis		$HYST_{SET}$ = GND		5			5		°C
			$HYST_{SET}$ = V_S		10			10		
DIGITAL OUTPUT										
	Logic family				CMOS			CMOS		
	Open-drain leakage current		OUT = V_S			10			10	µA
V_{OL}	Logic levels		V_S = 1.8 V to 18 V, I_{SINK} = 5 mA			0.3			0.3	V
ANALOG OUTPUT										
	Accuracy				±2	±3		±2	±5	°C
	Temperature sensitivity				10			10		mV/°C
	Output voltage		T_A = +25°C	720	750	780	720	750	780	mV
	V_{TEMP} pin output resistance				210			210		kΩ
POWER SUPPLY										
I_Q	Quiescent current(2)		V_S = 1.8 V to 18 V, T_A = –40°C to +125°C			110			110	µA
TEMPERATURE RANGE										
T_A	Specified range		V_S = 2.35 V to 18 V	–40		+125	–40		+125	°C
			V_S = 1.8 V to 2.35 V	–40		100 × (V_S – 0.95)	–40		100 × (V_S – 0.95)	
	Functional range(4)		V_S = 2.35 V to 18 V	–40		+150	–40		+150	
			V_S = 1.8 V to 2.35 V	–50		100 × (V_S – 0.95)	–50		100 × (V_S – 0.95)	
θ_{JA}	Thermal resistance	SC70			250			250		°C/W
		SOT23-6			180			180		

(1) 100% of production is tested at T_A = +85°C. Specifications over temperature range are ensured by design.
(2) See 图 6-1 for typical quiescent current.
(3) Shaded cells indicate characteristic performance difference.
(4) The TMP300 is functional over this range and no indication of performance is implied.

6.4 Typical Characteristics

At V_S = 5 V, unless otherwise noted.

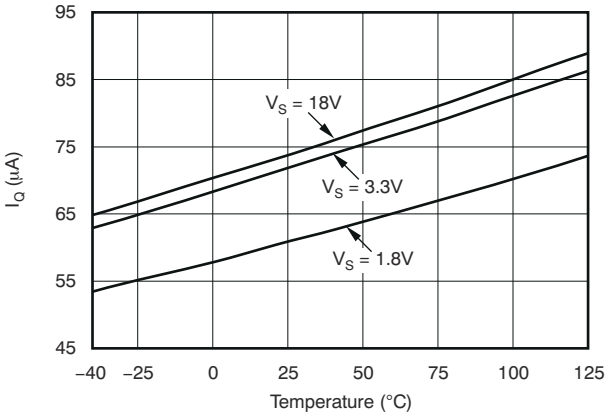


图 6-1. Quiescent Current Over Temperature and Supply

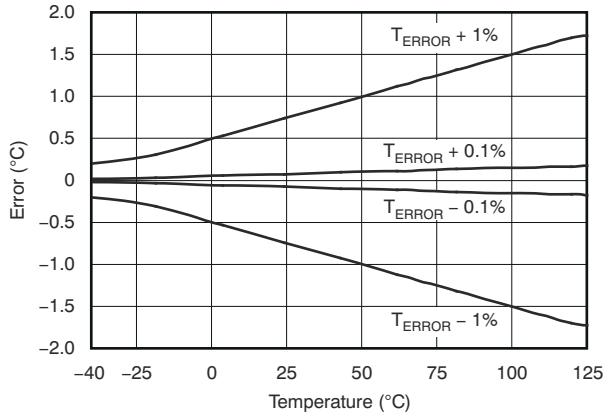


图 6-2. R_{SET} Shift Resulting From R_{SET} Tolerance

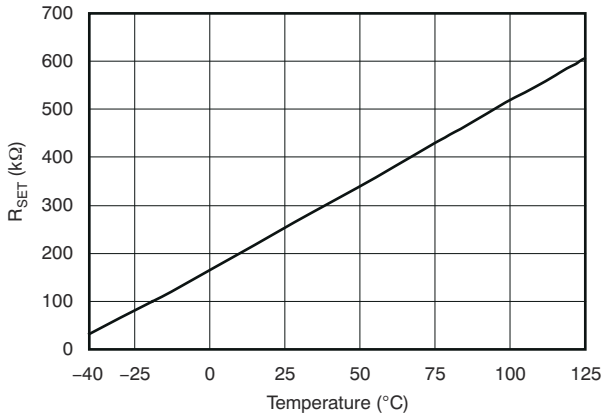


图 6-3. R_{SET} vs Temperature

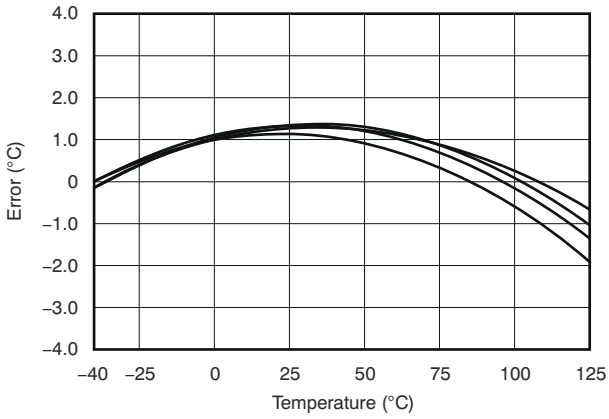


图 6-4. Typical Trip Error

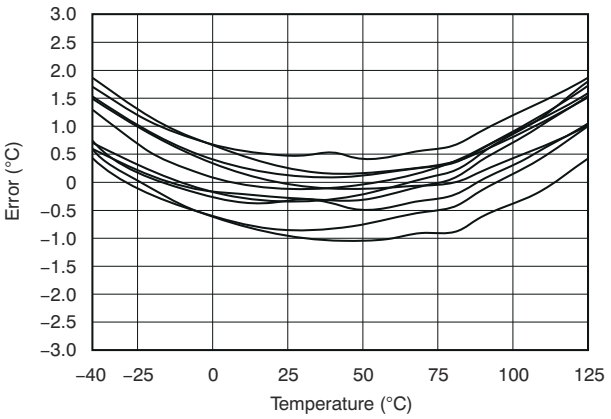


图 6-5. Typical Analog Output Error

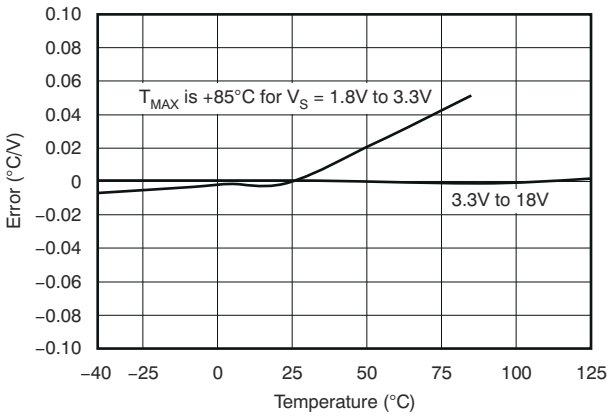


图 6-6. Analog PSR Over Temperature

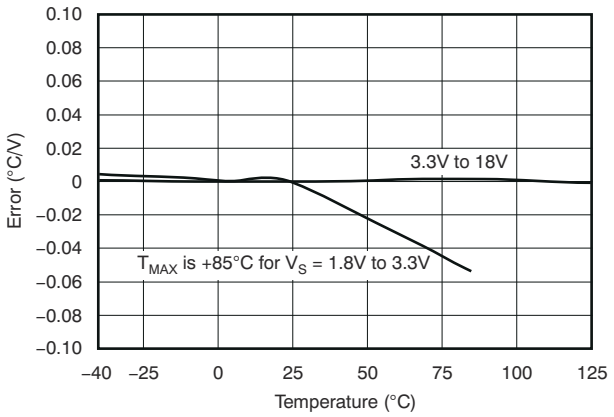


图 6-7. Trip PSR Over Temperature

7 Detailed Description

7.1 Overview

The TMP300 is a thermal sensor designed for overtemperature protection circuits in electronic systems. The TMP300 uses a set resistor to program the trip temperature of the digital output. An additional high-impedance (210 kΩ) analog voltage output provides the temperature reading.

7.2 Feature Description

7.2.1 Calculating R_{SET}

The set resistor (R_{SET}) provides a threshold voltage for the comparator input. The TMP300 trips when the V_{TEMP} pin exceeds the T_{SET} voltage. The value of the set resistor is determined by the analog output function and the 3- μ A internal bias current.

To set the TMP300 to trip at a preset value, calculate the R_{SET} resistor value according to 方程式 1 or 方程式 2:

$$R_{SET} = \frac{(T_{SET} \times 0.01 + 0.5)}{3e^{-6}} \quad (1)$$

where

- T_{SET} is in °C; or

$$R_{SET} \text{ in } k\Omega = \frac{10(50 + T_{SET})}{3} \quad (2)$$

where

- T_{SET} is in °C.

7.2.2 Using V_{TEMP} to Trip the Digital Output

The analog voltage output can also serve as a voltage input that forces a trip of the digital output to simulate a thermal event. This simulation facilitates easy system design and test of thermal safety circuits, as shown in 图 7-1.

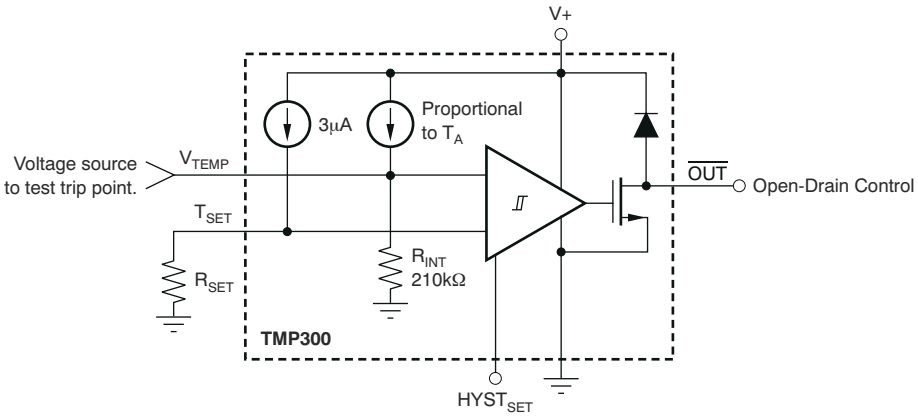


图 7-1. Applying Voltage to Trip Digital Output

7.2.3 Analog Temperature Output

The analog out or V_{TEMP} pin is high-impedance (210 kΩ). Avoid loading this pin to prevent degrading the analog out value or trip point. Buffer the output of this pin when used for direct thermal measurement. 图 7-2 shows buffering of the analog output signal.

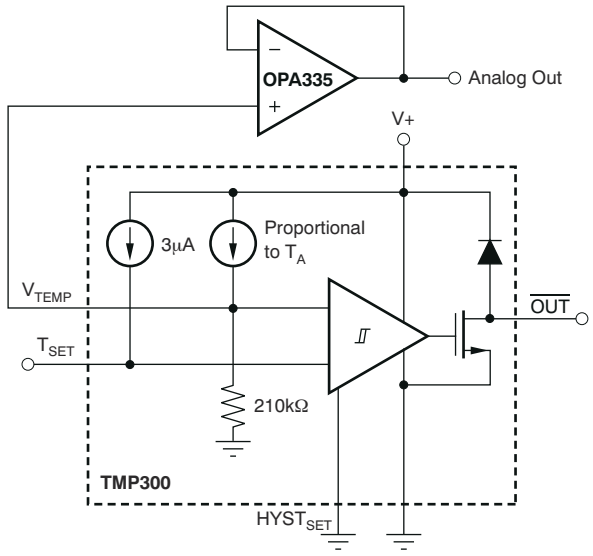


图 7-2. Buffering the Analog Output Signal

7.2.4 Using a DAC to Set the Trip Point

The trip point is easily converted by changing the digital-to-analog converter (DAC) code. This technique can be useful for control loops where a large thermal mass is being brought up to the set temperature and the $\overline{OUT}$ pin is used to control the heating element. The analog output can be monitored in a control algorithm that adjusts the set temperature to prevent overshoot. 图 7-3 shows the trip set voltage error versus temperature, which shows error in °C of the comparator input over temperature. 图 7-4 shows an alternative method of setting the trip point by using a DAC.

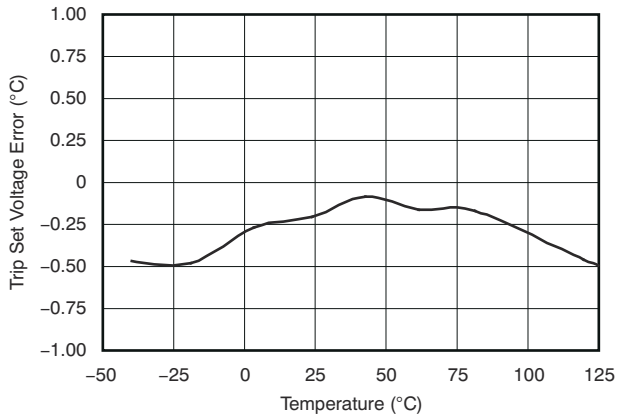


图 7-3. Trip Set Voltage Error vs Temperature

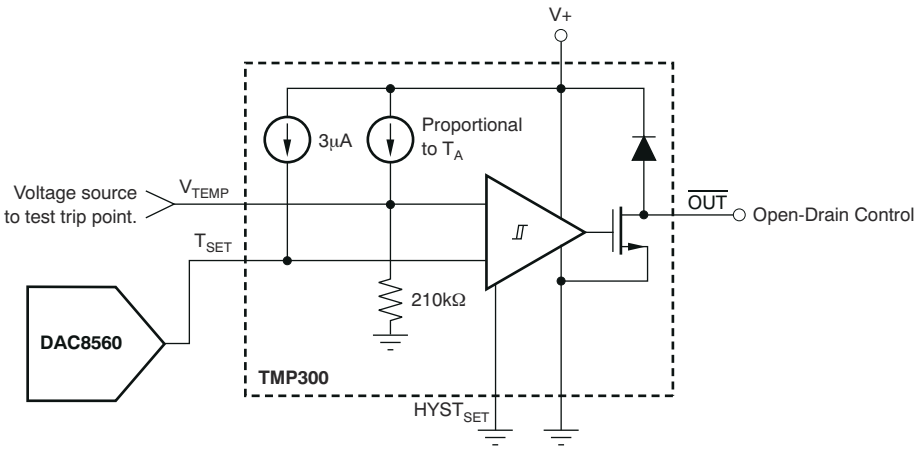


图 7-4. DAC Generates the Voltage-Driving T_{SET} Pin

7.2.5 Hysteresis

The hysteresis pin has two settings. Grounding $HYST_{SET}$ results in 5°C of hysteresis. Connecting $HYST_{SET}$ to V_S results in 10°C of hysteresis. 图 7-5 and 图 7-6 show the hysteresis error variation over temperature.

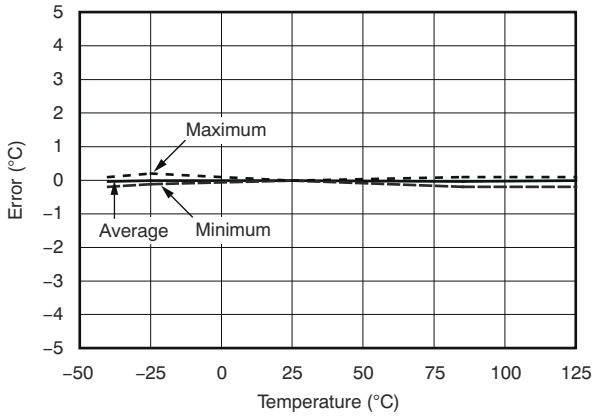


图 7-5. 5°C Hysteresis Error vs Temperature

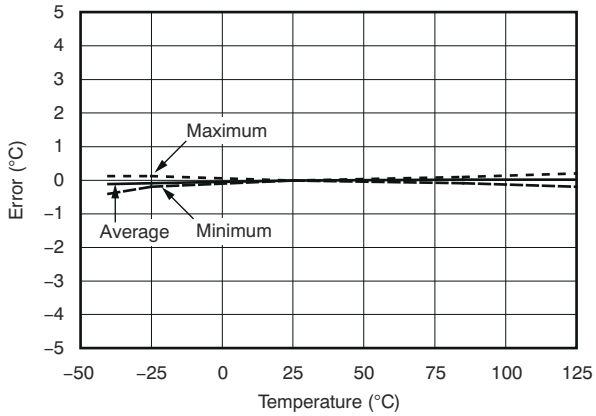


图 7-6. 10°C Hysteresis Error vs Temperature

Use bypass capacitors on the supplies as well as on the R_{SET} and analog out (V_{TEMP}) pins when in noisy environments, as shown in 图 7-7. These capacitors reduce premature triggering of the comparator.

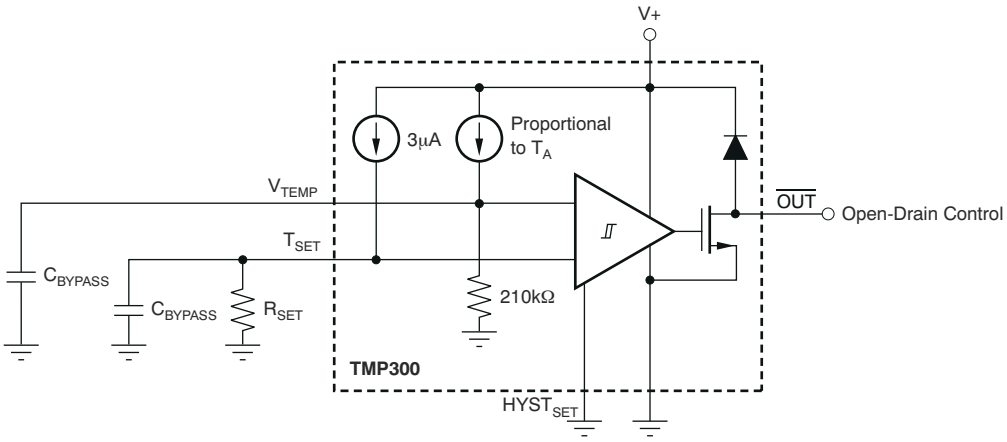


图 7-7. Bypass Capacitors Prevent Early Comparator Toggling Due to Circuit Board Noise

8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP300AIDBVR	NRND	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T300	
TMP300AIDCKR	NRND	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BPN	
TMP300BIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DUDC	Samples
TMP300BIDBVT	OBSOLETE	SOT-23	DBV	6		TBD	Call TI	Call TI	-40 to 125	DUDC	
TMP300BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QWL	Samples
TMP300BIDCKT	OBSOLETE	SC70	DCK	6		TBD	Call TI	Call TI	-40 to 125	QWL	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMP300 :

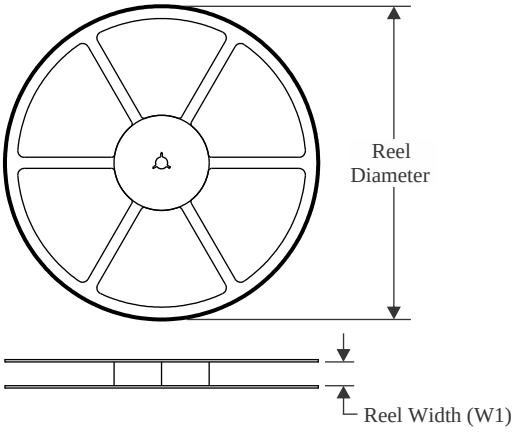
- Automotive : TMP300-Q1

NOTE: Qualified Version Definitions:

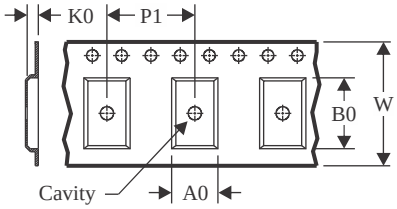
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

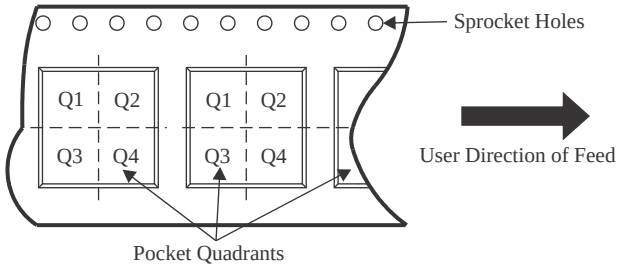


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

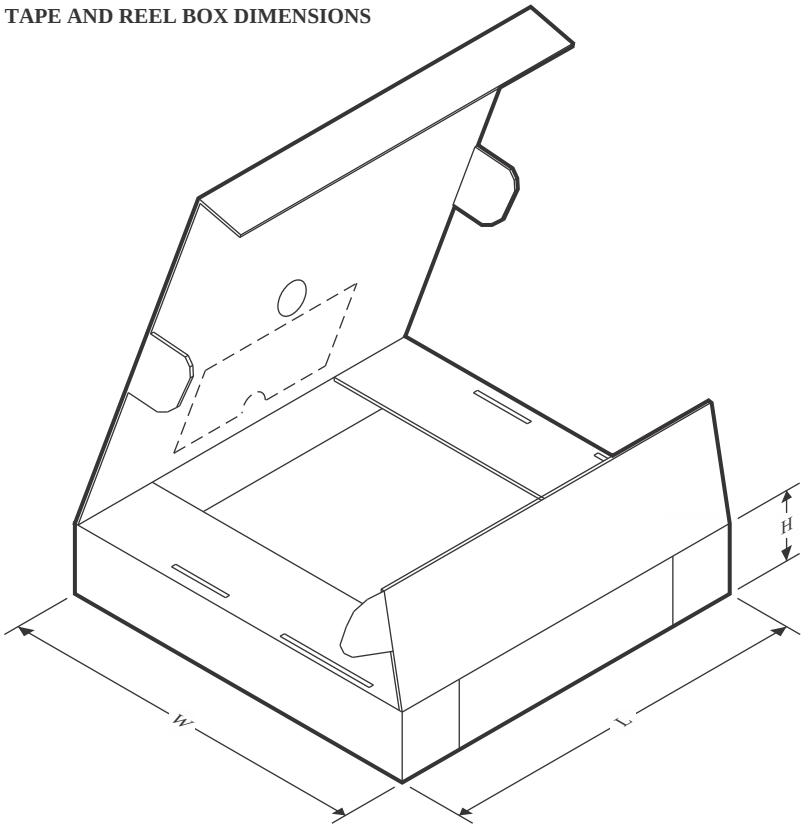
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP300AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TMP300BIDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP300BIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

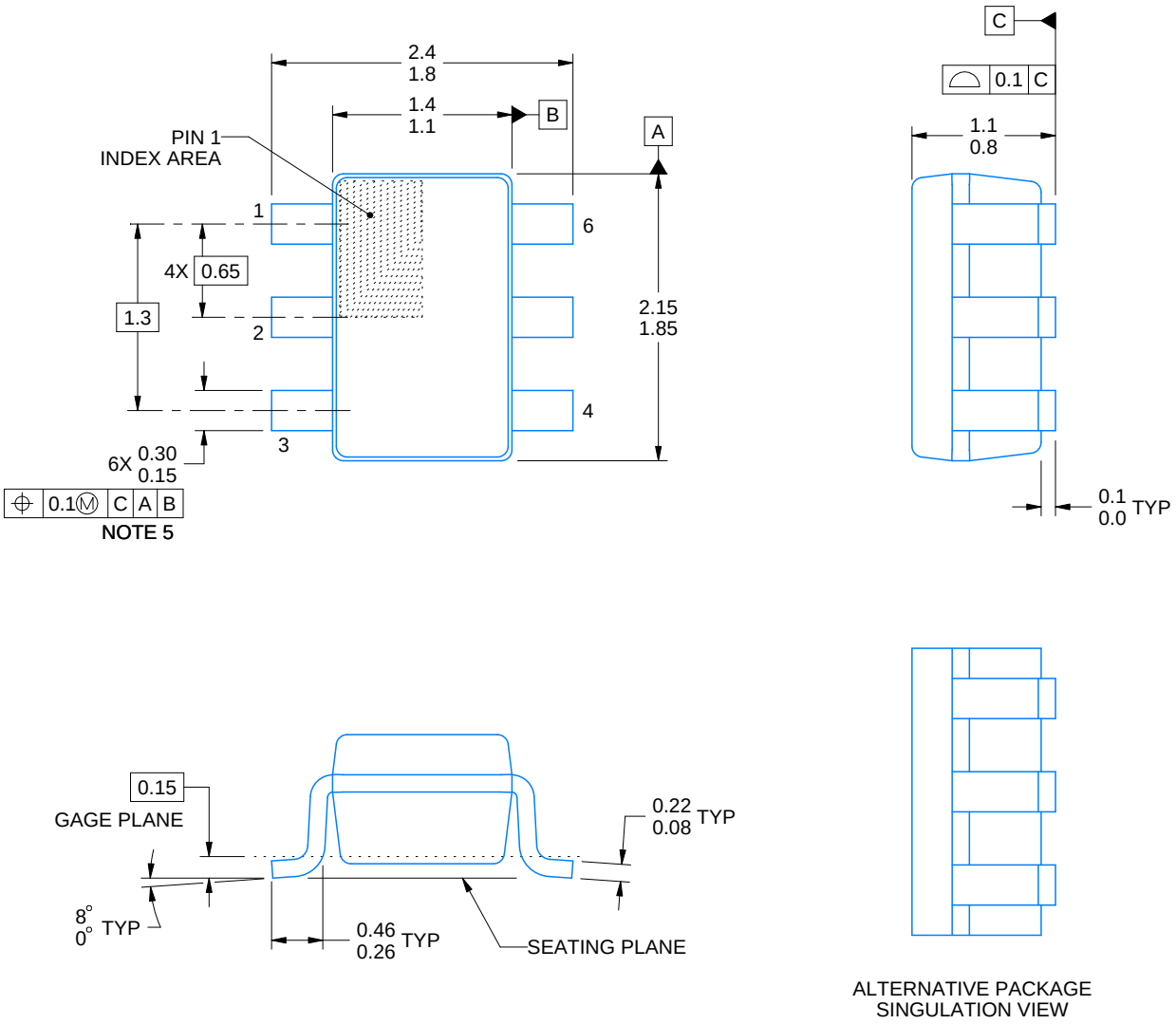
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP300AIDBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TMP300AIDCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TMP300BIDBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TMP300BIDCKR	SC70	DCK	6	3000	200.0	183.0	25.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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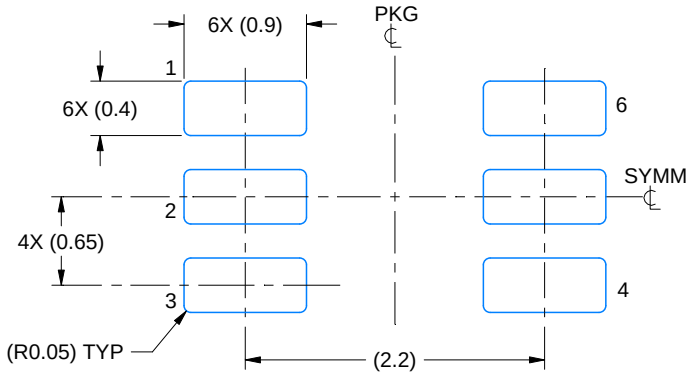
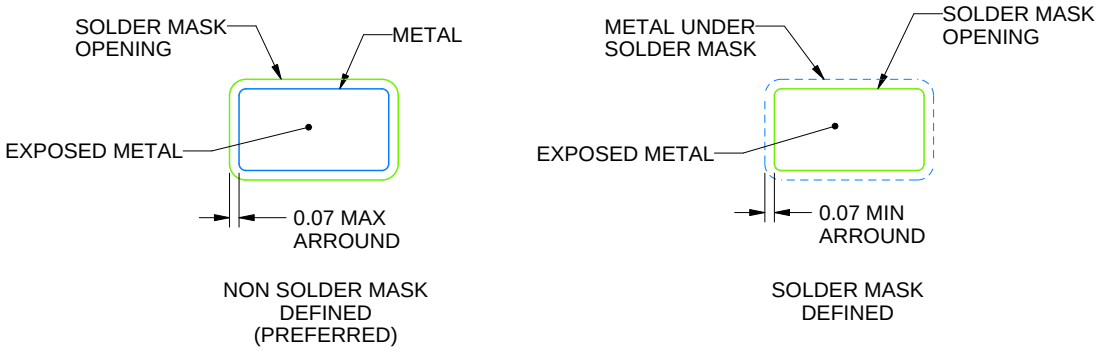
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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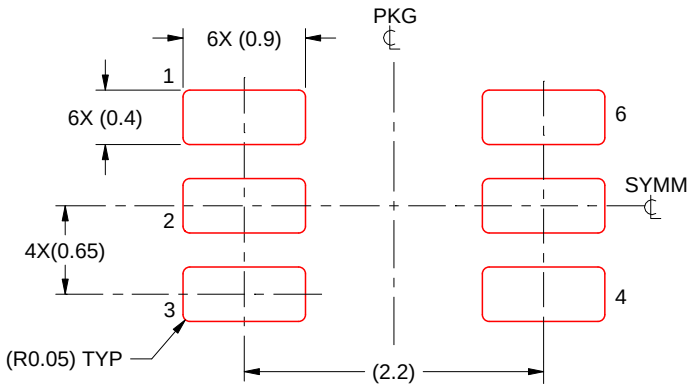
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/B 04/2024

NOTES: (continued)

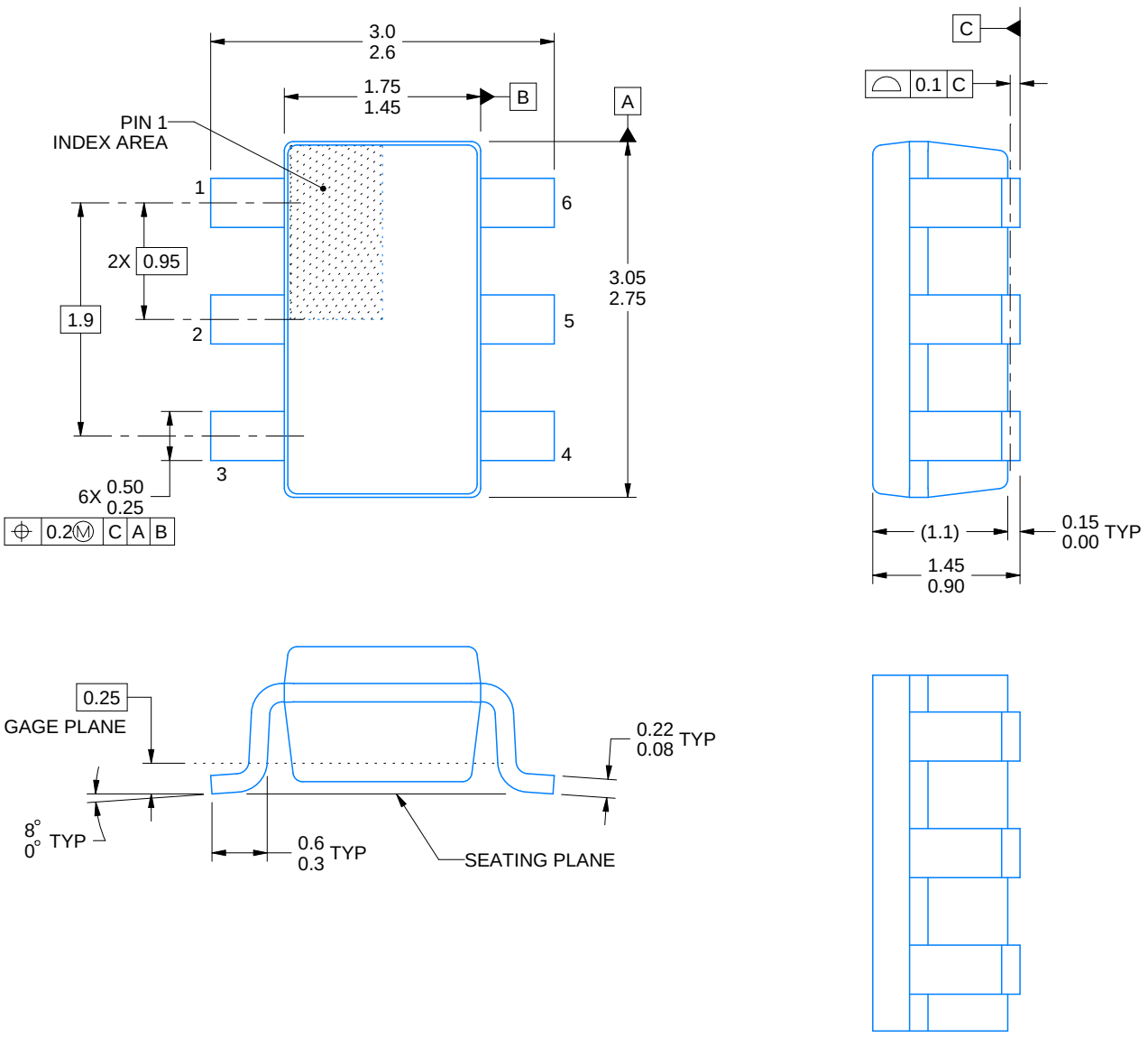
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

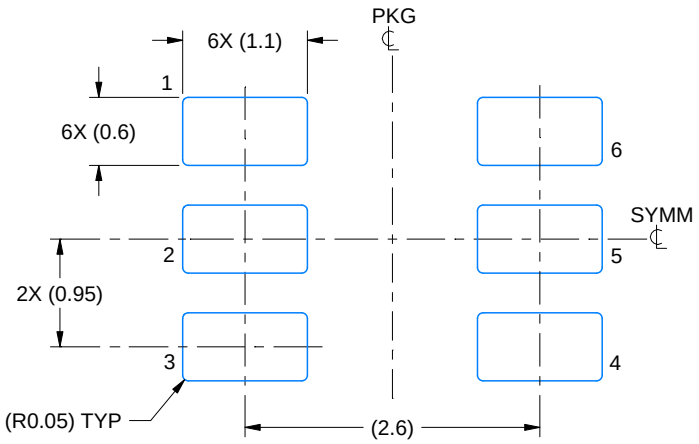


ALTERNATIVE PACKAGE SINGULATION VIEW

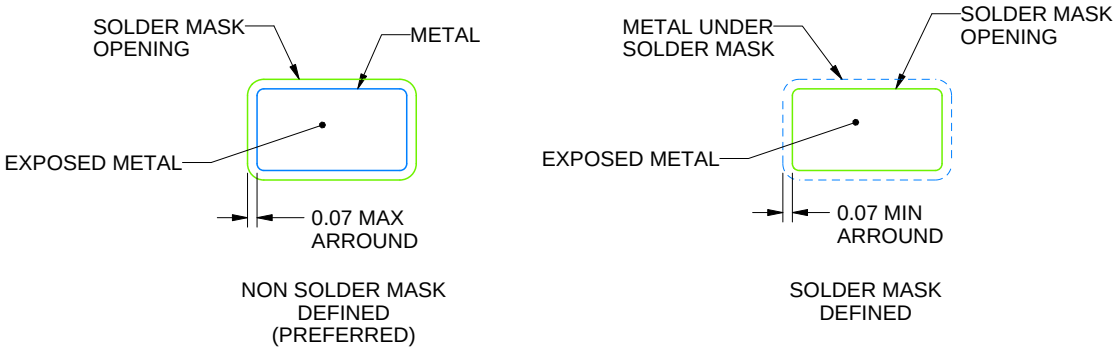
4214840/F 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

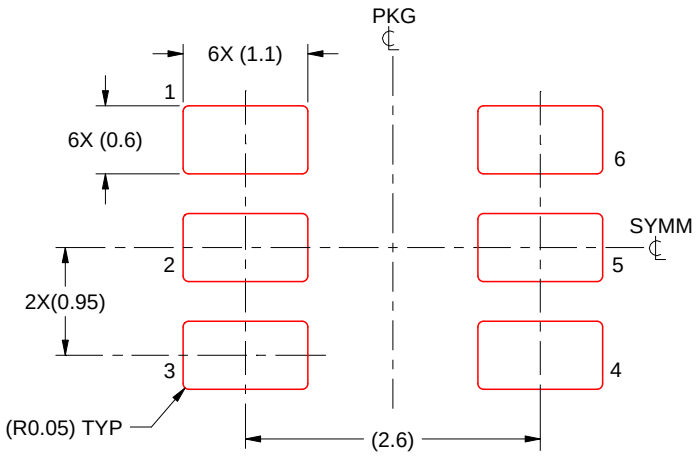


SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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