配备 SMAART Wire™ 接口的 TMP104 低功耗数字温度传感器

1 特性

- 多器件访问 (MDA)：
  – 全局读/写操作
- SMAART Wire™ 接口
- 分辨率：8 位
- 精度：±0.5°C（典型值，–10°C 至 +100°C）
- 低静态电流：
  – 0.25Hz 频率下的工作 I_Q 为 3µA
  – 关断电流为 1µA
- 电源范围：1.4V 至 3.6V
- 数字输出
- 封装：0.8mm (±5%) × 1mm (±5%)，4 焊球 WCSP (DSBGA)

2 应用

- 手持终端
- 笔记本电脑

3 说明

TMP104 器件是一款采用 4 焊球晶圆级芯片规模封装 (WCSP) 的数字输出温度传感器。TMP104 读取温度的分辨率可达 1℃。

TMP104 采用 SMAART wire™ 接口，可支持菊花链配置。此外，该接口还支持多器件存取 (MDA) 命令，允许主控器与总线上的多个器件同时进行通信，从而不必向总线上的每个 TMP104 单独发送命令。

最多可并联 16 个 TMP104 并由主机轻松进行读取。TMP104 专为具有多个温度测量区域需要监测的空间受限类功率敏感型 应用 而设计。

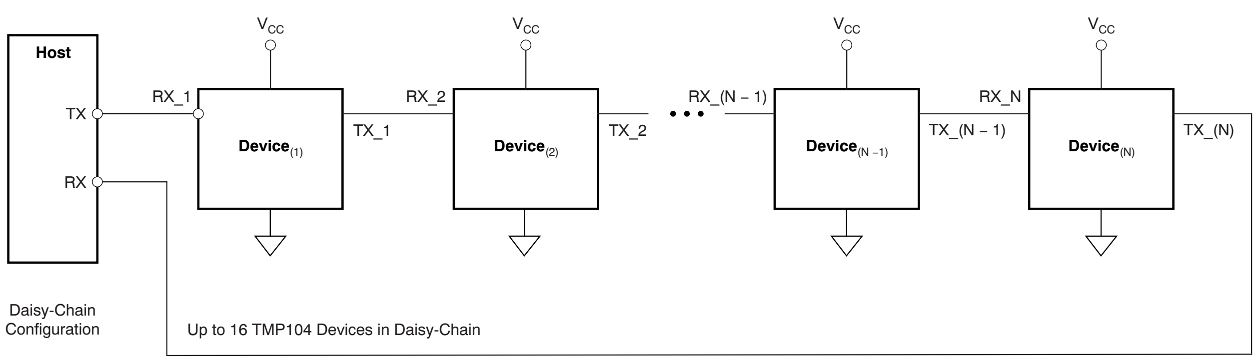
TMP104 的额定运行温度范围为 –40℃ 至 +125℃。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMP104	DSBGA (4)	1.20mm × 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (November 2011) to Revision B **Page**

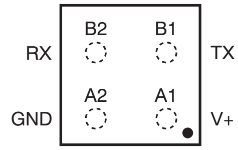
- 添加了*设备信息* 表、*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 1
- Changed supply voltage maximum value from: 3.6 V to: 4 V 3
- Changed input voltage maximum value from: (V+) + 0.3 to:(V+) + 0.5 and ≤ 4 V 3
- 已将*封装/订购信息* 表中的内容移至*机械、封装和订购信息* 部分 16

Changes from Original (November 2011) to Revision A **Page**

- 已更改 *将“单线 UART 式接口”*更改为*“SMAART 线接口”* 1
- Changed description of protocol in *Communication Protocol* section 7
- Updated Figure 7 7

5 Pin Configuration and Functions

YFF PACKAGE
WCSP-4 (DSBGA-4)
(TOP VIEW)



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
A1	V+	Supply voltage
A2	GND	Ground
B1	TX	Serial data output pin (push-pull output)
B2	RX	Serial data input pin

6 Specifications

6.1 Absolute Maximum Ratings[1]

	MIN	MAX	UNIT
Supply voltage		4	V
Input voltage	–0.3	(V+) + 0.5 and ≤ 4	V
Operating temperature	–55	150	°C
Junction temperature		+150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±100	
		Machine model (MM)	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMP104	UNIT
		YFF (DSBGA)	
		4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

Thermal Information (continued)

THERMAL METRIC(1)		TMP104 YFF (DSBGA) 4 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

6.4 Electrical Characteristics

At T_A = +25°C and V+ = +1.4 V to +3.6 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Range		–40		+125	°C
	Accuracy (temperature error)	–10°C to +100°C, V+ = 1.8 V		±0.5	±2	°C
		–40°C to +125°C, V+ = 1.8 V		±1	±3	°C
		vs supply		±0.2	±0.5	°C/V
	Resolution			1.0		°C
DIGITAL INPUT/OUTPUT						
V_{IH}	Input logic levels		0.7 × (V+)		V+	V
V_{IL}			–0.5		0.3 × (V+)	V
I_{IN}	Input current	0 < V_{IN} < (V+) + 0.3 V			1	µA
V_{OL}	Output logic levels	V+ > 2 V, I_{OL} = 1 mA	0		0.4	V
		V+ < 2 V, I_{OL} = 1 mA	0		0.2 × (V+)	V
V_{OH}		V+ > 2 V, I_{OH} = 1 mA	(V+) – 0.4		V+	V
		V+ < 2 V, I_{OH} = 1 mA	0.8 × (V+)		V+	V
	Resolution			8		Bit
	Conversion time			26	35	ms
	Conversion modes	CR1 = 0, CR0 = 0 (default)		0.25		Conv/s
		CR1 = 0, CR0 = 1		1		Conv/s
		CR1 = 1, CR0 = 0		4		Conv/s
		CR1 = 1, CR0 = 1		8		Conv/s
	Timeout time	Interface		28		ms
	SMAART wire interface	Serial baud rate	4.8		114	kbps
POWER SUPPLY						
	Operating supply range		+1.4		+3.6	V
I_Q	Quiescent current	Serial bus inactive, CR1 = 0, CR0 = 0 (default), V+ = 1.8 V		1.5	3	µA
		Serial bus active, CR1 = 0, CR0 = 0, V+ = 1.8 V		20		µA
I_{SD}	Shutdown current	Serial bus inactive, V+ = 1.8 V		0.5	1	µA
TEMPERATURE						
	Specified range		–40		+125	°C
	Operating range		–55		+150	°C

6.5 Typical Characteristics

At T_A = +25°C and V+ = 1.8 V, unless otherwise noted.

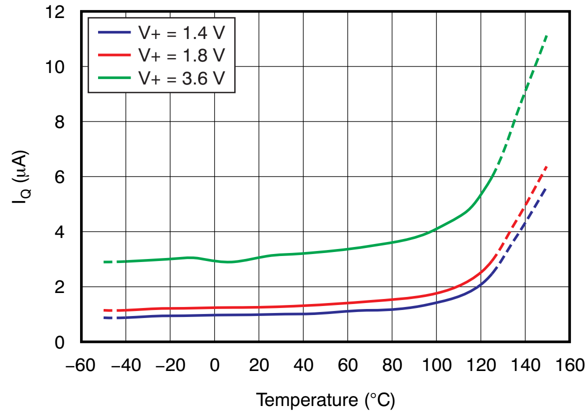


Figure 1. Quiescent Current vs Temperature (0.25 Conversions per Second)

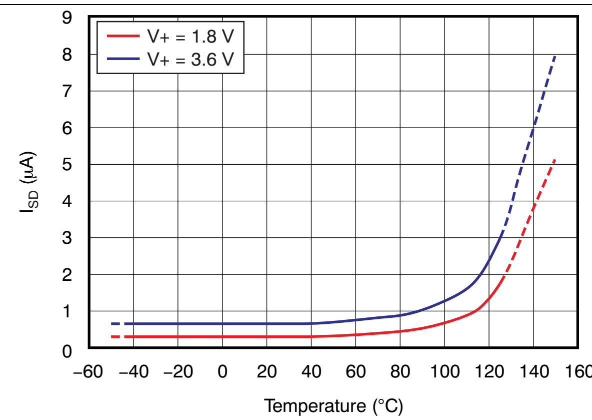


Figure 2. Shutdown Current vs Temperature

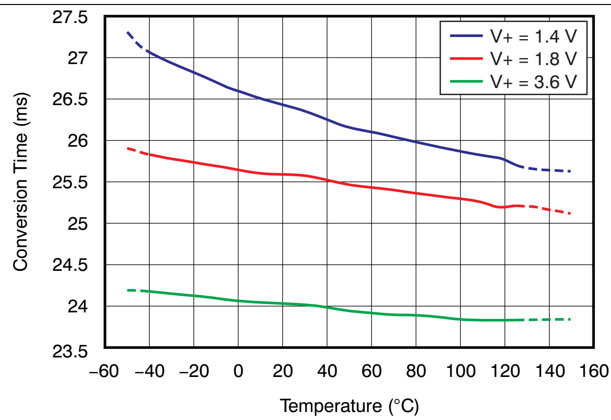


Figure 3. Conversion Time vs Temperature

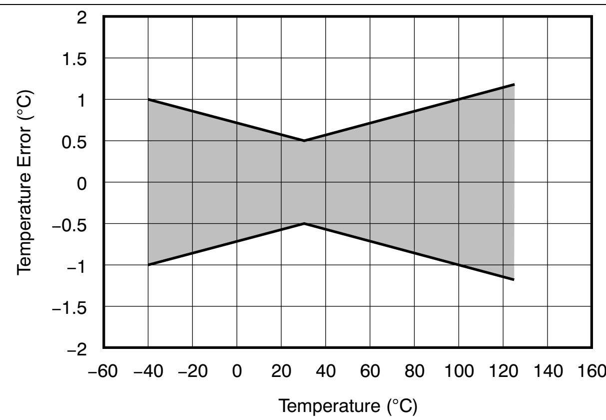


Figure 4. Temperature Error vs Temperature

7 Detailed Description

7.1 Overview

The TMP104 is a digital output temperature sensor in a wafer chip-scale package (WCSP) that is optimal for thermal management and thermal profiling. The TMP104 includes a SMAART wire interface that is capable of communicating in a daisy-chain with up to 16 devices on a single bus. The interface requires two pins from the host; the first device in the daisy-chain receives data from the host and the last device in the daisy-chain returns data to the host. In addition, the TMP104 has the capability of executing multiple device access (MDA) commands that allow multiple TMP104s to respond to a single global bus command. MDA commands reduce communication time and power in a bus that contains multiple TMP104 devices. The TMP104 is specified over a temperature range of –40ºC to +125ºC.

The TMP104 also has the capability of configuring the bus in a transparent mode, where the input from the host is sent directly to the next device in the chain without delay. Additionally, the TMP104 can disconnect the chain and create a serial communication controlled by each TMP104 on the bus, thereby allowing each device to have configurable addressing and interrupt capabilities. The input pin, RX, is a high-impedance node. The output pin, TX, has an internal push-pull output stage that can drive the host to GND or V+.

After an initialization sequence, each device on the bus is programmed with its own interface address that allows it to respond to its own address and also respond to general commands that permit the user to read or write to all of the devices on the bus without having to send its individual address and command to each individual device.

The temperature sensor in the TMP104 is the chip itself. Thermal paths run through the package bumps as well as the package. The lower thermal resistance of metal causes the bumps to provide the primary thermal path. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package from ambient air temperature. A thermally-conductive adhesive can help to achieve accurate surface temperature measurement.

7.2 Feature Description

7.2.1 Timeout Function

A timeout mechanism is implemented on the TMP104 to allow for re-synchronization of the SMAART wire interface if synchronization between the host and the TMP104 is lost for 28 ms (typical). If the timeout period expires between the calibration byte and the command byte, or between the command byte and any data byte, or between any data bytes, the TMP104 resets the SMAART wire interface circuitry so that it expects the baud rate calibration command to restart. Every time a byte is transmitted on the SMAART wire interface, this timeout period restarts.

7.2.2 Noise

The TMP104 is a very low-power device and generates very low noise on the supply bus. Applying a bypass capacitor to the V+ pin of the TMP104 can further reduce any noise the TMP104 might propagate to other components. C_F in Figure 5 should be greater than 0.1 µF.

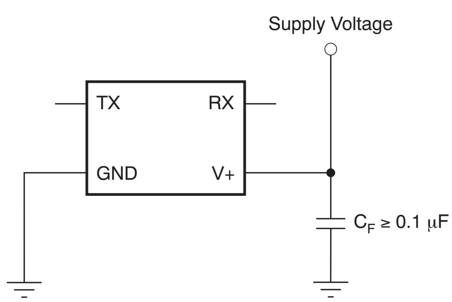


Figure 5. Noise Reduction

Feature Description (continued)

7.2.3 SMAART Wire™ Interface Timing Specifications

Figure 6 shows the key timing and jitter considerations for the SMAART wire interface. Table 1 lists the timing specifications for ensured, reliable operation. During a transaction, the baud rate must remain within ±1% of its initialization byte value; however, the baud rate can change from transaction to transaction. There is an allowed delay between each byte transfer of less than 28 ms, which is the bus inactivity timeout check for the TMP104 SMAART wire interface.

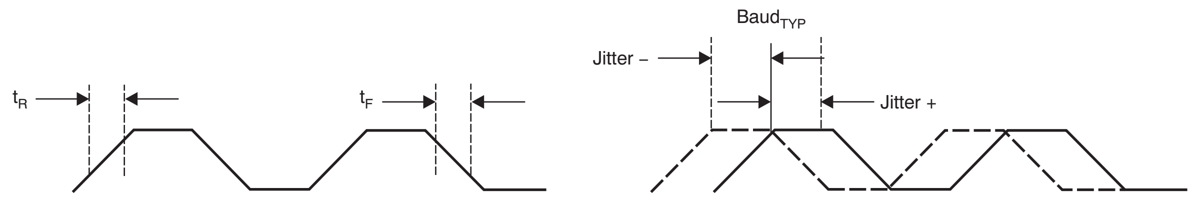


Figure 6. SMAART Wire™ Timing Diagram

Table 1. Timing Diagram Definitions

PARAMETER		MIN	MAX	UNIT
Baud		4.8 k	114 k	Bits/s
t_R	Clock/data rise time		0.5	%Baud
t_F	Clock/data fall time		0.5	%Baud
Jitter			±1	%Baud

7.3 Programming

7.3.1 Communication Protocol

Each communication of the SMAART wire protocol consists of 8-bit words, transferred least significant bit (LSB) first. Each 8-bit word begins with a *Start* bit that is logic low, and ends with a *Stop* bit that is logic high. By using a Start bit and Stop bit for each 8-bit word, the TMP104 can calibrate each word and maintain synchronous communication throughout the process. The host commences the communication by sending a Start bit followed by the calibration byte (55h), allowing the TMP104 to sync to the baud rate of the host, followed by the Stop bit. Then, another Start bit is sent, followed by the command register byte and a Stop bit. Finally, a third Start bit is sent followed by the data byte, where master sends data if the instruction is a write command, or the TMP104 breaks the chain and sends data if the instruction is a read command. The process finishes with a Stop bit. The sequence is shown in Table 2 and Figure 7.

Table 2. Communication Format

Start bit	Calibration	Stop bit	Start bit	Command byte	Stop bit	Start bit	Data byte	Stop bit

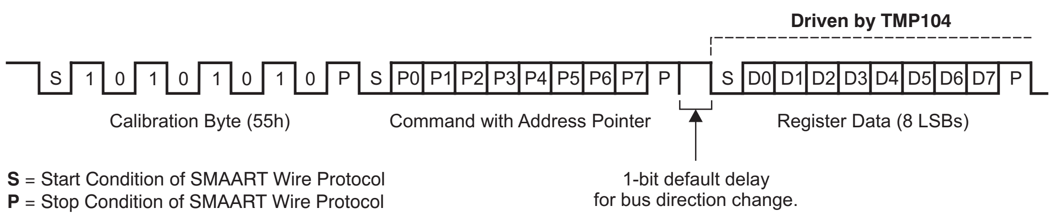


Figure 7. Generic Communication BitStream

The TMP104 has two dedicated pins for communication: TX and RX. Usually, these two pins are connected internally and the signal on the RX propagates to the TX; that is, the TMP104 works in a transparent mode. The TMP104 breaks this buffer configuration only when it must send data on the bus or during address assignment and alert procedures.

The TMP104 supports unique *address assignment* and *alert interrupt* procedures. There are general-call read and write commands that allow simultaneous reads or writes to all devices in the daisy-chain. The interface has built-in time-outs (typically 28 ms) that return the interface to a known state if communication is disrupted.

7.3.2 Command Register

Figure 8 shows the internal register structure of the TMP104. Communications between the registers are transferred through the interface in LSB-first order. The 8-bit Command Register, as shown in Table 3, is used to determine the type of instruction being addressed. These eight bits could either interpret a global instruction or an individual instruction, which is determined by the value of P7. When P7 = 0, the command byte interprets an individual instruction; when P7 = 1, the command byte interprets a global instruction.

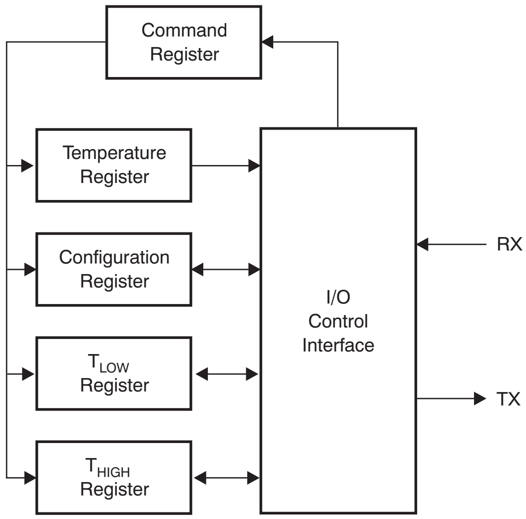


Figure 8. Internal Register Structure

Table 3. Command Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
GLB	IN3/ID3	IN2/ID2	IN1/ID1	IN0/ID0	P1	P0	R/W

7.3.3 Global Initialization and Address Assignment Sequence

At device power-up, every TMP104 in the daisy-chain is connected in transparent mode, as shown in Figure 9. The host must send the initialization command (P7-P0 = 10001100) in order for the bus to program its internal address depending on the number of devices on the bus.

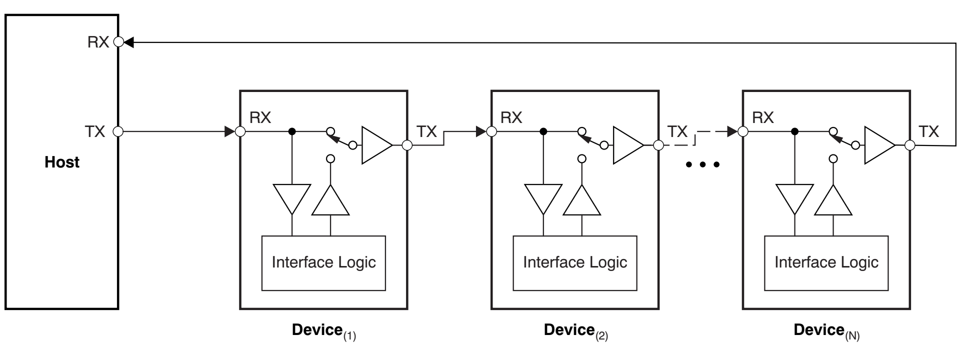


Figure 9. TMP104 Daisy-Chain: Bus Status at Start of Global Initialization

Each TMP104 in the chain interprets the initialization command byte and disconnects the chain, as shown in Figure 10. The host must then send the address assignment command, consisting of P7-P4 = 1001 and P3-P0 = 0000, where P3-P0 represents the address of the first device in the chain; this word is stored internally as its device ID. The first device increments the unit in the device address and then reconnects the bus, as shown in Figure 11. This address is then sent to the next device in the chain. Once all devices on the chain have received the respective addresses, the host receives the last programmed address on the chain + 1. The host can use this information to determine the total number of devices in the chain and the respective address of each device.

After the initialization sequence, every device can be addressed individually or through global commands. This global initialization sequence is a requirement and must be performed before any other communication.

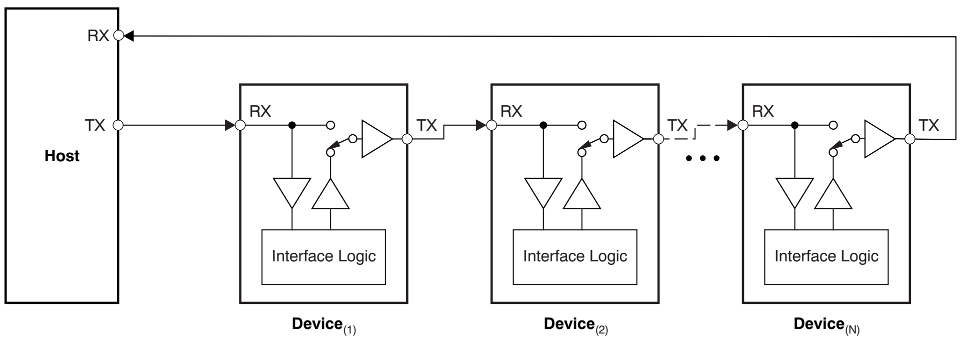


Figure 10. TMP104 Daisy-Chain: Bus Status at Start of Address Assignment

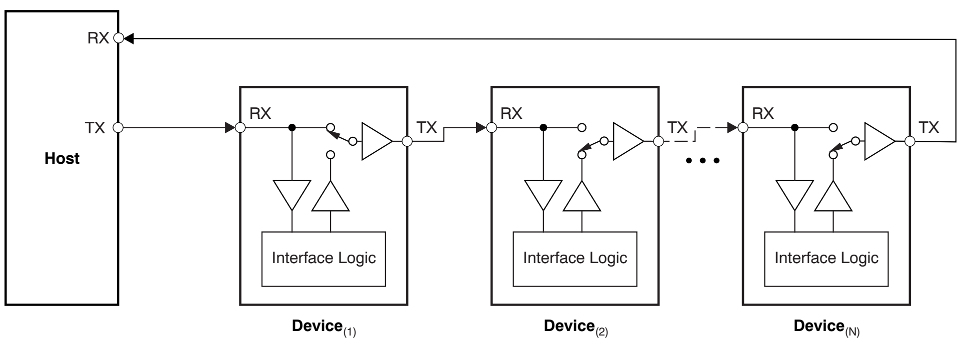


Figure 11. TMP104 Daisy-Chain: Bus Status After First Device Address Assignment

7.3.4 Global Read and Write

The host can initiate a global read or write command to all TMP104s in the daisy-chain by sending the read/write command, consisting of P7-P3 = 11110. P2-P1 indicate the data register pointer, as shown in Table 4, and P0 indicates read/write control. P0 = 0 indicates a global write command. The host must transfer one more byte of data for the register (indicated by bits P2-P1), and every TMP104 in the daisy-chain updates the appropriate register. P0 = 1 indicates a global read command. The TMP104 with the device ID of '0000' then breaks the bus connection, transmits the data from the register indicated by bits P2-P1, and then reconnects the bus. The TMP104 with the device ID of '0001' then repeats the same sequence, followed by the rest of the TMP104 devices in the daisy-chain.

Table 4. Pointer Addresses

P0	P0	REGISTER
0	0	Temperature register (read-only)
0	1	Configuration register (read/write)
1	0	T_{LOW} register (read/write)
1	1	T_{HIGH} register (read/write)

7.3.5 Global Clear Interrupt

The host can initiate a global clear interrupt command (P7-P0 = 10101001) to all TMP104s in the daisy-chain. Upon receiving this command, the TMP104 disables future interrupts (D7 in the Configuration Register is set to '0'). If a TMP104 has previously broken the bus connection and sent an interrupt (logic low on the bus), it now stops holding the bus low. The device sends the baud rate calibration command and clear interrupt command to the next TMP104 in the chain, and then reconnects the bus. In the case of multiple devices having active interrupts, the clear interrupt command propagates through the daisy-chain, disables all interrupts, and reconnects the bus across all devices.

7.3.6 Global Software Reset

The host can initiate a global software reset command (P7-P0 = 10110100) to all TMP104s in the daisy-chain. Upon receiving this command, the TMP104 resets its internal registers except for the device ID, which is not reset, and reconnects the bus. If the bus is broken before the initiation of this command, all TMP104s before the broken bus point receive the command. If the host intends to initiate a global software reset across all TMP104s in the chain, this command must be transmitted multiple times until it echoes back to the host.

7.3.7 Individual Read and Write

The host can initiate an individual read/write command to a particular TMP104 in the daisy-chain by sending the read/write command. The read/write command consists of these parameters:

- P7 = 0
- P6-P3 = the device ID
- P2-P1 = the data register pointer; see Table 4
- P0 = indicates read/write control

P0 = 0 indicates an individual write command; the host must transfer one more byte of data for the register indicated by bits P2-P1. The TMP104 in the daisy-chain that corresponds to the device ID noted by bits P6-P3 then updates the appropriate register. P0 = 1 indicates an individual read command; as shown in Figure 12, the TMP104 in the daisy-chain that corresponds to the device ID pointed by bits P6-P3 then breaks the bus, transmits the data from the register pointed by bits P2-P1, and reconnects the bus.

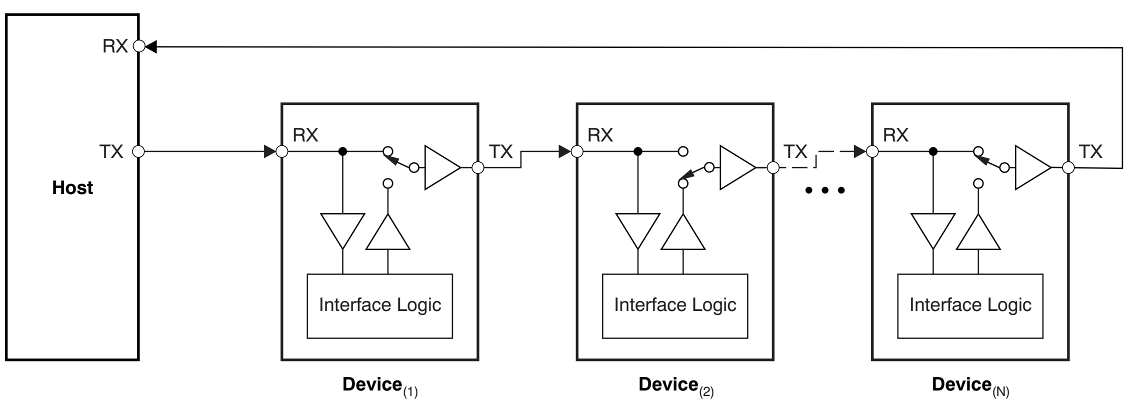


Figure 12. TMP104 Daisy-Chain: Bus Status During Individual Read Operation of Second Device

7.4 Register Maps

7.4.1 Temperature Register

The Temperature Register of the TMP104 is configured as an 8-bit, read-only register that stores the output of the most recent conversion. A single byte must be read to obtain data, and is described in Table 5. The data format for temperature is summarized in Table 6. One LSB equals 1°C.

Table 5. Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T7	T6	T5	T4	T3	T2	T1	T0

Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature Register reads 0°C until the first conversion is complete.

Table 6. 8-Bit Temperature Data Format(1)

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111	7F
127	0111 1111	7F
100	0110 0100	64
80	0101 0000	50
75	0100 1011	4B
50	0011 0010	32
25	0001 1001	19
0	0000 0000	00
–1	1111 1111	FF
–25	1110 0111	E7
–55	1100 1001	C9

(1) The resolution for the analog-to-digital converter (ADC) is 1°C/count, where *count* is equal to the digital output of the ADC.

For positive temperatures (for example, +50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code, left-justified format. Denote a positive number with most significant bit (MSB) = 0.

Example: (+50°C)/(1°C/count) = 50 = 32h = 0011 0010

For negative temperatures (for example, –25°C):

Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Denote a negative number with MSB = 1.

Example: (|–25°C|)/(1°C/count) = 25 = 19h = 0001 1001

Twos complement format: 1110 0110 + 1 = 1110 0111

7.4.2 Configuration Register

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed LSB first. The format and power-up/reset value of the Configuration Register is shown in Table 7.

Table 7. Configuration and Power-Up/Reset Format

D7	D6	D5	D4	D3	D2	D1	D0
INT_EN	CR1	CR0	FH	FL	LC	M1	M0
0	0	0	0	0	0	1	0

7.4.2.1 Temperature Watchdog Function (FH, FL)

The TMP104 contains a watchdog function that monitors device temperature and compares the result to the values stored in the temperature limit registers (T_{HIGH} and T_{LOW}) in order to determine if the device temperature is within these set limits. If the temperature of the TMP104 becomes greater than the value in the T_{HIGH} register, then the flag-high bit (FH) in the Configuration Register is set to '1'. If the temperature falls below value in the T_{LOW} register, then the flag-low bit (FL) is set to '1'. If both flag bits remain '0', then the temperature is within the temperature *window* set by the temperature limit registers, as shown in Figure 13.

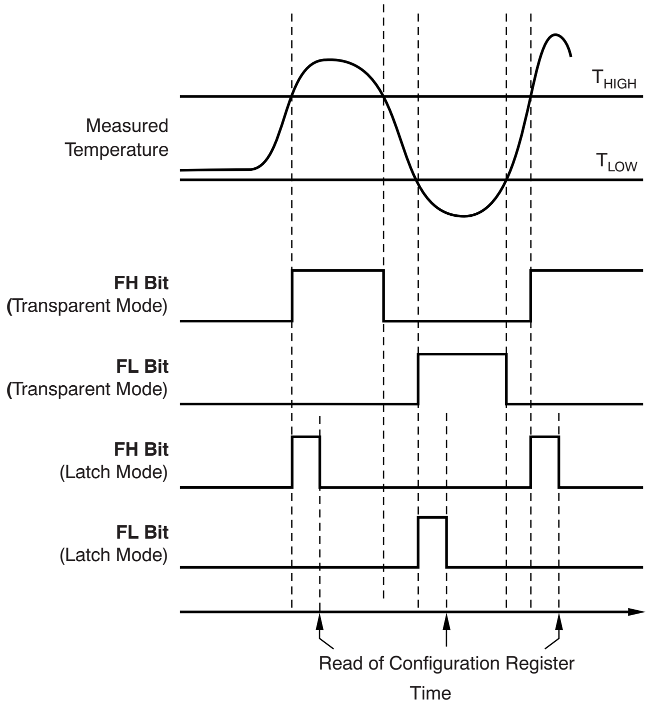


Figure 13. Temperature Flag Functional Diagram

The latch bit (LC) in the Configuration Register is used to latch the value of the flag bits (FH and FL) until the master issues a read command to the Configuration Register. The flag bits are set to '0' if a read command is received by the TMP104, or if LC = 0 and the temperature is within the temperature limits. The power-on default values for these bits are FH = 0, FL = 0, and LC = 0.

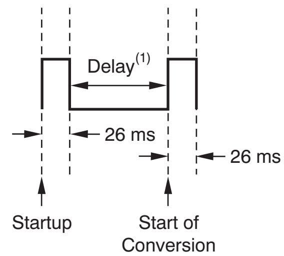
7.4.2.2 Conversion Rate (CR1, CR0)

The conversion rate bits (CR1 and CR0), located in the Configuration Register, configure the TMP104 for conversion rates of 8 Hz, 4 Hz, 1 Hz, or 0.25 Hz (default). The TMP104 has a typical conversion time of 26 ms. To achieve different conversion rates, the TMP104 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 8 shows the settings for CR1 and CR0.

Table 8. Conversion Rate Settings

CR1	CR0	CONVERSION RATE
0	0	0.25 Hz (default)
0	1	1 Hz
1	0	4 Hz
1	1	8 Hz

After power-up or general-call reset, the TMP104 immediately starts a conversion, as shown in Figure 14. The first result is available after 26 ms (typical). The active quiescent current during conversion is 40 μA (typical at +25°C, V+ = 1.8 V). The quiescent current during delay is 1.0 μA (typical at +25°C, V+ = 1.8 V).



(1) Delay is set by CR1 and CR0.

Figure 14. Conversion Start

7.4.2.3 Conversion Modes

7.4.2.3.1 Shutdown Mode (M1 = 0, M0 = 0)

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 μA. Shutdown mode is enabled when bits M1 and M0 (in the Configuration Register) read '00'. The device shuts down when the current conversion is completed.

7.4.2.3.2 One-Shot Mode (M1 = 0, M0 = 1)

The TMP104 features a One-Shot Temperature Measurement mode. When the device is in Shutdown mode, writing '01' to bits M1 and M0 starts a single temperature conversion. During the conversion, bits M1 and M0 read '01'. The device returns to the shutdown state at the completion of the single conversion. After the conversion, bits M1 and M0 read '00'. This feature is useful for reducing power consumption in the TMP104 when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP104 can achieve a higher conversion rate. A single conversion typically takes 26 ms and an individual read can take place in less than 300 μs. When using One-Shot mode, 30 or more conversions per second are possible.

7.4.2.3.3 Continuous Conversion Mode (M1 = 1)

When the TMP104 is in Continuous Conversion mode (M1 = 1), continuous conversions are performed at a rate determined by the conversion rate bits, CR1 and CR0 (in the Configuration Register). The TMP104 performs a single conversion, and then powers down and waits for the appropriate delay set by CR1 and CR0. See Table 8 for CR1 and CR0 settings.

7.4.2.4 Interrupt Functionality (INT_EN)

The TMP104 interrupts the host by disconnecting the bus and issuing an interrupt request by holding the bus low if all of these conditions are met, as shown in Figure 15:

- INT_EN in the Configuration Register is set to '1';
- The temperature result is higher than the value in the T_{HIGH} register or lower than the value in the T_{LOW} register (as indicated by a '1' in either FL or FH);
- The bus is logic high and idle for more than 28 ms.

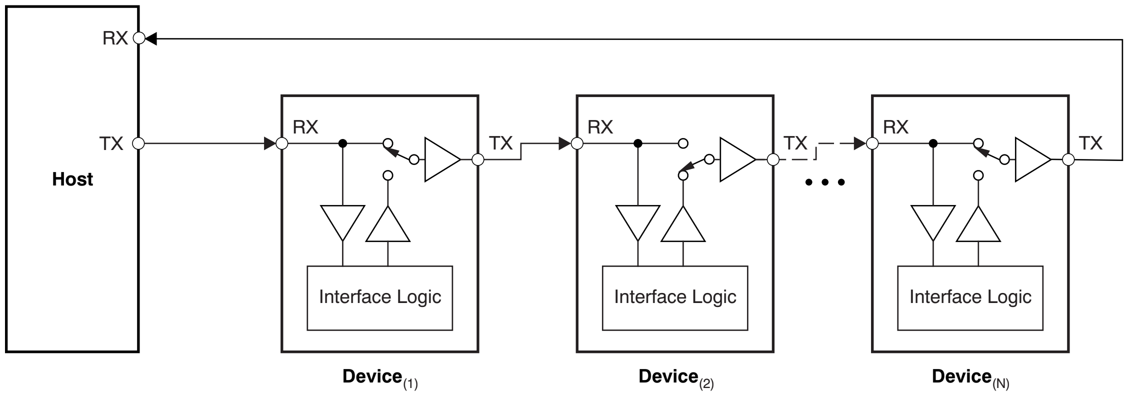


Figure 15. TMP104 Daisy-Chain: Bus Status During an Interrupt Request (Logic Low) From Second Device

The interrupt on the bus is latched regardless of the status of LC. Writing a '1' to INT_EN automatically sets the LC bit. The TMP104 holds the bus low until one of the following events happen:

- Global Interrupt Clear command received;
- Global Software Reset command received;
- A power-on reset event occurs.

Each of these events clears INT_EN; the TMP104 does not issue future interrupts until the host writes '1' to bit D7 in the Configuration Register to re-enable future interrupts.

In a system with enabled interrupts, it is possible for a TMP104 on the bus to issue an interrupt at the same time that the host starts a communication sequence. To avoid this scenario, it is recommended that the host should check the status on the receiving side of the bus after transmitting the calibration byte. If it is '1', then the host can continue with the communication. If it is '0', one of the TMP104 devices on the bus is issuing an alert and the host must transmit a Global Interrupt Clear command.

7.4.3 Temperature Limit Registers

The T_{HIGH} and T_{LOW} registers are used to store the temperature limit thresholds for the TMP104 watchdog function. At the end of each temperature measurement, the TMP104 compares the temperature results to each of these limits. If the temperature result is greater than the T_{HIGH} limit, then the FH bit in the Configuration Register is set to '1'. If the temperature result is less than the T_{LOW} limit, then the FL bit in the Configuration Register is set to '1'; see Figure 13.

Table 9 and Table 10 describe the format for the T_{HIGH} and T_{LOW} registers. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = +60°C and T_{LOW} = –10°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

Table 9. T_{HIGH} Register

D7	D6	D5	D4	D3	D2	D1	D0
H7	H6	H5	H4	H3	H2	H1	H0

Table 10. T_{LOW} Register

D7	D6	D5	D4	D3	D2	D1	D0
L7	L6	L5	L4	L3	L2	L1	L0

8 器件和文档支持

8.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

8.3 商标

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8.4 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP104YFFR	ACTIVE	DSBGA	YFF	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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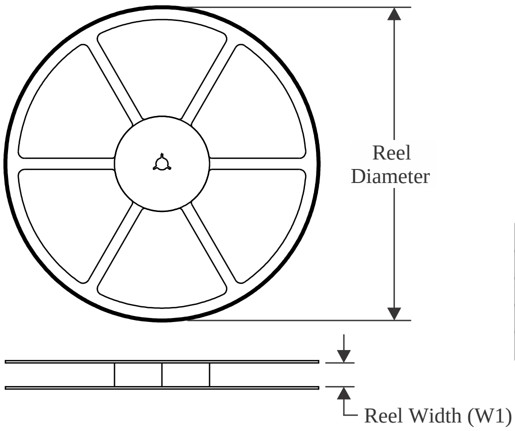
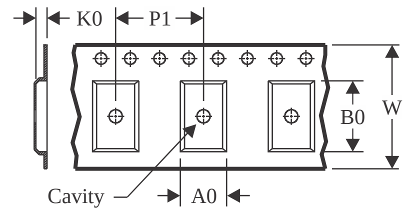
TAPE AND REEL INFORMATION

REEL DIMENSIONS

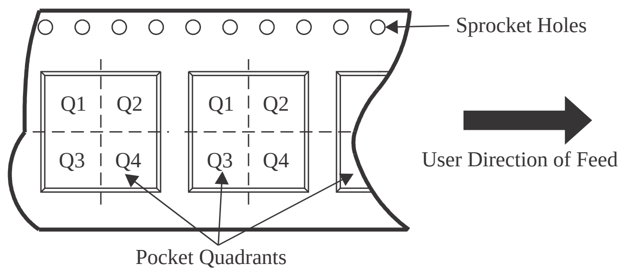


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

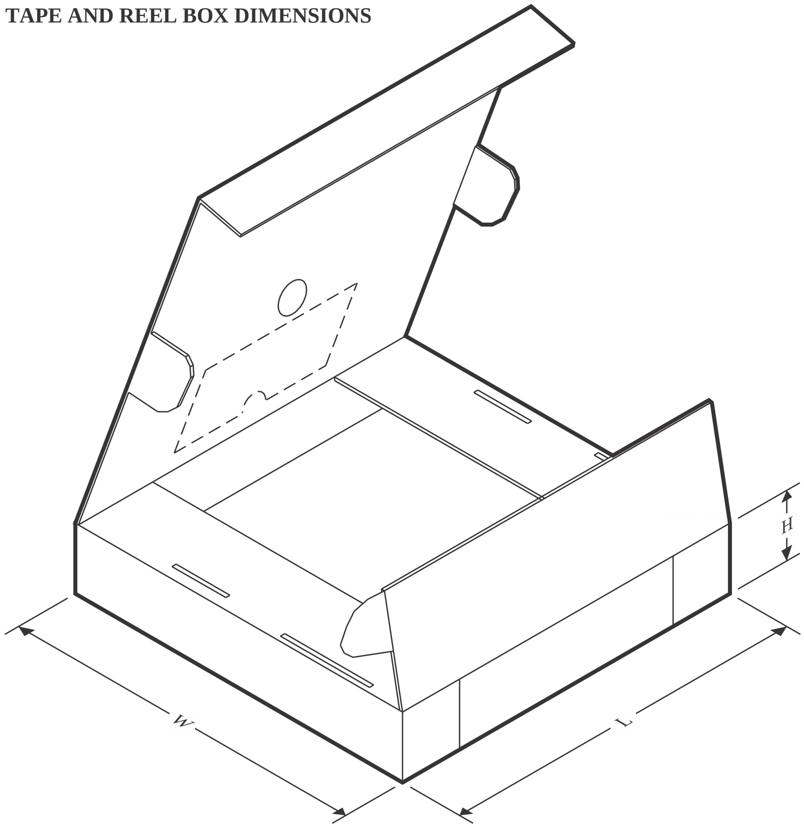
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

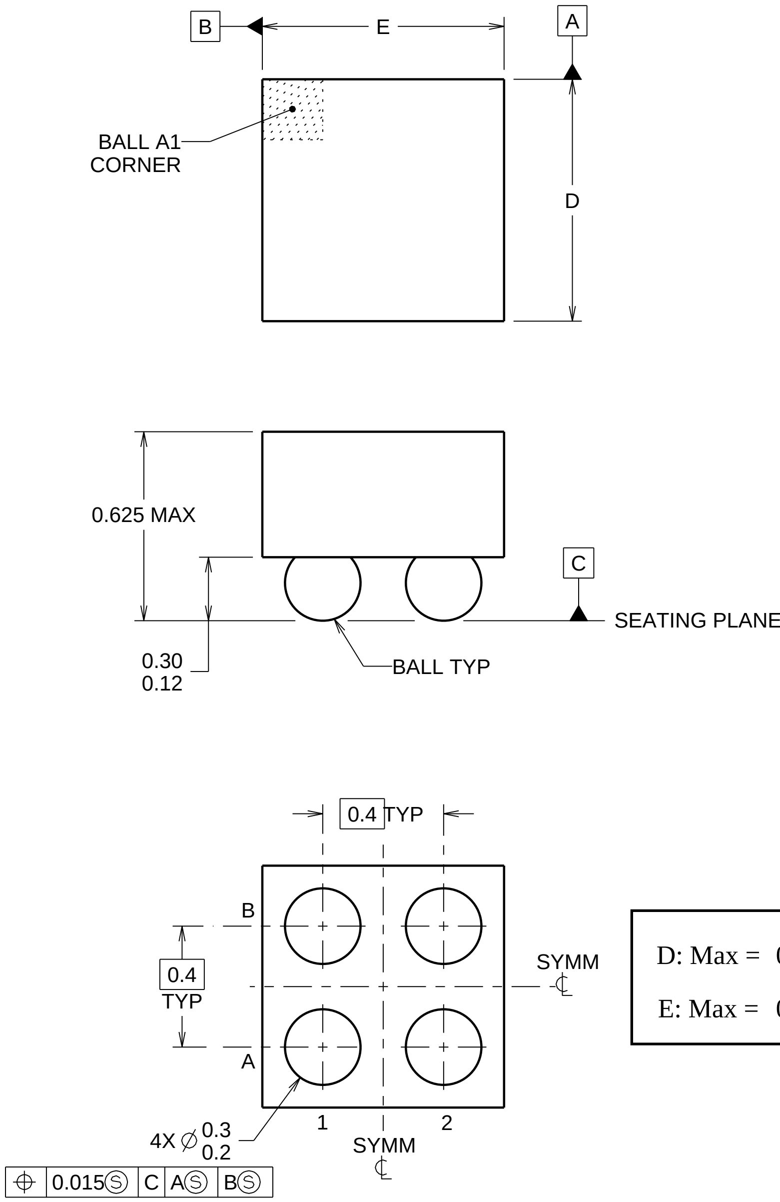
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP104YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.86	1.06	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP104YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0



D: Max = 0.99 mm, Min = 0.93 mm

E: Max = 0.79 mm, Min = 0.73 mm

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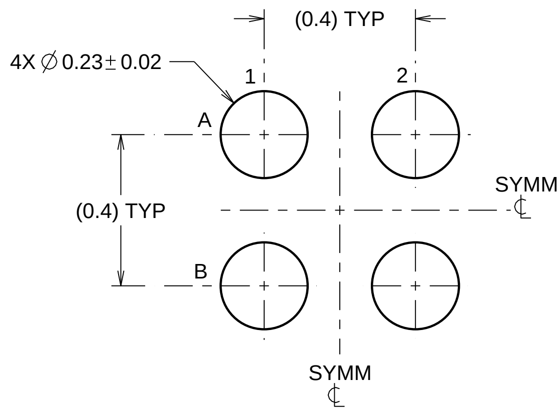
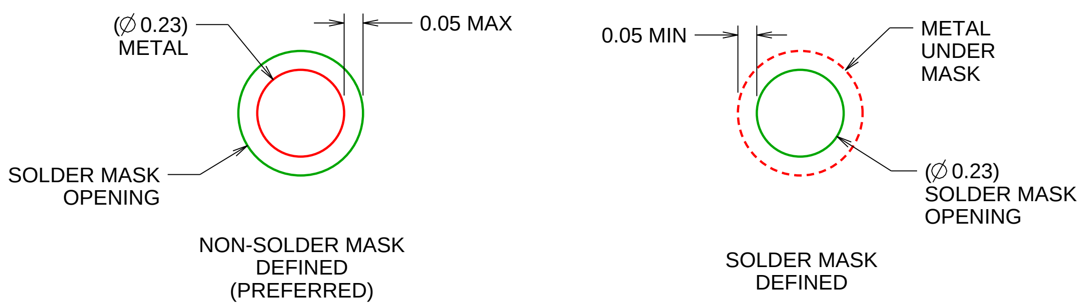
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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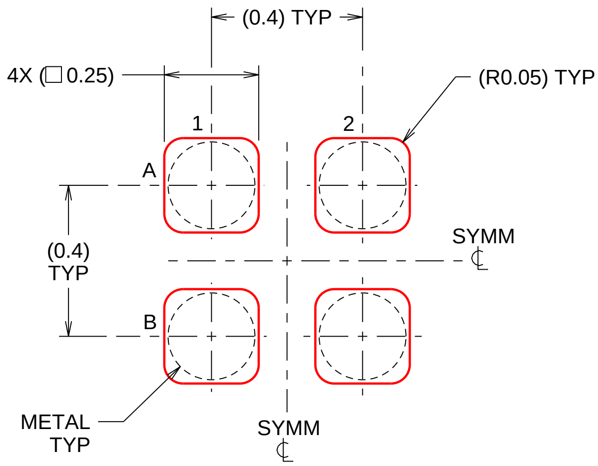
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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