SN74LVC1T45-Q1 汽车类 1.65V 至 5.5V 一位双电源电平转换器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
  - 器件人体放电模型 (HBM) 静电防护 (ESD) 分类等级 H2
  - 器件 CDM ESD 分类等级 C3B
- 完全可配置的双轨设计，支持各个端口在 1.65V 至 5.5V 的整个电源电压范围内运行
- V_{CC} 隔离特性 – 如果任何一个 V_{CC} 输入接地 (GND)，则两个端口均处于高阻抗状态
- 以 V_{CCA} 为基准的 DIR 输入电路
- 电压为 3.3V 时，输出驱动为 ±24mA
- I_{off} 支持局部断电模式运行
- 最大数据速率：
  - 420Mbps（3.3V 至 5V 转换）
  - 210Mbps（转换至 3.3 V）
  - 140Mbps（转换至 2.5 V）
  - 75Mbps（转换至 1.8 V）

2 应用

- 音响主机
- ADAS – 摄像头
- 远程信息处理系统

3 说明

SN74LVC1T45-Q1 器件是一款采用两个独立可配置电源轨的一位同相总线收发器。A 端口旨在跟踪 V_{CCA}。V_{CCA} 可接受从 1.65V 到 5.5V 范围内的任意电源电压。B 端口旨在跟踪 V_{CCB}。V_{CCB} 可接受从 1.65 至 5.5V 间的任一电源电压值。这可实现 1.8V，2.5V，3.3V 和 5V 电压节点间的通用低压双向转换。

SN74LVC1T45-Q1 器件是一款一位同相电平转换器，采用完全可配置的双轨设计，支持每个端口在 1.65V 至 5.5V 的完整电源电压范围内运行。它非常适合需要双向宽转换范围的应用。

SN74LVC1T45-Q1 旨在实现通过 V_{CCA} 对 DIR 输入供电。

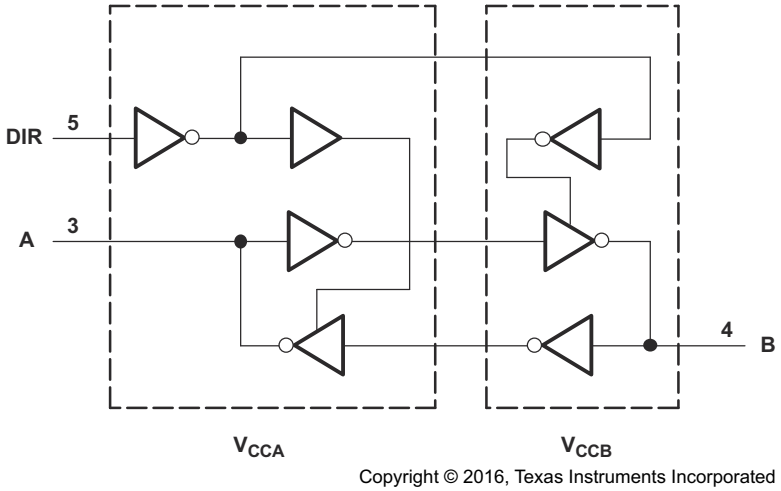
该器件完全符合使用 I_{off} 的部分断电应用的规范要求。I_{off} 电路禁用输出，从而可防止其断电时破坏性电流从该器件回流。

V_{CC} 隔离特性可确保如果任何一个 V_{CC} 输入接地，则两个端口都处于高阻抗状态。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
SN74LVC1T45-Q1	DCK (SC70, 6)	1.25mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

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4 Revision History

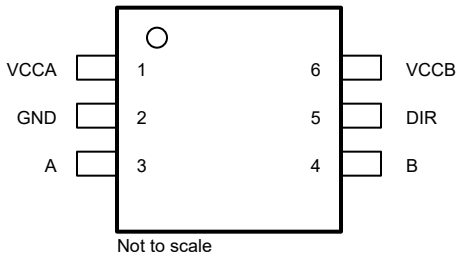
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (July 2017) to Revision E (December 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated the thermals in the *Thermal Information* section	5
• Updated the *Switching Characterisitcs* sections: extended some minimum specifications for lower delays	7

Changes from Revision C (September 2016) to Revision D (July 2017)	Page
• Added Junction temperature, T_J in *Absolute Maximum Ratings*	4
• Added revised steps for power-up sequence in *Power Supply Recommendations*	16

Changes from Revision B (September 2012) to Revision C (September 2016)	Page
• 将数据表标题从 SN74LVC1T45-Q1 “具有可配置电压转换和三态输出的一位双电源总线收发器”更改为 SN74LVC1T45-Q1 “1.65V 至 5.5V 一位双电源电平转换器”	1
• 添加了 *器件信息* 表、*ESD 等级* 表、*特性说明* 部分、*器件功能模式* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分	1
• 删除了“订购信息”表；请参阅数据表末尾的 POA	1

5 Pin Configuration and Functions



See mechanical drawings for dimensions.

图 5-1. DCK Package, 6-Pin SC70 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A	3	I/O	Output level depends on V_{CC1} voltage
B	4	I/O	Input threshold value depends on V_{CC2} voltage
DIR	5	I	GND (low level) determines B-port to A-port direction
GND	2	G	Device GND
V_{CCA}	1	P	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
V_{CCB}	6	P	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CCA}, V_{CCB}		– 0.5	6.5	V
Input voltage, V_I (2)		– 0.5	6.5	V
Voltage applied to any output in the high-impedance or power-off state, V_O (2)		– 0.5	6.5	V
Voltage applied to any output in the high or low state, V_O (2) (3)	A port	– 0.5	V_{CCA} + 0.5	V
	B port	– 0.5	V_{CCB} + 0.5	
Input clamp current, I_{IK} (V_I < 0)			– 50	mA
Output clamp current, I_{OK} (V_O < 0)			– 50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See(1) (2) (3)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		1.65	5.5	V
V_{CCB}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage, data inputs(4)	V_{CCI} = 1.65 V to 1.95 V	V_{CCI} × 0.65		V
		V_{CCI} = 2.3 V to 2.7 V	1.7		
		V_{CCI} = 3 V to 3.6 V	2		
		V_{CCI} = 4.5 V to 5.5 V	V_{CCI} × 0.7		
V_{IL}	Low-level input voltage, data inputs(4)	V_{CCI} = 1.65 V to 1.95 V		V_{CCI} × 0.35	V
		V_{CCI} = 2.3 V to 2.7 V		0.7	
		V_{CCI} = 3 V to 3.6 V		0.8	
		V_{CCI} = 4.5 V to 5.5 V		V_{CCI} × 0.3	
V_{IH}	High-level input voltage, DIR (referenced to V_{CCA})(5)	V_{CCI} = 1.65 V to 1.95 V	V_{CCA} × 0.65		V
		V_{CCI} = 2.3 V to 2.7 V	1.7		
		V_{CCI} = 3 V to 3.6 V	2		
		V_{CCI} = 4.5 V to 5.5 V	V_{CCA} × 0.7		

6.3 Recommended Operating Conditions (continued)

See(1) (2) (3)

			MIN	MAX	UNIT
V_{IL}	Low-level input voltage, DIR (referenced to V_{CCA})(5)	V_{CCI} = 1.65 V to 1.95 V		V_{CCA} × 0.35	V
		V_{CCI} = 2.3 V to 2.7 V		0.7	
		V_{CCI} = 3 V to 3.6 V		0.8	
		V_{CCI} = 4.5 V to 5.5 V		V_{CCA} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CCO}	V
I_{OH}	High-level output current	V_{CCO} = 1.65 V to 1.95 V		–4	mA
		V_{CCO} = 2.3 V to 2.7 V		–8	
		V_{CCO} = 3 V to 3.6 V		–24	
		V_{CCO} = 4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current	V_{CCO} = 1.65 V to 1.95 V		4	mA
		V_{CCO} = 2.3 V to 2.7 V		8	
		V_{CCO} = 3 V to 3.6 V		24	
		V_{CCO} = 4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs, V_{CCI} = 1.65 V to 1.95 V		20	ns/V
		Data inputs, V_{CCI} = 2.3 V to 2.7 V		20	
		Data inputs, V_{CCI} = 3 V to 3.6 V		10	
		Data inputs, V_{CCI} = 4.5 V to 5.5 V		5	
		Control inputs, V_{CCI} = 1.65 V to 5.5 V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to assure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1T45-Q1 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	139.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72	°C/W
ψ_{JT}	Junction-to-top characterization parameter	54.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range with all limits at T_A = –40°C to 125°C (unless otherwise noted)(1) (2)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$	I_{OH} = –100 µA, V_{CCA} = 1.65 V to 4.5 V, V_{CCB} = 1.65 V to 4.5 V		V_{CCO} – 0.1			V
		I_{OH} = –4 mA, V_{CCA} = 1.65 V, V_{CCB} = 1.65 V		1.2			
		I_{OH} = –8 mA, V_{CCA} = 2.3 V, V_{CCB} = 2.3 V		1.9			
		I_{OH} = –24 mA, V_{CCA} = 3 V, V_{CCB} = 3 V		2.3			
		I_{OH} = –32 mA, V_{CCA} = 4.5 V, V_{CCB} = 4.5 V		3.8			
V_{OL}	$V_I = V_{IL}$	I_{OL} = 100 µA, V_{CCA} = 1.65 V to 4.5 V, V_{CCB} = 1.65 V to 4.5 V				0.1	V
		I_{OL} = 4 mA, V_{CCA} = 1.65 V, V_{CCB} = 1.65 V				0.45	
		I_{OL} = 8 mA, V_{CCA} = 2.3 V, V_{CCB} = 2.3 V				0.4	
		I_{OL} = 24 mA, V_{CCA} = 3 V, V_{CCB} = 3 V				0.65	
		I_{OL} = 32 mA, V_{CCA} = 4.5 V, V_{CCB} = 4.5 V				0.65	
I_I	DIR at V_I = V_{CCA} or GND, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V		T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±4	
I_{off}	V_I or V_O = 0 to 5.5 V	A port at V_{CCA} = 0 V, V_{CCB} = 0 to 5.5 V	T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±10	
		B port at V_{CCA} = 0 to 5.5 V, V_{CCB} = 0 V	T_A = 25°C			±1	
			T_A = –40°C to 125°C			±10	
I_{OZ}	A or B port at V_O = V_{CCO} or GND, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V		T_A = 25°C			±1	µA
			T_A = –40°C to 125°C			±10	
I_{CCA}	V_I = V_{CCI} or GND, I_O = 0	V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V				10	µA
		V_{CCA} = 5.5 V, V_{CCB} = 0 V				4	
		V_{CCA} = 0 V, V_{CCB} = 5.5 V				–10	
I_{CCB}	V_I = V_{CCI} or GND, I_O = 0	V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V				10	µA
		V_{CCA} = 5.5 V, V_{CCB} = 0 V				–10	
		V_{CCA} = 0 V, V_{CCB} = 5.5 V				4	
I_{CCA} + I_{CCB}	V_I = V_{CCI} or GND, I_O = 0, V_{CCA} = 1.65 V to 5.5 V, V_{CCB} = 1.65 V to 5.5 V					20	µA
ΔI_{CCA}	V_{CCA} = 3 V to 5.5 V, V_{CCB} = 3 V to 5.5 V	A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open				50	µA
		DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND				50	
ΔI_{CCB}	B port at V_{CCB} – 0.6 V, DIR at GND, A port = open, V_{CCA} = 3 V to 5.5 V, V_{CCB} = 3 V to 5.5 V					50	µA
C_i	DIR at V_I = V_{CCA} or GND, T_A = 25°C, V_{CCA} = 3.3 V, V_{CCB} = 3.3 V				2.5		pF
C_{io}	A or B port at V_O = $V_{CCA/B}$ or GND, T_A = 25°C, V_{CCA} = 3.3 V, V_{CCB} = 3.3 V				6		pF
C_{pdA} (3)	C_L = 0 pF, f = 10 MHz, t_r = t_f = 1 ns	A-port input, B-port output	V_{CCA} = V_{CCB} = 1.8 V		3		pF
			V_{CCA} = V_{CCB} = 2.5 V		4		
			V_{CCA} = V_{CCB} = 3.3 V		4		
			V_{CCA} = V_{CCB} = 5 V		4		
		B-port input, A-port output	V_{CCA} = V_{CCB} = 1.8 V		18		
			V_{CCA} = V_{CCB} = 2.5 V		19		
			V_{CCA} = V_{CCB} = 3.3 V		20		
			V_{CCA} = V_{CCB} = 5 V		21		

6.5 Electrical Characteristics (continued)

over operating free-air temperature range with all limits at T_A = –40°C to 125°C (unless otherwise noted)(1) (2)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
C_{pdB} (3)	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	A-port input, B-port output	$V_{CCA} = V_{CCB}$ = 1.8 V		18		pF
			$V_{CCA} = V_{CCB}$ = 2.5 V		19		
			$V_{CCA} = V_{CCB}$ = 3.3 V		20		
			$V_{CCA} = V_{CCB}$ = 5 V		21		
		B-port input, A-port output	$V_{CCA} = V_{CCB}$ = 1.8 V		3		
			$V_{CCA} = V_{CCB}$ = 2.5 V		4		
			$V_{CCA} = V_{CCB}$ = 3.3 V		4		
			$V_{CCA} = V_{CCB}$ = 5 V		4		

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) Power dissipation capacitance per transceiver

6.6 Switching Characteristics: V_{CCA} = 1.8 V ±0.15 V

over operating free-air temperature range (unless otherwise noted; see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	20.7	2.2	13.3	1.7	11.3	1.4	10.2	ns
t_{PHL}			2.8	17.3	2.2	11.5	1.8	10.1	1.7	10	
t_{PLH}	B	A	3	20.7	2.3	19	2.1	18.5	1.9	18.1	ns
t_{PHL}			2.8	17.3	2.1	15.9	2	15.6	1.8	15.2	
t_{PHZ}	DIR	A	5.2	22.7	4.8	21.5	4.7	21.4	5.1	20.1	ns
t_{PLZ}			2.3	13.5	2.1	13.5	2.4	13.7	3.1	13.9	
t_{PHZ}	DIR	B	5.2	27.9	4.9	14.5	3.6	13.3	2.3	11.2	ns
t_{PLZ}			4.2	19	2.2	12.2	2.3	11.4	2	9.4	
t_{PZH} (1)	DIR	A		39.7		31.2		29.9		27.5	ns
t_{PZL} (1)				45.2		30.4		28.9		26.4	
t_{PZH} (1)	DIR	B		34.2		26.8		25		24.1	ns
t_{PZL} (1)				40.7		33		31.5		30.1	

(1) The enable time is a calculated value, derived using the formula shown in 节 8.1.1.

6.7 Switching Characteristics: V_{CCA} = 2.5 V ±0.2 V

over operating free-air temperature range (unless otherwise noted; see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	19	1.5	11.5	1.3	9.4	1.1	8.1	ns
t_{PHL}			2.1	15.9	1.4	10.5	1.3	8.4	0.9	7.6	
t_{PLH}	B	A	2.2	13.3	1.5	11.5	1.4	11	1	10.5	ns
t_{PHL}			2.2	11.5	1.4	10.7	1.3	10	0.9	9.2	
t_{PHZ}	DIR	A	3	11.1	3.1	11.1	2.8	11.1	3.2	11.1	ns
t_{PLZ}			1.3	8.9	1.3	8.9	1.3	8.9	1	8.8	
t_{PHZ}	DIR	B	5.2	26.7	4.1	14.4	3.9	13.2	2.4	10.1	ns
t_{PLZ}			3.9	21.9	3.2	12.6	2.8	11.4	1.8	8.3	

6.7 Switching Characteristics: V_{CCA} = 2.5 V ±0.2 V (continued)

over operating free-air temperature range (unless otherwise noted; see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PZH} (1)	DIR	A		35.2		24.1		22.4		18.8	ns
t_{PZL} (1)				38.2		24.9		23.2		19.3	
t_{PZH} (1)	DIR	B		27.9		20.4		18.3		16.9	ns
t_{PZL} (1)				27		21.6		19.5		18.7	

6.8 Switching Characteristics: V_{CCA} = 3.3 V ±0.3 V

over operating free-air temperature range (unless otherwise noted; see 图 7-1)

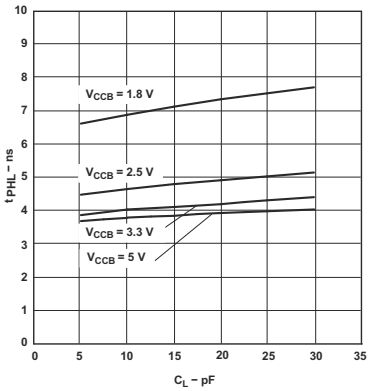
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	18.5	1.4	11	0.7	8.8	0.7	7.4	ns
t_{PHL}			2	15.6	1.3	10	0.8	8	0.7	7	
t_{PLH}	B	A	1.7	11.3	1.3	9.4	0.7	8.8	0.6	8.4	ns
t_{PHL}			1.8	10.1	1.3	8.4	0.8	8	0.7	7.5	
t_{PHZ}	DIR	A	2.9	10.3	3	10.3	2.8	10.3	3.4	10.3	ns
t_{PLZ}			1.8	8.6	1.6	8.6	2.2	8.7	2.2	8.7	
t_{PHZ}	DIR	B	5.4	27.5	3.9	13.1	2.9	11.8	2.4	9.8	ns
t_{PLZ}			3.3	17.5	2.9	10.8	2.4	10.1	1.7	7.9	
t_{PZH} (1)	DIR	A		26.8		20.2		18.9		16.3	ns
t_{PZL} (1)				37.6		21.5		19.8		17.3	
t_{PZH} (1)	DIR	B		27.1		19.6		17.5		16.1	ns
t_{PZL} (1)				25.9		20.3		18.3		17.3	

6.9 Switching Characteristics: V_{CCA} = 5 V ±0.5 V

over operating free-air temperature range (unless otherwise noted; see 图 7-1)

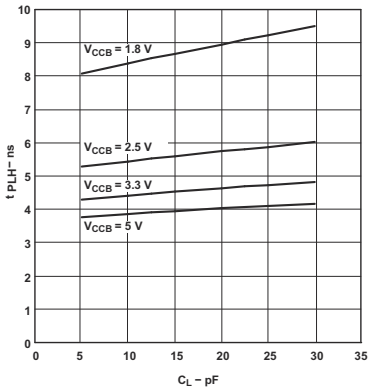
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		V_{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	18.1	1	10.5	0.6	8.4	0.5	6.9	ns
t_{PHL}			1.8	15.2	0.9	9.2	0.7	7.5	0.5	6.5	
t_{PLH}	B	A	1.4	10.2	1	8.1	0.7	7.4	0.5	6.9	ns
t_{PHL}			1.7	10	0.9	7.6	0.7	7	0.5	6.5	
t_{PHZ}	DIR	A	2.1	8.4	2.2	8.4	2.2	8.5	2.2	8.4	ns
t_{PLZ}			0.9	6.8	1	6.8	0.7	6.7	0.7	6.7	
t_{PHZ}	DIR	B	4.8	26.2	2.5	14.8	1	11.5	2.5	9.5	ns
t_{PLZ}			3.2	17.8	2.5	10.4	2.5	10	1.6	7.5	
t_{PZH} (1)	DIR	A		28		18.5		17.4		14.4	ns
t_{PZL} (1)				36.2		22.4		18.5		16	
t_{PZH} (1)	DIR	B		24.9		17.3		15.1		13.6	ns
t_{PZL} (1)				23.6		17.6		16		14.9	

6.10 Typical Characteristics



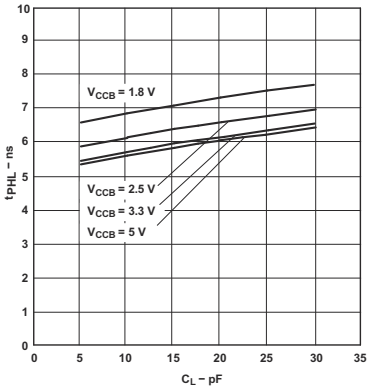
T_A = 25°C, V_{CCA} = 1.8 V

图 6-1. Typical Propagation Delay (A to B) vs Load Capacitance



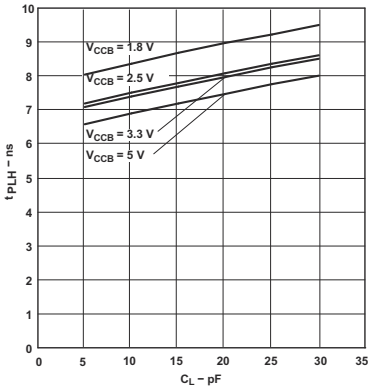
T_A = 25°C, V_{CCA} = 1.8 V

图 6-2. Typical Propagation Delay (A to B) vs Load Capacitance



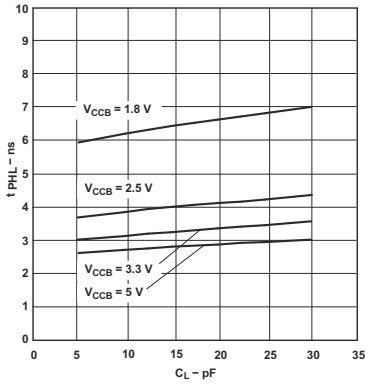
T_A = 25°C, V_{CCA} = 1.8 V

图 6-3. Typical Propagation Delay (B to A) vs Load Capacitance



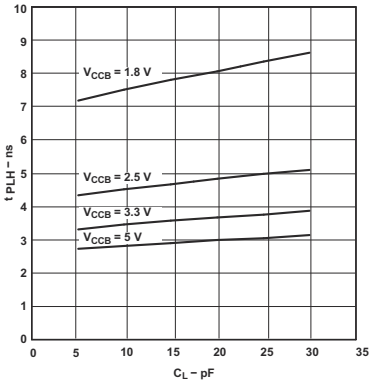
T_A = 25°C, V_{CCA} = 1.8 V

图 6-4. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 2.5 V

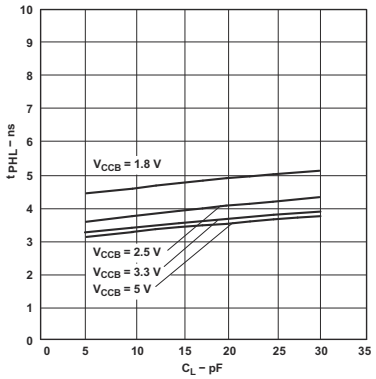
图 6-5. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 2.5 V

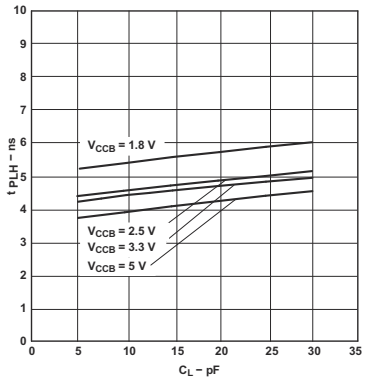
图 6-6. Typical Propagation Delay (A to B) vs Load Capacitance

6.10 Typical Characteristics (continued)



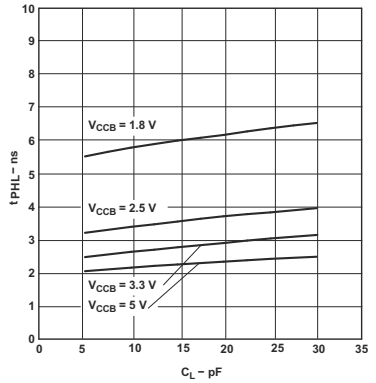
T_A = 25°C, V_{CCA} = 2.5 V

图 6-7. Typical Propagation Delay (B to A) vs Load Capacitance



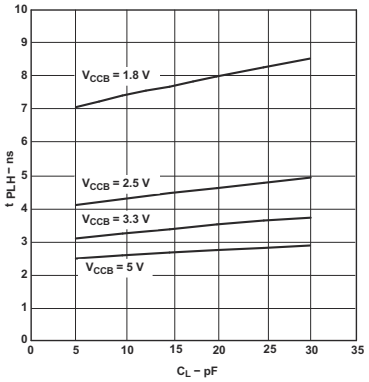
T_A = 25°C, V_{CCA} = 2.5 V

图 6-8. Typical Propagation Delay (B to A) vs Load Capacitance



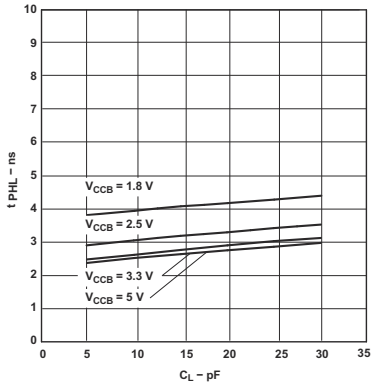
T_A = 25°C, V_{CCA} = 3.3 V

图 6-9. Typical Propagation Delay (A to B) vs Load Capacitance



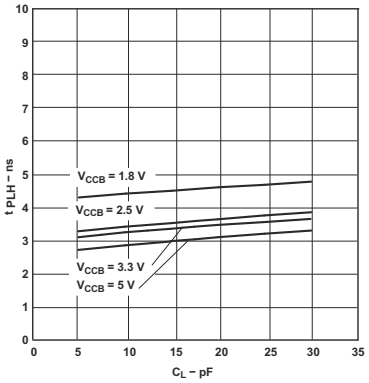
T_A = 25°C, V_{CCA} = 3.3 V

图 6-10. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 3.3 V

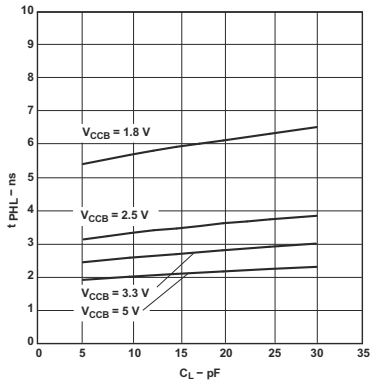
图 6-11. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 3.3 V

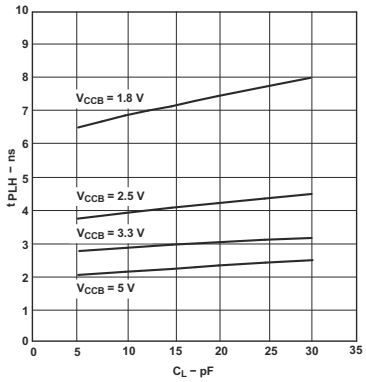
图 6-12. Typical Propagation Delay (B to A) vs Load Capacitance

6.10 Typical Characteristics (continued)



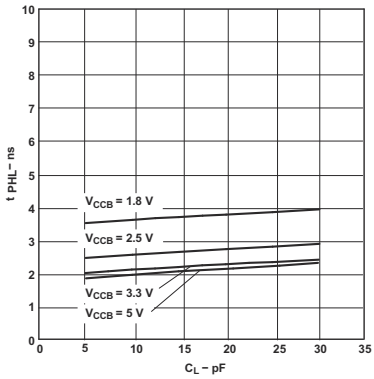
T_A = 25°C, V_{CCA} = 5 V

图 6-13. Typical Propagation Delay (A to B) vs Load Capacitance



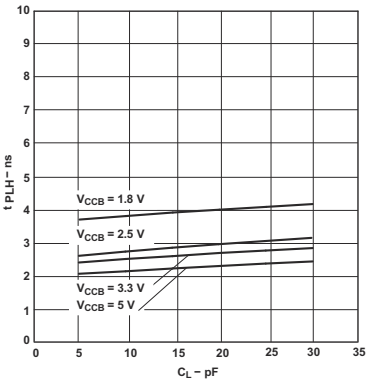
T_A = 25°C, V_{CCA} = 5 V

图 6-14. Typical Propagation Delay (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5 V

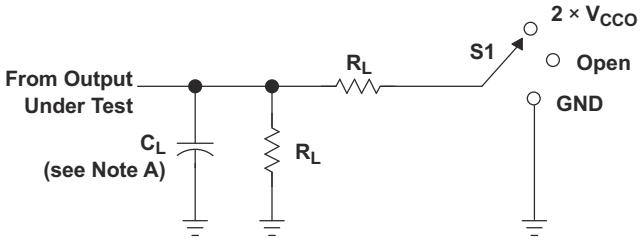
图 6-15. Typical Propagation Delay (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5 V

图 6-16. Typical Propagation Delay (B to A) vs Load Capacitance

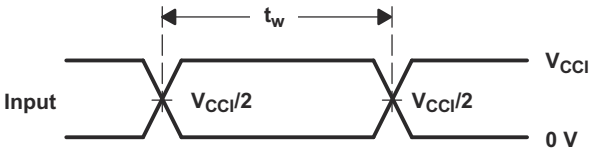
Parameter Measurement Information



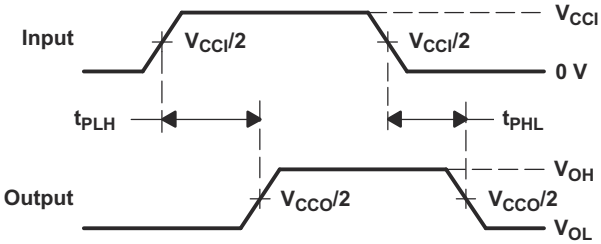
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CCO} GND

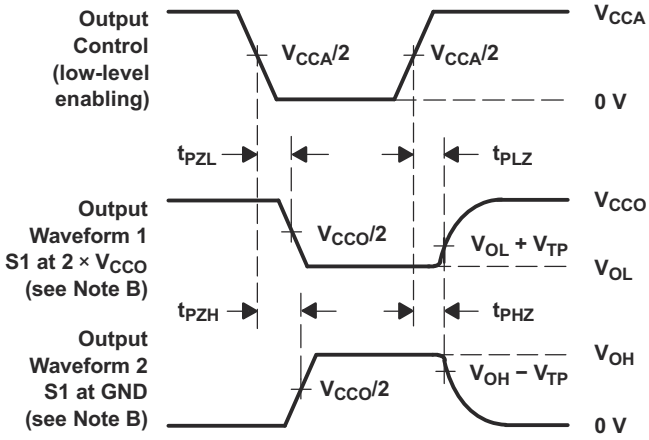
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC1T45-Q1 is single-bit, dual-supply, non-inverting voltage level translation. Pin A and that direction control pin (DIR) are supported by V_{CCA} and pin B is supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The high on the DIR allows data transmissions from A to B and a low on the DIR allows data transmissions from B to A.

7.2 Functional Block Diagram

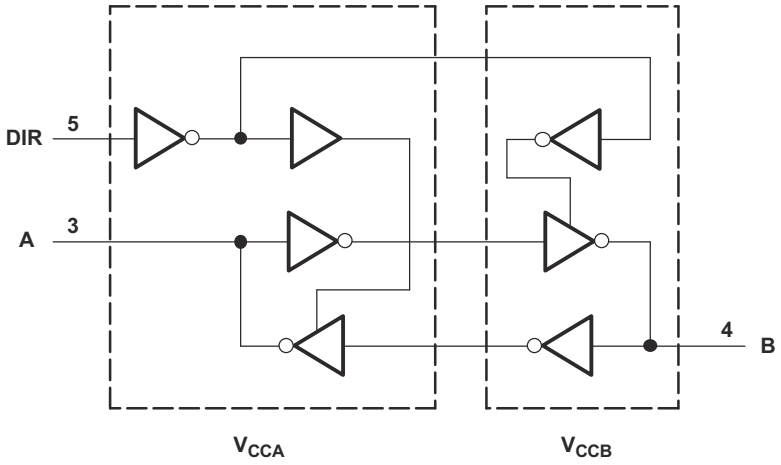


图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The SN74LVC1T45-Q1 has a fully configurable dual-rail design that allows each port to operate over the full 1.65-V to 5.5-V power-supply range. Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8-V, 2.5-V, 3.3-V, and 5-V).

SN74LVC1T45-Q1 can support high data rate applications. The translated signal data rate can be up to 420 Mbps when the signal is translated from 3.3 V to 5 V.

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.

7.4 Device Functional Modes

表 7-1 lists the operational modes of SN74LVC1T45-Q1.

表 7-1. Function Table(1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1T45-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The max data rate can be up to 420 Mbps when device translates signals from 3.3 V to 5 V.

8.1.1 Enable Times

Calculate the enable times for the SN74LVC1T45-Q1 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

8.2 Typical Applications

8.2.1 Unidirectional Logic Level-Shifting Application

图 8-1 shows an example of the SN74LVC1T45-Q1 being used in a unidirectional logic level-shifting application.

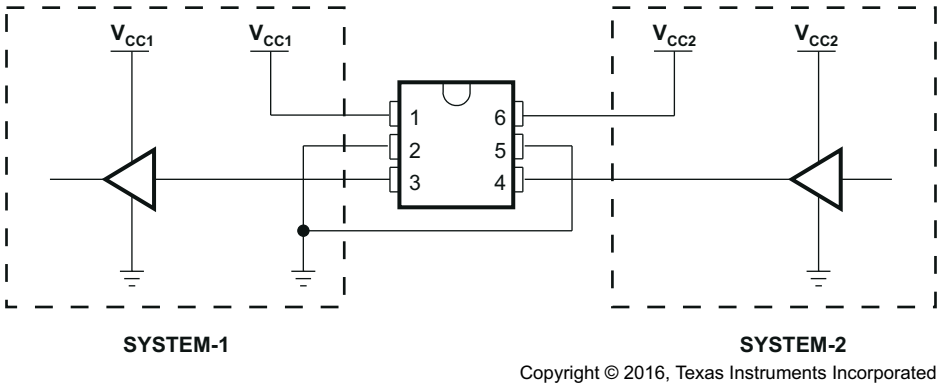


图 8-1. Unidirectional Logic Level-Shifting Application

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LVC1T45-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the VIH of the input port. For a valid logic low the value must be less than the VIL of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LVC1T45-Q1 device is driving to determine the output voltage range.

8.2.1.3 Application Curves

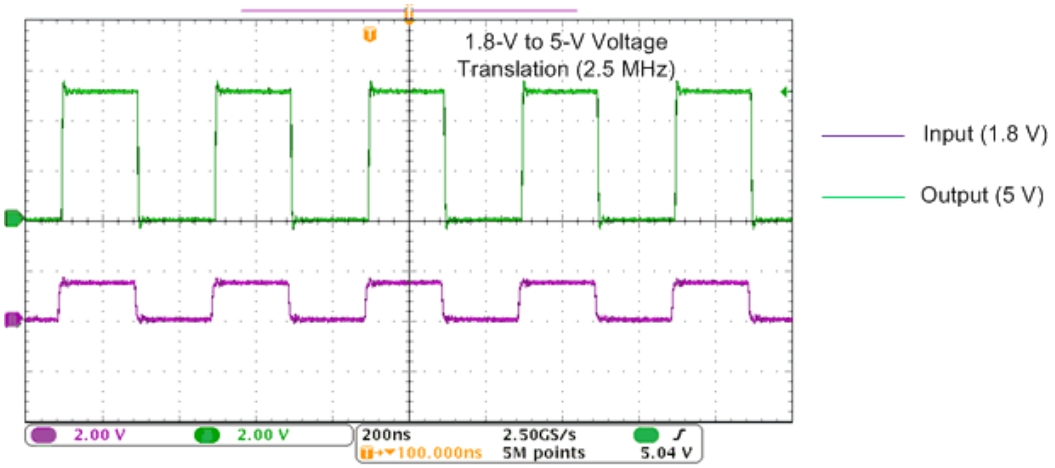


图 8-2. Translation Up (1.8 V to 5 V) at 2.5 MHz

8.2.2 Bidirectional Logic Level-Shifting Application

图 8-3 shows the SN74LVC1T45-Q1 being used in a bidirectional logic level-shifting application. Because the SN74LVC1T45-Q1 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

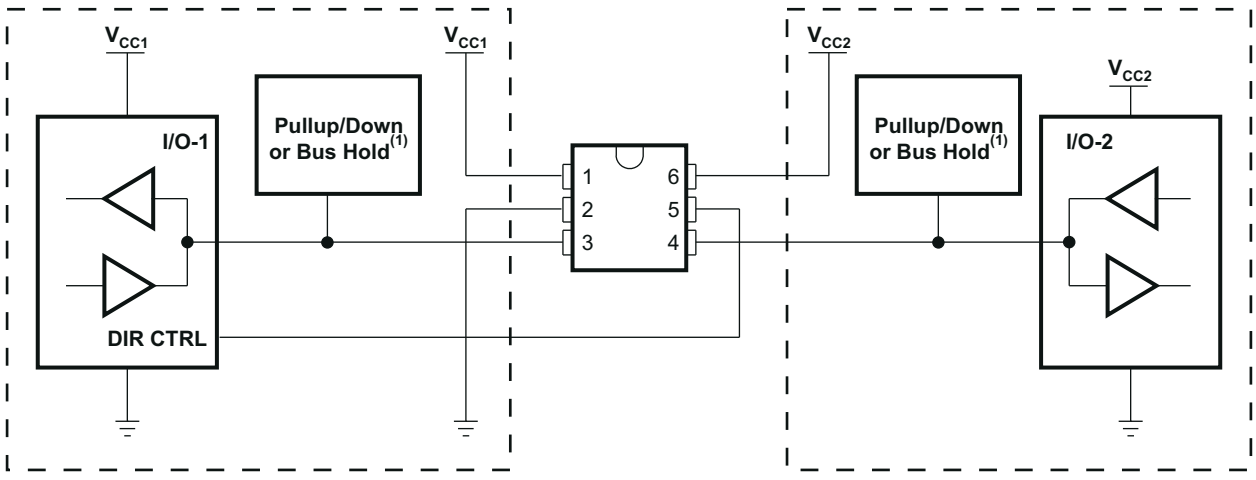


图 8-3. Bidirectional Logic Level-Shifting Application

8.2.2.1 Detailed Design Procedure

表 8-2 shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

表 8-2. Data Transmission

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

8.2.2.2 Application Curves

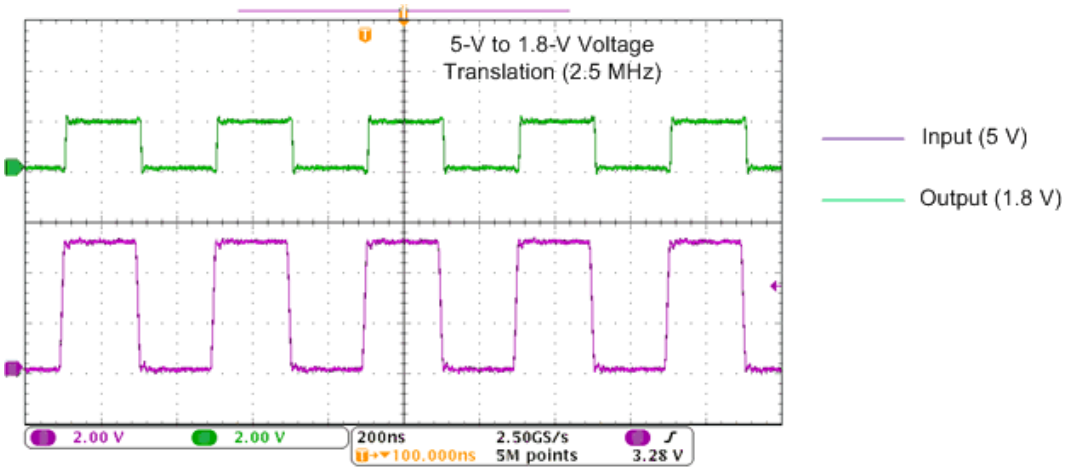


图 8-4. Translation Down (5 V to 1.8 V) at 2.5 MHz

8 Power Supply Recommendations

The SN74LVC1T45-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V, and V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. The A port and B port are designed to track V_{CCA} and V_{CCB}, respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For multiple V_{CC} pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

A proper power-up sequence is advisable as listed in the following:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCB}.
3. V_{CCA} can be ramped up along with V_{CCB}.

TI recommends that the inputs are grounded during power up. Take care to assure that any state changes do not affect system level operation.

9 Layout

9.1 Layout Guidelines

To assure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depends on the system requirements.

9.2 Layout Example

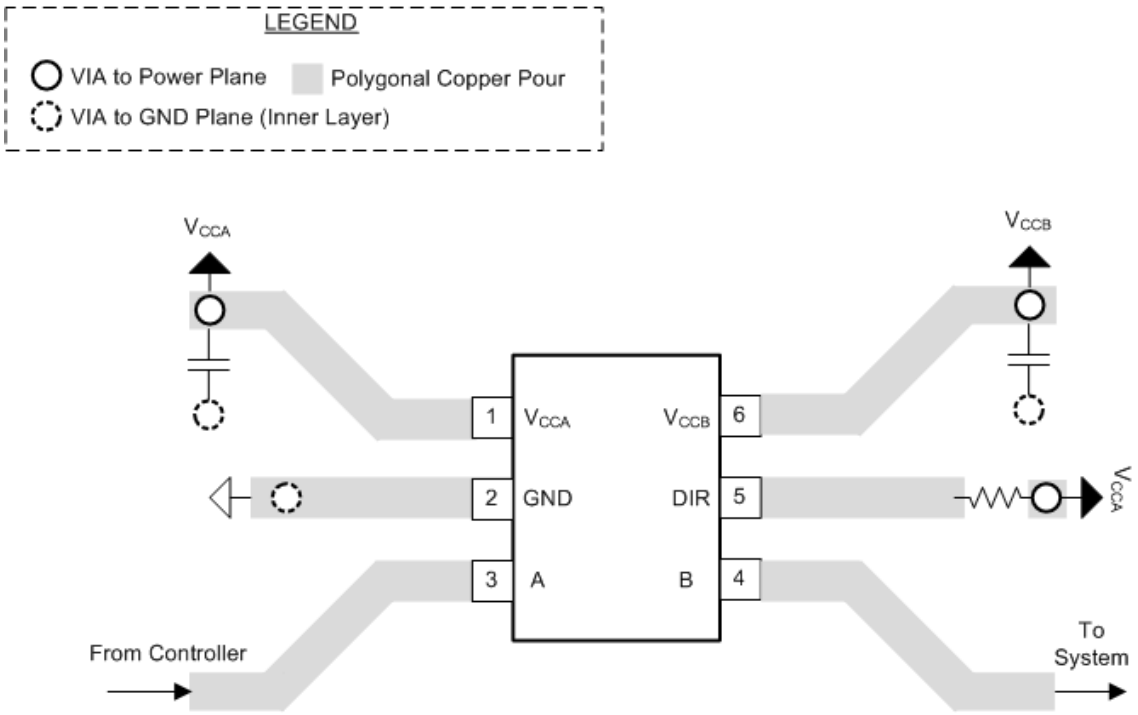


图 9-1. Layout Schematic

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1T45QDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5TR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC1T45-Q1 :

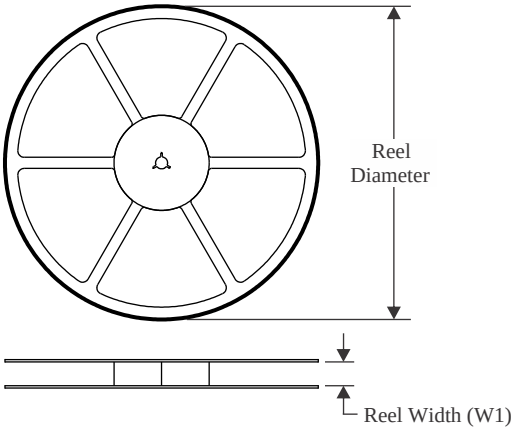
- Catalog : SN74LVC1T45
- Enhanced Product : SN74LVC1T45-EP

NOTE: Qualified Version Definitions:

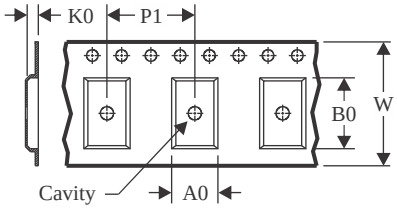
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

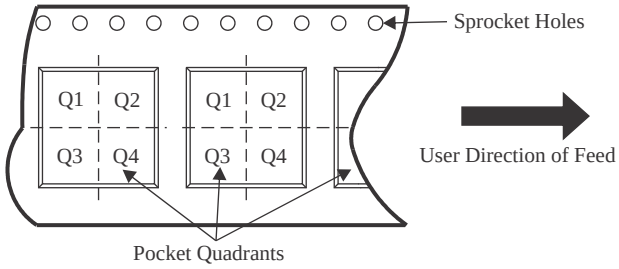


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

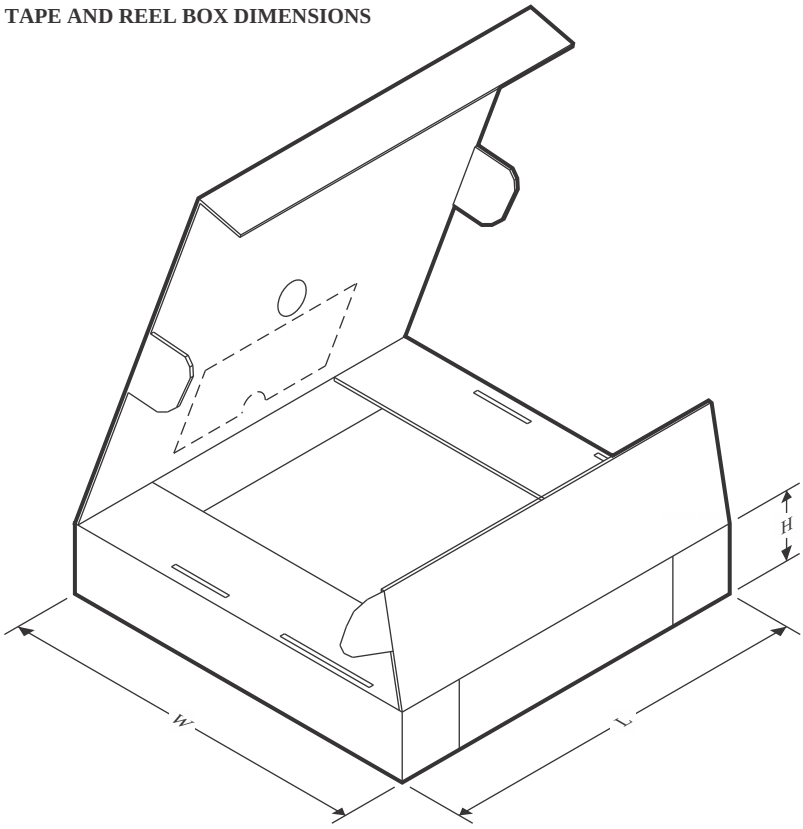
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

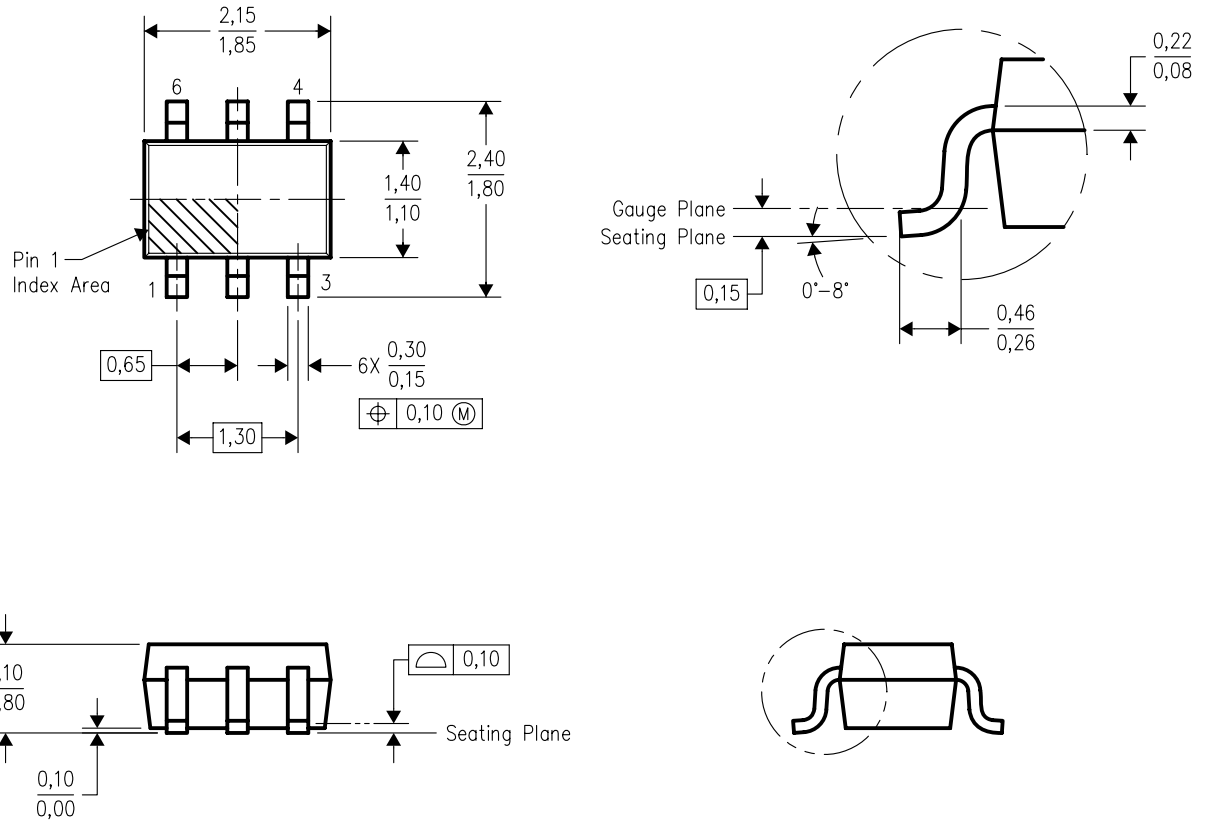
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	202.0	201.0	28.0

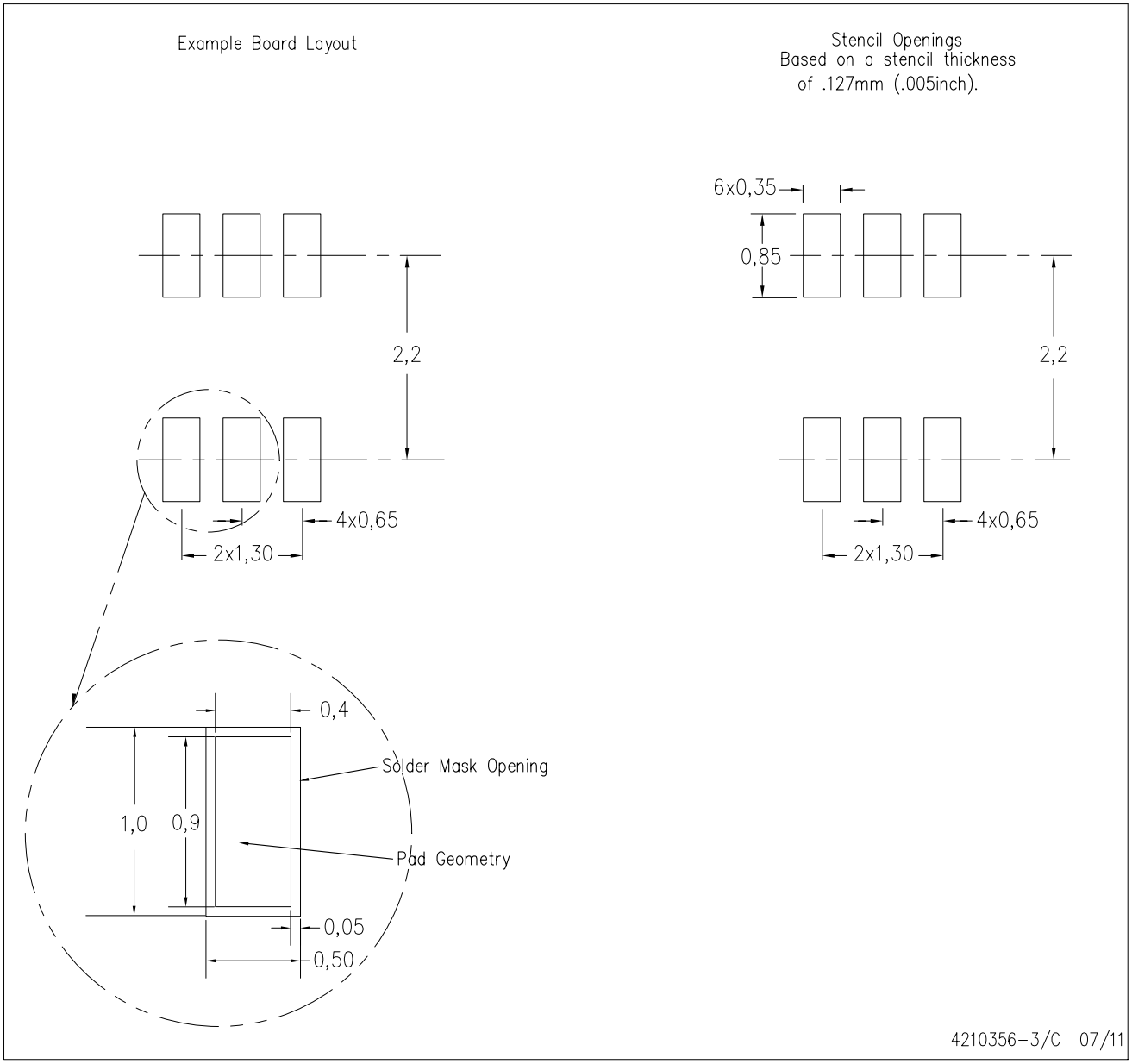
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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