TEXAS INSTRUMENTS

SN74LVC11A 三路 3 输入与门

1 特性

- 工作范围为 1.2V 至 3.6V
- 5.5V 容限输入引脚
- 支持标准引脚排列
- 闩锁性能超过 250mA，
  符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
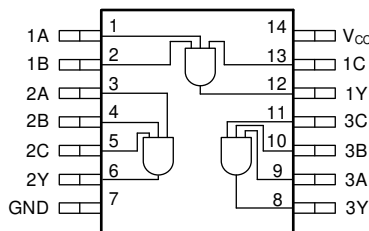 - 1000V 组件充电模式 (C101)

2 应用

- 将电源正常信号进行结合
- 使能数字信号

3 说明

此器件包含三个独立 3 输入与门。每个逻辑门以正逻辑执行布尔函数 $Y = A \times B \times C$。

封装信息

器件型号	封装[1]	封装尺寸[2]	封装尺寸（标称值）[3]
SN74LVC11A	D（SOIC，14）[4]	8.65mm x 6mm	8.65mm × 3.9mm
	BQA（WQFN，14）	3mm × 2.5mm	3mm × 2.5mm
	PW（TSSOP，14）[4]	5mm × 6.4mm	5mm × 4.4mm

(1) 有关更多信息，请参阅 节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。
(4) 仅限预发布封装。

功能引脚分配

English Data Sheet: SCLS993

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English Data Sheet: *SCLS993*

4 Pin Configuration and Functions
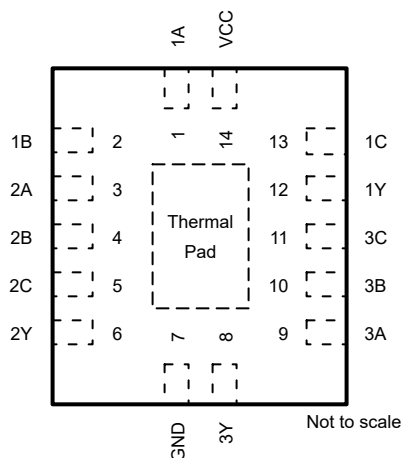
图 4-1. SN74LVC11A BQA Package, 14-Pin WQFN
(Top View)
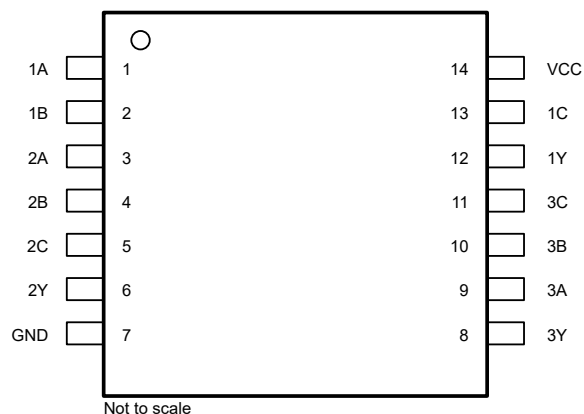
图 4-2. SN74LVC11A D or PW (Preview) Packages,
14-Pin SOIC or TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
2A	3	Input	Channel 2, Input A
2B	4	Input	Channel 2, Input B
2C	5	Input	Channel 2, Input C
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
3C	11	Input	Channel 3, Input C
1Y	12	Output	Channel 1, Output Y
1C	13	Input	Channel 1, Input C
V_{CC}	14	—	Positive Supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.
(2) BQApackage only.

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Product Folder Links: *SN74LVC11A*

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range[2]		-0.5	6.5	V
V_O	Output voltage range[2]		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.2	3.6	V
V_I	Input voltage			5.5	V
V_O	Output voltage	(High or low state)		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 2.7V		-12	
		V_{CC} = 3V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.8V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 2.7V		12	
		V_{CC} = 3V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	125	°C
V_{IH}	High-level input voltage	V_{CC} = 1.2V	0.78		V
V_{IH}	High-level input voltage	V_{CC} = 1.5V	0.975		V
V_{IH}	High-level input voltage	V_{CC} = 1.65V	1.075		V
V_{IH}	High-level input voltage	V_{CC} = 1.95V	1.2675		V

Product Folder Links: *SN74LVC11A*

English Data Sheet: SCLS993

5.3 Recommended Operating Conditions （续）

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{IH}	High-level input voltage	V_{CC} = 2.3V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 2.7V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 3.6V	2		V
V_{IL}	Low-Level input voltage	V_{CC} = 1.2V		0.42	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.5V		0.525	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V		0.5775	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.95V		0.6825	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.3V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.7V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 3.6V		0.8	V

5.4 Thermal Information

THERMAL METRIC[1]		PW (TSSOP)	D (SOIC)	BQA (WQFN)	UNIT
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150.8	127.8	102.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.3	81.9	96.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.8	84.4	70.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	24.7	39.6	16.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	93.2	83.9	70.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	50.1	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= −100μA	1.2V to 3.6V	V_{CC} - 0.2			V
V_{OH}	I_{OH}= −4mA	1.65V	1.2	1.53		V
V_{OH}	I_{OH}= −8mA	2.3V	1.75	2.1		V
V_{OH}	I_{OH}= −12mA	2.7V	2.2	2.45		V
V_{OH}		3V	2.4	2.7		V
V_{OH}	I_{OH}= −24mA	3V	2.2	2.47		V
V_{OL}	I_{OH}= 100μA	1.2V to 3.6V			0.2	V
V_{OL}	I_{OH}= 4mA	1.65V		0.08	0.45	V
V_{OL}	I_{OH}= 8mA	2.3V		0.15	0.7	V
V_{OL}	I_{OH}= 12mA	2.7V		0.23	0.4	V
V_{OL}	I_{OH}= 24mA	3V		0.42	0.55	V
I_I	V_I = V_{CC} or GND	3.6V		±1	±5	μA
I_{off}	V_I or V_O = V_{CC}	0V		±1	±10	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6V		1	40	μA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	2.7V to 3.6V		20	500	μA

Product Folder Links: SN74LVC11A

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5.5 Electrical Characteristics（续）

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C MIN	-40°C to 125°C TYP	-40°C to 125°C MAX	UNIT
C_I	V_I = V_{CC} or GND	3.3V		4.9		pF
C_O	V_O = V_{CC} or GND	3.3V		6.3		pF
C_{PD}	f = 10MHz	1.8V		31		pF
C_{PD}	f = 10MHz	2.5V		31		pF
C_{PD}	f = 10MHz	3.3V		32		pF
C_{PD}	Outputs disabled, f = 10MHz	1.8V		2		pF
		2.5V		3		
		3.3V		4		

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C MIN	-40°C to 125°C TYP	-40°C to 125°C MAX	UNIT
t_{pd}	A, B or C	Y	C_L = 15pF	1.2V		12	20	ns
			C_L = 15pF	1.5V		9	11	
t_{pd}	A, B or C	Y	C_L = 30pF	1.8V ± 0.15V		3.8	10.2	ns
			C_L = 30pF	2.5V ± 0.2V		2.6	6.9	
			C_L = 50pF	2.7V		2.8	4.8	
			C_L = 50pF	3.3V ± 0.3V		2.5	4.1	
$t_{sk(o)}$				3.3V ± 0.3V			1.5	ns

5.7 Noise Characteristics

VCC = 3.3V, CL = 50pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.2	3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.0			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

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English Data Sheet: *SCLS993*

5.8 Typical Characteristics

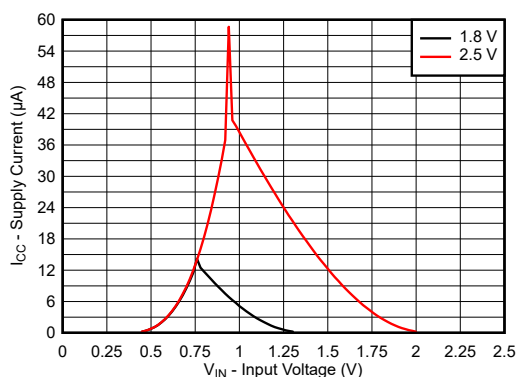$T_A = 25°C$ (unless otherwise noted)

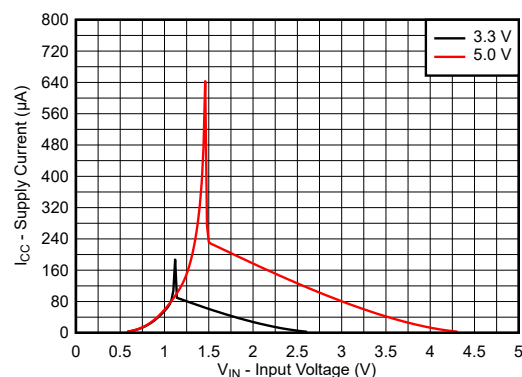图 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

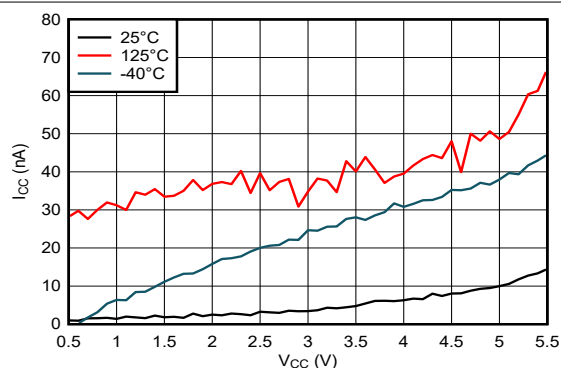图 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply
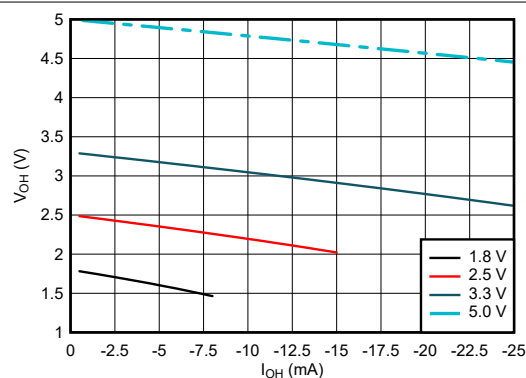

图 5-3. Supply Current Across Supply Voltage

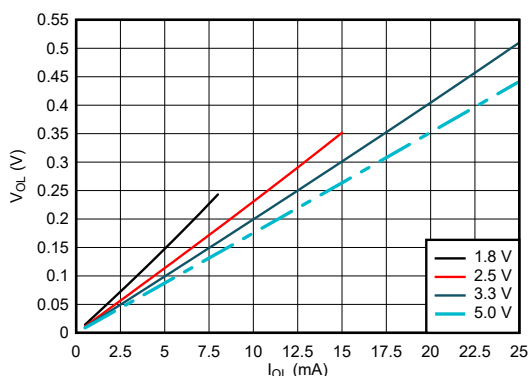图 5-4. Output Voltage vs Current in HIGH State
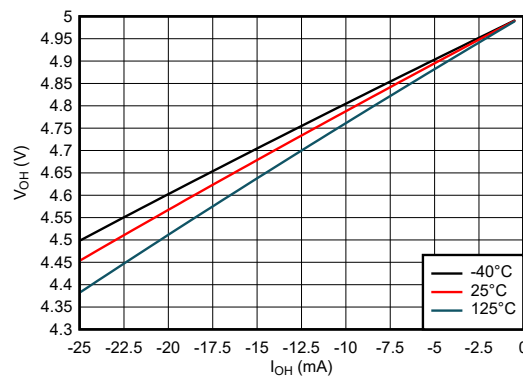

图 5-5. Output Voltage vs Current in LOW State

图 5-6. Output Voltage vs Current in HIGH State; 5V Supply

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5.8 Typical Characteristics (continued)

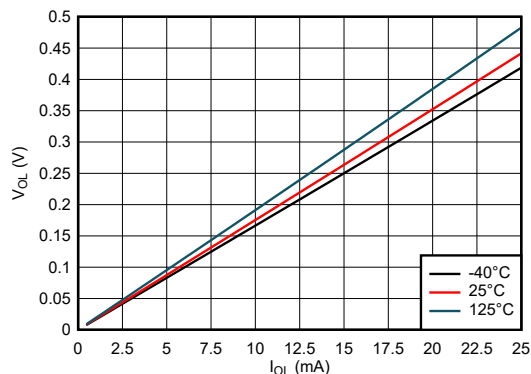T_A = 25°C (unless otherwise noted)

图 5-7. Output Voltage vs Current in LOW State; 5V Supply
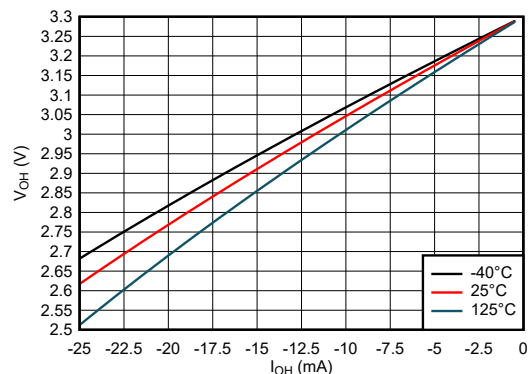
图 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

图 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

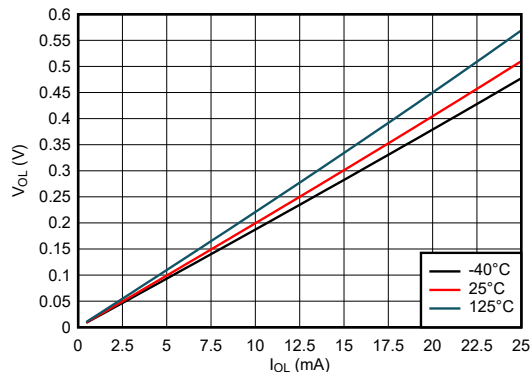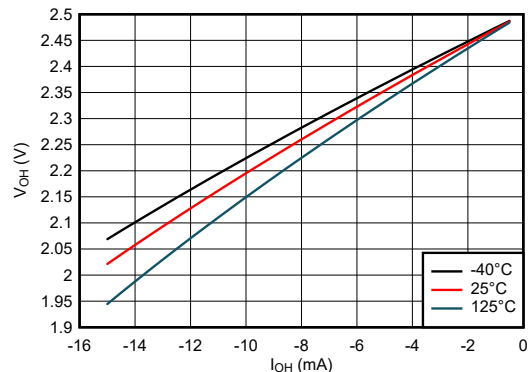图 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

图 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

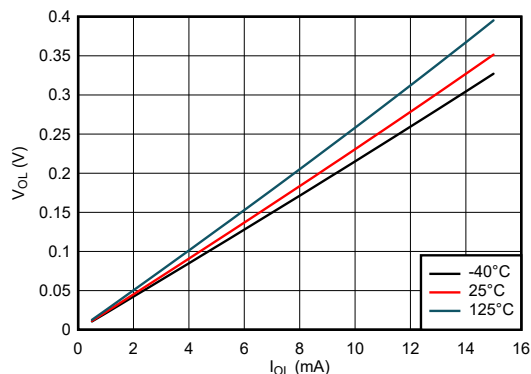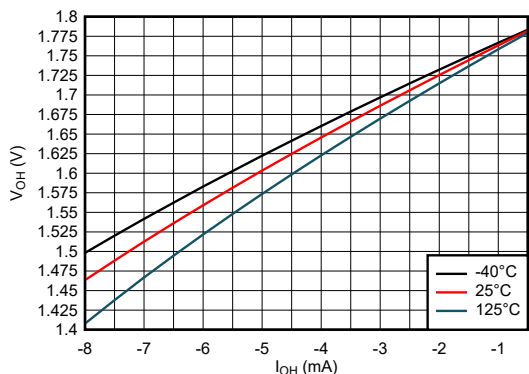图 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

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5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)
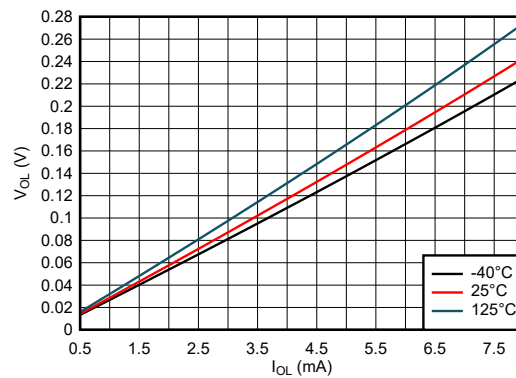
图 **5-13. Output Voltage vs Current in LOW State; 1.8V Supply**

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.
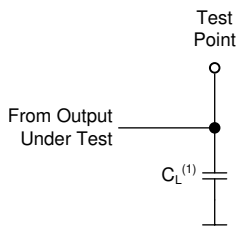
(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs
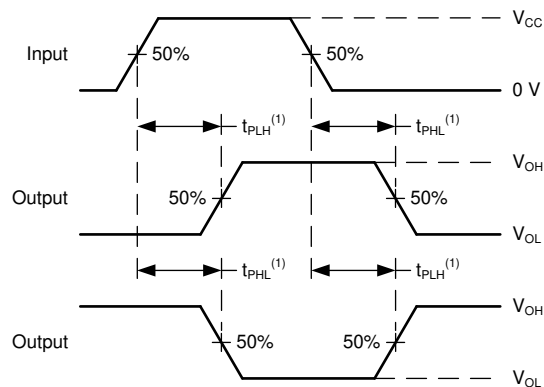
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 6-2. Voltage Waveforms Propagation Delays
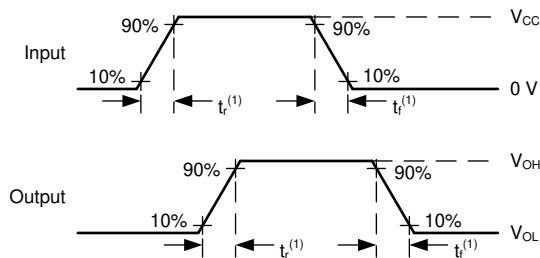
(1) The greater between t_r and t_f is the same as t_t.

图 6-3. Voltage Waveforms, Input and Output Transition Times

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7 Detailed Description

7.1 Overview

This device contains three independent 3-input AND gates. Each gate performs the Boolean function Y = A × B × C in positive logic.

7.2 Functional Block Diagram
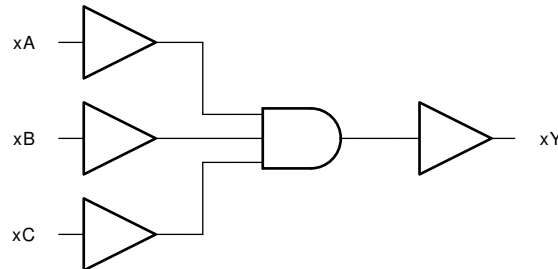
7.3 Feature Description

7.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *Electrical Characteristics - 74*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics - 74*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.2 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74LVC11A can drive a load with a total capacitance less than or equal to the maximum load listed in the *Switching Characteristics -74* connected to a high-impedance CMOS input while still meeting all of the data sheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

7.3.3 Clamp Diode Structure

图 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

> **小心**
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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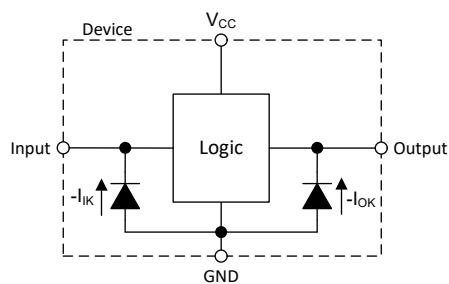
图 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

表 7-1. Function Table[1]

INPUTS			OUTPUT
A	**B**	**C**	**Y**
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

(1)   H = high voltage level, L = low voltage level, X = do not care

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English Data Sheet: SCLS993

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, this device is used to directly control the RESET pin of a motor controller. The controller requires three input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 3-input AND gate function combines the three individual reset signals into a single active-low reset signal.
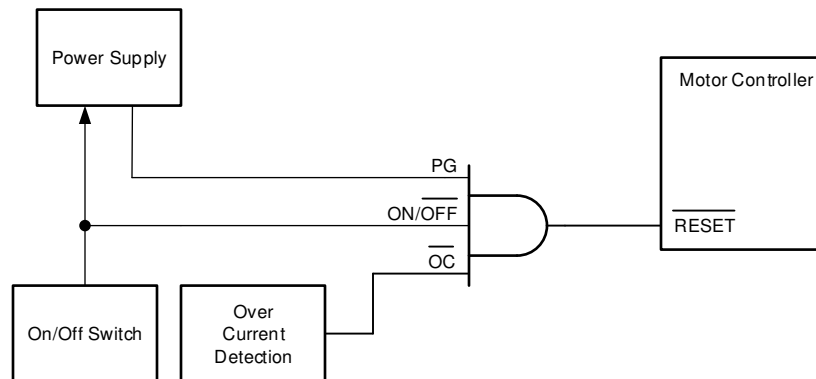
8.2 Typical Application

图 8-1. Typical Application Schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC11A plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC11A plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LVC11A can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC11A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the

output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

> **小心**
>
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC11A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC11A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in *Layout Examples*.
2. Ensure the capacitive load at the output is ≤ 70pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC11A to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / I_O(max)) Ω, so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in mega ohms; much larger than the minimum calculated previously.

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*
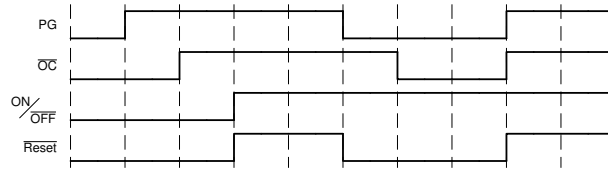
8.2.3 Application Curves

图 8-2. **Typical Application Timing Diagram**

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Layout Example*.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.
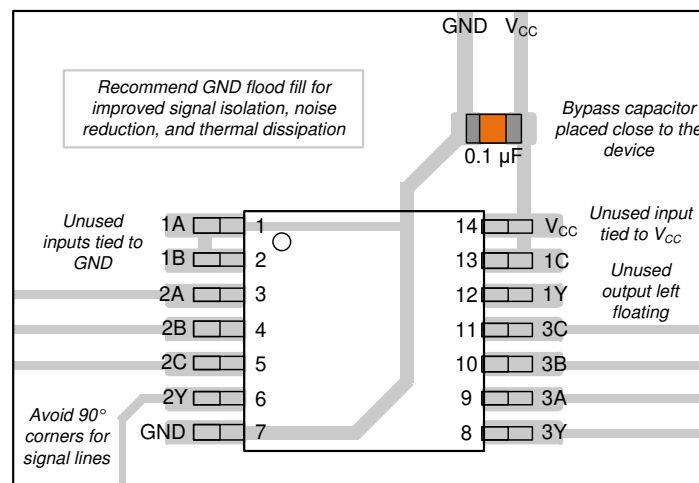
8.4.2 Layout Example

图 8-3. **Example Layout for the SN74LVC11A**

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC11ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC11A	Samples
SN74LVC11APWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	SN	Level-1-260C-UNLIM	-40 to 125	LVC11A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC11A :

● Automotive : SN74LVC11A-Q1

NOTE: Qualified Version Definitions:

     ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC11ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC11APWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS
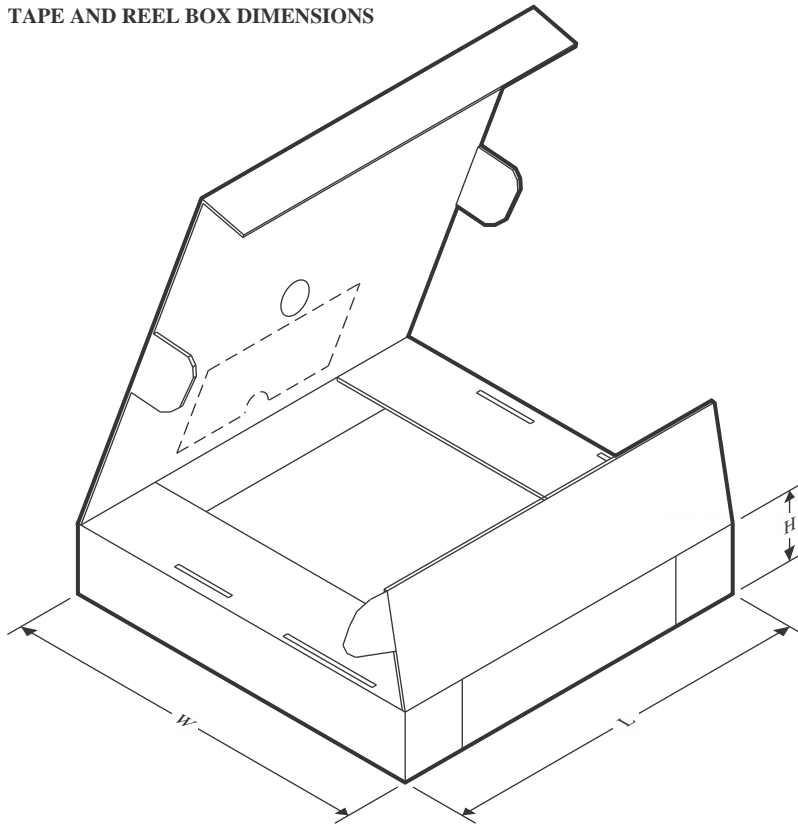
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC11ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC11APWR	TSSOP	PW	14	3000	356.0	356.0	35.0

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

14   8

D | 4,50
     4,30

6,60
6,20

1   7

5,10
4,90

C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ | 0,10

4040064−3/G   02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
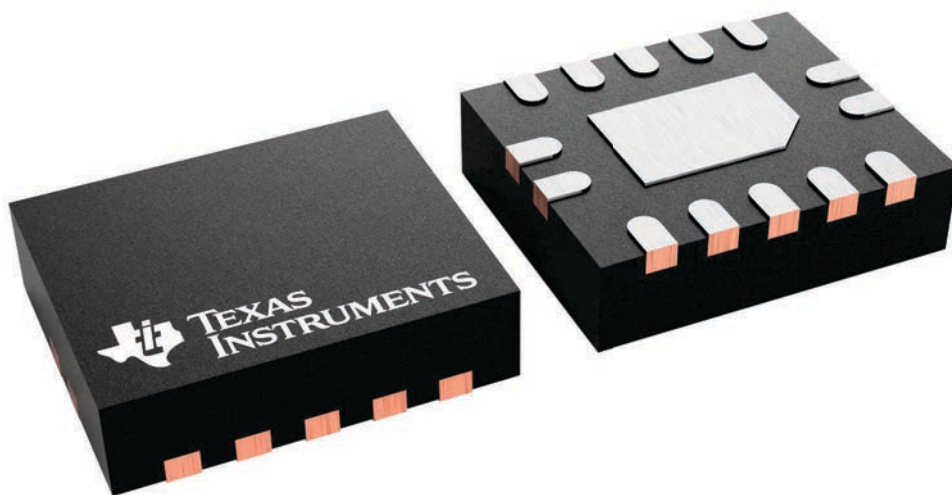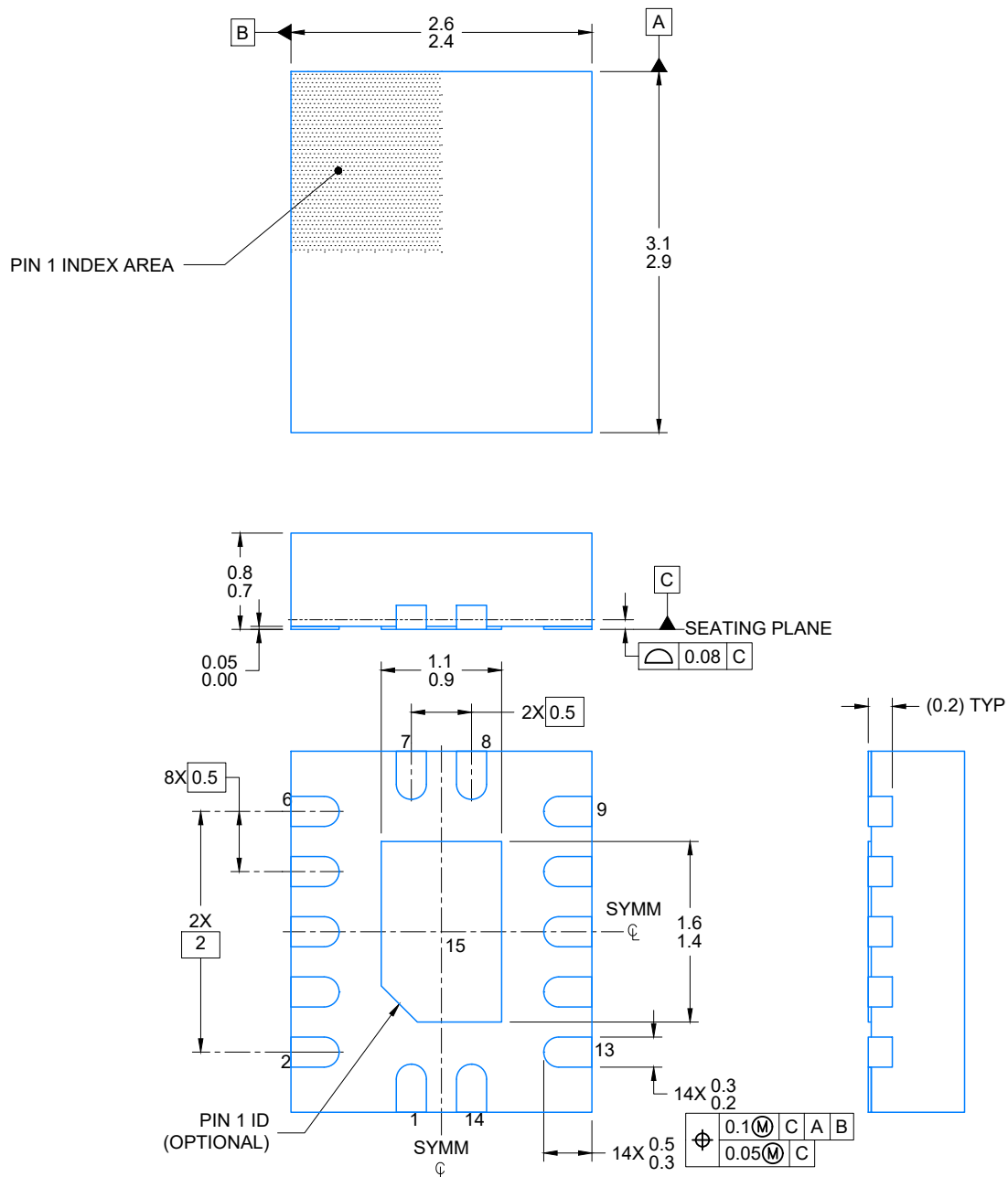   E.   Falls within JEDEC MO−153

BQA 14

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
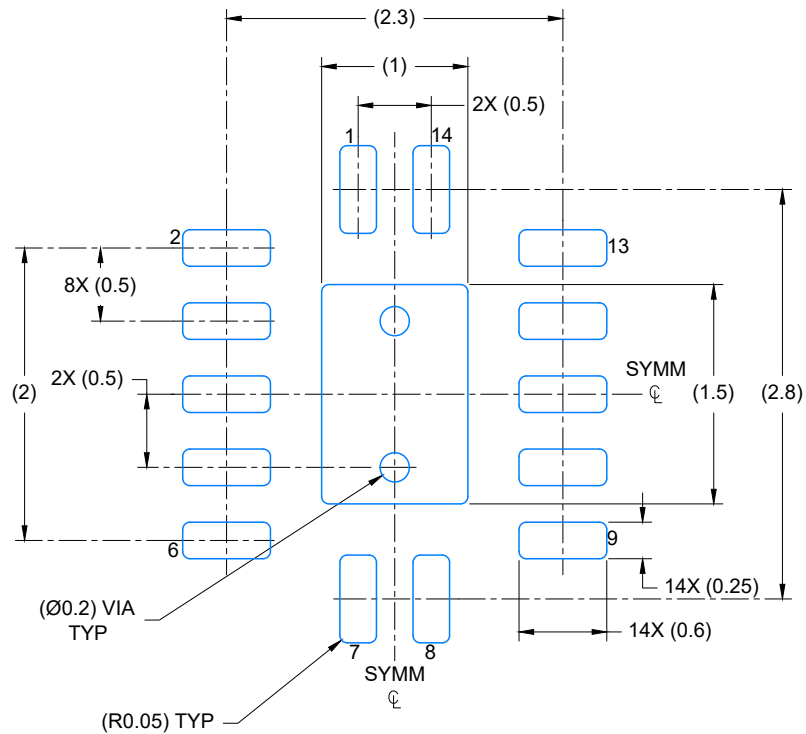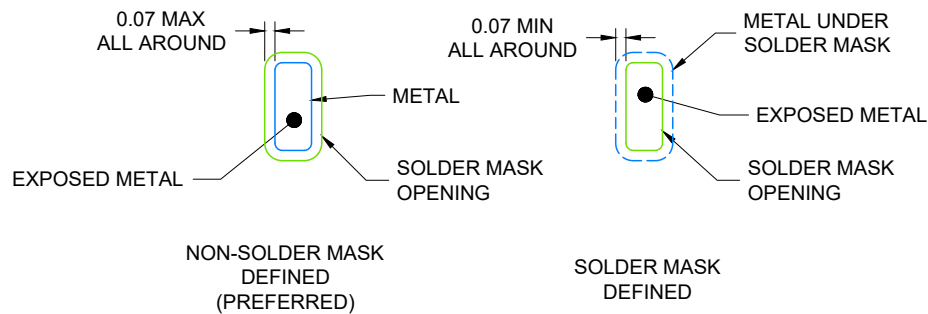Refer to the product data sheet for package details.

4227145/A

B | 2.6 / 2.4 | A

PIN 1 INDEX AREA

3.1 / 2.9

0.8 / 0.7

0.05 / 0.00

C

SEATING PLANE

0.08 C

1.1 / 0.9

2X 0.5

(0.2) TYP

8X 0.5

7 8

6

9

2X 2

SYMM ℄

1.6 / 1.4

15

13

PIN 1 ID (OPTIONAL)

2

1 14

SYMM ℄

14X 0.3 / 0.2

14X 0.5 / 0.3

⊕ | 0.1 Ⓜ C A B
0.05 Ⓜ C

4224636/A   11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

(2.3)

(1)

2X (0.5)

1   14

2

8X (0.5)

13

2X (0.5)

(2)

SYMM
℄   (1.5)   (2.8)

6

9

(Ø0.2) VIA
TYP

14X (0.25)

14X (0.6)

7   8

SYMM
℄

(R0.05) TYP

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

METAL

EXPOSED METAL

EXPOSED METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

4224636/A   11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
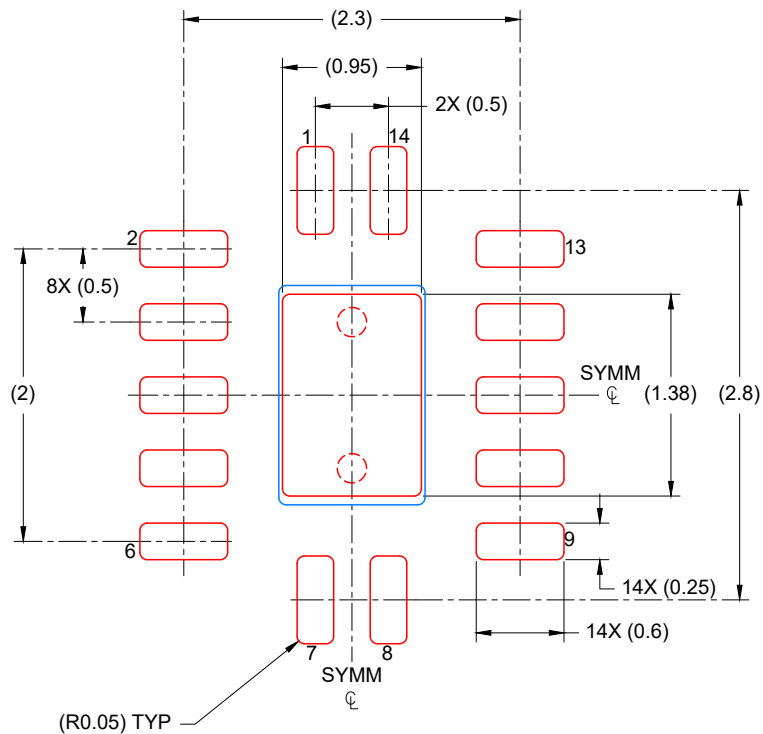
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A   11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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