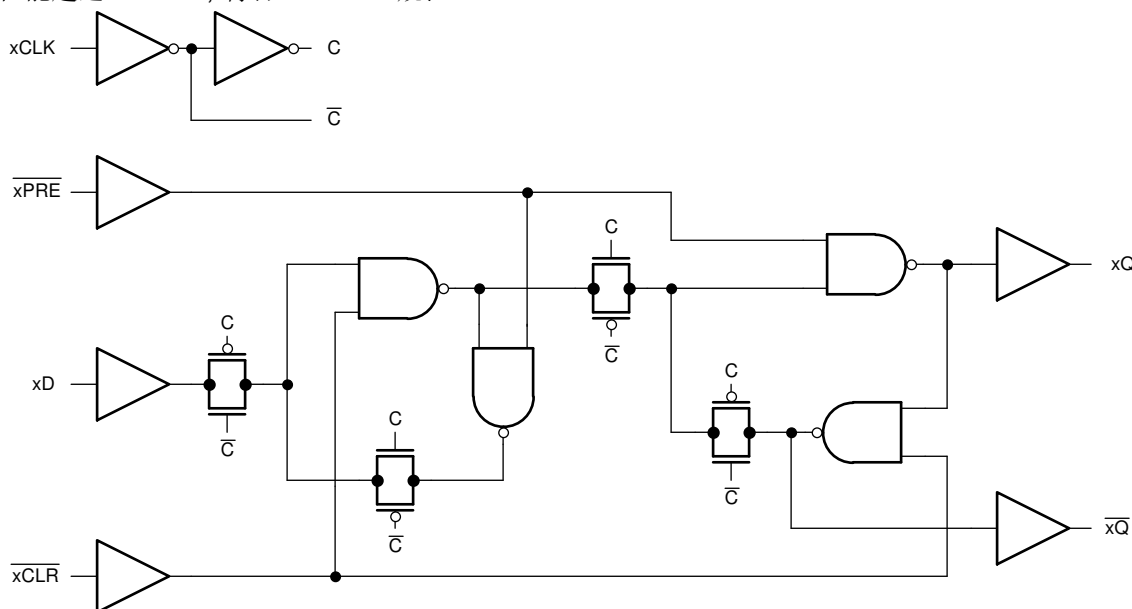


SN74LV74A-Q1 汽车类双路正边沿触发式 D 型触发器

1 特性

- 符合汽车应用要求
- 工作范围为 2V 至 5.5V V_{CC}
- 电压为 5V 时, t_{pd} 最大值为 13ns
- V_{OLP} (输出接地反弹) 典型值小于 0.8V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时)
- V_{OHV} (输出 V_{OH} 下冲) 典型值大于 2.3V ($V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ 时)
- 所有端口上均支持混合模式电压运行
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 250mA, 符合 JESD 17 规范



展示各触发器的逻辑图 (正逻辑)

2 说明

这款双路上升沿触发 D 类触发器需在 2V 至 5.5V V_{CC} 下运行。

封装信息

器件型号	封装 ¹	封装尺寸 ²
SN74LV74A-Q1	PW (TSSOP, 14)	5.00 mm x 6.4 mm
	D (SOIC, 14)	8.65 mm x 6 mm

- 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。
- 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



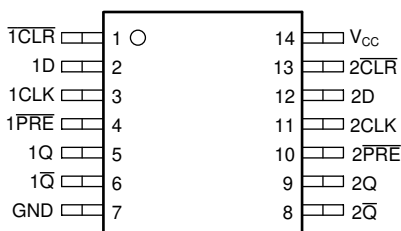
Table of Contents

1 特性	1	5.12 Noise Characteristics.....	7
2 说明	1	5.13 Operating Characteristics.....	7
3 Revision History	2	6 Parameter Measurement Information	8
4 Pin Configuration and Functions	3	7 Detailed Description	9
5 Specifications	4	7.1 Overview.....	9
5.1 Absolute Maximum Ratings	4	7.2 Functional Block Diagram.....	9
5.2 ESD Ratings.....	4	7.3 Device Functional Modes.....	9
5.3 Recommended Operating Conditions.....	4	8 Device and Documentation Support	10
5.4 Thermal Information.....	5	8.1 Documentation Support.....	10
5.5 Electrical Characteristics.....	5	8.2 接收文档更新通知.....	10
5.6 Timing Requirements, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	5	8.3 支持资源.....	10
5.7 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	8.4 Trademarks.....	10
5.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	8.5 静电放电警告.....	10
5.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	6	8.6 术语表.....	10
5.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	9 Mechanical, Packaging, and Orderable Information ..	10
5.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6		

3 Revision History

Changes from Revision B (April 2008) to Revision C (August 2023)	Page
• 添加了封装信息表、引脚功能表、ESD 等级表、热信息表、器件功能模式、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

4 Pin Configuration and Functions



**图 4-1. D and PW Package
14-Pin SOIC and TSSOP
(Top View)**

表 4-1. Pin Functions

PIN			
NO.	NAME	TYPE ¹	DESCRIPTION
1	1 $\overline{\text{CLR}}$	I	1 clear
2	1D	I	1D input
3	1CLK	I	1 clock
4	1 $\overline{\text{PRE}}$	I	1 preset
5	1Q	O	1Q output
6	1 $\overline{\text{Q}}$	O	1 $\overline{\text{Q}}$ output
7	GND	-	GND
8	2 $\overline{\text{Q}}$	O	2 $\overline{\text{Q}}$ output
9	2Q	O	2Q output
10	2 $\overline{\text{PRE}}$	I	2 preset
11	2CLK	I	2 clock
12	2D	I	2D input
13	2 $\overline{\text{CLR}}$	I	2 clear
14	Vcc	-	Supply voltage input

1. Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		- 0.5	7	V
V _I	Input voltage range ⁽²⁾		- 0.5	7	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾		- 0.5	7	V
V _O	Output voltage range ⁽²⁾ ⁽³⁾		- 0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		- 20	mA
I _{OK}	Output clamp current	V _O < 0		- 50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	- 25	25	mA
	Continuous current through V _{CC} or GND		- 50	50	mA
T _{stg}	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value is limited to 5.5-V maximum.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ¹	±2000
		Charged device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	- 50	μA
		V _{CC} = 2.3 V to 2.7 V	- 2	mA
		V _{CC} = 3 V to 3.6 V	- 6	
		V _{CC} = 4.5 V to 5.5 V	- 12	

over operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$	50	$\mu\text{ A}$
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	20	
T_A	Operating free-air temperature	- 40	125	$^{\circ}\text{C}$

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

5.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC ⁽¹⁾		D	PW	UNIT
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	113	$^{\circ}\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	$I_{OH} = -50\text{ }\mu\text{ A}$	2 to 5.5 V	$V_{CC} - 0.1$		V
		$I_{OH} = -2\text{ mA}$	2.3 V	2		
		$I_{OH} = -6\text{ mA}$	3 V	2.48		
		$I_{OH} = -12\text{ mA}$	4.5 V	3.8		
V_{OL}	Low level output voltage	$I_{OL} = 50\text{ }\mu\text{ A}$	2 to 5.5 V		0.1	V
		$I_{OL} = 2\text{ mA}$	2.3 V		0.4	
		$I_{OL} = 6\text{ mA}$	3 V		0.44	
		$I_{OL} = 12\text{ mA}$	4.5 V		0.55	
I_I	Input leakage current	$V_I = 5.5\text{ V or GND}$	0 to 5.5 V		± 1	$\mu\text{ A}$
I_{CC}	Supply current	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		20	$\mu\text{ A}$
I_{off}	Input/Output Power-Off Leakage Current	V_I or $V_O = 0$ to 5.5 V	0		5	$\mu\text{ A}$
C_i	Input Capacitance	$V_I = V_{CC}$ or GND	3.3 V	2		pF
			5 V	2		

5.6 Timing Requirements, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER		$T_A = 25^{\circ}\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration	PRE or CLR low	8	9		ns
		CLK	8	9		
t_{su}	Setup time before CLK $\uparrow$	Data	8	9		ns
		PRE or CLR low	7	7		
t_h	Hold time, data after CLK $\uparrow$		0.5	0.5		ns

5.7 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	PRE or $\overline{\text{CLR}}$ low	6	7			ns
		CLK	6	7			
t_{su}	Setup time before CLK $\uparrow$	Data	6	7			ns
		PRE or $\overline{\text{CLR}}$ low	5	5			
t_h	Hold time, data after CLK $\uparrow$		0.5	0.5			ns

5.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	PRE or $\overline{\text{CLR}}$ low	5	5			ns
		CLK	5	5			
t_{su}	Setup time before CLK $\uparrow$	Data	5	5			ns
		PRE or $\overline{\text{CLR}}$ low	3	3			
t_h	Hold time, data after CLK $\uparrow$		0.5	0.5			ns

5.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50\text{ pF}$	30	70		25		MHz
t_{pd}	PRE or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$		13	17.4	1	20	ns
	CLK				14.2	20	1	23	

5.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50\text{ pF}$	50	90		45		MHz
t_{pd}	PRE or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$		9.2	15.8	1	18	ns
	CLK				10.2	15.4	1	18	

5.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50\text{ pF}$	90	140		75		MHz
t_{pd}	PRE or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$		6.6	9.7	1	12	ns
	CLK				7.2	9.3	1	13	

5.12 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.1	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		0	- 0.8	
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		
$V_{IH(D)}$	High-level dynamic input voltage	2.31			
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	

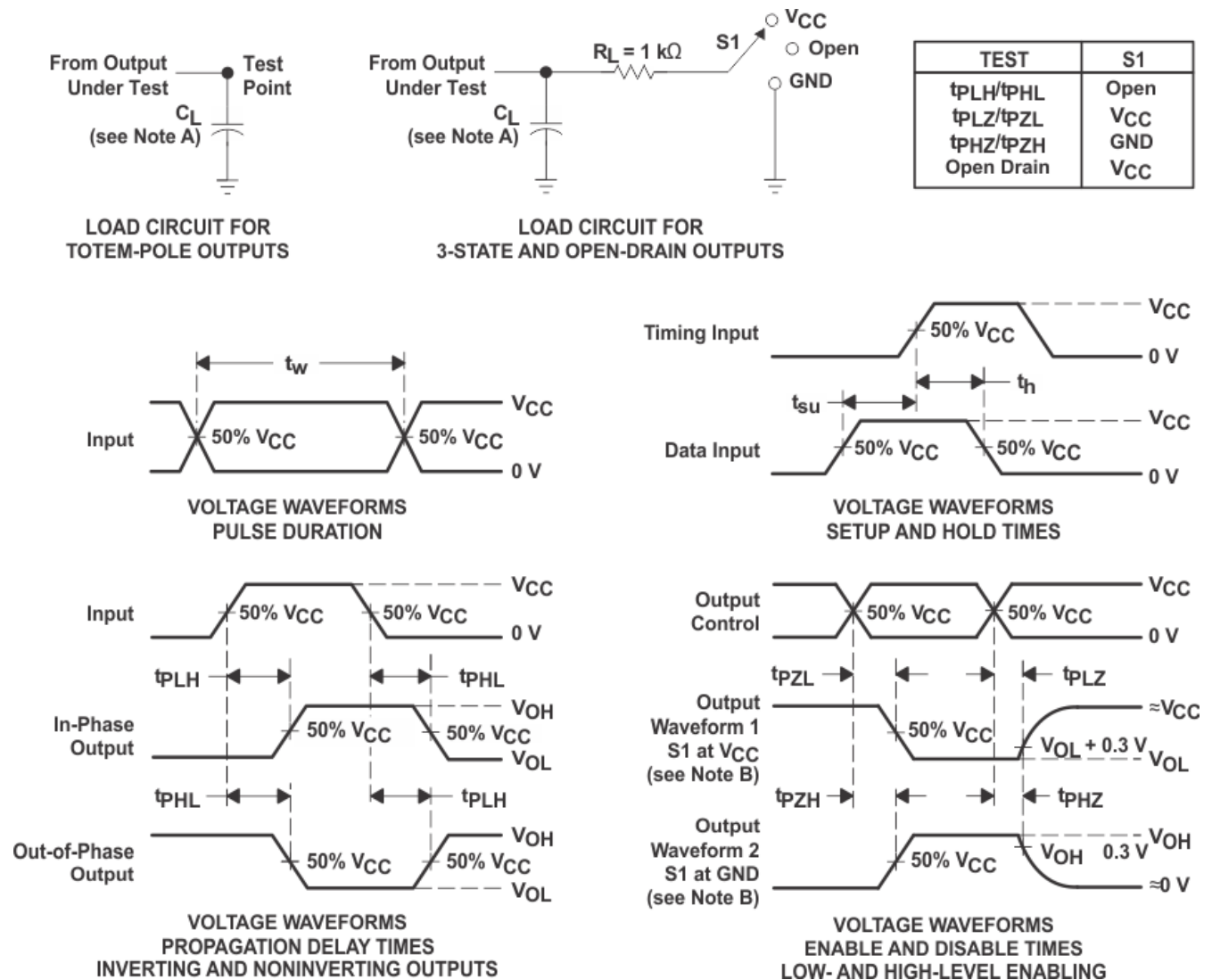
(1) Characteristics are for surface-mount packages only.

5.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	21	pF
			5 V	23	

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This dual positive-edge-triggered D-type flip-flop is designed for 2-V to 5.5-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram

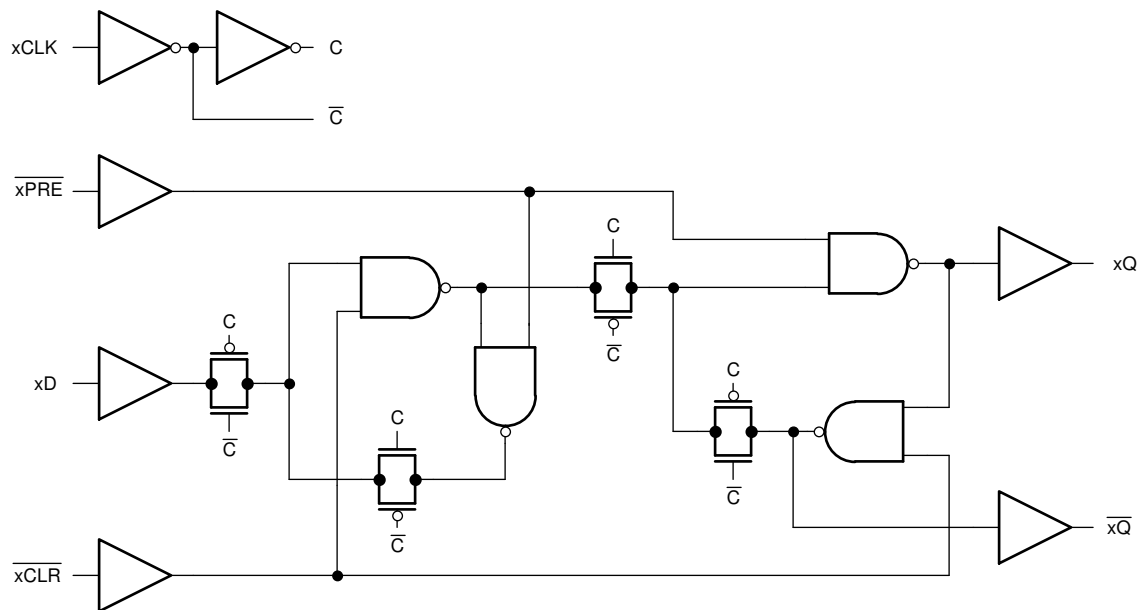


图 7-1. Logic Diagram, Each Flip-flop (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table

INPUTS ⁽¹⁾				OUTPUTS ⁽²⁾	
PRE	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽³⁾	H ⁽³⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

(3) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV74A-Q1	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV74AQDRG4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74AQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

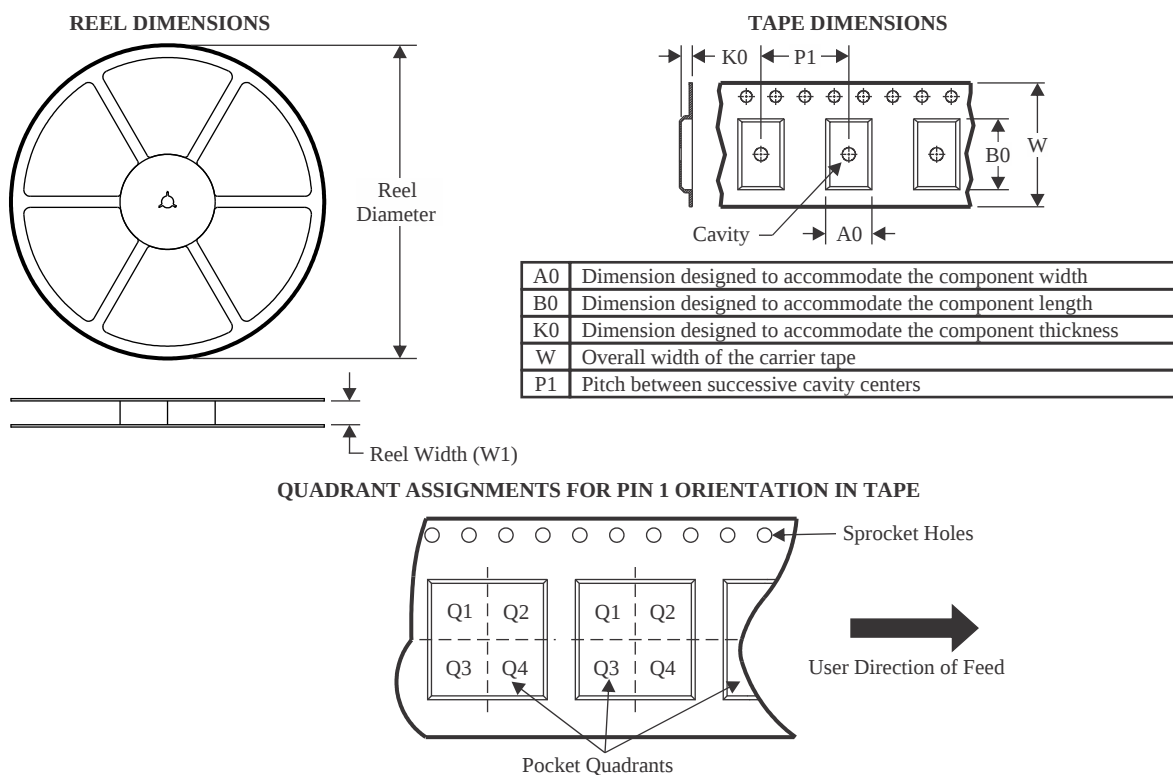
OTHER QUALIFIED VERSIONS OF SN74LV74A-Q1 :

- Catalog : [SN74LV74A](#)
- Enhanced Product : [SN74LV74A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

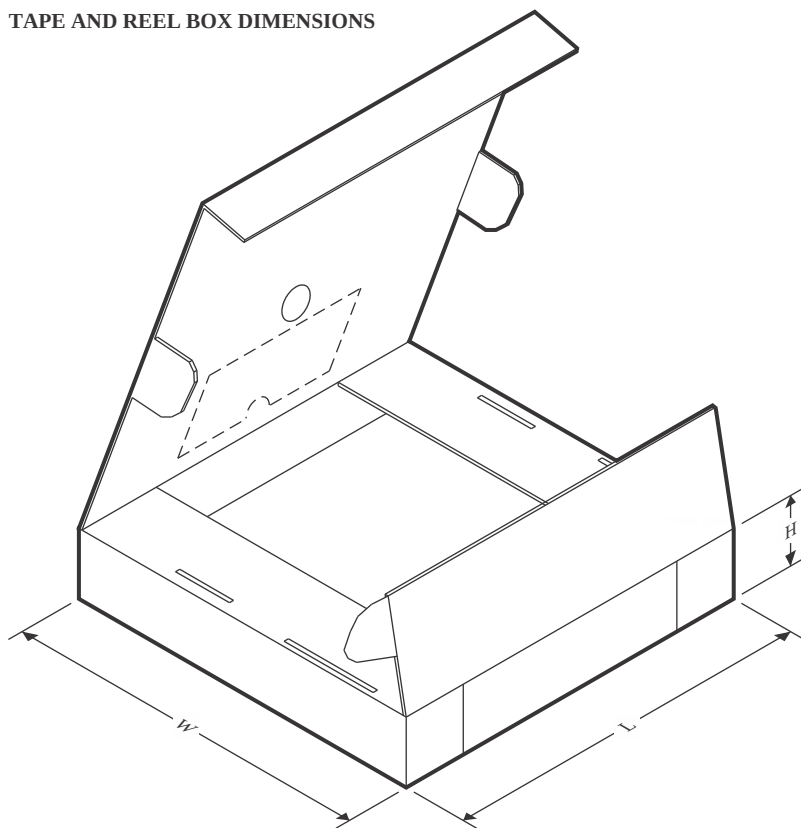
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV74AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV74AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

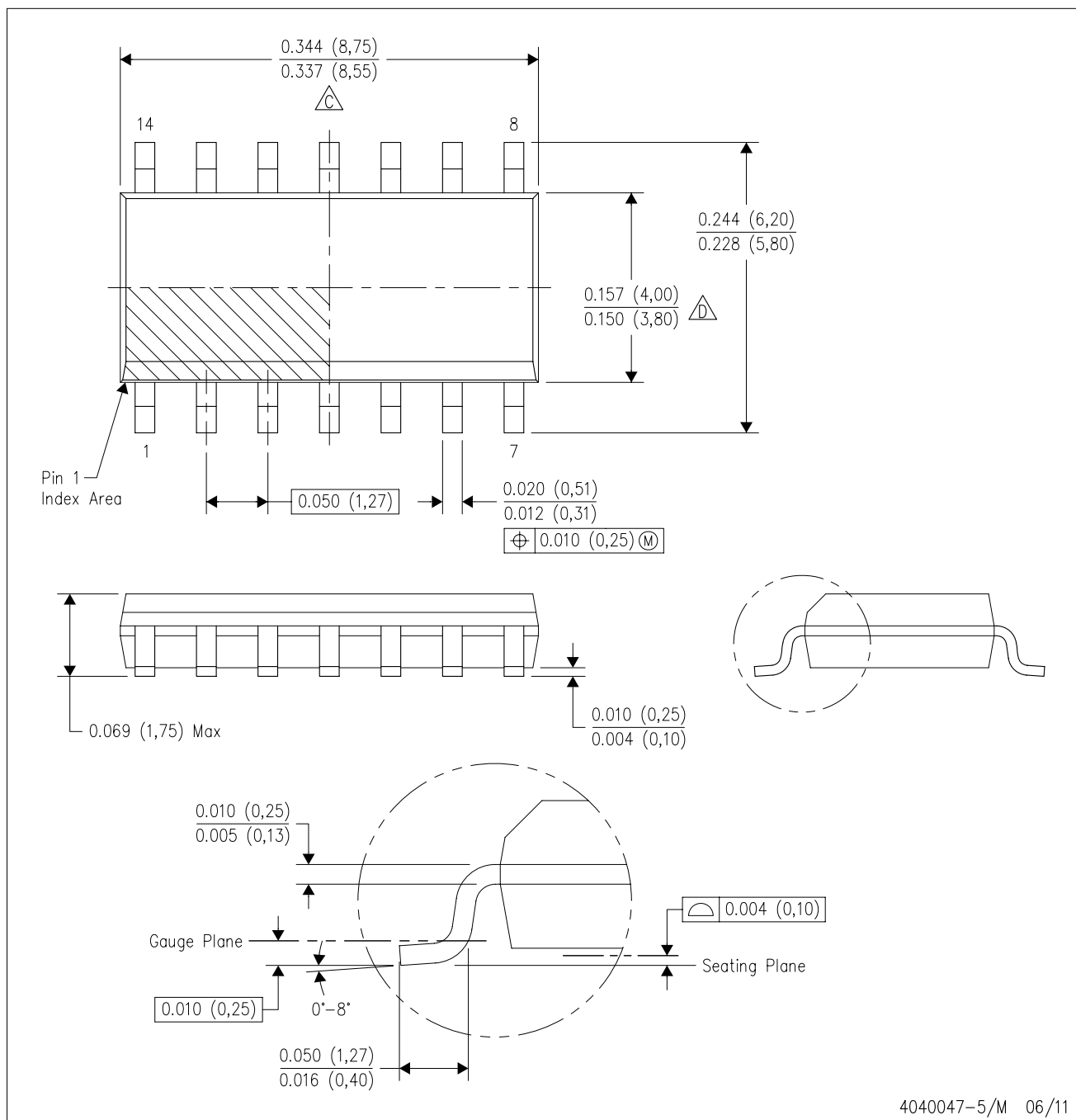


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV74AQPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV74AQPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

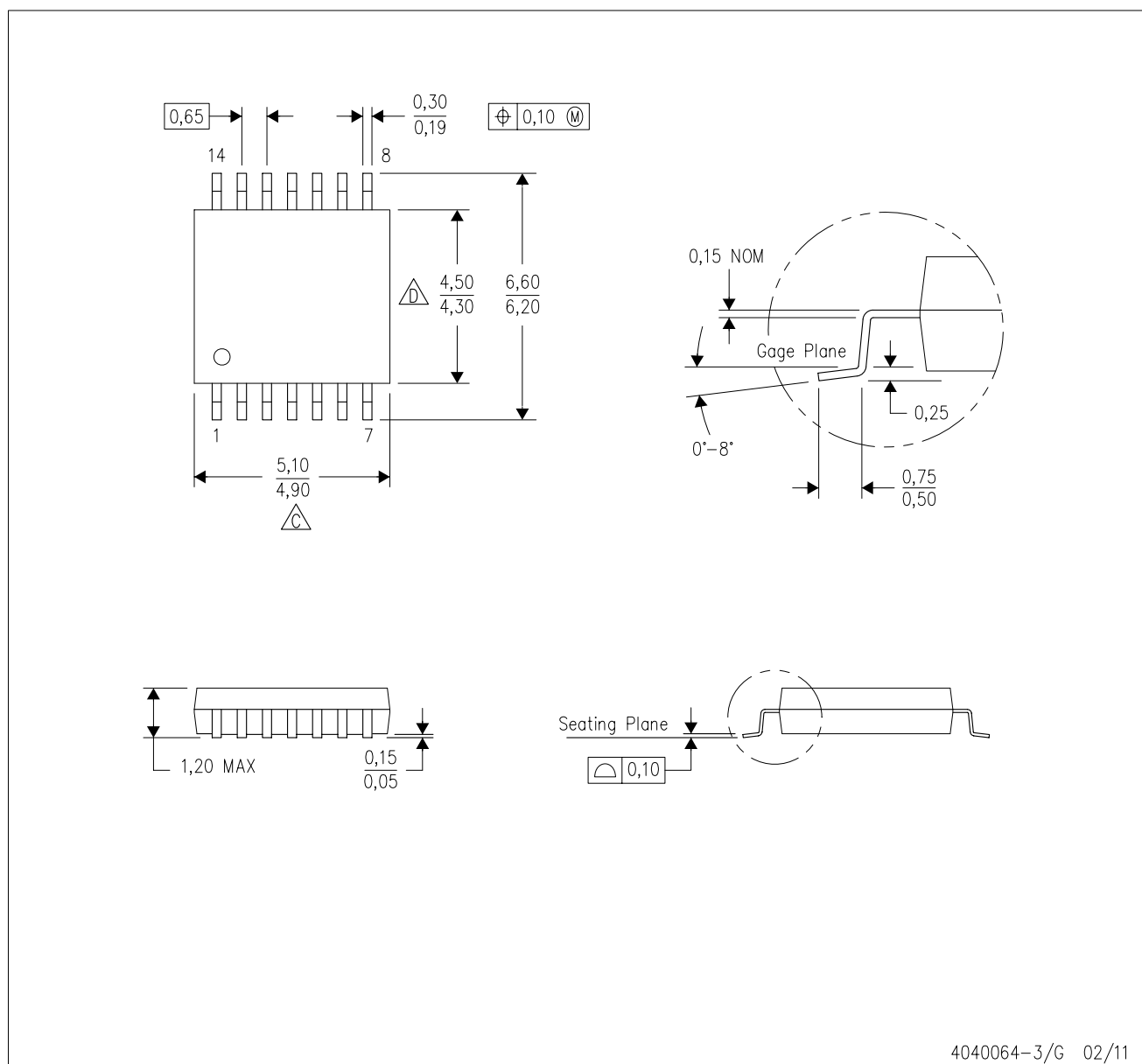


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

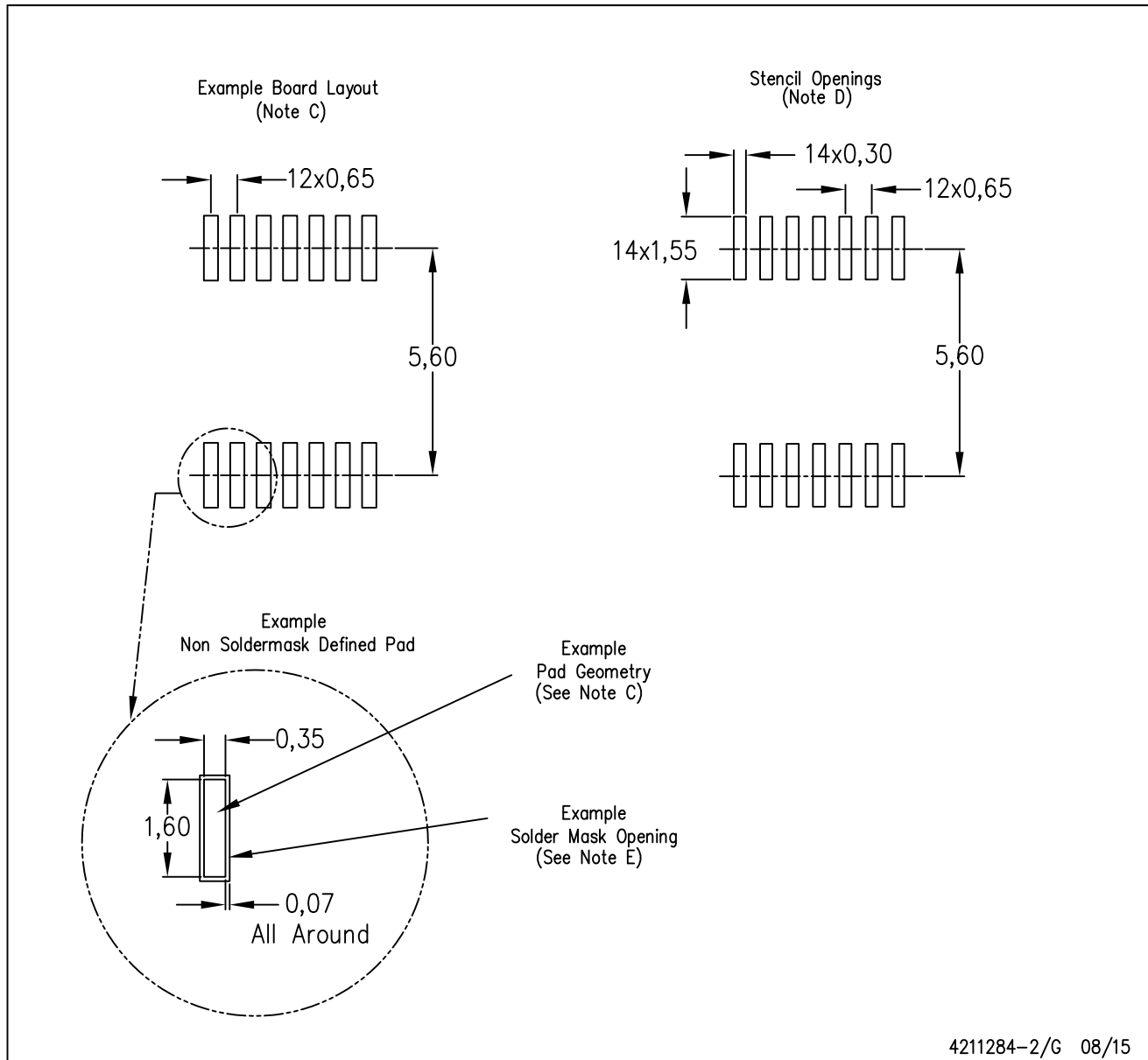
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司