

SN74AHCT138Q-Q1 汽车级 3 线至 8 线解码器/多路信号分离器

1 特性

- 符合汽车应用要求
- EPIC (增强性能植入式 CMOS) 工艺
- 输入兼容 TTL 电压
- 专门为高速存储器解码器和数据传输系统设计
- 包含三个使能输入以简化级联和/或数据接收
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护超过 MIL-STD-883C 方法 3015 规定的 2000V

2 说明

SN74AHCT138Q 3 线至 8 线解码器/多路信号分离器设计用于需要极短传播延迟时间的高性能存储器解码和数据路由应用。在高性能存储器系统中，可使用此解码器来尽可能地消除系统解码的影响。与使用快速使能电路的高速存储器一同使用时，该解码器的延迟时间和存储器的使能时间通常小于存储器的典型存取时间。这意味着解码器引起的有效系统延迟可以忽略不计。

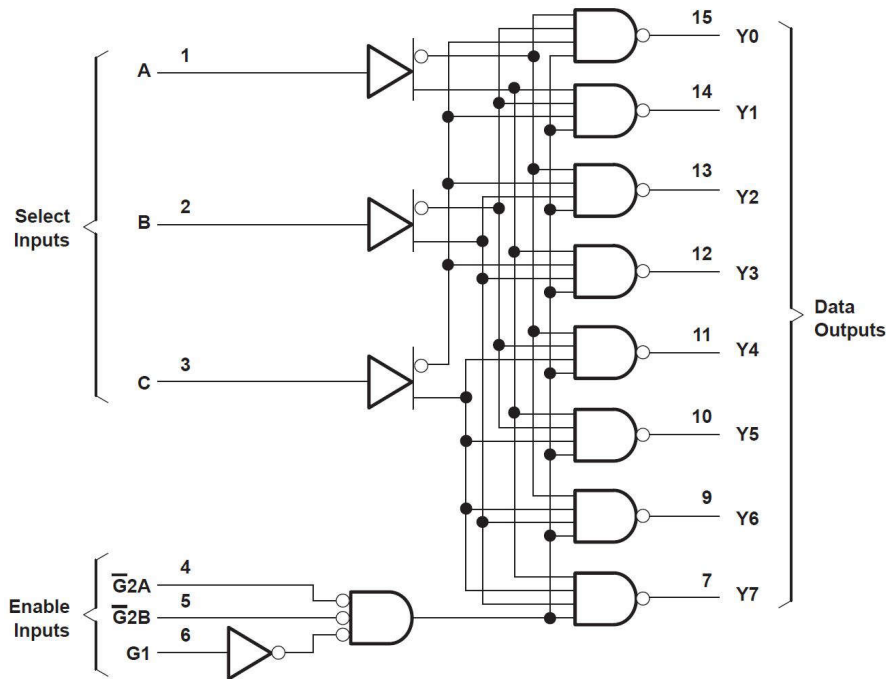
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN74AHCT138Q-Q1	BQB (WQFN , 16)	3.5mm x 2.5mm	3.5mm x 2.5mm
	D (SOIC , 16)	9.9mm x 6mm	9.9mm x 3.9mm
	PW (TSSOP , 16)	5.00mm x 6.4mm	5.00mm x 4.40mm

(1) 有关更多信息，请参阅第 10 节。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



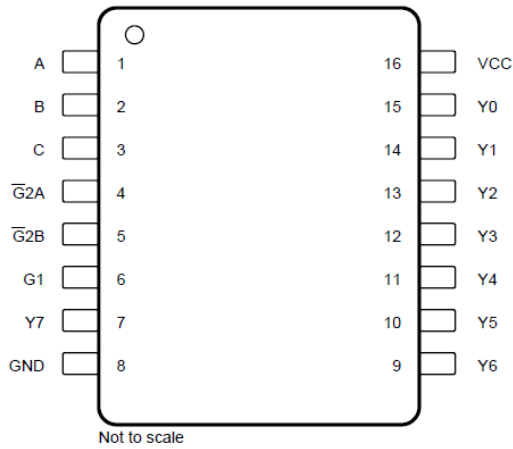
逻辑图 (正逻辑)



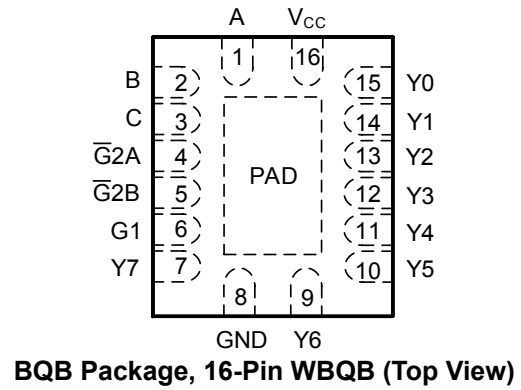
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3 Pin Configuration and Functions



D or PW Package, 16-Pin SOIC or TSSOP (Top View)



PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	SOIC, TSSOP, WQFN		
A	1	I	Select input A (least significant bit)
B	2	I	Select input B
C	3	I	Select input C (most significant bit)
$\overline{G2A}$	4	I	Active low enable A
$\overline{G2B}$	5	I	Active low enable B
G1	6	I	Active high enable
GND	8	—	Ground
NC	—	—	No internal connection
V _{CC}	16	—	Supply voltage
Y0	15	O	Output 0 (least significant bit)
Y1	14	O	Output 1
Y2	13	O	Output 2
Y3	12	O	Output 3
Y4	11	O	Output 4
Y5	10	O	Output 5
Y6	9	O	Output 6
Y7	7	O	Output 7 (most significant bit)
Thermal pad ⁽²⁾		The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.	

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

(2) WBQB package only.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	- 0.5	7	V
V_I	Input voltage range	- 0.5	7	V
V_O	Output voltage range	-0.5V	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$	-20	mA
I_{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$	±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	±25	mA
	Continuous current through V_{CC} or GND		±75	mA
T_{stg}	Storage temperature	- 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level input voltage	2		V
V_{IL} Low-level input voltage		0.8	V
V_I Input voltage	0	5.5	V
V_O Output voltage	0	V_{CC}	V
I_{OH} High-level output current		-8	
I_{OL} Low-level output current		8	
$\Delta t / \Delta v$ Input transition rise or fall time		20	ns/V
T_A Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

4.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHCT138Q-Q1			UNIT
	BQB (WQFN)	D (SOIC)	PW (TSSOP)	
	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	105.6	73	135.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\mu\text{A}$	4.5V	4.4	4.5		4.4		V
	$I_{OH} = -8\text{mA}$		3.94			3.8		
V_{OL}	$I_{OL} = 50\mu\text{A}$	4.5V			0.1		0.1	V
	$I_{OL} = 8\text{mA}$				0.36		0.5	
I_I	$V_I = 5.5\text{V}$ or GND	0 V to 5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5V			4		40	μA
ΔI_{CC} 1	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5V			1.35		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5V		2	10			pF

1. This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0V or V_{CC} .

4.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5\text{V} \pm 0.5\text{V}$ (unless otherwise noted) See [Load Circuit and Voltage Waveforms](#)

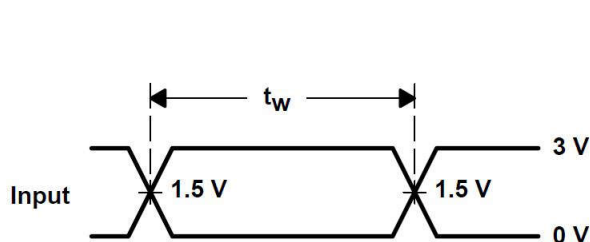
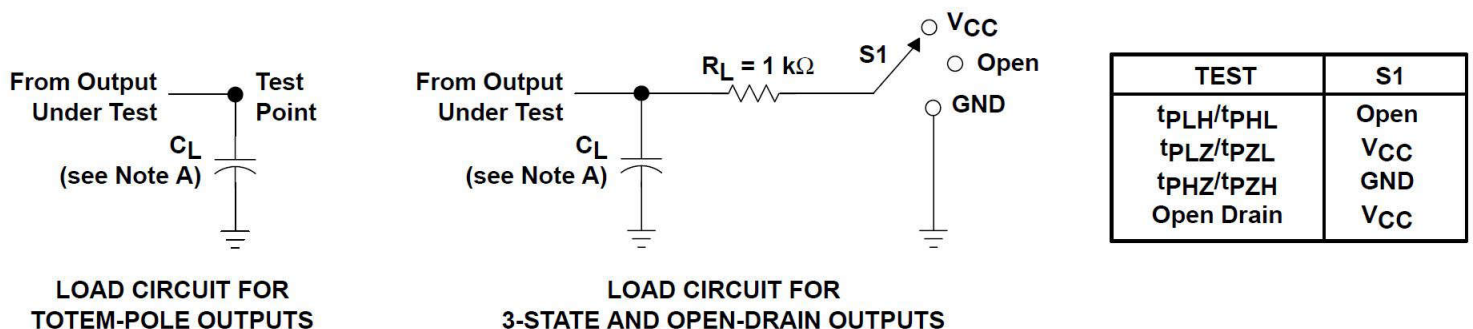
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A, B, C	Any Y	$C_L = 15\text{ pF}$		7.6	10.4	1	12	ns
t_{PHL}					7.6	10.4	1	12	
t_{PLH}	G1	Any Y	$C_L = 15\text{ pF}$		6.6	9.1	1	10.5	ns
t_{PHL}					6.6	9.1	1	10.5	
t_{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	$C_L = 15\text{ pF}$		7	9.6	1	11	ns
t_{PHL}					7	9.6	1	11	
t_{PLH}	A, B, C	Any Y	$C_L = 50\text{ pF}$		8.1	11.4	1	13	ns
t_{PHL}					8.1	11.4	1	13	
t_{PLH}	G1	Any Y	$C_L = 50\text{ pF}$		7.1	10.1	1	11.5	ns
t_{PHL}					7.1	10.1	1	11.5	
t_{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	$C_L = 50\text{ pF}$		7.5	10.6	1	12	ns
t_{PHL}					7.5	10.6	1	12	

4.7 Operating Characteristics

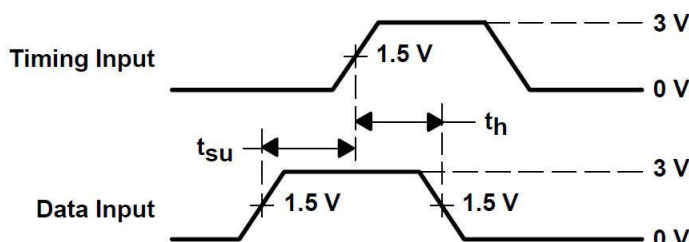
$V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1MHz$	14	pF

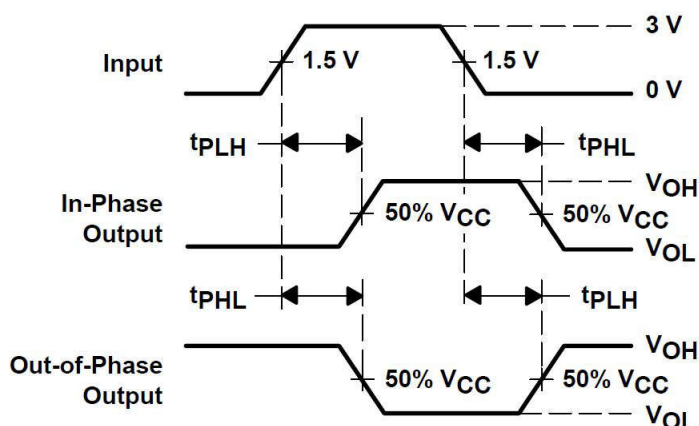
5 Parameter Measurement Information



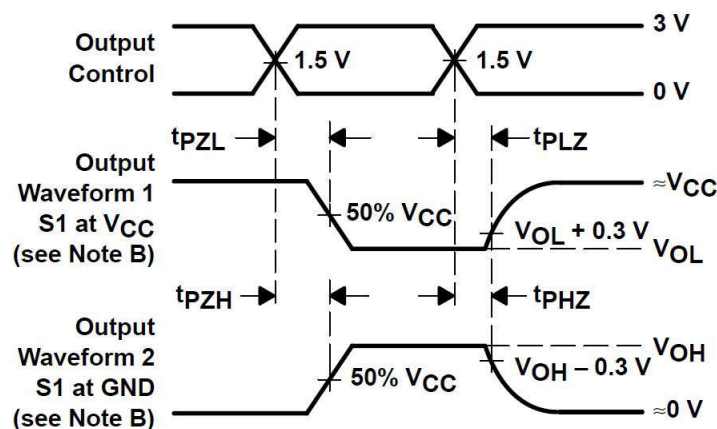
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- E. The outputs are measured one at a time with one input transition per measurement.

图 5-1. Load Circuit and Voltage Waveforms

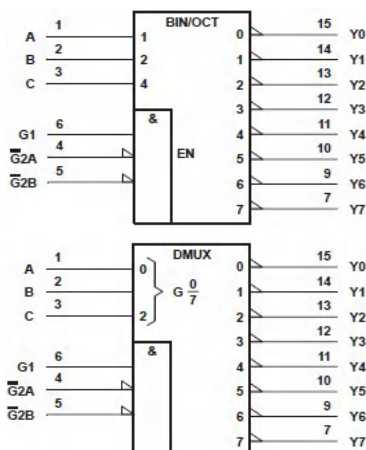
6 Detailed Description

6.1 Overview

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

6.2 Functional Block Diagram

Logic Symbols (Alternatives)



6.3 Device Functional Modes

表 6-1. Function Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

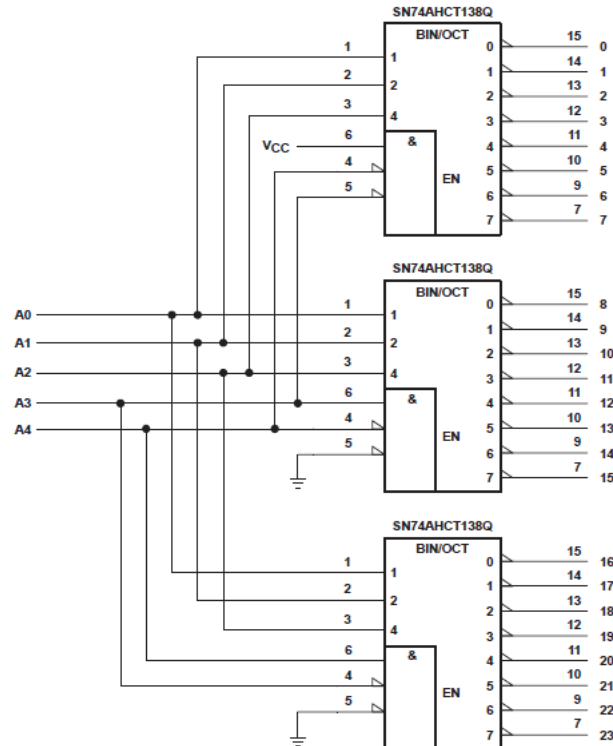


图 7-1. 24-Bit Decoding Scheme

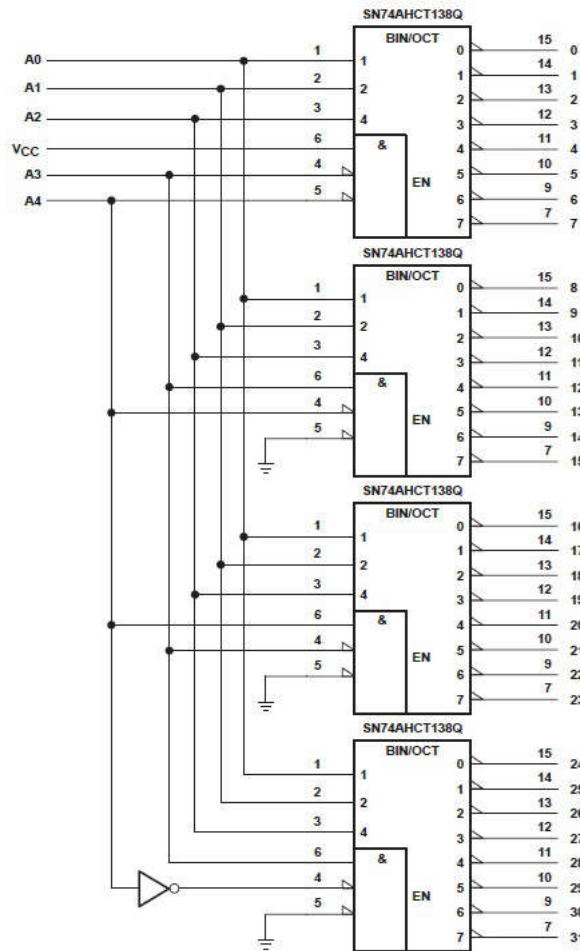


图 7-2. 32-Bit Decoding Scheme

7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [节 4.3](#).

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ bypass capacitor is recommended to be placed close to the V_{CC} terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise; $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

7.3 Layout

7.3.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace (resulting in the reflection). It is a given that not all PCB traces can be straight, and so they have to turn corners. [图 7-3](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

7.3.2 Layout Example

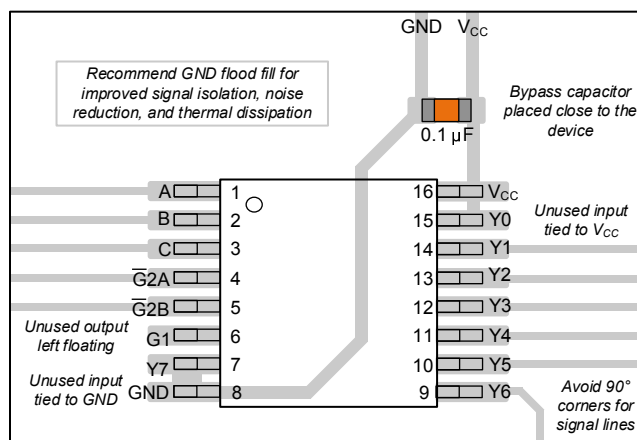


图 7-3. Example Layout for the SN74AHCT138Q-Q1

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

8.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT138Q-Q1	Click here	Click here	Click here	Click here	Click here

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (February 2002) to Revision B (March 2024)	Page
• 向封装信息表、引脚配置和功能以及热性能信息表中添加了 BQB 封装.....	1
• Updated thermal value for PW package from R _{θJA} = 108 to 135.9; added R _{θJC(top)} , ΨJT, ΨJB, all values in °C/W	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAHCT138QPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB138Q	Samples
SN74AHCT138QDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT138Q	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAHCT138QPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAHCT138QPWRG4Q1	TSSOP	PW	16	2000	356.0	356.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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NOTES:

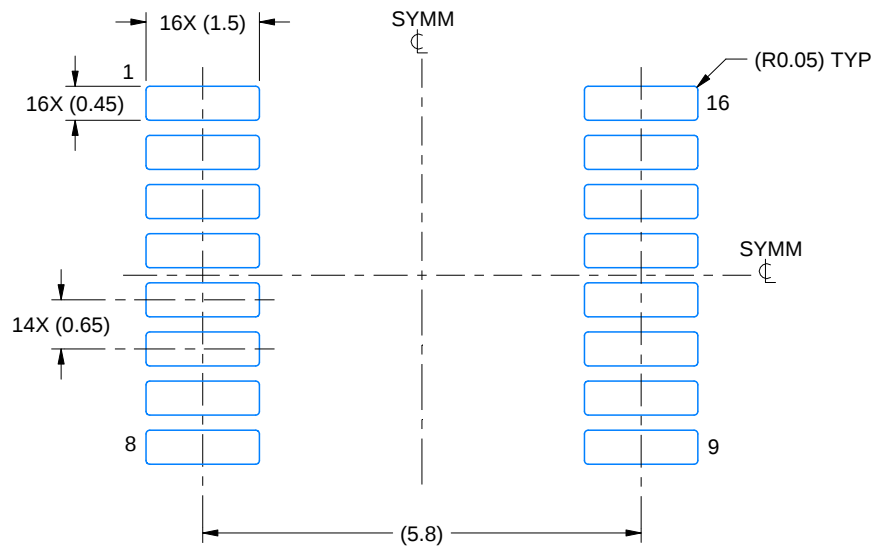
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

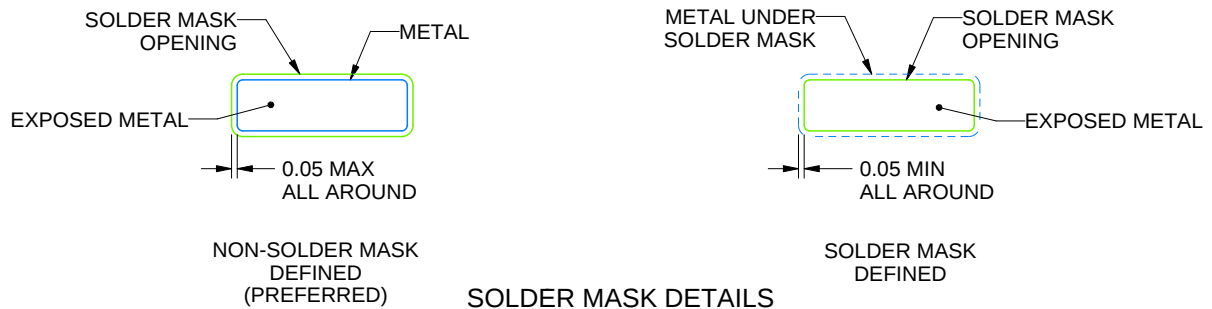
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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