

# SN74AHC367 具有三态输出的六通道缓冲器和线路驱动器

## 1 特性

- 工作范围为 2V 至 5.5V  $V_{CC}$
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

## 2 应用

- 启用或禁用数字信号
- 控制指示灯 LED
- 通信模块和系统控制器之间的转换

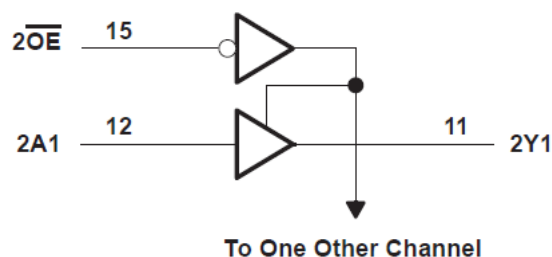
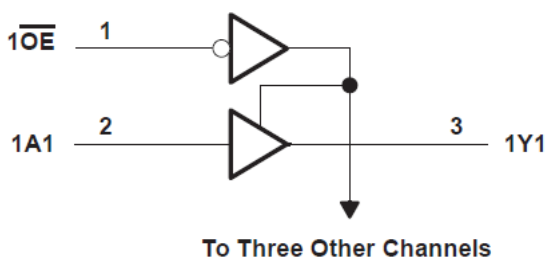
## 3 说明

'AHC367 器件是六通道缓冲器和线路驱动器，可在 2V 至 5.5V  $V_{CC}$  电压下运行。

### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 <sup>(3)</sup>
SN74AHC367	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	N (PDIP, 16)	19.3mm × 9.4mm	19.3mm × 6.35mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.4mm

- 如需了解更多信息，请参阅机械、封装和可订购信息。
- 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



逻辑图 (正逻辑)



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## 4 Pin Configurations and Functions

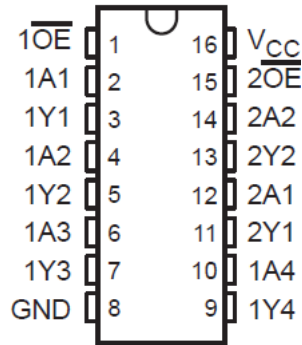


图 4-1. D, DB, DGV, N, or PW Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	Output Enable 1
2	1A1	I	1A1 Input
3	1Y1	O	1Y1 Output
4	1A2	I	1A2 Input
5	1Y2	O	1Y2 Output
6	1A3	I	1A3 Input
7	1Y3	O	1Y3 Output
8	GND	—	Ground Pin
9	1Y4	O	1Y4 Output
10	1A4	I	1A4 Input
11	2Y1	O	2Y1 Output
12	2A1	I	2A1 Input
13	2Y2	O	2Y2 Output
14	2A2	I	2A2 Input
15	2 $\overline{OE}$	I	Output Enable 2
16	V <sub>CC</sub>	—	Power Pin

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	- 0.5	7	V
V <sub>I</sub> <sup>(2)</sup>	Input voltage range	- 0.5	7	V
V <sub>O</sub> <sup>(2)</sup>	Output voltage range	- 0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0)	- 20	mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0)	±20	mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±75	mA
T <sub>stg</sub>	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-Body Model (A114-A), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-Device Model (C101), per JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 3 V	2.1	
		V <sub>CC</sub> = 5.5 V	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 3 V	0.9	
		V <sub>CC</sub> = 5.5 V	1.65	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	- 50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	- 4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V	- 8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V	20	
T <sub>A</sub>	Operating free-air temperature	- 40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHC367					UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	73	82	120	67	135.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN74AHC367		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58		2.48			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94		3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			± 0.1	± 1	μA	
I <sub>OZ</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = V <sub>CC</sub> or GND, $\overline{OE}$ = V <sub>IH</sub>	5.5 V			± 0.25	± 2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4	40	μA	
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3	10	10	pF	
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		5.1			pF	

## 5.6 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN74AHC367		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		4.7 <sup>1</sup>	8.3 <sup>1</sup>	1	10	ns
t <sub>PHL</sub>					4.7 <sup>1</sup>	8.3 <sup>1</sup>	1	10	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		5.1 <sup>1</sup>	10.5 <sup>1</sup>	1	12.5	ns
t <sub>PZL</sub>					5.1 <sup>1</sup>	10.5 <sup>1</sup>	1	12.5	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		4 <sup>1</sup>	10.5 <sup>1</sup>	1	12.5	ns
t <sub>PLZ</sub>					4.9 <sup>1</sup>	10.5 <sup>1</sup>	1	12.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		6.1	11.8	1	13.5	ns
t <sub>PHL</sub>					6.2	11.8	1	13.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		6.4	14	1	16	ns
t <sub>PZL</sub>					6.8	14	1	16	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		6.2	13.6	1	15.5	ns
t <sub>PLZ</sub>					7.3	13.6	1	15.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74AHC367		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$		3.4 <sup>1</sup>	5.9 <sup>1</sup>	1	7	ns
$t_{PHL}$					3.6 <sup>1</sup>	5.9 <sup>1</sup>	1	7	
$t_{PZH}$	OE	Y	$C_L = 15\text{ pF}$		3.6 <sup>1</sup>	7.2 <sup>1</sup>	1	8.5	ns
$t_{PZL}$					3.8 <sup>1</sup>	7.2 <sup>1</sup>	1	8.5	
$t_{PHZ}$	OE	Y	$C_L = 15\text{ pF}$		2.6 <sup>1</sup>	7.2 <sup>1</sup>	0	8.5	ns
$t_{PLZ}$					2.6 <sup>1</sup>	7.2 <sup>1</sup>	0	8.5	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$		4.3	7.9	1	9	ns
$t_{PHL}$					4.5	7.9	1	9	
$t_{PZH}$	OE	Y	$C_L = 50\text{ pF}$		4.6	9.2	1	10.5	ns
$t_{PZL}$					4.9	9.2	1	10.5	
$t_{PHZ}$	OE	Y	$C_L = 50\text{ pF}$		3.4	9.2	0	10.5	ns
$t_{PLZ}$					4.5	9.2	0	10.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.8 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

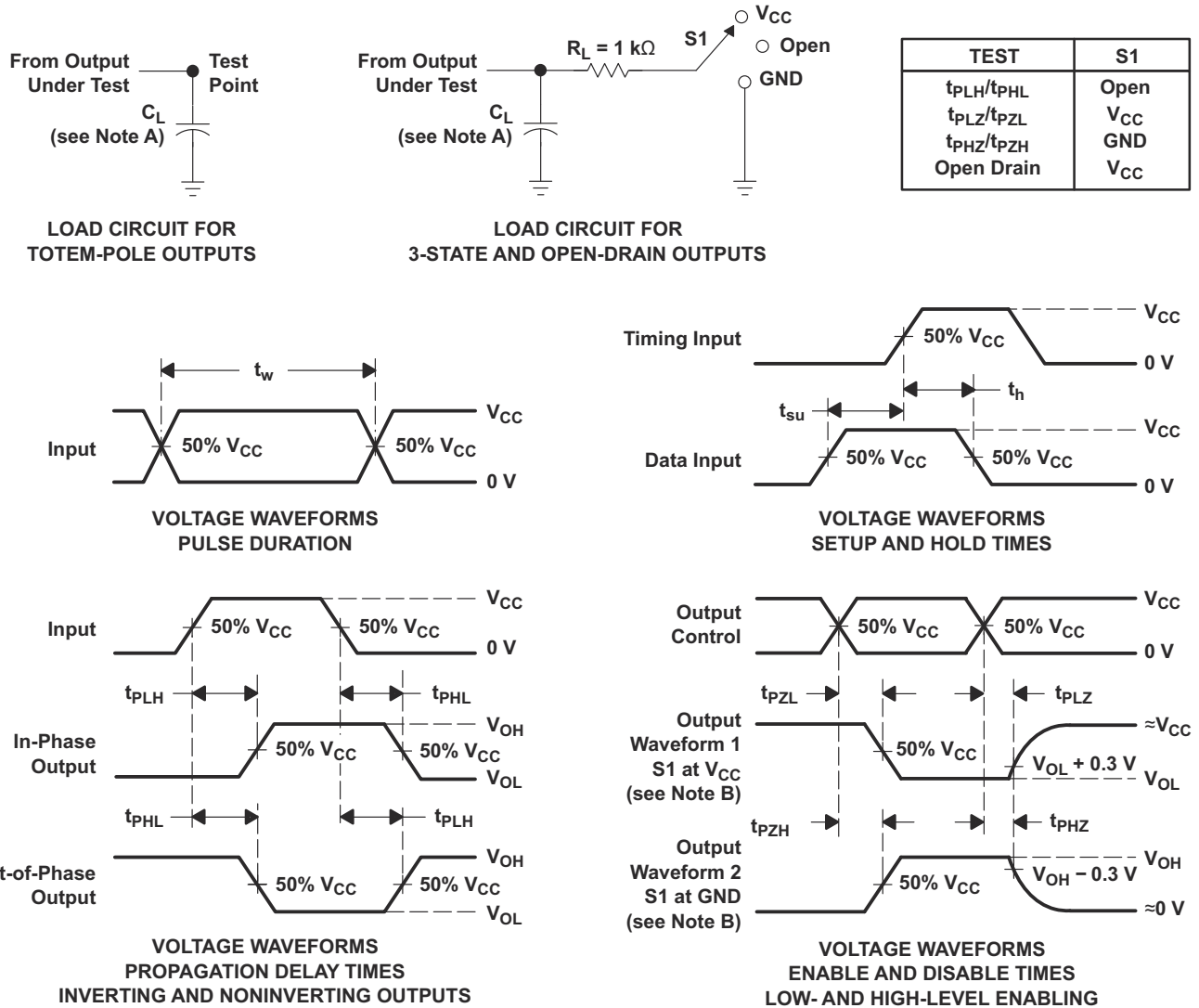
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.2		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

## 5.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load,	$f = 1\text{ MHz}$	22.4	pF

## 6 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_0 = 50 \ \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'AHC367 devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ( $1\overline{OE}$  and  $2\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes noninverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 7.2 Functional Block Diagram



图 7-1. Logic Diagram (Positive Logic)

### 7.3 Device Functional Modes

表 7-1. Function Table  
(Each Buffer/ Driver)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z



## 8 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in [Block Diagram](#). The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74AHC367 is used to directly control the **RESET** pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

### 8.2 Typical Application

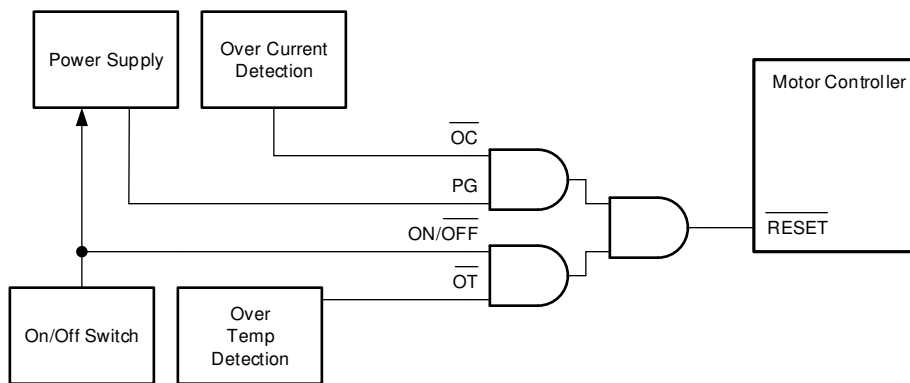


图 8-1. Typical Application Block Diagram

### 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

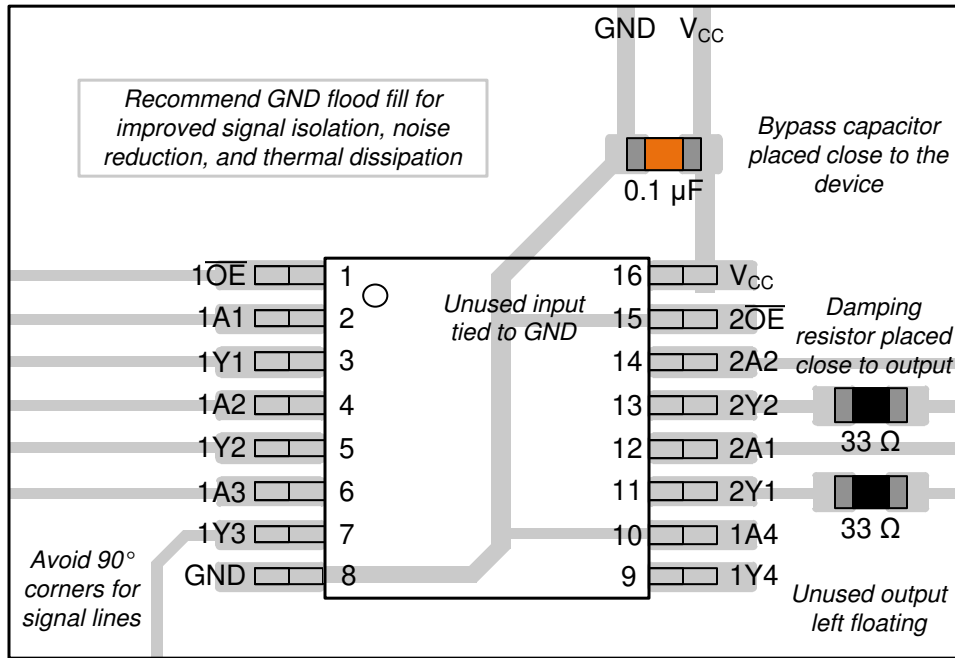


图 8-2. Example Layout for the SN74AHC367

## 9 Device and Documentation Support

### 9.1 Documentation Support (Analog)

#### 9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 9-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC367	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

### Changes from Revision F (November 2023) to Revision G (July 2024) Page

- Updated R<sub>θ</sub> JA value: PW = 108 to 135.9, all values in °C/W .....5

### Changes from Revision E (February 2002) to Revision F (November 2023) Page

- 添加了应用部分、封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、应用和实施部分、器件和文档支持部分以及机械、封装和可订购信息部分 .....1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC367D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	AHC367	
SN74AHC367DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC367	Samples
SN74AHC367N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC367N	Samples
SN74AHC367PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA367	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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