

## SN65HVD308xE 低功耗 RS-485 全双工驱动器和接收器

### 1 特性

- 低静态功率
  - 375  $\mu$ A (典型值) 使能模式
  - 2nA (典型值) 关断模式
- 小型 MSOP 封装
- 1/8 单位负载：每个总线多达 256 个节点
- 16kV 总线引脚 ESD 保护, 6kV 所有引脚
- 失效保护接收器 (总线开路、短路及空闲状态)
- 符合 TIA/EIA-485A 标准
- 兼容 RS-422
- 加电、断电无毛刺脉冲运行

### 2 应用

- 运动控制器
- 销售点 (POS) 终端
- 机架到机架通信
- 工业网络
- 电源逆变器
- 电池供电型应用
- 楼宇自动化

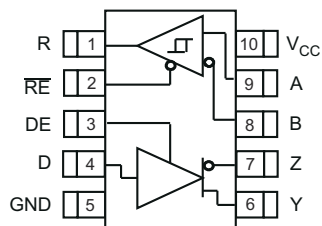
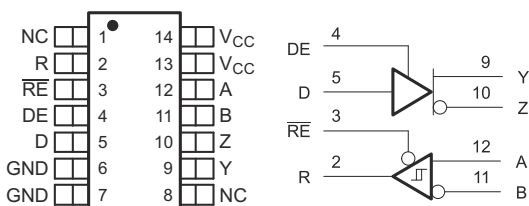


图 2-1. DGS 封装 (顶视图)



NC - No internal connection  
Pins 6 and 7 are connected together internally  
Pins 13 and 14 are connected together internally

图 2-2. D 封装 (顶视图)

### 3 说明

这些器件均为平衡驱动器和接收器，专为全双工 RS-485 或 RS-422 数据总线网络而设计。由 5V 电源供电，完全符合 TIA/EIA-485A 标准。

器件具有受控的总线输出转换时间，适合于 200kbps 至 20Mbps 的信号传输速率。

设计初衷是在低电源电流 (典型值不到 1 mA, 不包括负载) 下工作。在非活动关断模式下，电源电流可降至几纳安，因此这些器件非常适合对功率敏感的应用。

这些器件具有宽共模范围和高 ESD 保护级别，因此适用于各种要求苛刻的应用，例如运动控制器、电气逆变器、工业网络，以及噪声容限至关重要的有线机箱互连。

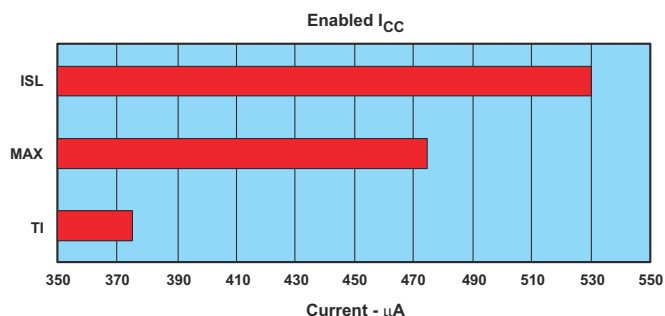
其额定运行温度范围为 -40°C 至 85°C。

#### 器件信息

| 器件型号         | 信令速率    | 封装 <sup>(1)</sup>                  |
|--------------|---------|------------------------------------|
| SN65HVD3080E | 200kbps | DGS、DGSR 10 引脚 MSOP <sup>(2)</sup> |
| SN65HVD3083E | 1Mbps   |                                    |
| SN65HVD3086E | 20Mbps  | D 14 引脚 SOIC                       |

(1) 如需了解最新的封装及订购信息，请参见本文件结尾处的“Package Option Addendum (封装选项附录)”，或登录 TI 的网站 [www.ti.com](http://www.ti.com) 进行查询。

(2) R 后缀表示卷带。



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| <b>Changes from Revision E (November 2012) to Revision F (March 2023)</b> | <b>Page</b> |
|---------------------------------------------------------------------------|-------------|
| • 删除了“订购信息”表.....                                                         | <b>1</b>    |
| • 添加了器件信息表.....                                                           | <b>1</b>    |
| • Added the <i>Thermal Information</i> table.....                         | <b>4</b>    |
| • Changed the <i>Typical Characteristics</i> .....                        | <b>7</b>    |

| <b>Changes from Revision D (January 2011) to Revision E (November 2012)</b> | <b>Page</b> |
|-----------------------------------------------------------------------------|-------------|
| • 向 <i>特性</i> 中添加了“加电、断电无毛刺脉冲运行” .....                                      | <b>1</b>    |
| • Changed ENABLE in DRIVER FUNCTION TABLE from L to L or OPEN.....          | <b>11</b>   |
| • Changed ENABLE in RECEIVER FUNCTION TABLE from H to H or OPEN.....        | <b>11</b>   |
| • Added <i>Application Information</i> section.....                         | <b>13</b>   |

| <b>Changes from Revision C (December 2009) to Revision D (January 2011)</b>         | <b>Page</b> |
|-------------------------------------------------------------------------------------|-------------|
| • Added Differential input voltage dynamic to RECOMMENDED OPERATING CONDITIONS..... | <b>4</b>    |
| • Added 图 7-1 .....                                                                 | <b>11</b>   |

| <b>Changes from Revision B (March 2007) to Revision C ( )</b>   | <b>Page</b> |
|-----------------------------------------------------------------|-------------|
| • 添加了 D 封装.....                                                 | <b>1</b>    |
| • Added D package information to Power Dissipation Ratings..... | <b>3</b>    |
| • Changed Electrostatic Discharge Protection.....               | <b>3</b>    |
| • Changed Supply Current information.....                       | <b>4</b>    |
| • Changed Receiver Switching Characteristics.....               | <b>6</b>    |
| • Changed 图 6-5 .....                                           | <b>8</b>    |
| • Changed 图 6-6 .....                                           | <b>8</b>    |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

|                                      |                                                                                  | UNIT                             |
|--------------------------------------|----------------------------------------------------------------------------------|----------------------------------|
| $V_{CC}$                             | Supply voltage range <sup>(2)</sup>                                              | – 0.3 V to 7 V                   |
| $V_{(A)}, V_{(B)}, V_{(Y)}, V_{(Z)}$ | Voltage range at any bus terminal (A, B, Y, Z)                                   | – 9 V to 14 V                    |
| $V_{(TRANS)}$                        | Voltage input, transient pulse through 100 $\Omega$ .<br>See 图 6-10 (A, B, Y, Z) | – 50 to 50 V                     |
| $V_I$                                | Input voltage range (D, DE, RE)                                                  | –0.3 V to $V_{CC}+0.3$ V         |
| $P_D$                                | Continuous total power dissipation                                               | See the dissipation rating table |
| $T_J$                                | Junction temperature                                                             | 170°C                            |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

### 5.2 Power Dissipation Ratings

| PACKAGE           | $T_A < 25^\circ\text{C}$ | DERATING FACTOR <sup>(1)</sup><br>ABOVE $T_A < 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ |
|-------------------|--------------------------|------------------------------------------------------------------|--------------------------|
| 10-pin MSOP (DGS) | 463 mW                   | 3.71 mW/°C                                                       | 241 mW                   |
| 14-pin SOIC (D)   | 765 mW                   | 6.1 mW/°C                                                        | 400 mW                   |

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

### 5.3 Electrostatic Discharge Protection

| PARAMETER                          | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|------------------------------------|------------------|-----|-----|-----|------|
| Human Body Model <sup>(1)</sup>    | A,B,Y,Z, and GND |     | 16  |     | kV   |
|                                    | All pins         |     | 6   |     | kV   |
| Charged Device Mode <sup>(2)</sup> | All pins         |     | 1.5 |     | kV   |
| Machine Model <sup>(3)</sup>       | All pins         |     | 400 |     | V    |

- (1) Tested in accordance JEDEC Standard 22, Test Method A114-A. Bus pin stressed with respect to a common connection of GND and  $V_{CC}$ .
- (2) Tested in accordance JEDEC Standard 22, Test Method C101.
- (3) Tested in accordance JEDEC Standard 22, Test Method A115.

## 5.4 Supply Current

over recommended operating conditions unless otherwise noted

| PARAMETER |                | TEST CONDITIONS                                              | MIN                                   | TYP | MAX  | UNIT    |
|-----------|----------------|--------------------------------------------------------------|---------------------------------------|-----|------|---------|
| $I_{CC}$  | Supply current | $\overline{RE}$ at 0 V, D and DE at $V_{CC}$ , No load       | Receiver enabled,<br>Driver enabled   | 375 | 750  | $\mu A$ |
|           |                | $\overline{RE}$ at 0 V, D and DE at 0 V, No load             | Receiver enabled,<br>Driver disabled  | 300 | 680  | $\mu A$ |
|           |                | $\overline{RE}$ at $V_{CC}$ , D and DE at $V_{CC}$ , No load | Receiver disabled,<br>Driver enabled  | 240 | 600  | $\mu A$ |
|           |                | $\overline{RE}$ and D at $V_{CC}$ , DE at 0 V, No load       | Receiver disabled,<br>Driver disabled | 2   | 1000 | nA      |

## 5.5 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

|                   |                                                         |                        | MIN                | NOM | MAX      | UNIT        |
|-------------------|---------------------------------------------------------|------------------------|--------------------|-----|----------|-------------|
| $V_{CC}$          | Supply voltage                                          |                        | 4.5                | 5   | 5.5      | V           |
| $V_I$ or $V_{IC}$ | Voltage at any bus terminal (separately or common mode) |                        | - 7 <sup>(1)</sup> |     | 12       |             |
| $V_{IH}$          | High-level input voltage                                | D, DE, $\overline{RE}$ | 2                  |     | $V_{CC}$ | V           |
| $V_{IL}$          | Low-level input voltage                                 | D, DE, $\overline{RE}$ | 0                  |     | 0.8      |             |
| $V_{ID}$          | Differential input voltage                              |                        | - 12               |     | 12       | V           |
|                   |                                                         | Dynamic, See 图 7-1     |                    |     |          | V           |
| $I_{OH}$          | High-level output current                               | Driver                 | - 60               |     |          | mA          |
|                   |                                                         | Receiver               | - 10               |     |          |             |
| $I_{OL}$          | Low-level output current                                | Driver                 |                    |     | 60       | mA          |
|                   |                                                         | Receiver               |                    |     | 10       |             |
| $T_J$             | Junction temperature                                    |                        |                    |     | 150      | $^{\circ}C$ |
| $T_A$             | Ambient still-air temperature                           |                        | - 40               |     | 85       |             |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## 5.6 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | D (SOIC) | DGS (VSSOP) | UNIT          |
|-------------------------------|----------------------------------------------|----------|-------------|---------------|
|                               |                                              | 14 PINS  | 10 PINS     |               |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 93.2     | 75.8        | $^{\circ}C/W$ |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 47.5     | 22.0        | $^{\circ}C/W$ |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 49.4     | 44.9        | $^{\circ}C/W$ |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 11.2     | 1.0         | $^{\circ}C/W$ |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 48.9     | 44.3        | $^{\circ}C/W$ |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.7 Driver Electrical Characteristics

over recommended operating conditions unless otherwise noted

| PARAMETER                                                                  | TEST CONDITIONS                                                                          | MIN  | TYP | MAX             | UNIT |
|----------------------------------------------------------------------------|------------------------------------------------------------------------------------------|------|-----|-----------------|------|
| V <sub>OD</sub>   Differential output voltage                              | No load, I <sub>O</sub> = 0                                                              | 3    | 4.3 | V <sub>CC</sub> | V    |
|                                                                            | R <sub>L</sub> = 54 Ω, See 图 6-1                                                         | 1.5  | 2.3 |                 |      |
|                                                                            | V <sub>test</sub> = -7 V to 12 V, See 图 6-2                                              | 1.5  |     |                 |      |
|                                                                            | R <sub>L</sub> = 100 Ω, See 图 6-1                                                        | 2    |     |                 |      |
| Δ V <sub>OD</sub>   Change in magnitude of differential output voltage     | R <sub>L</sub> = 54 Ω, See 图 6-1 and 图 6-2                                               | -0.2 | 0   | 0.2             | V    |
| V <sub>OC(SS)</sub> Steady-state common-mode output voltage                | See 图 6-3                                                                                | 1    | 2.6 | 3               | V    |
| ΔV <sub>OC(SS)</sub> Common-mode output voltage (Dominant)                 |                                                                                          | -0.1 | 0   | 0.1             |      |
| V <sub>OC(PP)</sub> Peak-to-peak common-mode output voltage                |                                                                                          |      | 0.5 |                 |      |
| I <sub>Z(Y)</sub> or I <sub>Z(Z)</sub> High-impedance state output current | V <sub>CC</sub> = 0 V, V <sub>(Z)</sub> or V <sub>(Y)</sub> = 12 V<br>Other input at 0 V |      |     | 1               | μA   |
|                                                                            | V <sub>CC</sub> = 0 V, V <sub>(Z)</sub> or V <sub>(Y)</sub> = -7 V<br>Other input at 0 V | -1   |     |                 |      |
|                                                                            | V <sub>CC</sub> = 5 V, V <sub>(Z)</sub> or V <sub>(Y)</sub> = 12 V<br>Other input at 0 V |      |     | 1               |      |
|                                                                            | V <sub>CC</sub> = 5 V, V <sub>(Z)</sub> or V <sub>(Y)</sub> = -7 V<br>Other input at 0 V | -1   |     |                 |      |
| I <sub>I</sub> Input current                                               | D, DE                                                                                    | -100 |     | 100             | μA   |
| I <sub>OS</sub> Short-circuit output current                               | -7 V ≤ V <sub>O</sub> ≤ 12 V                                                             | -250 |     | 250             | mA   |

## 5.8 Driver Switching Characteristics

over recommended operating conditions unless otherwise noted

| PARAMETER                                                                                                                                                                  | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|-----|-----|-----|------|
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> Propagation delay time, low-to-high-level output<br>Propagation delay time, high-to-low-level output                                | HVD3080E                                       |     | 0.7 | 1.3 | μs   |
|                                                                                                                                                                            | HVD3083E                                       |     | 150 | 500 | ns   |
|                                                                                                                                                                            | HVD3086E                                       |     | 12  | 20  | ns   |
| t <sub>r</sub> ,<br>t <sub>f</sub> Differential output signal rise time<br>Differential output signal fall time                                                            | HVD3080E                                       | 0.5 | 0.9 | 1.5 | μs   |
|                                                                                                                                                                            | HVD3083E                                       |     | 200 | 300 | ns   |
|                                                                                                                                                                            | HVD3086E                                       |     | 7   | 15  | ns   |
| t <sub>sk(p)</sub> Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )                                                                                                     | HVD3080E                                       |     | 20  | 200 | ns   |
|                                                                                                                                                                            | HVD3083E                                       |     | 5   | 50  | ns   |
|                                                                                                                                                                            | HVD3086E                                       |     | 1.4 | 5   | ns   |
| t <sub>PZH</sub> Propagation delay time,<br>high-impedance-to-high-level output                                                                                            | HVD3080E                                       |     | 2.5 | 7   | μs   |
|                                                                                                                                                                            | HVD3083E                                       |     | 1   | 2.5 | μs   |
|                                                                                                                                                                            | HVD3086E                                       |     | 13  | 30  | ns   |
| t <sub>PHZ</sub> Propagation delay time,<br>high-level-to-high-impedance output                                                                                            | HVD3080E                                       |     | 80  | 200 | ns   |
|                                                                                                                                                                            | HVD3083E                                       |     | 60  | 100 | ns   |
|                                                                                                                                                                            | HVD3086E                                       |     | 12  | 30  | ns   |
| t <sub>PZL</sub> Propagation delay time, high-impedance-to-low-level<br>output                                                                                             | HVD3080E                                       |     | 2.5 | 7   | μs   |
|                                                                                                                                                                            | HVD3083E                                       |     | 1   | 2.5 | μs   |
|                                                                                                                                                                            | HVD3086E                                       |     | 13  | 30  | ns   |
| t <sub>PLZ</sub> Propagation delay time, low-level-to-high-impedance<br>output                                                                                             | HVD3080E                                       |     | 80  | 200 | ns   |
|                                                                                                                                                                            | HVD3083E                                       |     | 60  | 100 | ns   |
|                                                                                                                                                                            | HVD3086E                                       |     | 12  | 30  | ns   |
| t <sub>PZH</sub> ,<br>t <sub>PZL</sub> Propagation delay time, standby-to-high-level output (See 图 6-5)<br>Propagation delay time, standby-to-low-level output (See 图 6-6) | R <sub>L</sub> = 110 Ω, $\overline{RE}$ at 3 V |     | 3.5 | 7   | μs   |

## 5.9 Receiver Electrical Characteristics

over recommended operating conditions unless otherwise noted

| PARAMETER        |                                                           | TEST CONDITIONS                                                             | MIN                                                            | TYP <sup>(1)</sup> | MAX    | UNIT   |    |
|------------------|-----------------------------------------------------------|-----------------------------------------------------------------------------|----------------------------------------------------------------|--------------------|--------|--------|----|
| V <sub>IT+</sub> | Positive-going differential input threshold voltage       | I <sub>O</sub> = - 10 mA                                                    |                                                                | -0.08              | - 0.01 | V      |    |
| V <sub>IT-</sub> | Negative-going differential input threshold voltage       | I <sub>O</sub> = 10 mA                                                      | - 0.2                                                          | -0.1               |        |        |    |
| V <sub>hys</sub> | Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> ) |                                                                             |                                                                | 30                 |        | mV     |    |
| V <sub>OH</sub>  | High-level output voltage                                 | V <sub>ID</sub> = 200 mV, I <sub>OH</sub> = - 10 mA,<br>See 图 6-7 and 图 6-8 | 4                                                              | 4.6                |        | V      |    |
| V <sub>OL</sub>  | Low-level output voltage                                  | V <sub>ID</sub> = - 200 mV, I <sub>OH</sub> = 10 mA,<br>See 图 6-7 and 图 6-8 |                                                                | 0.15               | 0.4    | V      |    |
| I <sub>OZ</sub>  | High-impedance-state output current                       | V <sub>O</sub> = 0 or V <sub>CC</sub>                                       | - 1                                                            |                    | 1      | μA     |    |
| I <sub>I</sub>   | Bus input current                                         | Other input at 0V                                                           | V <sub>A</sub> or V <sub>B</sub> = 12 V                        |                    | 0.04   | 0.11   | mA |
|                  |                                                           |                                                                             | V <sub>A</sub> or V <sub>B</sub> = 12 V, V <sub>CC</sub> = 0 V |                    | 0.06   | 0.13   |    |
|                  |                                                           |                                                                             | V <sub>A</sub> or V <sub>B</sub> = -7 V                        |                    | - 0.1  | - 0.04 |    |
|                  |                                                           |                                                                             | V <sub>A</sub> or V <sub>B</sub> = -7 V, V <sub>CC</sub> = 0 V |                    | - 0.05 | - 0.03 |    |
| I <sub>IH</sub>  | High-level input current                                  | V <sub>IH</sub> = 2 V                                                       | - 60                                                           | -30                |        | μA     |    |
| I <sub>IL</sub>  | Low-level input current                                   | V <sub>IL</sub> = 0.8 V                                                     | -60                                                            | -30                |        | μA     |    |
| C <sub>ID</sub>  | Differential input capacitance                            | V <sub>I</sub> = 0.4 sin (4E6 π t) + 0.5 V                                  |                                                                | 7                  |        | pF     |    |

(1) All typical values are at 25°C and with a 3.3-V supply.

## 5.10 Receiver Switching Characteristics

over recommended operating conditions unless otherwise noted

| PARAMETER                              |                                                     | TEST CONDITIONS                                                         | MIN | TYP | MAX | UNIT |
|----------------------------------------|-----------------------------------------------------|-------------------------------------------------------------------------|-----|-----|-----|------|
| t <sub>PLH</sub>                       | Propagation delay time, low-to-high-level output    | V <sub>ID</sub> = -1.5 V to 1.5 V,<br>C <sub>L</sub> = 15 pF, See 图 6-8 |     | 75  | 100 | ns   |
| t <sub>PHL</sub>                       | Propagation delay time, high-to-low-level output    |                                                                         |     | 79  | 100 |      |
| t <sub>sk(p)</sub>                     | Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  ) |                                                                         |     | 4   | 10  |      |
| t <sub>r</sub>                         | Output signal rise time                             |                                                                         |     | 1.5 | 3   |      |
| t <sub>f</sub>                         | Output signal fall time                             |                                                                         |     | 1.8 | 3   |      |
| t <sub>PZH</sub> ,<br>t <sub>PZL</sub> | Output enable time                                  | DE at V <sub>CC</sub> ,<br>See 图 6-9                                    |     | 10  | 50  | ns   |
|                                        |                                                     | From standby<br>DE at GND,<br>See 图 6-9                                 |     | 1.7 | 3.5 | μs   |
| t <sub>PHZ</sub> ,<br>t <sub>PLZ</sub> | Output disable time                                 | DE at GND or V <sub>CC</sub> ,<br>See 图 6-9                             |     | 7   | 50  | ns   |

## 5.11 Typical Characteristics

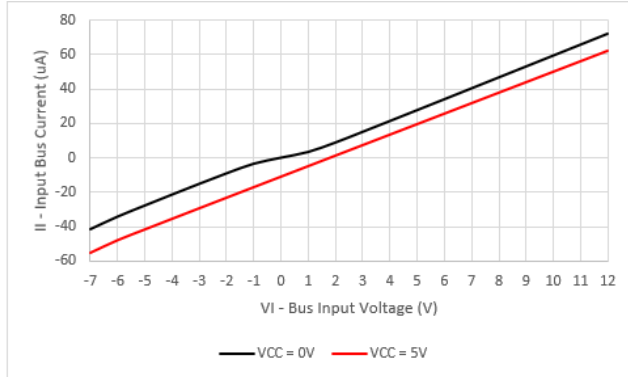


图 5-1. Input Bias Current vs BUS Input Voltage

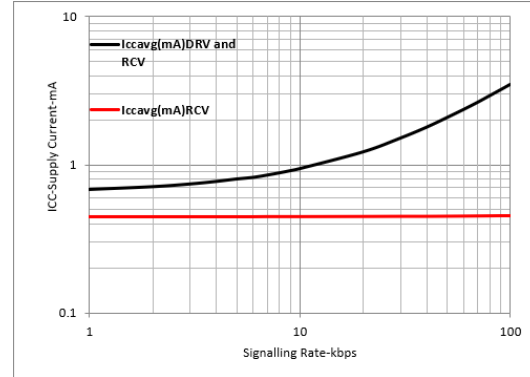


图 5-2. HVD3080E Supply Current vs Signaling Rate

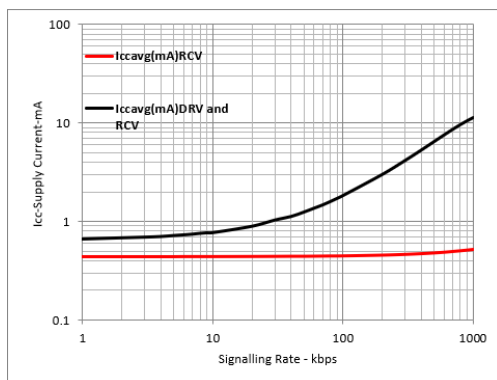


图 5-3. HVD3083E Supply Current vs Signaling Rate

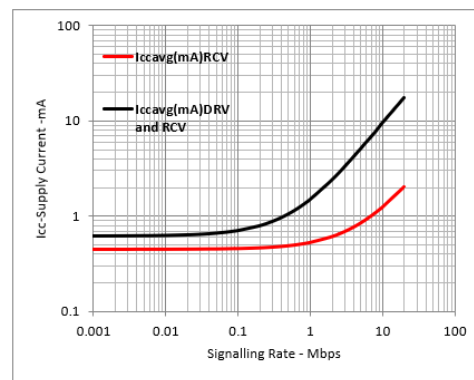


图 5-4. HVD3086E Supply Current vs Signaling Rate

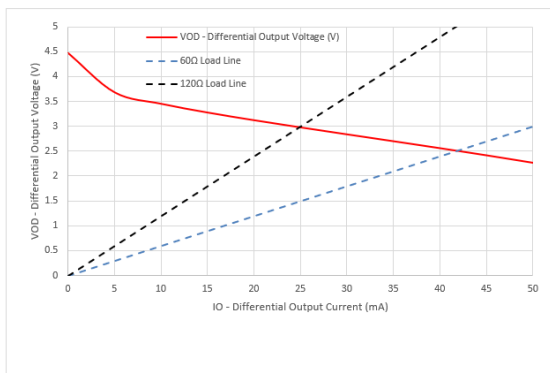


图 5-5. Differential Output Voltage vs Differential Output Current

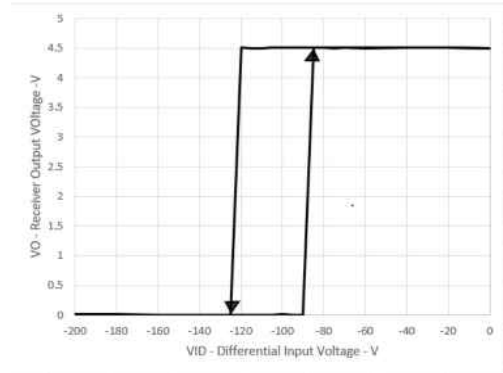
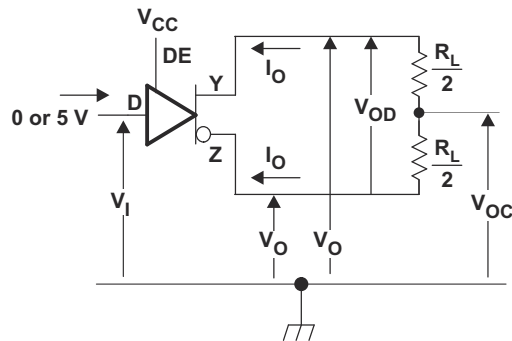
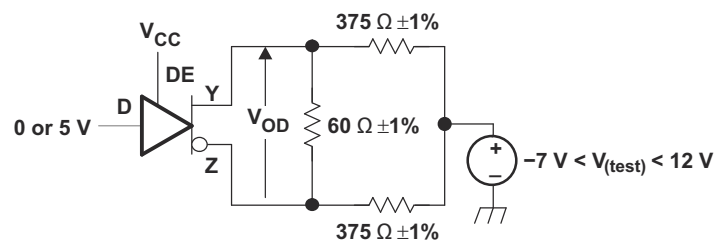


图 5-6. Receiver Output Voltage vs Differential Input Voltage

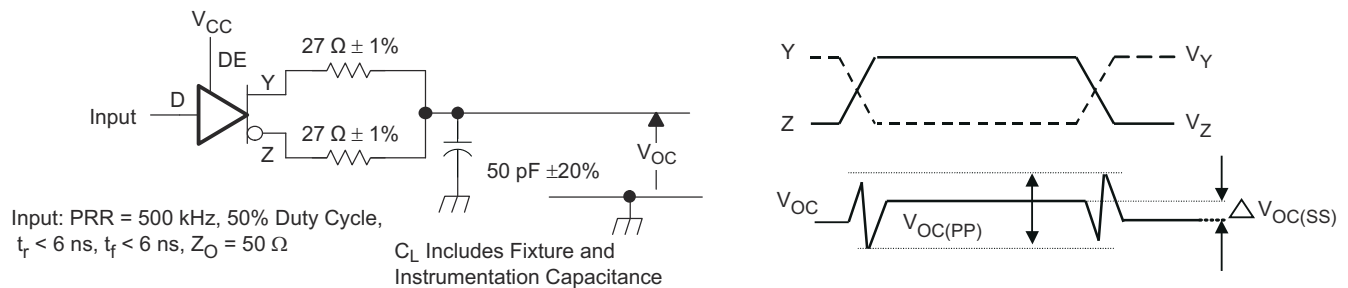
## 6 Parameter Measurement Information



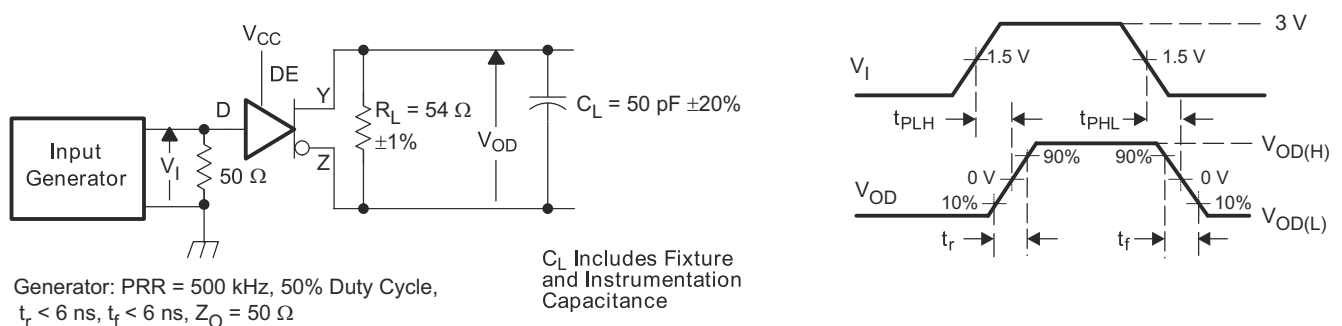
**图 6-1. Driver  $V_{OD}$  Test Circuit and Current Definitions**



**图 6-2. Driver  $V_{OD}$  With Common-Mode Loading Test Circuit**



**图 6-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**



### 图 6-4. Driver Switching Test Circuit and Voltage Waveforms



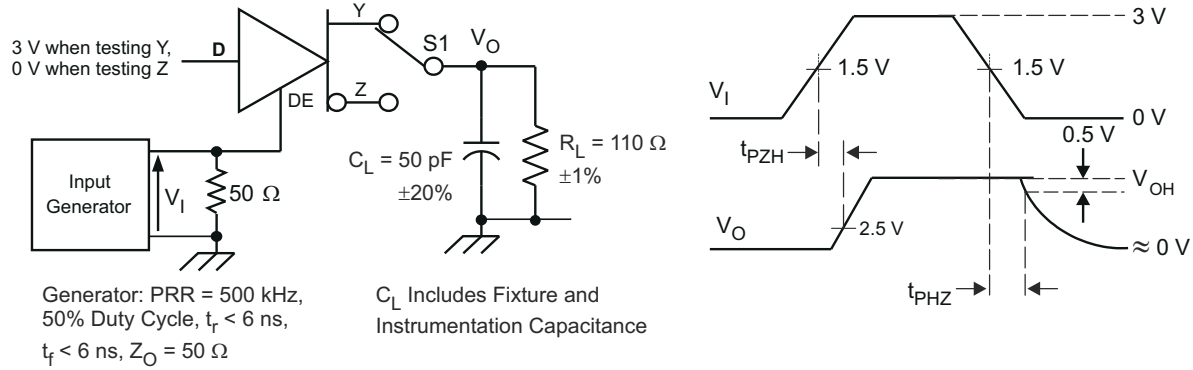


图 6-5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

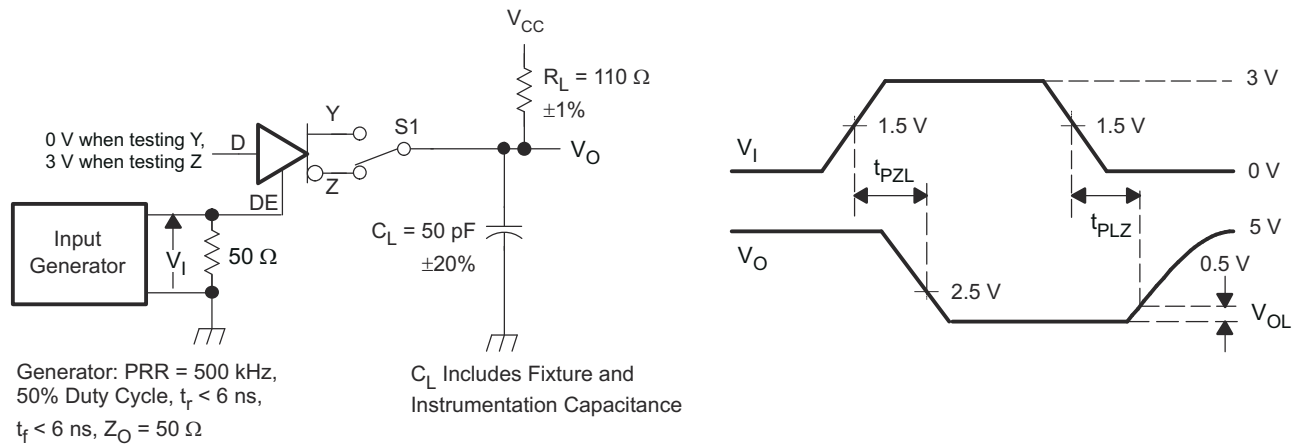


图 6-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

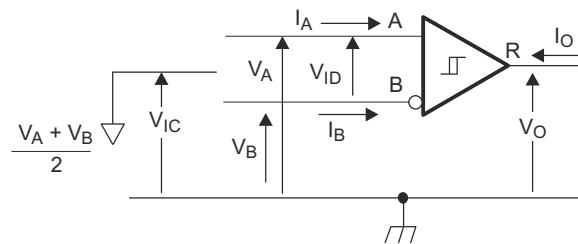


图 6-7. Receiver Voltage and Current Definitions

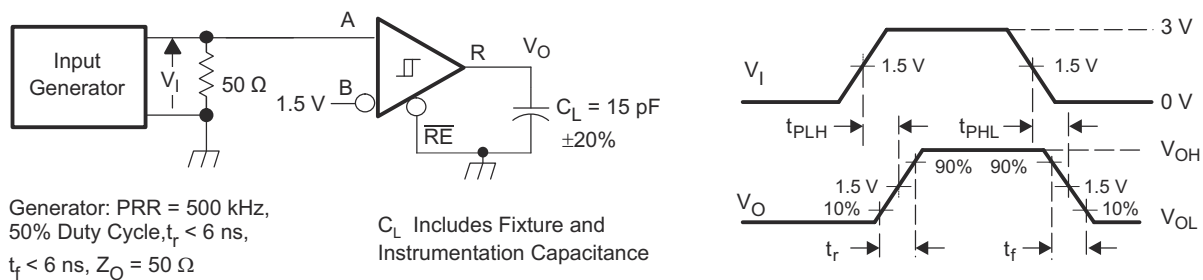


图 6-8. Receiver Switching Test Circuit and Voltage Waveforms

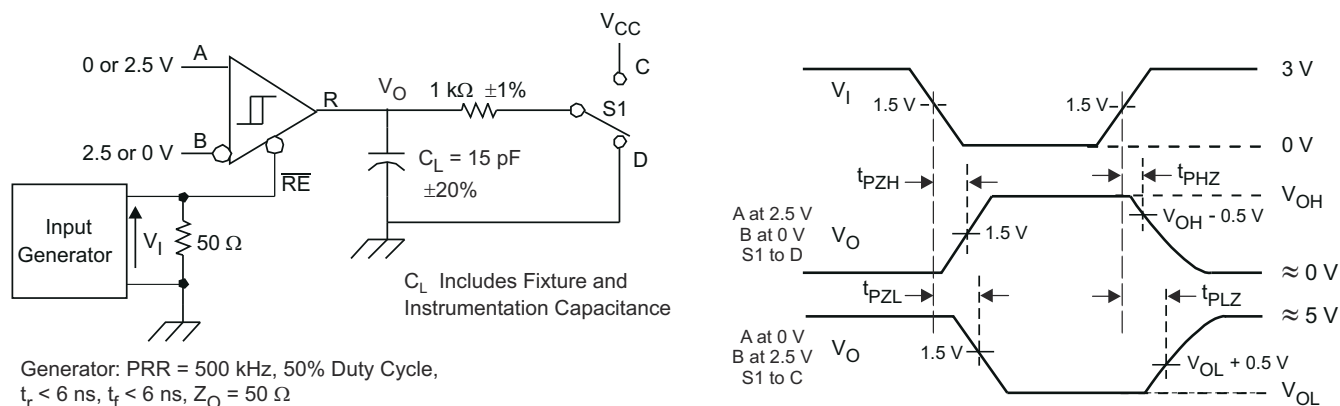
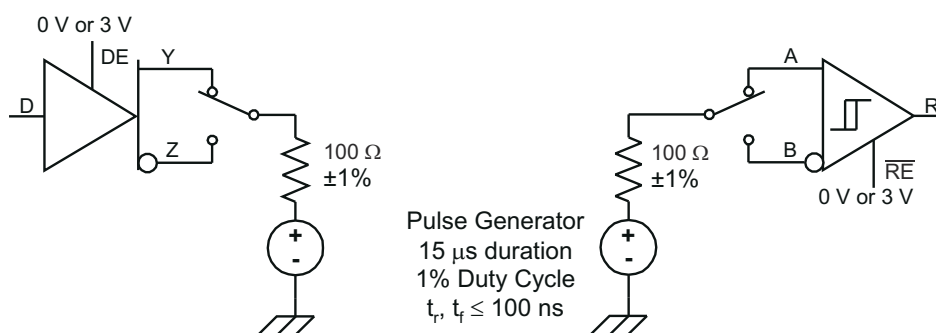


图 6-9. Receiver Enable and Disable Test Circuit and Voltage Waveforms



A. This test is conducted to test survivability only. Data stability at the R output is not specified.

图 6-10. Transient Overvoltage Test Circuit

## 7 Device Information

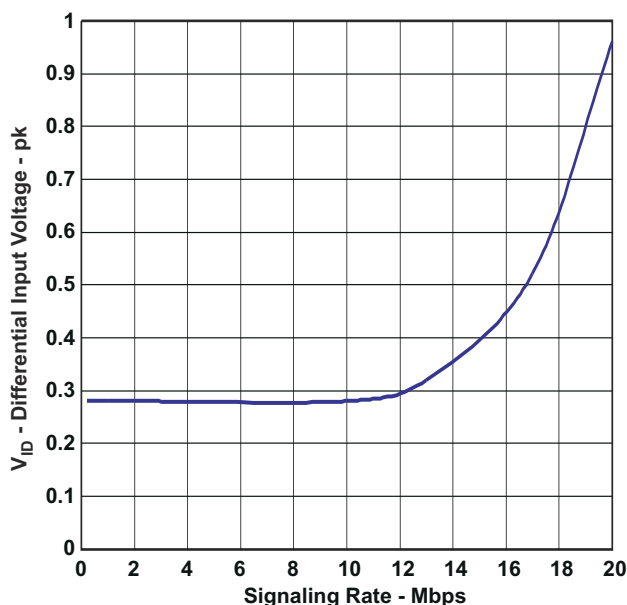


图 7-1. Recommended Minimum Differential Input Voltage vs Signaling Rate

### 7.1 Function Tables

#### DRIVER

| INPUT <sup>(1)</sup> | ENABLE    | OUTPUTS |   |
|----------------------|-----------|---------|---|
| D                    | DE        | Y       | Z |
| H                    | H         | H       | L |
| L                    | H         | L       | H |
| X                    | L or OPEN | Z       | Z |
| Open                 | H         | H       | L |

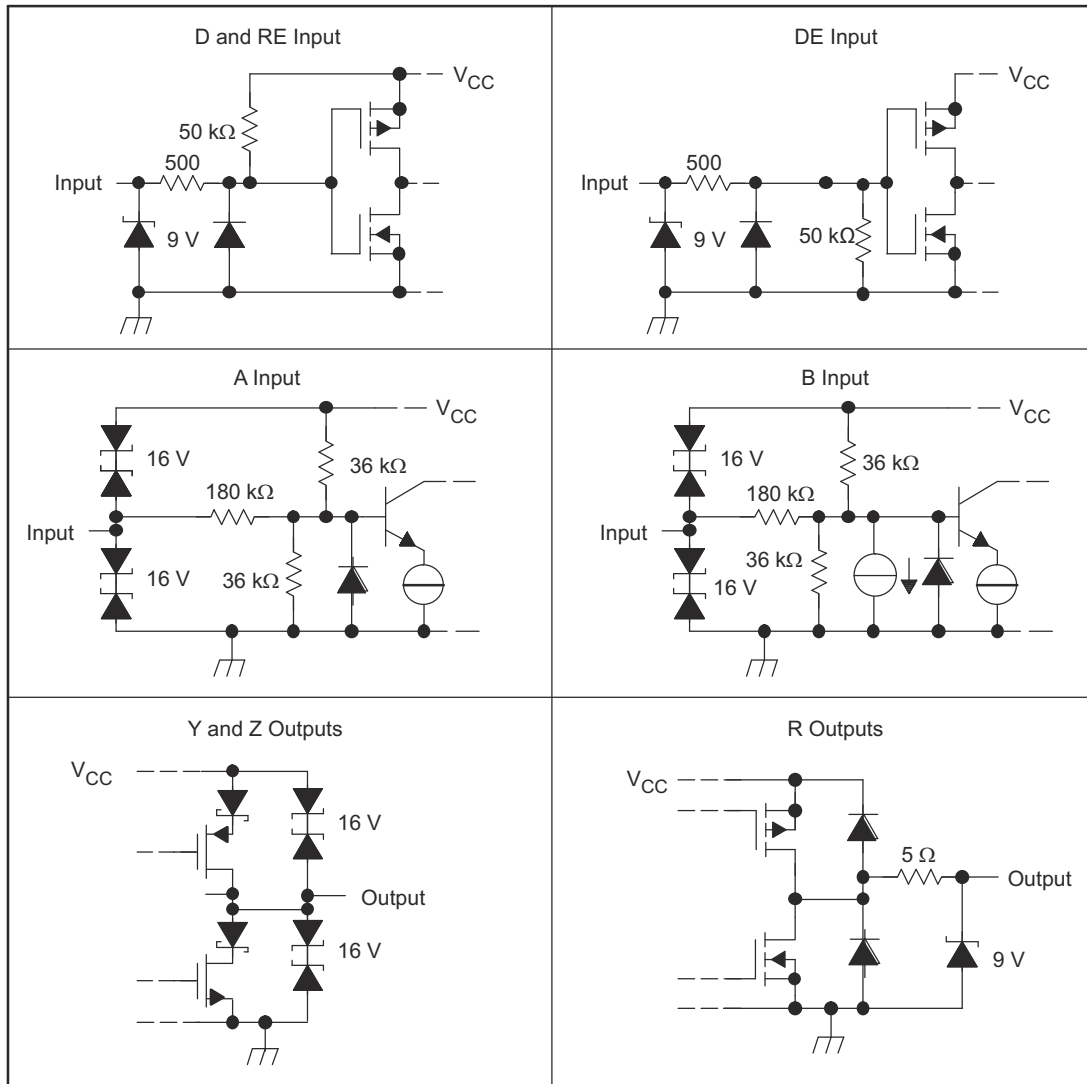
(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

#### RECEIVER

| DIFFERENTIAL INPUTS <sup>(1)</sup><br>$V_{ID} = V_{(A)} - V_{(B)}$ | ENABLE<br>RE | OUTPUT<br>R |
|--------------------------------------------------------------------|--------------|-------------|
| $V_{ID} \leq -0.2 \text{ V}$                                       | L            | L           |
| $-0.2 \text{ V} < V_{ID} < -0.01 \text{ V}$                        | L            | ?           |
| $-0.01 \text{ V} \leq V_{ID}$                                      | L            | H           |
| X                                                                  | H or OPEN    | Z           |
| Open Circuit                                                       | L            | H           |
| BUS Idle                                                           | L            | H           |
| Short Circuit                                                      | L            | H           |

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

## 7.2 Equivalent Input and Output Schematic Diagrams



## 8 Application Information

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### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

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### 8.1 Hot-Plugging

These devices are designed to operate in “hot swap” or “hot pluggable” applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. An internal Power-On Reset circuit keeps the outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLES, the ENABLE inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

## 9 Device and Documentation Support

### 9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.2 支持资源

**TI E2E™ 支持论坛**是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 9.3 商标

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### 9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.5 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN65HVD3080EDGS   | NRND          | VSSOP        | DGS                | 10   | 80             | RoHS & Green    | Call TI   NIPDAU                     | Level-2-260C-1 YEAR  | -40 to 85    | BTT                     |         |
| SN65HVD3080EDGSG4 | NRND          | VSSOP        | DGS                | 10   | 80             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | BTT                     |         |
| SN65HVD3080EDGSR  | ACTIVE        | VSSOP        | DGS                | 10   | 2500           | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 85    | BTT                     | Samples |
| SN65HVD3083EDGS   | NRND          | VSSOP        | DGS                | 10   | 80             | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | BTU                     |         |
| SN65HVD3083EDGSR  | ACTIVE        | VSSOP        | DGS                | 10   | 2500           | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 85    | BTU                     | Samples |
| SN65HVD3086ED     | NRND          | SOIC         | D                  | 14   | 50             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HVD3086E                |         |
| SN65HVD3086EDGS   | NRND          | VSSOP        | DGS                | 10   | 80             | RoHS & Green    | Call TI   NIPDAU                     | Level-2-260C-1 YEAR  | -40 to 85    | BTF                     |         |
| SN65HVD3086EDGSR  | ACTIVE        | VSSOP        | DGS                | 10   | 2500           | RoHS & Green    | SN                                   | Level-2-260C-1 YEAR  | -40 to 85    | BTF                     | Samples |
| SN65HVD3086EDR    | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HVD3086E                | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65HVD3080EDGSR | VSSOP        | DGS             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| SN65HVD3083EDGSR | VSSOP        | DGS             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| SN65HVD3086EDGSR | VSSOP        | DGS             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| SN65HVD3086EDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



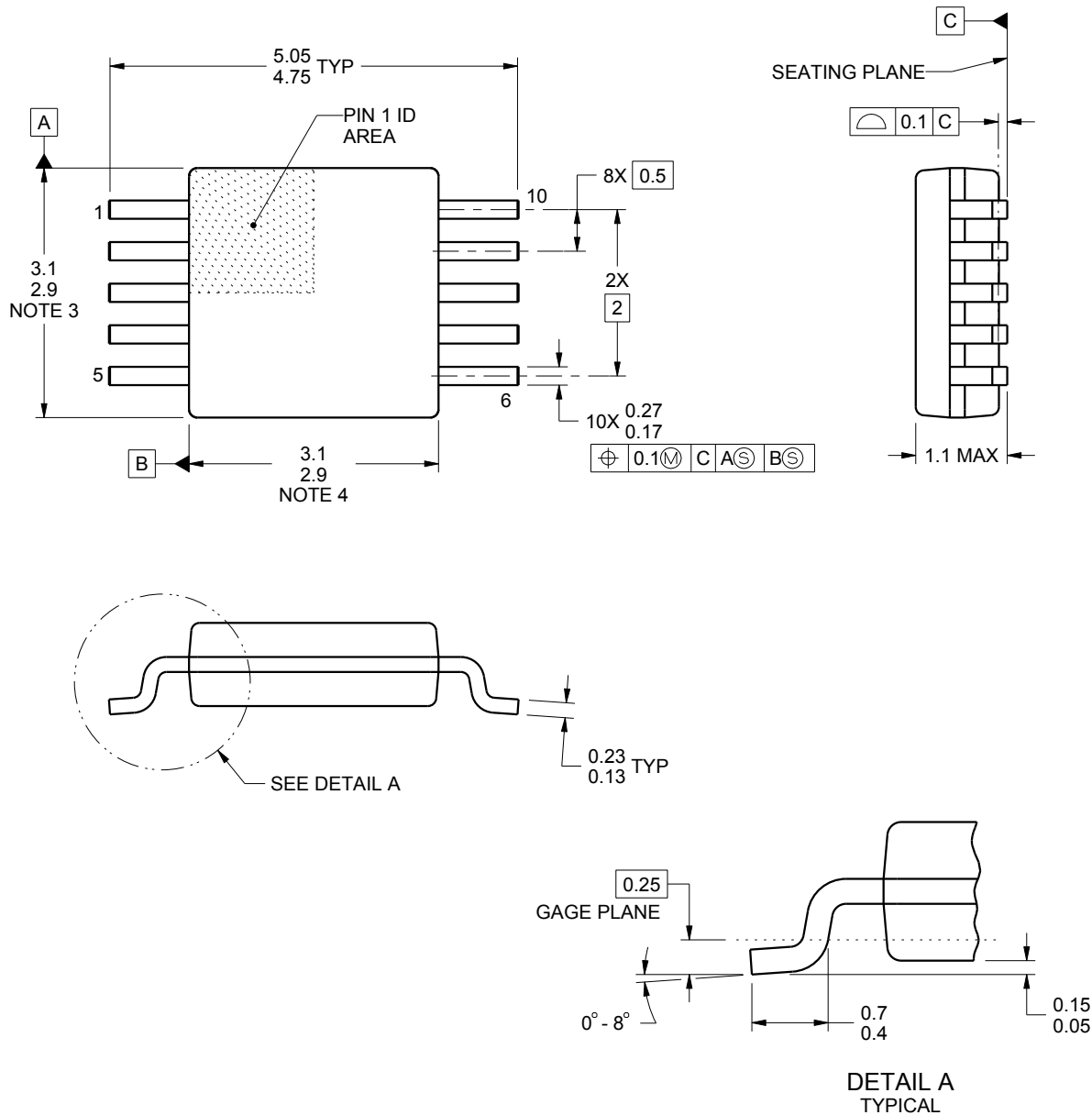
\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65HVD3080EDGSR | VSSOP        | DGS             | 10   | 2500 | 366.0       | 364.0      | 50.0        |
| SN65HVD3083EDGSR | VSSOP        | DGS             | 10   | 2500 | 366.0       | 364.0      | 50.0        |
| SN65HVD3086EDGSR | VSSOP        | DGS             | 10   | 2500 | 366.0       | 364.0      | 50.0        |
| SN65HVD3086EDR   | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65HVD3080EDGS   | DGS          | VSSOP        | 10   | 80  | 330.2  | 6.6    | 3005   | 1.88   |
| SN65HVD3080EDGSG4 | DGS          | VSSOP        | 10   | 80  | 330.2  | 6.6    | 3005   | 1.88   |
| SN65HVD3083EDGS   | DGS          | VSSOP        | 10   | 80  | 330.2  | 6.6    | 3005   | 1.88   |
| SN65HVD3086ED     | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN65HVD3086EDGS   | DGS          | VSSOP        | 10   | 80  | 330.2  | 6.6    | 3005   | 1.88   |



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## NOTES:

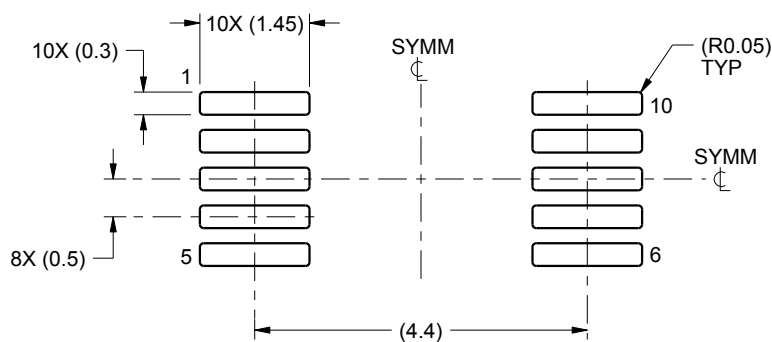
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

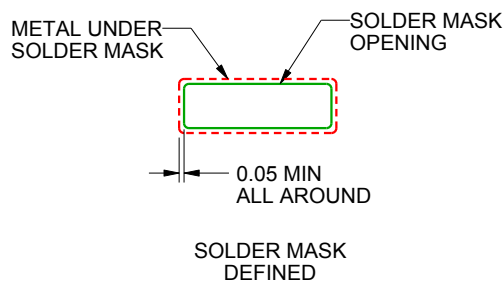
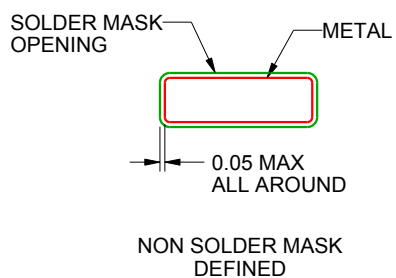
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

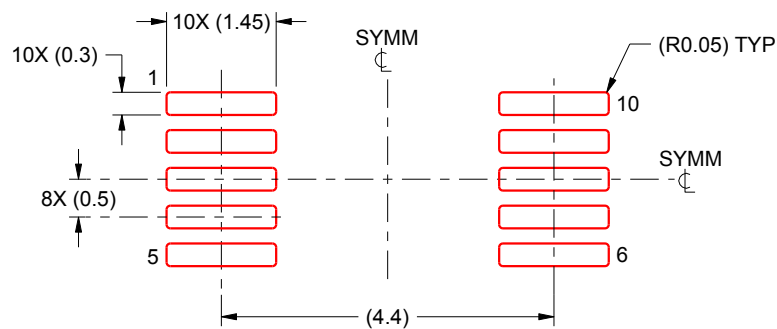
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

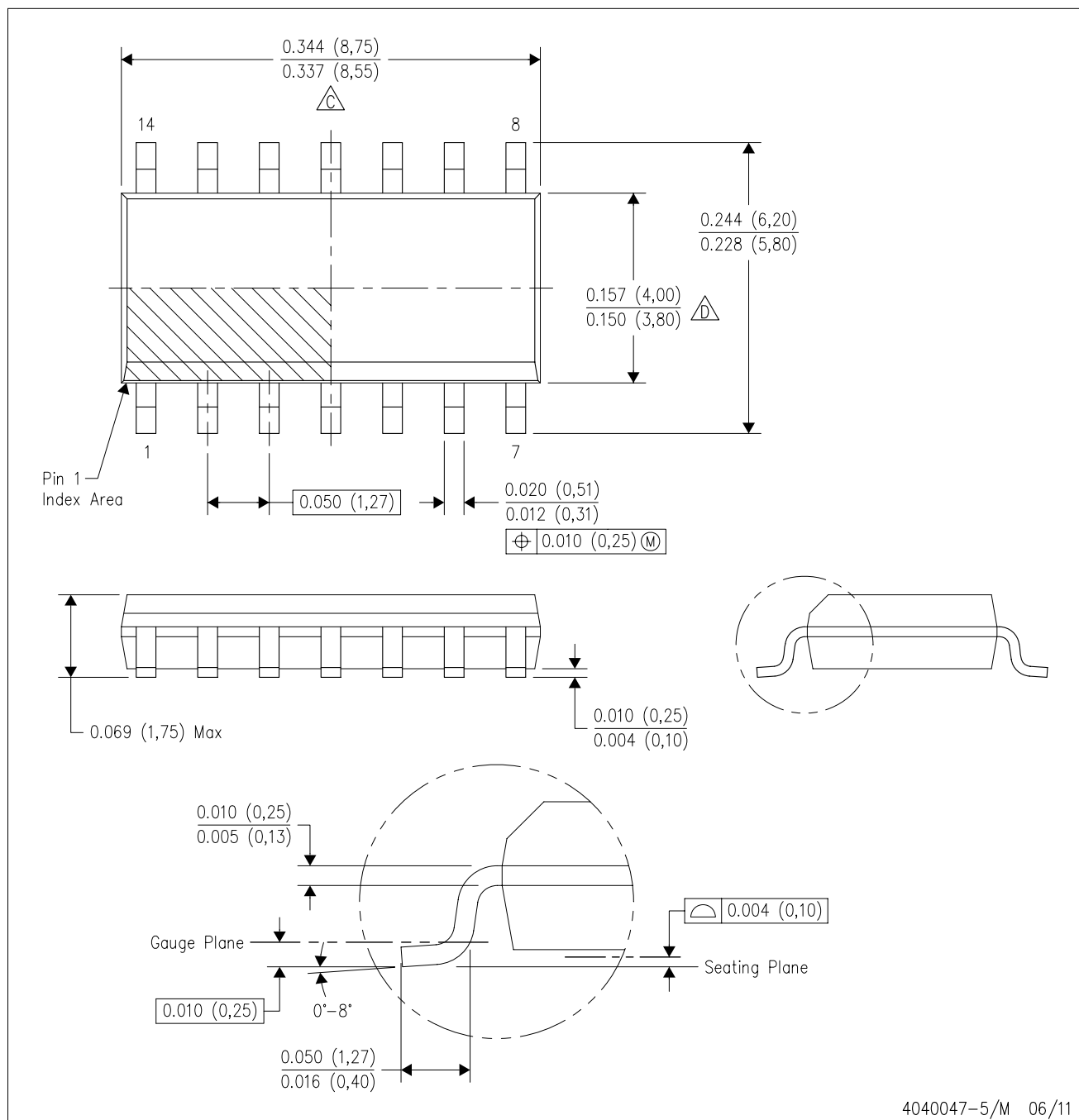
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

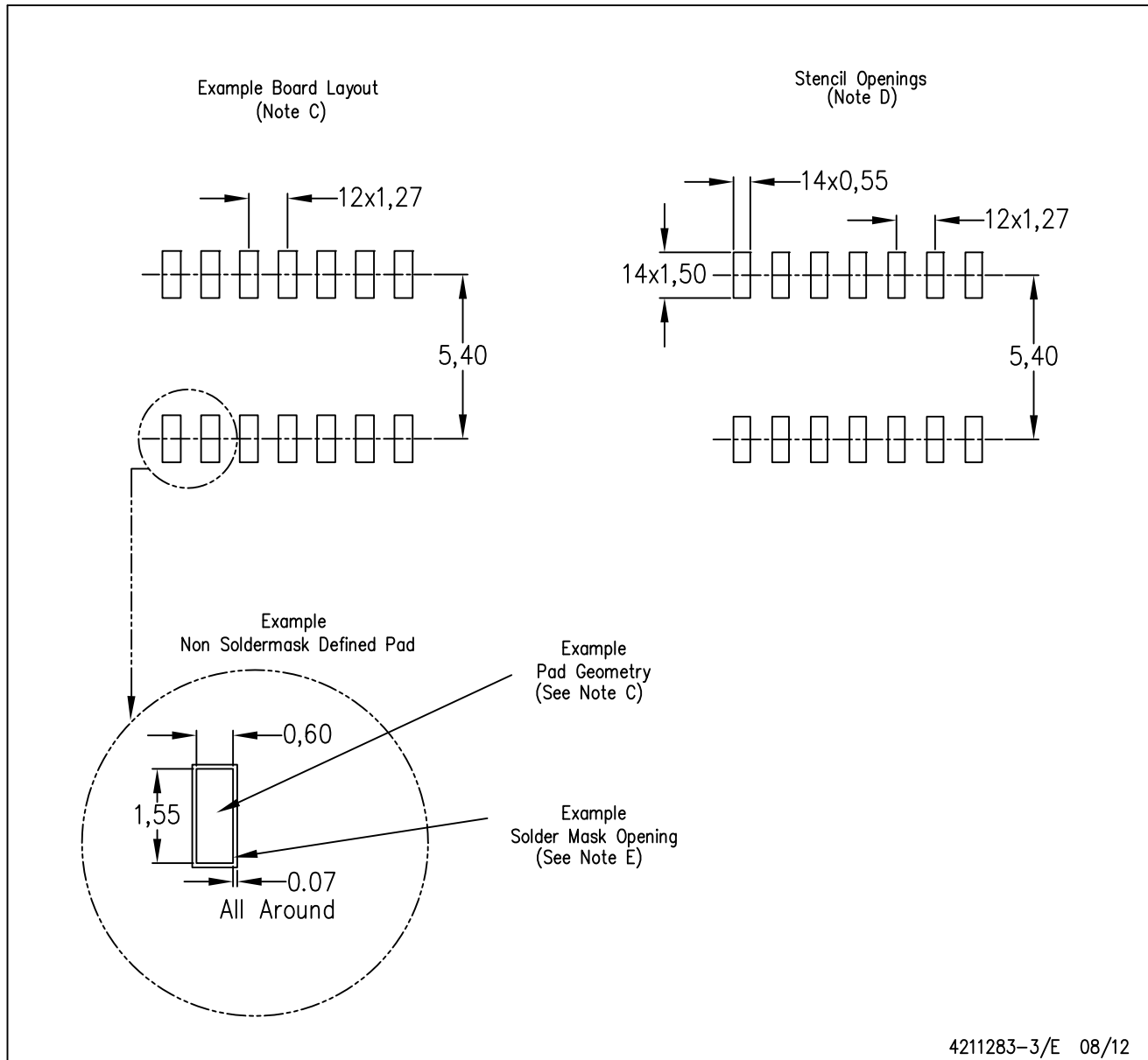


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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