

# SMV512K32-SP

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# 16Mb 抗辐射 SRAM

查询样片: SMV512K32-SP

### 特性

- 20ns 读取, 13.8ns 写入(最大存取时间)
- 与商用
   512K x 32 SRAM 器件功能兼容
- 内置 EDAC(错误侦测和校正)以减轻软错误
- 用于自主校正的内置引擎
- CMOS 兼容输入和输出电平,3 态双向数据总线
  - 3.3 ± 0.3V I/O, 1.8 ± 0.15V 内核

- 辐射性能<sup>(1)</sup>
  - 设计使用基底工程和抗辐射 (HBD) (2)
  - TID 抗扰度 > 3e5 rad (Si)
  - SER < 5e-17 翻转/位-天 (使用 EDAC 和擦除的内核)<sup>(3)</sup>
  - 闭锁抗扰度 > LET = 110 MeV (T = 398K)
- 采用 76 引线陶瓷方形扁平封装
- 可提供工程评估 (/EM) 样品 (4)
- (1) 放射耐受性是一个基于最初器件标准的典型值。 辐射数据和批 量验收测试可用 细节请与厂家联系。\_\_\_\_\_
- (2) 与硅空间技术公司 (SST) 许可协议下的 HardSIL<sup>™</sup> 技术和存储 器设计。
- (3) 使用 CREME96 来计算用于与地同步轨道,太阳安静期的 SER。
- (4) 这些部件只用于工程评估。它们的加工工艺为非兼容流程(例如,无预烧过程等),并且只在 25℃ 的温度额定值下进行测试。这些部件不适合于品质检定、生产、辐射测试或飞行使用。不担保完全军用额定温度 -55℃ 至 125℃ 范围内或使用寿命内的部件性能。

说明

SMV512K32 是一款高性能异步 CMOS SRAM,由 32 位 524,288 个字组成。可在两种模式:主控或受控间进行 引脚选择。主器件为用户提供了定义的自主 EDAC 擦除选项。从器件选择采用按要求擦除特性,此特性可由一个 主器件启动。根据用户需要,可提供 3 个读周期和 4 个写周期(描述如下)。

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## **TERMINAL FUNCTIONS**

PIN NAME	ТҮРЕ	ACTIVE	DESCRIPTION
A[18:0]	Input	N/A	Address
DQ[31:0]	Bidirectional	N/A	Data input/output
E1Z	Input	Low	Chip enable - 1
E2	Input	High	Chip enable - 2
WZ	Input	Low	Write enable
GZ	Input	Low	Output enable for bidirectional input/output
VDD1	Power	N/A	Power supply (1.8 V)
VDD2	Power	N/A	Power supply (3.3 V)
VSS1	Power	N/A	Ground (core)
VSS2	Power	N/A	Ground (I/O)
MSS	Input	N/A	Used for setting master/slave selection. Connect to VSS2 for master operation and VDD2 for slave operation.
MBE	Bidirectional	High	Multiple bit or single bit error indicator (output - user programmable) EDAC function select (input)
SCRUBZ	Bidirectional	Low	Master SCRUBZ (output) Slave SCRUBZ (input)
BUSYZ	Output	Low	Master BUSYZ (output) Slave (do not use)

### **ABSOLUTE MAXIMUM RATINGS**

Over operating free-air temperature range (unless otherwise noted). <sup>(1)</sup>

		VALUE	UNIT
V <sub>DD1</sub>	DC supply voltage(core)	-0.3 to 2.0	V
$V_{DD2}$	DC supply voltage (I/O)	-0.3 to 3.8	V
V <sub>I/O</sub>	Voltage on any pin	-0.3 to 3.8	V
T <sub>STG</sub>	Storage temperature	-65 to 150	°C
P <sub>D</sub>	Maximum power dissipation	1.2	W
TJ	Maximum junction temperature	150	°C
$\theta_{\text{JC}}$	Thermal resistance, junction-to-case	5	°C/W
lj –	DC input current	±5	mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Notes:

- (1) See datasheet for absolute maximum and minimum recommended operating conditions.
- (2) Mil-Prf 38535, appendix B, section B.3.4 targets a 15 year operating life at  $65^{\circ}C \le T_J \le 95^{\circ}C$ .
- (3) Above derating is based upon a worse-case power supply current condition for continuous  $I_{DD1}(OP_2)$  write operation at 50 MHz and may not reflect actual usage.

# Figure 3. SMV512K32 Operating Life Derating Chart (Electromigration Fail Mode)

### **RECOMMENDED OPERATING CONDITIONS**

Over operating free-air temperature range (unless otherwise noted).

		MIN	TYP	MAX	UNIT
$V_{DD1}$	DC supply voltage (core)	1.7	1.8	1.9	V
$V_{DD2}$	DC supply voltage (I/O)	3.0	3.3	3.6	V
T <sub>C</sub>	Case temperature range	-55		125	°C
V <sub>IN</sub>	DC input voltage	0		$V_{DD2}$	V

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## **ELECTRICAL CHARACTERISTICS**

 $T_{C} = -55^{\circ}C$  to 125°C,  $V_{DD1} = 1.7$  V to 1.9 V,  $V_{DD2} = 3$  V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CON	,	MIN	MAX	UNIT		
V <sub>IH</sub>	HIgh-level input voltage				0.7 x V <sub>DD2</sub>		V	
V <sub>IL</sub>	Low-level input voltage					0.3 x V <sub>DD2</sub>	V	
V <sub>OL</sub>	Low-level output voltage	$I_{OL} = 4 \text{ mA}, V_{DD2} = V_{DD2}(\text{min})$				0.2 x V <sub>DD2</sub>	V	
V <sub>OH</sub>	High-level output voltage	$I_{OH}$ = -4 mA, $V_{DD2}$ = $V_{DD2}$ (min)			0.8 x V <sub>DD2</sub>		V	
C <sub>IN</sub> <sup>(1)</sup>	Input capacitance	f = 1 MHz at 0 V				4.5	pF	
C <sub>IO</sub> <sup>(1)</sup>	Bidirectional I/O capacitance	f = 1 MHz at 0 V				4.5	pF	
I <sub>IN</sub>	Input leakage current	$V_{IN}=V_{DD2}$ and $V_{SS}$			-500	500	nA	
I <sub>OZ</sub>	Tri-state output leakage current	$V_{O}$ = $V_{DD2}$ and $V_{SS}$ $V_{DD2}$ = $V_{DD2}$ (max), GZ= $V_{DD2}$ (max)	<)		-500	500	nA	
I <sub>OS</sub> <sup>(2)</sup> <sup>(3)</sup>	Short-circuit output current	$V_{DD2} = V_{DD2}(max), V_O = V_{DD2}$ $V_{DD} = V_{DD2}(max), V_O = V_{SS}$			-46	46	mA	
				–55°C to 25°C		18		
	Vpp1 supply operating current	Input: $V_{IL} = V_{SS} + 0.2 V$ , $V_{IH} = V_{DD2} - 0.2 V$ , $I_{OUT} = 0 A$ .	Write	125°C		31		
I <sub>DD1</sub> (OP <sub>1</sub> )	at 1 MHz	$V_{DD1} = V_{DD1}(max),$	<b>.</b> .	–55°C to 25°C		13	mA	
		$V_{DD2} = V_{DD2}(max)$	Read	125°C		27		
		Input: $V_{IL} = V_{SS} + 0.2 V$ , $V_{IH} = V_{DD2} - 0.2 V$ , $I_{OUT} = 0 A$ , $V_{DD1} = V_{DD1}(max)$ ,	14/ 1/	–55°C to 25°C		635		
	VDD1 supply operating current		Write	125°C		460	mA	
$I_{DD1}(OP_2)$	(OP <sub>2</sub> ) at 50 MHz		Deed	–55°C to 25°C		365		
		$V_{DD2} = V_{DD2}(max)$	Read	125°C		315		
			-55°C to 25°	–55°C to 25°C		255		
	Voperating current	V <sub>DD2</sub> supply operating current	Input: $V_{IL} = V_{SS} + 0.2 V$ , $V_{IH} = V_{DD2} - 0.2 V$ , $I_{OUT} = 0 A$ ,	vvrite	125°C		255	μA
$I_{DD2}(OP_1)$	at 1 MHz	$V_{DD1} = V_{DD1}(max),$	$= V_{DD1}(max),$ $-55^{\circ}C \text{ to } 25^{\circ}C$	–55°C to 25°C		5.2		
		$v_{DD2} = v_{DD2}(max)$	Read	125°C		5.1	mA	
			10/11:4 0	–55°C to 25°C		5.9		
	V <sub>DD2</sub> supply operating current	Input: $V_{IL} = V_{SS} + 0.2 V$ , $V_{IH} = V_{DD2} - 0.2 V$ , $I_{OUT} = 0 A$ ,	vvrite	125°C		1.2		
$I_{DD2}(OP_2)$	at 50 MHz	$V_{DD1} = V_{DD1}(max),$	Deed	–55°C to 25°C		275	MA	
		$V_{DD2} = V_{DD2}(max)$	Read	125°C		120		
		CMOS inputs, I <sub>OUT</sub> = 0 A	-55	°C to 25°C		0.375		
I <sub>DD1</sub> (SB) <sup>(4)</sup>	Supply stand-by current at 0 MHz	$E1Z = V_{DD2} - 0.2 V, E2 = GND,$ $V_{DD1} = V_{DD1}(max),$ $V_{DD2} = V_{DD2}(max)$		125°C		17	mA	
		CMOS inputs. $I_{OUT} = 0.A$	-55	5°C to 25°C		330		
I <sub>DD2</sub> (SB) <sup>(4)</sup>	Supply stand-by current at 0 MHz	$E1Z = V_{DD2} - 0.2 V, E2 = GND, V_{DD1} = V_{DD1}(max), V_{DD2} = V_{DD2}(max)$	ID, 125°C			330	μA	
		CMOS inputs, I <sub>OUT</sub> = 0 A	-55	5°C to 25°C		4.4		
I <sub>DD1</sub> (SB) <sup>(4)</sup>	Supply stand-by current A[16:0] at 50 MHz	$E1Z = V_{DD2} - 0.2 V, E2 = GND,$ $V_{DD1} = V_{DD1}(max),$ $V_{DD2} = V_{DD2}(max)$		125°C		21	mA	
		CMOS inputs, I <sub>OUT</sub> = 0 A	-55	5°C to 25°C		1.6		
I <sub>DD2</sub> (SB) <sup>(4)</sup>	Supply stand-by current A[16:0] at 50 MHz			125°C		0.8	mA	

(1) Measured for initial qualification and after process or design changes that could affect input/output capacitance.

(1) Measured for initial qualification and all process of design changes that could affect inp (2) Provided as a design limit but not guaranteed or tested. (3) No more than one output may be shorted at a time for maximum duration of one second. (4)  $V_{IH} = V_{DD2}(max), V_{IL} = 0 V$ 



### **OPERATIONS**

SMV512K32 has four control inputs called chip enable-1 (E1Z), chip enable-2 (E2), write enable (WZ) and output enable (GZ); 19 address inputs A[18:0] and a 32-bit bidirectional data bus DQ[31:0]. E1Z and E2 enable control device selection, active and stand-by modes (with and without scrub). WZ controls read and write operations. During read operation, GZ must be asserted to enable the outputs.

E1Z	E2	GZ	wz	MBE	I/O MODE	MODE
Н	х	х	х	х	DQ[31:0] 3-State	Standby without EDAC scrub enable
L	L	х	х	х	DQ[31:0] 3-state	Standby with EDAC scrub enable <sup>(1)</sup>
L	Н	L	Н	х	DQ[31:0] Data out	Word read
L	Н	х	L	х	DQ[31:0] Data in	Word write
L	Н	Н	Н	L	DQ[31:0] 3-state	3-state
L	н	Н	н	Н	DQ[31:0] Data in/out	EDAC function select (see Table 6) <sup>(2)</sup>

### Table 1. SRAM Device Control Operation Truth Table

(1) During SCRUB mode, MBE is 3-state if GZ is high and indicates multiple or single bit error if GZ is low.

(2) Special precautions must be observed to prevent accidental over-writing of the Control Register in the memory after a bit error is detected and the memory drives MBE high (please refer to the next section).

### Procedures for Controlling the MBE Pin

A 1-k $\Omega$  resistor must be attached from the MBE pin to ground to insure that MBE cannot float high during time intervals when it is not actively driven HIGH by the memory or actively driven by the external memory control.

During normal EDAC operation, the control registers are set as shown by Sequence 1 in Table 2. Whenever the EDAC circuit encounters either a multiple-bit error or single-bit error (depending on user configuration), the MBE pin is driven high by the memory as shown by Sequence 2 in Table 2. Following this the MBE will need to be reset (low) to restore the detection circuit for the next bit error event. The MBE pin will be pulled low by the 1-k $\Omega$  resistor when GZ is switched to high state. However, to accomplish the MBE reset properly and avoid an accidental write to the control register, the memory must first be disabled by switching either E1Z to high or E2 to low (Sequence 3) before switching GZ from low to high (Sequence 4). Note however, that if E1Z is switched to high this will disable scrub during the interval that GZ is being set high after the memory is disabled.

The memory must remain disabled long enough to insure that MBE is pulled low before the memory is enabled again. During the time the memory is disabled the address at which the MBU was detected must also be changed to access the last known error free address. After the address is changed the memory can be enabled with GZ high. Then an Output Enable-controlled read operation can be performed using the last known error free address. This turns off the MBE error flag in the memory and causes the memory to drive MBE low after the GZ-controlled output data valid time,  $t_{GLMV}$ .

This procedure resets the memory back into its normal EDAC read state in which the memory will drive MBE low sequentially for each read operation until the next bit error is encountered. This avoids accidental over-writing of the Control Register in the memory. After this procedure is completed the system protocol for responding to bit errors can be executed.

ZHCS480I-JUNE 2011-REVISED JANUARY 2014

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Table 2	Example	Control	Settings	for	Resetting	MBF
		00110101	ocunga	101	Nesetting	

SEQUENCE	E1Z	E2	GZ	WZ	MBE	I/O MODE	MODE	
1	L	Н	L	Н	L	DQ[31:0] Data out	Normal read mode with EDAC enabled	
2	L	Н	L	н	н	DQ[31:0] Data out	MBE driven high when single bit or multiple bit error (depending on user configuration) is detected during read	
3	Н	L	L	н	Н	DQ[31:0] Data out	Memory disabled	
4	Н	L	н	Н	$H\toL$	DQ[31:0] Tri-state	Outputs tri-stated and MBE pulled low by load R	
5	L	Н	н	Н	L	DQ[31:0] Tri-state	Read at a last known error free address <sup>(1)</sup>	
6	L	Н	L	Н	L	DQ[31:0] Data out	Output enable-controlled read <sup>(2)</sup>	

(1) During this operation MBE drive circuitry in the memory is tri-stated but MBE is held low by the  $1-k\Omega$  resistor to ground.

(2) During this operation MBE is actively driven low by the MBE drive circuitry in the memory after a time, t<sub>GLMV</sub>, and the memory is back to the original state corresponding to normal read mode with EDAC enabled.

### **Read Operations**

A combination of E1Z low, E2 high and WZ high defines a read cycle. GZ low enables the outputs to drive read data to the DQ pins. Read access time is measured from the latter of device enable, output enable or valid address to valid data output.

- SRAM read cycle 1 (Figure 4): Address controlled access is initiated by a change in address inputs while device is selected with WZ high and GZ low. Valid data appears on DQ[31:0] after a specified t<sub>AVQV</sub> is satisfied. Outputs remain active throughout the entire cycle. As long as the device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time t<sub>AVAV</sub>.
- SRAM read cycle 2 (Figure 5): Chip-enable controlled access is initiated by the latter of either E1Z or E2 going active while GZ is low, WZ is high, and address remains stable for the entire cycle. After the specified time t<sub>ETQV</sub>, the 32-bit word addressed by A[18:0] is accessed and appears at DQ[31:0].
- SRAM read cycle 3 (Figure 6): Output-enable controlled access is initiated by GZ going active while E1Z and E2 are asserted, WZ is de-asserted, and address is stable. Read access time is t<sub>GLQV</sub> unless t<sub>AVQV</sub> or t<sub>ETQV</sub> have not been satisfied.

If EDAC is turned on during read operation:

- If MBE is low, data is valid.
- If MBE is high, data is corrupted (dependent on EDAC programming configuration on A[12], MBE can indicate a single bit or double bit error). Single bit error is correctable by EDAC.

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t <sub>AVAV1</sub>	Read cycle time	20		ns	Figure 4
t <sub>AVQV1</sub>	Address to data valid from address change <sup>(2)</sup>		20	ns	Figure 4
t <sub>AXQX</sub>	Output hold time	7.5		ns	Figure 4
t <sub>GLQX1</sub>	GZ-controlled output enable time	3.5		ns	Figure 6
t <sub>GLQV</sub>	GZ-controlled output data valid		8.6	ns	Figure 6
t <sub>GHQZ1</sub>	GZ-controlled output enable tri-state time	3.5	5	ns	Figure 6
t <sub>ETQX</sub>	E-controlled output enable time	3.5		ns	Figure 5
t <sub>ETQV</sub>	E-controlled access time		20	ns	Figure 5
t <sub>EFQZ</sub>	E-controlled tri-state time	3.5	5	ns	Figure 5
t <sub>AVMV</sub>	Address to error flag valid		20	ns	Figure 4
t <sub>AXMX</sub>	Address to error flag hold time from address change	7.5		ns	Figure 4

### Table 3. AC Characteristics Read Cycle <sup>(1)</sup>

(1)  $T_C = -55^{\circ}C$  to  $125^{\circ}C$ ,  $V_{DD1} = 1.7$  V to 1.9 V,  $V_{DD2} = 3$  V to 3.6 V (unless otherwise noted).

(2) 20 ns at 5-pF load.

ZHCS480I-JUNE 2011-REVISED JANUARY 2014

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SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t <sub>GLMV</sub>	GZ-controlled error flag valid		8.6	ns	Figure 6
t <sub>GLMX</sub>	GZ-controlled error flag enable time	3.5		ns	Figure 6
t <sub>ETMX</sub>	E-controlled error flag enable time	3.5		ns	Figure 5
t <sub>ETMV</sub>	E-controlled error flag time		20	ns	Figure 5
t <sub>GHMZ</sub> <sup>(3)</sup>	GZ-controlled error flag tri-state time	3.5	5	ns	Figure 6
t <sub>EFMZ</sub> <sup>(3)</sup>	Chip enable change to MBE tri-state	3.5	5	ns	Figure 5

### Table 3. AC Characteristics Read Cycle <sup>(1)</sup> (continued)

(3) Parameters ensured by design and/or characterization if not production tested.



Assumptions: E1Z low, E2 high, WZ high, GZ low and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.





Assumptions: GZ low, WZ high and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.

Figure 5. Read Cycle 2, Chip Enable-Controlled Access



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Assumptions: E1Z low, E2 high, WZ high and SCRUBZ high. Reading uninitialized addresses will cause MBE to be asserted.



### Write Operation With Write-Through Support

A combination of WZ and E1Z low with E2 high defines a write cycle. The state of GZ is "don't care" for a write cycle although it may be necessary to set GZ high for convenient setup of new data for some system operation modes in order to avoid data bus contention. During a write operation, data just written will be sent to the outputs. When the write operation has been completed, the output data bus will be updated by controlling either GZ going low or WZ goes high while GZ low. The outputs are placed in a high impedance state when GZ is high or WZ is low during standard read and write cycles.

- Write cycle 1 (Figure 7): Access and data write through controlled by WZ is initiated when WZ goes low and is terminated by WZ going high while E1Z and E2 remain active. The write pulse width is determined by t<sub>WLWH</sub> and t<sub>ETWH</sub>. To avoid bus contention, t<sub>WLQZ</sub> must be satisfied before write data is applied to the DQ[31:0] pins. In addition, at the end of the write operation write data must be removed from the DQ[31:0] pins after t<sub>WHDX</sub> is met, but before t<sub>WHQX</sub>. The output access time is determined by t<sub>WHQV</sub> as long as GZ remains low.
- Write cycle 1a (Figure 8): WZ controlled write cycle with GZ high is similar to write cycle 1 but with GZ fixed high so data outputs remain in high impedance state.
- Write cycle 2 (Figure 9): WZ controlled write access with data write through controlled by GZ is similar to write cycle 1 with the difference being that the output data comes out when GZ goes low with WZ high. The output access time is determined by t<sub>GLQV</sub>. The GZ high pulse is used to keep the DQ[31:0] outputs in a high impedance state during the write operation to avoid bus contention.
- Write cycle 3 (Figure 10): Chip enable controlled write access with data write through controlled by WZ is initiated when E1Z or E2 goes active, and the data write operation is terminated by WZ going high. The write pulse width is defined by t<sub>ETWHZ</sub> from the latter of E1Z or E2 going active to WZ high. The output access time is determined by t<sub>WHQV</sub> as long as GZ remains low. As with write cycle 1, the write data must be removed from the DQ[31:0] pins after the input data hold time, t<sub>WHDX</sub>, but before t<sub>WHQX</sub>.
- Write cycle 3a (Figure 11): chip enabled controlled write cycle with GZ high is similar to write cycle3, but with GZ fixed high so the data outputs remain in a high impedance state.
- Write cycle 4 (Figure 12): Chip enable controlled write access with data write through controlled by GZ is similar to Write cycle 3 with the difference that the data output is controlled by GZ going low. The output access time is determined by t<sub>GLQV</sub>. The GZ high pulse is used to keep the DQ[31:0] pins in a high impedance state during the write operation to avoid bus contention.

# SMV512K32-SP

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Table 4. AC Characteristics Write Cycle <sup>(1)</sup>

SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t <sub>AVAV</sub>	Write-through cycle time	20		ns	Figure 7 Figure 9 Figure 10 Figure 12
t <sub>AVAV2</sub> <sup>(2)</sup>	Write cycle time with GZ always high	13.8		ns	Figure 8 Figure 11
t <sub>ETWH</sub>	Device enable to end of write (WZ-controlled)	12		ns	Figure 7 Figure 8 Figure 9
t <sub>ETWH2</sub> <sup>(3)</sup>	Device enable to end of write (E-controlled)	11		ns	Figure 10 Figure 12
t <sub>AVET</sub>	Address setup time for write (E-controlled)	1.4		ns	Figure 10 Figure 11 Figure 12
t <sub>EFQZ</sub>	E-controlled tri-state time	3.5	5	ns	Figure 7 Figure 9 Figure 10 Figure 12
t <sub>AVWL</sub>	Address setup time for write (WZ-controlled)	3.6		ns	Figure 7 Figure 8 Figure 9
t <sub>WLWH</sub>	Write pulse width	7.9		ns	Figure 7 Figure 8 Figure 9
t <sub>WHAX</sub> <sup>(3)</sup>	Address hold time for write-through (WZ-controlled)	8.5		ns	Figure 7 Figure 9
t <sub>WHAX1</sub> <sup>(2)</sup>	Address hold time for write (WZ-controlled) with GZ always high	2.3		ns	Figure 8
t <sub>EFAX</sub>	Address hold time for device enable (E-controlled)	0.1		ns	Figure 10 Figure 11 Figure 12
t <sub>ETEF</sub> <sup>(3)</sup>	Device enable pulse width (E-controlled)	19.5		ns	Figure 10 Figure 12
t <sub>ETEF1</sub> <sup>(2)</sup>	Device enable pulse width (E-controlled) with GZ always high	12.3		ns	Figure 11
t <sub>DVWH</sub>	Data setup time	8.2		ns	Figure 7 Figure 8 Figure 9 Figure 10 Figure 12
t <sub>WHDX</sub>	Data hold time	0.2		ns	Figure 7 Figure 8 Figure 9 Figure 10 Figure 12
t <sub>WHEF</sub>	Write disable time to device disable for write-through	8.5		ns	Figure 7 Figure 9 Figure 10 Figure 12
t <sub>WHEF1</sub> <sup>(2)</sup>	Write disable time to device disable with GZ always high	2.3		ns	Figure 8
t <sub>WHWL</sub>	Write disable time. Write pulse width high for write-through.	12.1		ns	Figure 7 Figure 9
t <sub>WHWL1</sub> <sup>(2)</sup>	Write disable time. Write pulse width high with GZ always high.	2.6		ns	Figure 8
t <sub>WHQX</sub>	WZ-controlled tri-state end time	3		ns	Figure 7 Figure 10
t <sub>WHQV</sub>	WZ-controlled output data valid		10	ns	Figure 7 Figure 10
t <sub>WLQZ</sub>	WZ-controlled tri-state time	2	3.3	ns	Figure 7

 $T_{C}$  = -55°C to 125°C,  $V_{DD1}$  = 1.7 V to 1.9 V,  $V_{DD2}$  = 3 V to 3.6 V (unless otherwise noted). Write-only operations with GZ fixed high (no write-through). Parameters ensured by design and/or characterization if not production tested. (1) (2)

(3)

# SMV512K32-SP

ZHCS480I – JUNE 2011 – REVISED JANUARY 2014



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Table 4. AC Characteristics Write Cycle <sup>(1)</sup> (continued)

			,		
SYMBOL	PARAMETER	MIN	MAX	UNIT	FIGURE
t <sub>GLQX</sub>	GZ-controlled output enable time	1.3		ns	Figure 9 Figure 12
t <sub>GLQV</sub>	GZ-controlled output data valid		8.6	ns	Figure 9 Figure 12
t <sub>GLMX</sub>	GZ-controlled error flag enable time	3.5		ns	Figure 9 Figure 12
t <sub>GLMV</sub>	GZ-controlled error flag valid		8.6	ns	Figure 9 Figure 12
t <sub>WHMX</sub> <sup>(4)</sup>	WZ-controlled error flag enable time	4		ns	Figure 7 Figure 10
t <sub>WHMV</sub> <sup>(4)</sup>	WZ-controlled error flag valid		8.5	ns	Figure 7 Figure 10
t <sub>EFMZ</sub> <sup>(4)</sup>	Chip enable change to MBE tri-state	3.5	5	ns	Figure 7 Figure 9 Figure 10 Figure 12
t <sub>WLMZ</sub> <sup>(4)</sup>	WZ-controlled output MBE tri-state time	2	3.3	ns	Figure 7

(4) Parameters ensured by design and/or characterization if not production tested.



Assumption: SCRUBZ high, GZ low



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ZHCS480I-JUNE 2011-REVISED JANUARY 2014

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Assumptions: SCRUBZ high, GZ high

Figure 8. SRAM Write Cycle 1a, WZ-Controlled Write Only With GZ Fixed High



Assumptions: SCRUBZ high





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Assumptions: Either E1Z,/E2 scenario can occur, SCRUBZ high, GZ low

Figure 10. SRAM Write Cycle 3, Enable Controlled Write With Data Write Through Controlled by WZ



Assumptions: Either E1Z,/E2 scenario can occur, SCRUBZ high, GZ High

#### Figure 11. SRAM Write Cycle 3a, Enable Controlled Write Only With GZ Fixed High

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Figure 12. SRAM Write Cycle 4, Enable Controlled Write With Data Write Through Controlled by GZ

### **Scrub Operation**

The SMV512K32 uses embedded error detection and correction (EDAC) to correct single bit upset of each 32-bit word. The device pins BUSYZ and SCRUBZ are used differently depending on whether the device is operated as a slave device (MSS pin connected to VDD2) or as a master device (MSS pin connected to VSS2). The BUSYZ pin is an output for the master device and is driven low to indicate that a scrub cycle is about to be initiated. The BUSYZ signal can be used to generate wait states by the memory controller. The BUSYZ pin should should be left unconnected for slave devices. The SCRUBZ pin is an output on the master device and an input on slave devices. The master SCRUBZ pin is driven low when a scrub cycle initiates and can be used to trigger scrub cycles for slave units by connecting their respective SCRUBZ pins to the SCRUBZ master output.

The EDAC operation truth table is shown in Table 5.



ZHCS480I – JUNE 2011 – REVISED JANUARY 2014

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### Table 5. EDAC Control Operation Mode Truth Table

MBE (OUTPUT)	SCRUBZ	BUSYZ	I/O MODE	MODE
Н	Н	Н	Read	Data error detected <sup>(1)</sup>
L	Н	Н	Read	Valid data out <sup>(1)</sup>
Х	Н	Н	X	Device ready
х	Н	L	x	Device ready/early scrub request coming
Х	L	Х	Not accessible	Device busy (scrub in progress)

 MBE is only valid in EDAC operation modes (Read with EDAC enable or scrub). MBE indicates Multiple Bit Error if A[12] bit in the control register is '0'.

MBE indicates Single Bit Error if A[12] bit in the control register is '1'.

To allow system design flexibility, the time delay between falling edges of BUSYZ and SCRUBZ as well as the scrub rate are user programmable (see the control register programming description below). Depending on environment and usage, some users may want a high scrub rate to minimize error rate at the sacrifice of reduced data throughput, while others may want a lower scrub rate to increase the throughput and accept a higher error rate.

Data errors are detected and corrected not only during scrub cycles, but also during normal read cycles.

### EDAC Configuration and Scrub Address Polling (Master Device Only)

The user can program the scrub rate and the edge relationship between BUSYZ and SCRUBZ by writing configuration data to the control register. The value recorded in the control register determines scrub rate, SCRUBZ to BUSYZ delay, EDAC bypass selection, scrub enable/disable and single bit or multiple bit error detection. See Table 7 for more detail.

Table 8 and Table 9 give typical timing characteristics for various configuration options. Table 10 gives the AC characteristics for EDAC functions.

The following EDAC control operations are defined by Table 6.

- Control register write (Figure 15): This mode is used to write configuration values to the EDAC control register.
- Control register read (Figure 16): This mode is used to read the contents of the EDAC control register.
- Scrub address counter read (Figure 17): This mode is to read out the address counter which is used as a
  pointer for scrub operations. The address counter is reset to all '1' when the configuration register is written. It
  is then automatically incremented for each scrub cycle. In the event of a single or multiple bit error detected
  during a scrub cycle, the address can be polled to determine the location of the data error. During the
  address counter read, the 19 bits of the counter are output on data bits DQ[18:0]. The value of the other data
  bits DQ[31:19] are ignored.

E1Z	E2	GZ	WZ	MBE	A7	A8	A9	A10	MODE
L	Н	Н	Н	Н	Х	Х	L	L	Write control register
L	Н	Н	Н	Н	Х	Х	Н	L	Read control register
L	Н	Н	Н	Н	Н	Х	Х	Н	Address counter read

Table 6. EDAC Function Select Truth Table<sup>(1)</sup>

(1) All other combinations of A7-A10 are reserved and should be avoided.

ZHCS480I-JUNE 2011-REVISED JANUARY 2014

ADDRESS BIT	PARAMETER	VALUE	FUNCTION
A[3:0]	Scrub rate – Rates are approximate and will vary with temperature and voltage conditions as well as process parameters	0–15	As scrub rate changes from 0 to 15, then the interval between scrub cycles, $t_{BLBL}$ , will change as follows: 0 = N/A 6 = 222 kHz 11 = 7 kHz 1 = N/A 7 = 111 kHz 12 = 3.5 kHz 2 = N/A 8 = 55 kHz 13 = 1.75 kHz 3 = N/A 9 = 28 kHz 14 = 0.875 kHz 4 = 888 kHz 10 = 14 kHz 15 = 0.433 kHz 5 = 444 kHz See Table 8.
A[7:4]	BUSYZ to SCRUBZ – Delays are approximate and will vary with temperature and voltage conditions as well as process parameters	0–15	If A[7:4] changes from 0 to 15, the interval $t_{BLSL}$ between falling edges of BUSYZ and SCRUBZ will change as follows: 0 = 80 ns 6 = 480 ns 11 = 820 ns 1 = 160 ns 7 = 560 ns 12 = 880 ns 2 = 220 ns 8 = 620 ns 13 = 960 ns 3 = 280 ns 9 = 680 ns 14 = 1020 ns 4 = 360 ns 10 = 760 ns 15 = 1080 ns 5 = 420 ns See Table 9.
A[8]	EDAC bypass bit	0/1	0: Enable EDAC 1: Disable EDAC including scrub
A[11]	Scrub enable bit	0/1	0: Enable scrub 1: Disable scrub
A[12]	SE/DE indication bit	0/1	0: MBE indicates multiple-bit error 1: MBE indicates single-bit error

# Table 7. EDAC Control Register Programming<sup>(1)(2)</sup>

(1) A(10:9) must be '00' during control register programming according to Table 6.

(2) A(18:13) are don't care.

### NOTE

During power up, states of all registers are random so it is imperative that the user execute Write Control Register and preferably Read Control Register to affirm desired operations. The following values are recommended to set for initial use:

- 1. Scrub rate is 111 kHz.
- 2.  $t_{BLSL}$  is 760 ns.
- 3. EDAC bit is 0 (enabled).
- 4. Scrub enable bit is 0 (enabled).
- 5. SE/DE indication bit is 0 (multiple bit).

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ISTRUMENTS

XAS

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· · · ·
MAX (ns)
N/A
N/A
N/A
N/A
1,500
3,100
6,100
12,200
24,200
48,300
96,400
192,500
384,500
770,000
1,500,00
3,200,00

### Table 8. Scrub Rate Variation (Voltage = 1.8 V, Temperature = -55°C to 125°C)

### Table 9. BUSYZ Low to SCRUBZ Low Delay Variation (Voltage = 1.8 V, Temperature = -55°C to 125°C)

VALUE	MAX (ns)
0000	80
0001	180
0010	270
0011	370
0100	460
0101	600
0110	650
0111	800
1000	900
1001	1000
1010	1200
1011	1300
1100	1400
1101	1500
1110	1600
1111	1600

# SMV512K32-SP

EXAS STRUMENTS

### ZHCS480I-JUNE 2011-REVISED JANUARY 2014

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CVMDOL		MIN			FIGURE
SYMBOL	PARAMETER	MIN	MAX	UNII	FIGURE
t <sub>BLSL</sub>	User programmable, BUSYZ low to SCRUBZ low	:	See Table 9	ns	Figure 13 Figure 14
t <sub>BLBL</sub>	User programmable, BUSYZ low to BUSYZ low		See Table 8	ns	Figure 14
t <sub>SLSH</sub>	SCRUBZ low to SCRUBZ high	200	504	ns	Figure 13 Figure 14
t <sub>SHBH</sub>	SCRUBZ high to BUSYZ high	50	120	ns	Figure 13 Figure 14
t <sub>ЕТМН</sub>	Device enable to MBE high	5.5		ns	Figure 15 Figure 16 Figure 17
t <sub>GHMH</sub>	GZ high to MBE high	6.5		ns	Figure 15 Figure 16 Figure 17
t <sub>AVMH</sub>	Address valid to MBE high	0.9		ns	Figure 15 Figure 16 Figure 17
t <sub>MHML</sub>	MBE high to MBE low	12.8		ns	Figure 15 Figure 16 Figure 17
t <sub>MLEF</sub>	MBE low to device disable	0.4		ns	Figure 15 Figure 16 Figure 17
t <sub>MLGL</sub>	MBE low to GZ low	1.8		ns	Figure 15 Figure 16 Figure 17
t <sub>MLAX</sub>	MBE low to address change	0.1		ns	Figure 15 Figure 16 Figure 17
t <sub>MHQX</sub>	MBE high to data change	4.5		ns	Figure 16 Figure 17
t <sub>MHQV</sub>	MBE high to data valid		8.2	ns	Figure 16 Figure 17
t <sub>EFQZ</sub>	Memory enable change to output data tri-state	3.5	5	ns	Figure 16 Figure 17
t <sub>EFMZ</sub> <sup>(2)</sup>	Memory enable change to MBE tri-state	3.5	5	ns	Figure 14
t <sub>GLMX</sub>	GZ-controlled error flag enable time	3.5		ns	Figure 13
t <sub>ETMX</sub>	E-controlled error flag enable time	3.5		ns	Figure 14
t <sub>INIT_E</sub>	E1Z low to BUSYZ low		160	ns	Figure 14
t <sub>INIT_MBE</sub>	MBE low to BUSYZ low		160	ns	Figure 13
t <sub>SLMV</sub>	SCRUBZ low to MBE valid		146	ns	Figure 13 Figure 14
t <sub>E1ZHSH</sub>	E1Z high to SCRUBZ high		20	ns	Figure 14
t <sub>E1ZHBH</sub>	E1Z high to BUSYZ high		20	ns	Figure 14
t <sub>MHBH</sub>	MBE high to BUSYZ high		20	ns	Figure 15

Table 10. AC Characteristics for EDAC Function <sup>(1)</sup>

(1)  $T_C = -55^{\circ}C$  to  $125^{\circ}C$ ,  $V_{DD1} = 1.7$  V to 1.9 V,  $V_{DD2} = 3$  V to 3.6 V (unless otherwise noted). (2) Parameters ensured by design and/or characterization if not production tested.



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# SMV512K32-SP

ZHCS480I – JUNE 2011 – REVISED JANUARY 2014



Assumption: WZ is high





Assumptions: E2 and GZ are low, WZ is high





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Assumptions: SCRUBZ and WZ are high





Assumptions: SCRUBZ and WZ are high





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Assumptions: SCRUBZ and WZ are high

### Figure 17. Address Counter Read

ZHCS480I-JUNE 2011-REVISED JANUARY 2014



Ch	anges from Revision H (July 2013) to Revision I Pa	ıge
•	Added 将 /EM 添加到特性内	. 1
•	Deleted 订购信息表	. 1

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### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qtv	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		3		,	(2)	(6)	(3)		(+/3)	
5962-1123701VXC	ACTIVE	CFP	HFG	76	1	RoHS & Green	AU	N / A for Pkg Type	-55 to 125	SMV512K32HFG 5962-1123701VXC	Samples
SMV512K32HFG	ACTIVE	CFP	HFG	76	1	RoHS & Green	AU	N / A for Pkg Type	-55 to 125	SMV512K32HFG 5962-1123701VXC	Samples
SMV512K32HFG/EM	ACTIVE	CFP	HFG	76	1	RoHS & Green	Call TI	Call TI	0 to 0	SMV512K32HFG/EM EVAL ONLY	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# TEXAS INSTRUMENTS

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### TRAY



PACKAGE MATERIALS INFORMATION



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nomina	1											
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-1123701VXC	HFG	CFP	76	1	2 x 5	150	315	135.9	7620	57	43.5	39.45
SMV512K32HFG	HFG	CFP	76	1	2 x 5	150	315	135.9	7620	57	43.5	39.45

HFG (S-CQFP-F76)

CERAMIC QUAD FLATPACK WITH NCTB



NOTES: A

6: A. All linear dimensions are in millimeters (inches).

- B. This drawing is subject to change without notice.
- C. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
- D. This package is hermetically sealed with a metal lid.
- E. The leads are gold plated and can be solderdipped.
- F. Lid is connected to GND leads (see data sheet).



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