RF430FRL15xH NFC ISO 15693 传感器应答器

1 器件概述

1.1 特性

- 兼容 ISO/IEC 15693 和 ISO/IEC 18000-3（模式 1）标准的射频 (RF) 接口
- 电源系统采用电池或 13.56MHz 磁场供电
- 14 位 Σ-Δ 模数转换器 (ADC)
- 内部温度传感器
- 电阻传感器偏置接口
- CRC16 CCITT 发生器
- MSP430™ 混合信号微控制器
  - 2KB FRAM
  - 4KB SRAM
  - 8KB ROM
  - 电源电压范围：1.45V 至 1.65V
  - 低功耗
    - 激活模式 (AM)：140µA/MHz (1.5V)
    - 待机模式 (LPM3)：16µA
  - 16 位精简指令集计算机 (RISC) 架构
  - 最高 2MHz CPU 系统时钟
  - 紧凑型时钟系统
    - 4MHz 高频时钟
    - 256kHz 内部低频时钟源
    - 外部时钟输入
  - 具有 3 个捕捉/比较寄存器的 16 位 Timer_A
  - LV 端口逻辑
    - 400µA 时，V_{OL} 低于 0.15V
    - 400µA 时，V_{OH} 高于 (V_{DDB} – 0.15V)
    - 所有端口均可提供 Timer_A PWM 信号
  - eUSCI_B 模块支持 3 线和 4 线 SPI 和 I^2C
  - 32 位看门狗定时器 (WDT_A)
  - ROM 开发模式（将 ROM 地址映射到 SRAM 以进行固件开发）
  - 全 4 线制 JTAG 调试接口
- 如需完整的模块描述，请参见《*RF430FRL15xH 系列技术参考手册*》（文献编号：SLAU506）
- 关于应用操作和编程，请参见《*RF430FRL15xH 固件用户指南*》（文献编号：SLAU603）

1.2 应用

- 工业无线传感器
- 医用无线传感器

1.3 说明

RF430FRL15xH 器件是一款 13.56MHz 应答器芯片，该芯片中包含可编程的 16 位 MSP430™ 低功耗微控制器。 该器件采用嵌入式通用 FRAM 非易失性存储器来存储程序代码或用户数据，例如校准和测量数据。 RF430FRL15xH 支持通过兼容 ISO/IEC 15693 和 ISO/IEC 18000-3（模式 1）标准的 RFID 接口以及 SPI 或 I^2C 接口进行通信、参数设置和配置。 该器件具有内部温度传感器功能和板载 14 位 Σ-Δ 模数转换器 (ADC)，支持传感器测量，并且可通过 SPI 或 I^2C 来连接数字传感器。

RF430FRL15xH 器件经过优化可在完全无源（无电池）或单节电池供电（半有源）模式下运行，从而延长便携式和无线传感应用中电池的使用寿命。 FRAM 是非易失性存储器，其完美结合了 SRAM 的速度、灵活性和耐用性与闪存的稳定性和可靠性，并且总功耗更低。

器件信息(1)

器件型号	封装	封装尺寸(2)
RF430FRL152H	VQFN (24)	4mm x 4mm
RF430FRL153H	VQFN (24)	4mm x 4mm
RF430FRL154H	VQFN (24)	4mm x 4mm

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in 节 9, or see the TI web site at www.ti.com.
(2) 这里显示的尺寸为近似值。 要获得包含误差值的封装尺寸，请参见节 9中的*机械数据*。

1.4 功能方框图

图 1-1 显示了 RF430FRL15xH 器件的框图。

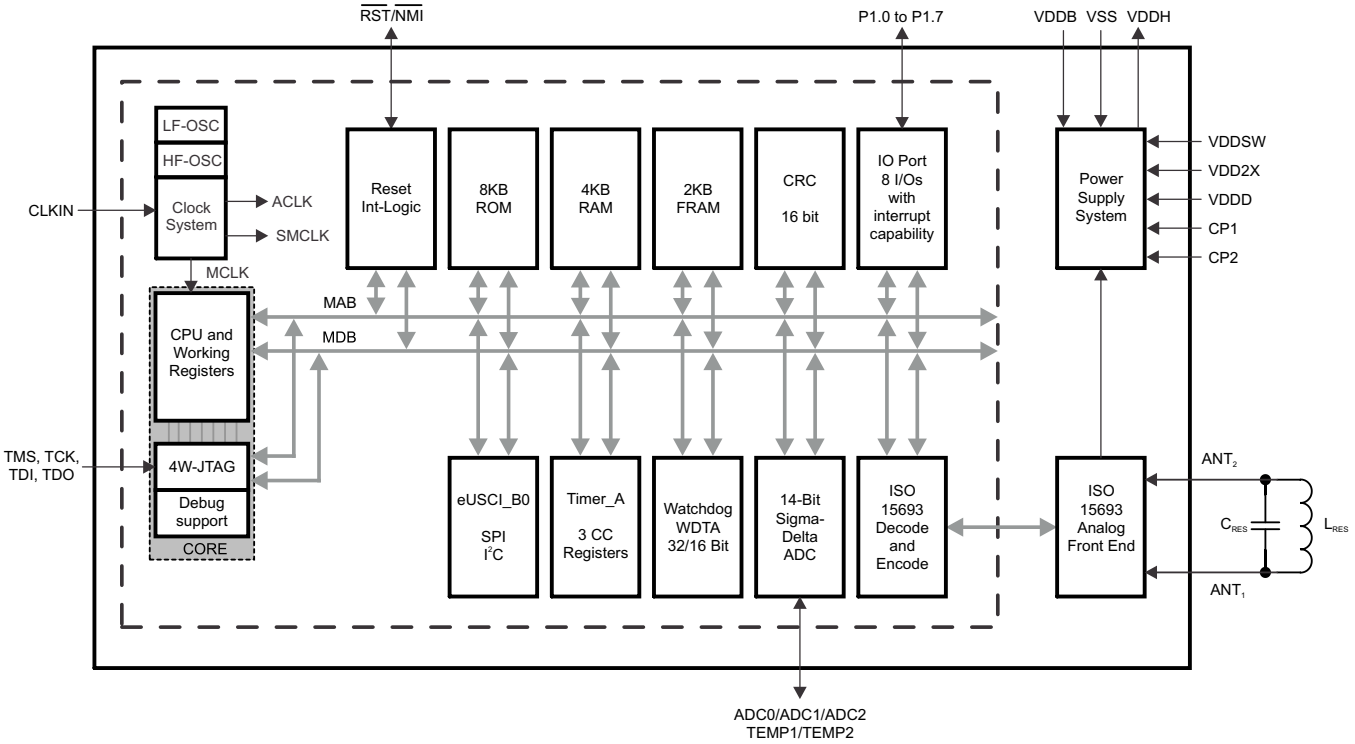


图 **1-1.** 功能框图

内容

2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 13, 2014 to December 8, 2014 **Page**

- 更正了《*RF430FRL15xH 系列技术参考手册*》标题的全部实例 1
- 更正了《*RF430FRL15xH 固件用户指南*》标题的全部实例 1
- Moved T_{stg} to *Absolute Maximum Ratings* table 10
- Changed title of Section 5.2 to *ESD Ratings* 10

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison(1)

Device	FRAM (KB)	SRAM (KB)	Timer	13.56-MHz ISO/IEC 15693 Front End	eUSCI_B	SD14
RF430FRL152H	2	4	Yes	Yes	Yes	Yes
RF430FRL153H	2	4	Yes	Yes	No	Yes
RF430FRL154H	2	4	Yes	Yes	Yes	No

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in 节 9, or see the TI web site at www.ti.com.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pin assignments on the 24-pin RGE package.

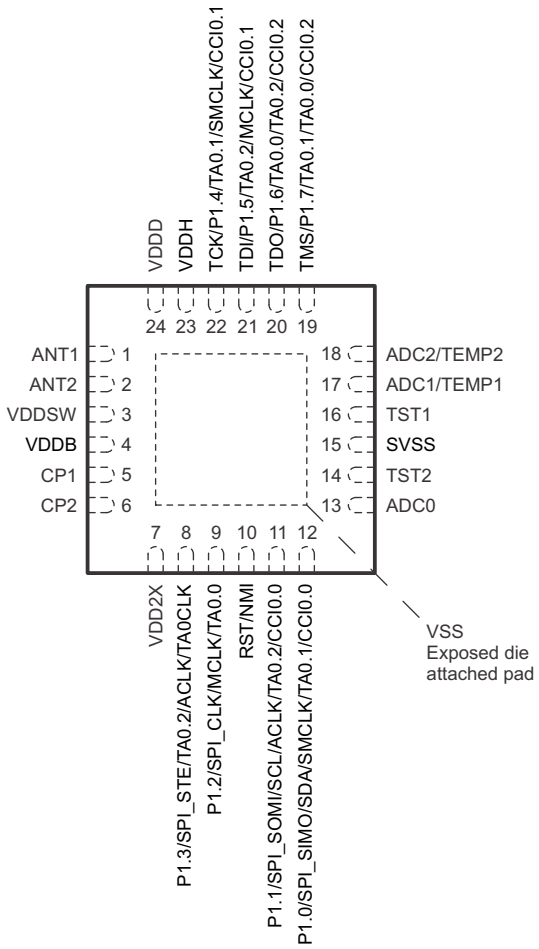


Figure 4-1. 24-Pin RGE Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals.

Table 4-1. Signal Descriptions

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
ANT1	1	I	Antenna input 1
ANT2	2	I	Antenna input 2
V_{DDSW}	3		Switched supply voltage
V_{DDB}	4		Battery supply voltage
CP1	5		Charge pump flying cap terminal 1
CP2	6		Charge pump flying cap terminal 2
V_{DD2X}	7		Voltage doubler output
P1.3 SPI_STE TA0.2 ACLK TA0CLK	8	I/O	General-purpose digital I/O SPI slave transmit enable Timer_A TA0 OUT2 output ACLK output (divided by 1, 2, 4, 8, 16, or 32) Timer_A TA0 clock signal TA0CLK input
P1.2 SPI_CLK MCLK TA0.0	9	I/O	General-purpose digital I/O SPI clock MCLK output Timer_A TA0 OUT0 output
RST/NMI	10	I	Reset input active low Non-maskable interrupt input
P1.1 SPI_SOMI SCL ACLK TA0.2 CCI0.0	11	I/O	General-purpose digital I/O SPI slave out master in I^2C clock ACLK output (divided by 1, 2, 4, or 8) Timer_A TA0 OUT2 output Timer_A TA0 CCR0 capture: CCI0B input, compare
P1.0 SPI_SIMO SDA SMCLK TA0.1 CCI0.0	12	I/O	General-purpose digital I/O SPI slave in master out I^2C data SMCLK output Timer0_A3 OUT1 output Timer_A TA0 CCR0 capture: CCI0A input, compare
ADC0	13	I	ADC input pin 0
TST2	14		Internal; connect to GND
SVSS	15		Sensor reference potential
TST1	16		Internal; connect to GND
ADC1 / TEMP1	17		ADC input pin 1 / Resistive bias pin 1
ADC2 / TEMP2	18		ADC input pin 2 / Resistive bias pin 2

(1) I = input, O = output

Table 4-1. Signal Descriptions (continued)

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
TMS	19	I/O	JTAG test mode select
P1.7			General-purpose digital I/O
TA0.1			Timer_A TA0 OUT1 output
TA0.0			Timer_A TA0 OUT0 output
CCI0.2			Timer_A TA0 CCR2 capture: CCI2B input, compare
TDO	20	I/O	JTAG test data output
P1.6			General-purpose digital I/O
TA0.0			Timer_A TA0 OUT0 output
TA0.2			Timer_A TA0 OUT2 output
CCI0.2			Timer_A TA0 CCR2 capture: CCI2A input, compare
TDI	21	I/O	JTAG test data input
P1.5			General-purpose digital I/O
TA0.2			Timer_A TA0 OUT2 output
MCLK			MCLK output
CCI0.1			Timer_A TA0 CCR1 capture: CCI1B input, compare
TCK	22	I/O	JTAG test clock
P1.4			General-purpose digital I/O
TA0.1			Timer_A TA0 OUT1 output
SMCLK			SMCLK output
CCI0.1			Timer_A TA0 CCR1 capture: CCI1A input, compare
CLKIN			External clock input pin
V_{DDH}	23	O	Rectified voltage from RF-AFE
V_{DDD}	24		Digital supply voltage
V_{SS}	Pad		Ground reference, bonded to exposed pad(2)

(2) VSS combines both digital ground (DV_{SS}) and analog ground (AV_{SS})

4.3 Pin Multiplexing

The GPIO port pins are multiplexed with other functions including analog peripherals and serial communication modules. The pin functions are selected by a combination of register values and device modes. For schematics of the port pins and details of the multiplexing for each, refer to 节 6.7.

4.4 Connections for Unused Pins

The correct termination of all unused pins is listed in Table 4-2.

Table 4-2. Connection of Unused Pins

Pin	Potential	Comment
TDI/TMS/TCK	Open	When used for JTAG function
$\overline{RST}$/$\overline{NMI}$	V_{CC} or V_{SS}	10-nF capacitor to GND/V_{SS}
Px.0 to Px.7	Open	Set to port function, output direction
TDO	Open	Convention: leave TDO terminal as JTAG function

5 Specifications

5.1 Absolute Maximum Ratings(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at V_{DDB} referenced to V_{SS} (V_{AMR})	-0.3	1.65	V
Voltage applied at V_{ANT} referenced to V_{SS} (V_{AMR})	-0.3	3.6	V
Voltage applied to any pin (references to V_{SS})	-0.3	V_{DDB} + 0.3	V
Diode current at any device pin(2)		±2	mA
Current derating factor when I/O ports are switched in parallel electrically and logically(3)		0.9	
Storage temperature range, T_{stg}(4) (5) (6)	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to V_{SS}.
(3) The diode current increases to ±4.5 mA when two pins are connected, it increases to ±6.75 mA when three pins are connected, and so on.
(4) Soldering during board manufacturing must follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels. If hand soldering is required for application prototyping, peak temperature must not exceed 250°C for a total of 5 minutes for any single device.
(5) Data retention on FRAM memory cannot be ensured when exceeding the specified maximum storage temperature, T_{stg}.
(6) Programming of devices with user application code should only be performed after reflow or hand soldering. Factory programmed information, such as calibration values, are designed to withstand the temperatures reached in the current JEDEC J-STD-020 specification.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge (ESD) performance	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Low leakage pin: ADC0 has reduced ESD tolerance of ±500 V HBM.

5.3 Recommended Operating Conditions

Typical data are based on V_{DDB} = 1.5 V, T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DDB}	Supply voltage during program execution	1.45		1.65	V
V_{SS}	Supply voltage (GND reference)		0		V
T_A	Operating free-air temperature	0		70	°C
C_{VDDB}	Capacitor on V_{DDB} (1)		100		nF
C_{VDDSW}	Capacitor on V_{DDSW} (1)		2.2		µF
C_{FLY}	Charge pump capacitor between CP1 and CP2. Recommended ratio between C_{FLY} and C_{VDD2X} is ≥ 1:10. (1)		10		nF
C_{VDD2X}	Capacitor on V_{DD2x}. Recommended ratio between C_{FLY} and C_{VDD2X} is ≥ 1:10.(1)		100		nF
C_{VDDD}	Capacitor on V_{DDD} (1)		1		µF
C_{SVSS}	Capacitor between SVSS and V_{SS} (1)		1		µF
f_{SYSTEM}	System frequency(2) (3)			2	MHz
f_{CLKIN}	External clock input frequency		32		kHz

(1) Low equivalent series resistance (ESR) capacitor
(2) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(3) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

5.4 Recommended Operating Conditions, Resonant Circuit

		MIN	NOM	MAX	UNIT
f_c	Carrier frequency		13.56		MHz
V_{ANT_peak}	Antenna input voltage			3.6	V
Z	Impedance of LC circuit	6.5	15.5		kΩ
L_{RES}	Coil inductance		2.66		µH
C_{RES}	Resonance capacitance		51.8 – C_{IN} (1)		pF
QT	Tank quality factor		30		

(1) See the RF13M parameter section.

5.5 Active Mode Supply Current Into V_{DDB} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1)

PARAMETER	EXECUTION MEMORY	V_{DDB}	Frequency ($f_{MCLK} = f_{SMCLK}$)				UNIT
			1 MHz		2 MHz		
			TYP	MAX	TYP	MAX	
$I_{AM,\ FRAM}$ (2)	FRAM	1.5 V	330	420	480	580	µA
$I_{AM,\ RAM}$ (2)	RAM	1.5 V	220	300	250	320	µA
$I_{AM,\ ROM}$ (2)	ROM	1.5 V	220	300	230	300	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) f_{ACLK} = 256 kHz, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0

5.6 Low-Power Mode Supply Current (Into V_{DDB}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		V_{DDB}	0ºC		20ºC		45ºC		70ºC		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0} (2)	f_{MCLK} = off, f_{SMCLK} = 1 MHz, f_{ACLK} = 32 kHz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	1.5 V	170	230	190		210		260	340	µA
I_{LPM3} (3)	f_{MCLK} = f_{SMCLK} = off, f_{ACLK} = 16 kHz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	1.5 V	12	20	13		16		25	65	µA
I_{LPM4} (4)	f_{MCLK} = f_{SMCLK} = f_{ACLK} = 0 Hz CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	1.5 V	11	16	12		15		24	60	µA

(1) Including current for WDT clocked by ACLK.
(2) CSS: SELM=SELS=HF_CLK, SELA=LF_CLK, DIVM=/2 (2MHz), DIVS=/4 (1MHz), DIVA=/8 (32kHz)
SD14: reset values
RFPMM: battery switch on (EN_BATSWITCH=1)
(3) CSS: SELM=HF_CLK, SELS=SELA=LF_CLK, DIVM=/2 (2MHz), DIVS=/32 (8kHz), DIVA=/16 (16kHz)
SD14: reset values
RFPMM: EN_BATSWITCH=1(battery switch enabled)
(4) CSS: SELM=HF_CLK, SELS=SELA=LF_CLK, DIVM=/2 (2MHz), DIVS=/32 (8kHz), DIVA=/16 (16kHz)
SD14: reset values
RFPMM: EN_BATSWITCH=1(battery switch enabled)

5.7 Digital I/Os (P1, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{DDB} = 1.5 V, I_{OH} = -400 µA(1) for port P1	V_{DDB} – 0.15			V
V_{OL}	Low-level output voltage	V_{DDB} = 1.5 V, I_{OL} = 400 µA(2) for port P1			0.15	V
V_{IH}	High-level input voltage	V_{DDB} = 1.5 V	0.7 × V_{DDB}			V
V_{IL}	Low-level input voltage	V_{DDB} = 1.5 V			0.3 × V_{DDB}	V
I_{OH}	High-level output current	V_{DDB} = 1.45 V to 1.65 V for port P1	-400			µA
I_{OL}	Low-level output current	V_{DDB} = 1.45 V to 1.65 V for port P1			400	µA
I_{LKG}	High-impedance leakage current	V_{DDB} = 1.45 V to 1.65 V	-100		100	nA
t_{INT}	External interrupt timing(3)	P1.x, V_{DDB} = 1.45 V to 1.65 V		200		ns
R_{PULL}	Pullup or pulldown resistor	V_{DDB}=1.5 V, For pullup: V_{IN} = V_{SS}, For pulldown: V_{IN} = V_{DDB} for port P1	30	35	40	kΩ
R_{RST}	Pullup on RST/NMI		30	35	40	kΩ
R_{EXT}	External pullup resistor on RST terminal (optional)			47		kΩ
C_{EXT}	External capacitor on RST terminal			10		nF

(1) The maximum total current I_{OH}, for all outputs combined should not exceed 500 µA to hold the maximum voltage drop specified, limited by low leakage switches.
(2) The maximum total current I_{OL}, for all outputs combined should not exceed 500 µA to hold the maximum voltage drop specified.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_{INT} is met.

5.8 High-Frequency Oscillator (4 MHz), HFOSC

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{HFOSC}	±20%	3.04	3.8	4.56	MHz
Duty cycle		45%	50%	55%	
t_{START}			1		µs

5.9 Low-Frequency Oscillator (256 kHz), LFOSC

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFO}	trimmed ±5%	243	256	269	kHz
Duty cycle		45%	50%	55%	
t_{START}				11	µs

5.10 Wake-Up From Low-Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DDB}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode(1)		1.5 V		3.2	6	µs
$t_{WAKE-UP\ LPM34}$	Wake-up time from LPM3 or LPM4 to active mode(1)		1.5 V		160	260	µs
$t_{WAKE-UP\ RESET}$	Wake-up time from $\overline{RST}$ to active mode.(2)	V_{DDB} stable	1.5 V		210	310	µs

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is fetched. This time includes the activation of the FRAM during wake-up. f_{MCLK} = 2 MHz.
(2) The wake-up time is measured from the rising edge of the $\overline{RST}$ signal until the first instruction of the user program is fetched. This time includes the activation of the FRAM during wake-up. f_{MCLK} = 2 MHz.

5.11 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DDB}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10%	1.5 V			4	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	1.5 V	20			ns

5.12 eUSCI (SPI Master Mode) Recommended Operating Conditions

PARAMETER		CONDITIONS	V_{DDB}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ± 10%	1.5 V			f_{SYSTEM}	MHz

5.13 eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{DDB}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 0, UCMODEx = 01 or 10	1.5 V	1			UCxCLK cycles
		UCSTEM = 1, UCMODEx = 01 or 10	1.5 V	1			
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 0, UCMODEx = 01 or 10	1.5 V	1			UCxCLK cycles
		UCSTEM = 1, UCMODEx = 01 or 10	1.5 V	1			
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	1.5 V			55	ns
		UCSTEM = 1, UCMODEx = 01 or 10	1.5 V			35	
$t_{STE,DIS}$	STE disable time, STE inactive to SIMO high impedance	UCSTEM = 0, UCMODEx = 01 or 10	1.5 V			40	ns
		UCSTEM = 1, UCMODEx = 01 or 10	1.5 V			30	
$t_{SU,MI}$	SOMI input data setup time		1.5 V	35			ns
$t_{HD,MI}$	SOMI input data hold time		1.5 V	0			ns
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	1.5 V			30	ns
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	1.5 V	0			ns

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-1 and Figure 5-2.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-1 and Figure 5-2.

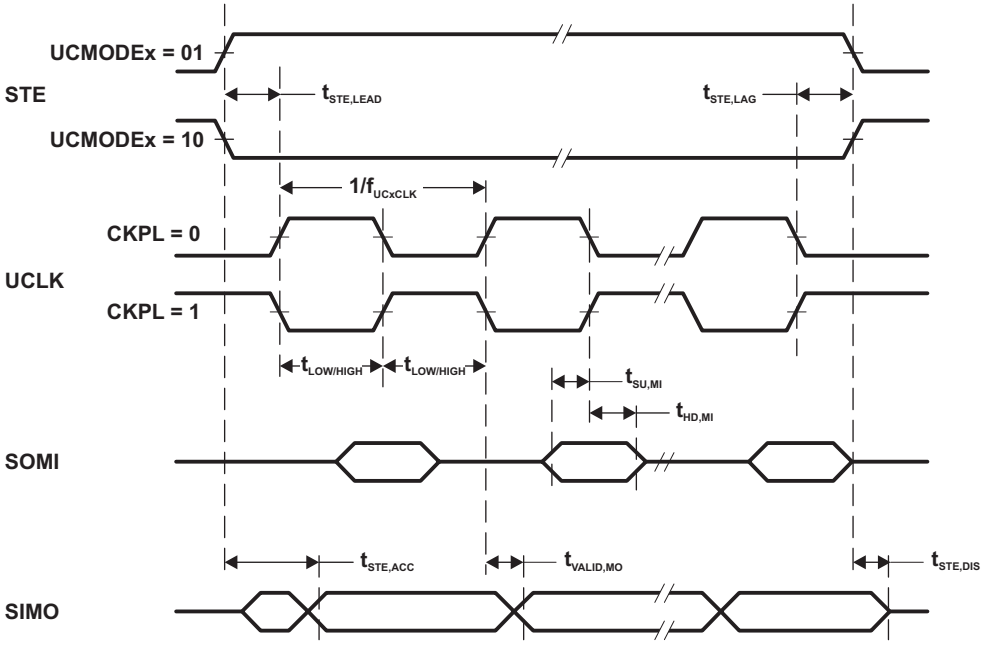


Figure 5-1. SPI Master Mode, CKPH = 0

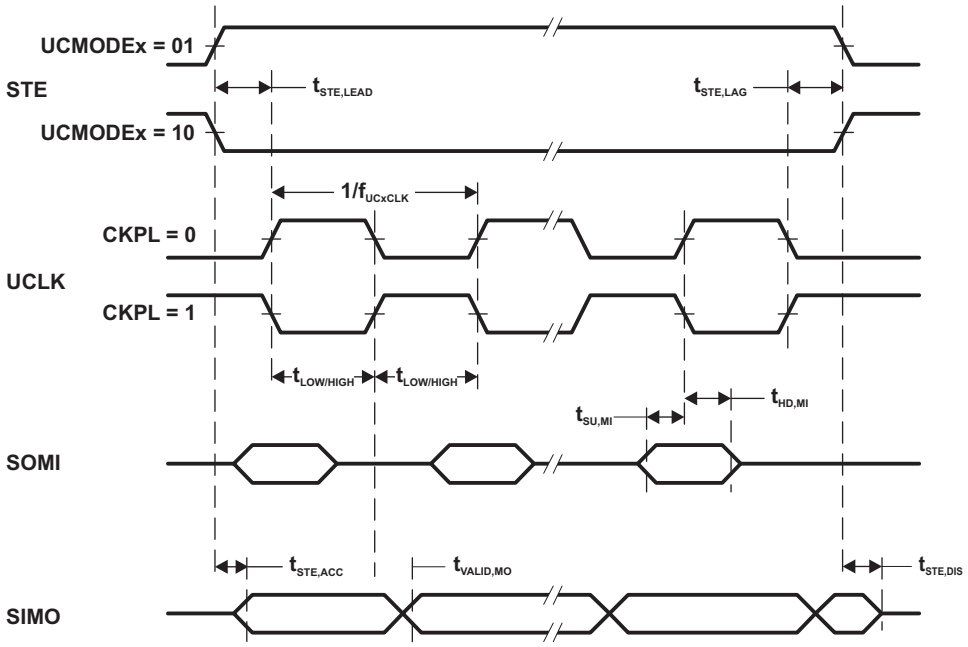


Figure 5-2. SPI Master Mode, CKPH = 1

5.14 eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{DDB}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		1.5 V	7			ns
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		1.5 V	0			ns
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		1.5 V			65	ns
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		1.5 V			40	ns
$t_{SU,SI}$	SIMO input data setup time		1.5 V	2			ns
$t_{HD,SI}$	SIMO input data hold time		1.5 V	5			ns
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	1.5 V			30	ns
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF	1.5 V	4			ns

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-3 and Figure 5-4.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-3 and Figure 5-4.

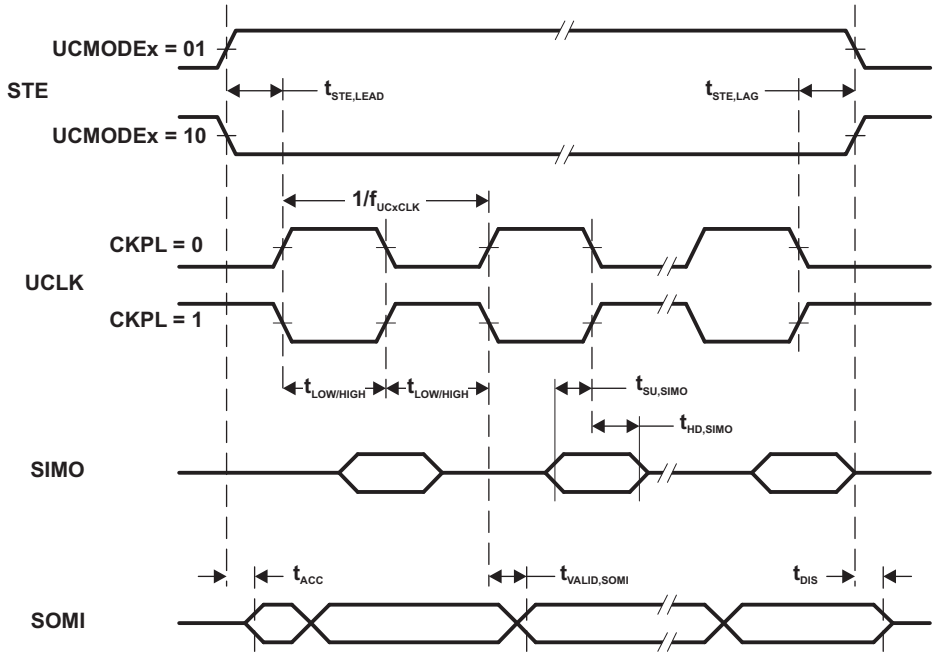


Figure 5-3. SPI Slave Mode, CKPH = 0

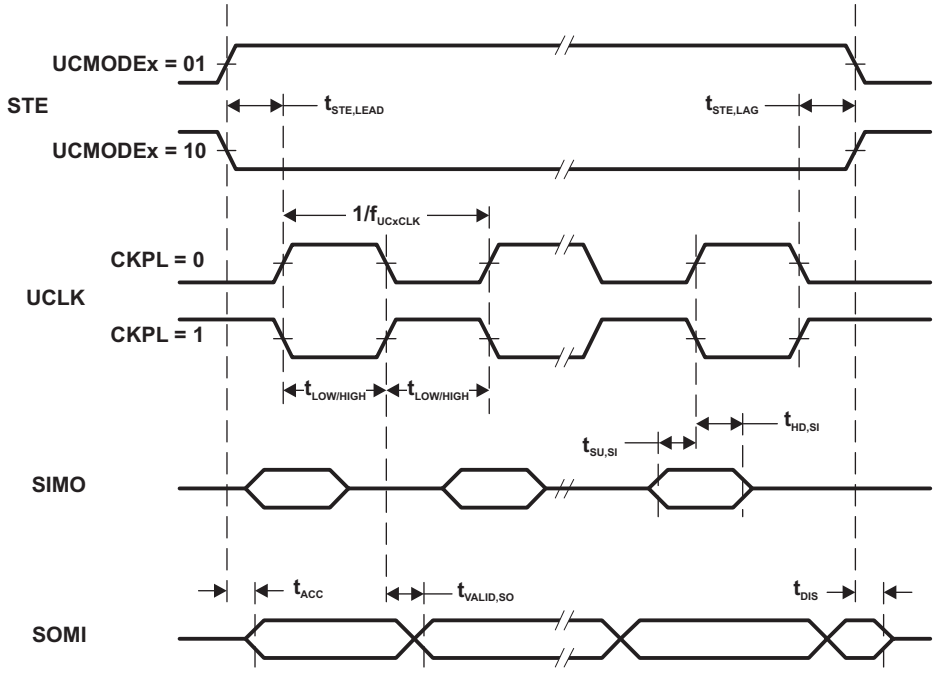


Figure 5-4. SPI Slave Mode, CKPH = 1

5.15 eUSCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-5)

PARAMETER		TEST CONDITIONS	V_{DDB}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		1.5 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	1.5 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	1.5 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		1.5 V	0			ns
$t_{SU,DAT}$	Data setup time		1.5 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	1.5 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	1.5 V	50		600	ns
		UCGLITx = 1		25		300	ns
		UCGLITx = 2		12.5		150	ns
		UCGLITx = 3		6.25		75	ns
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1	1.5 V		27		ms
		UCCLTOx = 2			30		ms
		UCCLTOx = 3			33		ms

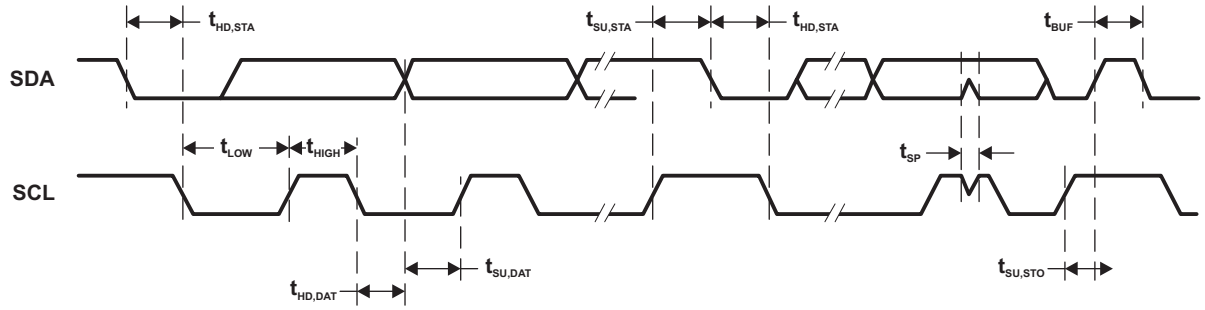


Figure 5-5. I^2C Mode Timing

5.16 FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WRITE}	Word or byte write time				125	ns
	Read/write endurance		10^{15}			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	10			years

5.17 JTAG

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{DDB}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency, 4-wire JTAG(1)	1.5 V	0		4	MHz

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.18 RFPMM, Power Supply Switch

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH+}	Positive going switching threshold $V_{TH+} = V_{DDB}-V_{DDR}$			35	60	mV
V_{TH-}	Negative going switching threshold $V_{TH-} = V_{DDB}-V_{DDR}$		-60	-35		mV
V_{HYST}	Switching voltage hysteresis $V_{HYST} = V_{TH+}-V_{TH-}$		30	70	110	mV
$I_{BASVBAT}$	V_{DDB} input leakage current	V_{DDB} = 1.65 V, Battery switch open			20	nA
V_{DROP}	$V_{DROP} = V_{DDB} - V_{DDSW}$ (1)				50	mV

(1) Battery switch closed. Current = 400 µA

5.19 RFPMM, Bandgap Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Output voltage	V_{DDSW} = 1.4 V to 1.65 V	892		908	mV

5.20 RFPMM, Voltage Doubler

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD2X}	Output voltage	V_{DDSW} = 1.4 V, I_{DD2X} = 1 µA, cont = 0	2 × V_{DDSW} – 74mV			mV
V_{DD2X}	Output voltage	V_{DDSW} = 1.4 V, I_{DD2X} = 100 µA, cont = 1	2 × V_{DDSW} – 104mV			mV

5.21 RFPMM, Voltage Supervision

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{DDSW}	MIN	TYP	MAX	UNIT
V_{DDBTH+}	Positive threshold	1.5 V		1.45		V
V_{DDBTH-}	Negative threshold	1.5 V		1.40		V
$V_{DDSWTH+}$	Positive threshold			1.40		V
$V_{DDSWTH-}$	Negative threshold			1.35		V
V_{DDDTH+}	Positive threshold	1.5 V		1.00		V
V_{DDDTH-}	Negative threshold	1.5 V		0.90		V
$V_{DD2XTH+}$	Positive threshold	1.5 V		2.70		V
$V_{DD2XTH-}$	Negative threshold	1.5 V		2.475		V

5.22 SD14, Performance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_M	Modulator clock frequency	Internal LF oscillator as clock source for SD14 module		2		kHz
RES	Resolution		8		14	Bit
OSR	Oversampling ratio		40		2048	
B	Bandwidth of input signal				1	Hz
V_I	Input voltage range	$V_I = V_{ADCx} - V_{SVSS}$	0		V_{REF}	mV
V_{offset}	Offset error	Complete signal chain	-0.75		0.75	% of FSR(1)
V_{GErr}	Gain error(2)	complete signal chain	-2%		2%	
$\Delta E_G/\Delta T$	Gain error temperature coefficient. (3)	complete signal chain			100	ppm/K
$E_{Unadjusted}$	Total unadjusted error		-2		2	% of FSR(1)
t_{Start}	Startup time			20		CLK cycles

(1) FSR = Full Scale Range (SD14 pre-amplifier Gain PGA gain - SD14 gain =1) .
(2) The gain error E_G specifies the deviation of the actual gain G_{act} from the nominal gain G_{nom}: $E_G = (G_{act} – G_{nom})/G_{nom}$. It covers process, temperature and supply voltage variations.
(3) Not production tested.

5.23 SVSS Generator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SVSS}	Output voltage	I_{SVSS} = -5uA .. 0uA	80	125	165	mV
$t_{Settling}$	Settling time after switching SVSS on (95% of final voltage)	Switch from VIRTGND = 1 to VIRTGND = 0		400	1000	ms

5.24 Thermistor Bias Generator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OUT,TH}$	Output current	V_{OUT} = 0 to 0.7 V	2.0	2.4	3.0	µA

5.25 Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	Temperature coefficient			35.7		LSB/K

5.26 RF13M, Power Supply and Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDH}	Antenna rectified voltage	I_{DDH} = 100 µA	1.8	2	3.6	V
C_{IN}	Input capacitance	2 V RMS	31.5	35	38.5	pF

5.27 RF13M, ISO/IEC 15693 ASK Demodulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
DR_{100}	Input signal data rate 100% downlink modulation, 100% ASK, ISO/IEC 15693	6		26	kbps
m100	Modulation depth 100%, test as defined in ISO10373	90%		100%	
m10	Modulation depth 10%, test as defined in ISO10373	7%		30%	
$\lvert t_{PLH} - t_{PHL} \rvert$	Delta propagation delay of RXD_10 to V_{IN}	0		2.35	µs
t_{PLH}, t_{PHL}	Propagation delay of RXD_10 to V_{IN}	0		7.07	µs
t_{pd100}	Propagation delay of RXD_100			7.07	µs
t_{D100}	Minimum pulse duration of RxD_100	5			µs

5.28 RF13M, ISO/IEC 15693 Compliant Load Modulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{PICC}	Uplink subcarrier modulation frequency	0.2		1	MHz
V_{A_MOD}	Modulated antenna voltage, V_{A_unmod} = 2,3V	0.5			V
V_{SUB15}	Uplink modulation subcarrier level, ISO/IEC 15693	10			mV

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-Bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data.

6.3 Operating Modes

The device has one active mode and three software selectable low-power modes of operation. An interrupt event can wake up the device from any of the three low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

注

The software-selected low-power mode might not be reached if at least one module still requests a clock on MCLK, SMCLK, or ACLK. The CPU, however, remains off until an interrupt occurs.

The following operating modes can be configured by software:

- Active mode AM
  - CPU is enabled
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is active
  - ACLK is active
  - HFOSC is off, if not selected for SMCLK or ACLK
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK is active
  - HFOSC is off, if not selected for ACLK
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK is disabled
  - HFOSC is off, LFOSC is on

LPM1 is identical to LPM0, and LPM2 is identical to LPM3, because the SCG0 bit has no influence on HFOSC.

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FFE0h. Address Range 0FFDFh to 0FFD0h is reserved for bootcode signatures. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

表 6-1. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog	WDTIFG (1)	Reset	FFFEh	15, highest
System NMI Vacant memory access	SVMIFG, VMAIFG (1)	(Non)maskable	0FFFCh	14
User NMI NMI	NMIIFG (1) (2)	(Non)maskable	0FFFAh	13
TimerA0_A3	TA0CCR0 CCIFG0 (3)	Maskable	0FFF8h	12
TimerA0_A3	TA0CCR1 CCIFG1 TA0CCR2 CCIFG2 TA0CTL TAIFGTA0IV (1) (3)	Maskable	0FFF6h	11
Watchdog, Interval Timer Mode	WDTIFG	Maskable	0FFF4h	10
RF13M Module	RF13MRXIFG, RF13MTXIFG, RF13MRXWMIFG, RF13MTXWMIFG, RF13MSLIFG, RF13MOUFLIFG, RF13MRXEIFG, RF13MIVx (1) (3)	Maskable	0FFF2h	9
eUSCIB	(SPI mode) UCB0RXIFG, UCB0TXIFG (I^2C mode) UCB0ALIFG, UCB0NACKIFG, UCB0STTIFG, UCB0STPIFG, UCB0RXIFG3, UCB0TXIFG3, UCB0RXIFG2, UCB0TXIFG2, UCB0RXIFG1, UCB0TXIFG1, UCB0RXIFG0, UCB0TXIFG0, UCB0CNTIFG, UCB0CLTOIFG, UCB0BIT9IFG (SD14IV) (1) (3)	Maskable	0FFF0h	8
Sigma Delta ADC	SD14OVIFG, SD14IFG (1) (3)	Maskable	0FFEEh	7
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV) (1) (3)	Maskable	0FFECh	6
RFPMM	RFPMMIFGV2X, RFPMMIFGVH, RFPMMIFGVR, RFPMMIFGVB, RFPMMIFGVF, RFPMMIV	Maskable	0FFEAh	5
Reserved	Reserved (4)		0FFE8h	4
			⋮	⋮
			0FFDCh	0

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Reserved interrupt vectors at these addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

表 6-1. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Signatures	CRC Value		0FFDAh	
	CRC Length		0FFD8h	
	Loader Signature 1		0FFD6h	
	Loader Signature 0		0FFD4h	
	JTAG Signature 1		0FFD2h	
	JTAG Signature 0		0FFD0h	

6.5 Memory

表 6-2 shows the memory organization of the devices.

表 6-2. Memory Map RF430FRL152H, RF430FRL153H, RF430FRL154H

	TYPE	RF430FRL152H RF430FRL153H RF430FRL154H Normal Mode	RF430FRL152H RF430FRL153H RF430FRL154H ROM Development Mode
Memory (FRAM) Main: interrupt vector	Total Size FRAM	2048 B = 2 KB 0FFFFh-0FFE0h	
Main: Code Memory	Bank A(1)(2)	512 B 0FFFFh-0FE00h	
	Bank B(1)	512 B 0FDFFh-0FC00h	
	Bank C(1)	512 B 0FBFFh-0FA00h	
	Bank D	448 B 0F9FFh-0F840h	
Boot Data (TLV)	Size FRAM	64 B 01A3Fh-01A00h	64 B 01A3Fh-01A00h
Application ROM	Size ROM	7168 B = 7 KB 05FFFh-04400h	3584 B = 3.5 KB 051FFh-04400h
ROM Development Memory	Size SRAM	- -	3584 B = 3.5 KB 02BFFh-01E00h
SRAM Memory	Size SRAM	4096 B = 4 KB 02BFFh-01C00h	512 B = 0.5 KB 01DFFh-01C00h
Peripherals	Size	4096 B = 4 KB 00FFFh-00000h	4096 B = 4 KB 00FFFh-00000h

(1) Write protectable. See also 表 6-3
(2) Address range includes interrupt vector.

6.5.1 FRAM

The FRAM can be programmed through the JTAG port or in-system by the CPU, data are received through RF, SPI or I^2C Sensor Interface.

Features of the FRAM include:

- Low-power ultra-fast-write non-volatile memory
- Byte and word access capability
- Automated wait state generation

The following address ranges can be write protected by setting the corresponding bit in the SYSCNF register, see the *RF430FRL15xH Family Technical Reference Manual* (SLAU506).

表 6-3. Write Protectable FRAM Address Ranges

BIT	Address Range
FRAMLCK2	512 B 0FFFFh-0FE00h
FRAMLCK1	512 B 0FDFFh-0FC00h
FRAMLCK0	512 B 0FBFFh-0FA00h

6.5.2 SRAM

The SRAM memory is made up of 8 sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the SRAM memory include:

- SRAM memory has 8 sectors of 512 B each.
- Each sector 0 to 8 can be complete disabled; however, data retention is lost.
- Each sector 0 to 8 automatically enters low-power retention mode when possible.

6.5.3 Application ROM

The Application ROM consists of four parts. The RF Library provides ISO/IEC 15693 functions necessary for operating the 13.65 MHz front end. The Function library holds the device and memory function used by the boot code and RF library. These functions are user accessible. The ROM contains the predefined application FW. The boot code checks the password and releases control to the application or enables JTAG on password match, enters LPM4 and waits for debug session, see the *RF430FRL15xH Firmware User's Guide* (SLAU603).

6.6 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be managed using all instructions. For complete module descriptions, see the *RF430FRL15xH Family Technical Reference Manual* (SLAU506).

6.6.1 Digital I/O, (P1.x)

There is one I/O port implemented, P1, with eight I/O lines RF430FRL15xH.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown resistor on all ports.
- Edge-selectable interrupt input capability for all ports on P1.
- Read and write access to port-control registers is supported by all instructions.

6.6.2 Versatile I/O Port P1

The versatile I/O ports P1 feature device dependent reset values. The reset values for the RF430FRL15xH devices are shown in 表 6-4.

表 6-4. Versatile Port Reset Values

PORT NUMBER	PxOUT	PxDIR	PxREN	PxSEL0	PxSEL1	RESET	PORTS ON	COMMENT
P1.0	0	0	0	0	0	PUC	yes	P1.0, input
P1.1	0	0	0	0	0	PUC	yes	P1.1, input
P1.2	0	0	0	0	0	PUC	yes	P1.2, input
P1.3	0	0	0	0	0	PUC	yes	P1.3, input
P1.4	1	0	1	1	1	PUC	yes	JTAG TCK, P1.4, input
P1.5	1	0	1	1	1	PUC	yes	JTAG TDI, P1.5, input
P1.6	0	0	0	1	1	PUC	yes	JTAG TDO, P1.6, output
P1.7	1	0	1	1	1	PUC	yes	JTAG TMS, P1.7, input

6.6.3 Oscillator and System Clock

The clock system in the RF430FRL15xH devices is supported by the Compact Clock System (CCS) module that includes support for an internal trimmable 256-kHz current-controlled low-frequency oscillator (LFOSC) and an internal 4-MHz current-controlled high-frequency oscillator (HFOSC).

The CCS module is designed to meet the requirements of both low system cost and low power consumption. The CCS provides a fast turn-on of the oscillators in less than 1 ms. The CCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from the 256-kHz internal LFOSC.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.

6.6.4 Compact System Module (C-SYS_A)

The Compact SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, as well as, configuration management. It also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application.

表 6-5. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	INTERRUPT VECTOR	WORD ADDRESS	OFFSET	PRIORITY
SYSRSTIV, System Reset	No interrupt pending	019Eh	00h	
	Brownout (BOR)		02h	Highest
	SVMBOR (BOR)		04h	
	RST/NMI (BOR)		06h	
	DoBOR (BOR)		08h	
	Security violation (BOR)		0Ah	
	DoPOR (POR)		0Ch	
	WDT time-out (PUC)		0Eh	
	WDT key violation (PUC)		10h	
	CCS key violation		12h	
	PMM key violation		14h	
	Peripheral area fetch (PUC)		16h	
	Reserved		18h-3Eh	Lowest
SYSSNIV, System NMI	No interrupt pending	019Ch	00h	
	SVMIFG		02h	Highest
	VMAIFG		04h	
	JMBINIFG		06h	
	JMBOUTIFG		08h	
	Reserved		0Ah-3Eh	Lowest
SYSUNIV, User NMI	No interrupt pending	019Ah	00h	
	NMIFG		02h	Highest
	OFIFG		04h	
	BERR		06h	
	Reserved		08h-3Eh	Lowest
SYSBERRIV, Bus Error	No interrupt pending	0198h	00h	
	Reserved		02h-3Eh	Lowest

6.6.5 Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.6.6 Reset, NMI, SVMOUT System

The reset system of the RF430FRL15xH devices features the function reset input, reset output, and NMI input.

6.6.7 Timer_A (Timer0_A3)

Timer_A is a 16-bit timer/counter with three capture/compare registers. Timer_A can support multiple capture/compares, PWM outputs, and interval timing. Timer_A also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-6. Timer0_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODUL INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
8 – P1.3	TA0CLK	TACLK	Timer	NA	NA	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
	TA0CLK	$\overline{\text{TACLK}}$				
12 – P1.0	TA0.0	CCI0A	CCR0	TA0	TA0.0	9 – P1.2
11 – P1.1	TA0.0	CCI0B				20 – P1.6
	V_{SS}	GND				19 – P1.7
	V_{DDB}	Vcc				
22 – P1.4	TA0.1	CCI1A	CCR1	TA1	TA0.1	12 – P1.0
21 – P1.5	TA0.1	CCI1B				22 – P1.4
	V_{SS}	GND				19 – P1.7
	V_{DDB}	Vcc				
20 – P1.6	TA0.2	CCI2A	CCR2	TA2	TA0.2	11 – P1.1
19 – P1.7	TA0.2	CCI2B				8 – P1.3
	V_{SS}	GND				21 – P1.5
	V_{DDB}	Vcc				20 – P1.6

6.6.8 Enhanced Universal Serial Communication Interface (eUSCI_B0)

The eUSCI_B0 module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin) and I^2C.

The eUSCI_B0 module provides support for SPI (3 pin or 4 pin) or I^2C.

6.6.9 ISO/IEC 15693 Analog Front End (RF13M)

The ISO/IEC 15693 module supports contact-less communication over the analog front end according to ISO/IEC 15693 with data rates up to 26.48 kbps for receive and 26.48 kbps for transmit. It includes decode of receive data and encode of transmit data, both synchronous with the AFE carrier clock.

6.6.10 ISO/IEC 15693 Decoder/Encoder (RF13M)

The module interfaces directly to the analog front end to ensure correct timing for transmit and receive of data derived from the 13.56-MHz carrier frequency.

6.6.11 CRC16 Module (CRC16)

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data

checking purposes. The CRC16 module is compliant with ISO/IEC 13239, it is 16 bits long, polynominal is: $x^{16} + x^{12} + x^5 + 1$, direction is backward, and preset is 0xFFFF. For more information see ISO/IEC 13239.

6.6.12 14-Bit Sigma-Delta ADC (SD14)

A sigma-delta modulator is provided for high resolution analog-to-digital conversion of quasi-dc voltages:

- First-order integrator, 1-bit comparator, 1-bit DAC
- Sampling frequency of up to 2 kHz
- Fully differential

6.6.13 Programmable Gain Amplifier (SD14)

The PGA features a very high-impedance input and a programmable gain combined with full offset compensation, very low offset drift, and low noise.

6.6.14 Peripheral Register Map

表 6-7. Peripheral Register Map

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
RF13M	RF13M RX/TX High/Low Watermark Configuration Register	RF13MWMCFG	0800h	0Eh
	RF13M RX/TX FIFO Fill Level register	RF13MFIFOFL		0Ch
	RF13M CRC accumulator Register	RF13MCRC		0Ah
	RF13M Transmit Data FIFO Register	RF13MTXF		08h
	RF13M Receive Data FIFO Register	RF13MRXF		06h
	RF13M Interrupt Vector Register	RF13MIV		04h
	RF13M Interrupt Register	RF13MINT		02h
	RF13M Control Register	RF13MCTL		00h
SD14	SD14 Interrupt Vector Register	SD14IV	0700h	0Ch
	SD14 Intermediate Conversion Result Register	SD14MEM3		0Ah
	SD14 Intermediate Conversion Result Register	SD14MEM2		08h
	SD14 Intermediate Conversion Result Register	SD14MEM1		06h
	SD14 Conversion Result	SD14MEM0		04h
	SD14 Control Register 1	SD14CTL1		02h
	SD14 Control Register 0	SD14CTL0		00h
eUSCI_B0	Interrupt Vector Word Register	UCB0IV	0640h	2Eh
	Interrupt Flags Register	UCB0IFG		2Ch
	Interrupt Enable Register	UCB0IE		2Ah
	I2C Slave Address Register	UCB0I2CSA		20h
	Address Mask Register	UCB0ADDMASK		1Eh
	Received Address Register	UCB0ADDRX		1Ch
	I2C Own Address 3 Register	UCB0I2COA3		1Ah
	I2C Own Address 2 Register	UCB0I2COA2		18h
	I2C Own Address 1 Register	UCB0I2COA1		16h
	I2C Own Address 0 Register	UCB0I2COA0		14h
	Transmit Buffer Register	UCB0TXBUF		0Eh
	Receive Buffer Register	UCB0RXBUF		0Ch
	Byte Counter Threshold Register	UCB0TBCNT		0Ah
	Status Word Register	UCB0STATW		08h
	Bit Rate 1 Register	UCB0BR1		07h
	Bit Rate 0 Register	UCB0BR0		06h
	Control Word 1 Register	UCB0CTLW1		02h
	Control Word 0 Register	UCB0CTLW0		00h

表 6-7. Peripheral Register Map (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
Timer0_A3	Timer0_A Interrupt Vector Register	TA0IV	0340h	2Eh
	Capture/Compare Register 2	TA0CCR2		16h
	Capture/Compare Register 1	TA0CCR1		14h
	Capture/Compare Register 0	TA0CCR0		12h
	Timer0_A Counter Register	TA0R		10h
	Capture/Compare Control 2 Register	TA0CCTL2		06h
	Capture/Compare Control 1 Register	TA0CCTL1		04h
	Capture/Compare Control 0 Register	TA0CCTL0		02h
	Timer0_A Control Register	TA0CTL		00h
Port P1	Port P1 Interrupt Flag Register	P1IFG	0200h	1Ch
	Port P1 Interrupt Enable Register	P1IE		1Ah
	Port P1 Interrupt Edge Select Register	P1IES		18h
	Port P1 Interrupt Vector Word Register	P1IV		0Eh
	Port P1 Selection 1 Register	P1SEL1		0Ch
	Port P1 Selection 0 Register	P1SEL0		0Ah
	Port P1 Pullup/Pulldown Enable Register	P1REN		06h
	Port P1 Direction Register	P1DIR		04h
	Port P1 Outout Register	P1OUT		02h
	Port P1 Input Register	P1IN		00h
CSYS_A	Reset Vector Generator Register	SYSRSTIV	0180h	1Eh
	System NMI Vector Generator Register	SYSSNIV		1Ch
	User NMI Vector Generator Register	SYSUNIV		1Ah
	Bus Error Vector Generator Register	SYSBERRIV		18h
	System Configuration Actuator 0 Register	SYSCA0		14h
	System Configuration Register	SYSCNF		10h
	JTAG Mailbox Output Register 1	SYSJMBO1		0Eh
	JTAG Mailbox Output Register 0	SYSJMBO0		0Ch
	JTAG Mailbox Input Register 1	SYSJMBI1		0Ah
	JTAG Mailbox Input Register 0	SYSJMBI0		08h
	JTAG Mailbox Control Register	SYSJMBC		06h
	System Control Register	SYSCTL		00h
CCS	CCS Control 8 Register	CCSCTL8	0160h	10h
	CCS Control 7 Register	CCSCTL7		0Eh
	CCS Control 6Register	CCSCTL6		0Ch
	CCS Control 5 Register	CCSCTL5		0Ah
	CCS Control 4 Register	CCSCTL4		08h
	CCS Control 1 Register	CCSCTL1		02h
	CCS Control 0 Register	CCSCTL0		00h
WDT_A, CRC	Watchdog Timer Control Register	WDTCTL	0150h	0Ch
	CRC Result Reverse Register	CRCRESR		06h
	CRC Initialization and Result Register	CRCINIRES		04h
	CRC Data In Reverse Byte Register	CRCDIRB		02h
	CRC Data In Register	CRCDI		00h
FRAM Control	General Control 1 Register	GCCTL1	0140h	06h
	General Control 0 Register	GCCTL0		04h
	FRAM Control 0 Register	FRCTL0		00h

表 6-7. Peripheral Register Map (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
RFPMM	RFPMM Interrupt Vector Register	RFPMMIV	0120h	08h
	RFPMM Interrupt Flag Register	RFPMMIFG		06h
	RFPMM Interrupt Enable Register	RFPMMIE		04h
	RFPMM Control Register 1	RFPMMCTL1		02h
	RFPMM Control Register 0	RFPMMCTL0		00h
Special Functions	SFR Reset Pin Control Register	SFRRPCR	0100h	04h
	SFR Interrupt Flag Register	SFRIFG1		02h
	SFR Interrupt Enable Register	SFRIE1		00h

6.7 Port Schematics

6.7.1 Port P1.0 Input/Output

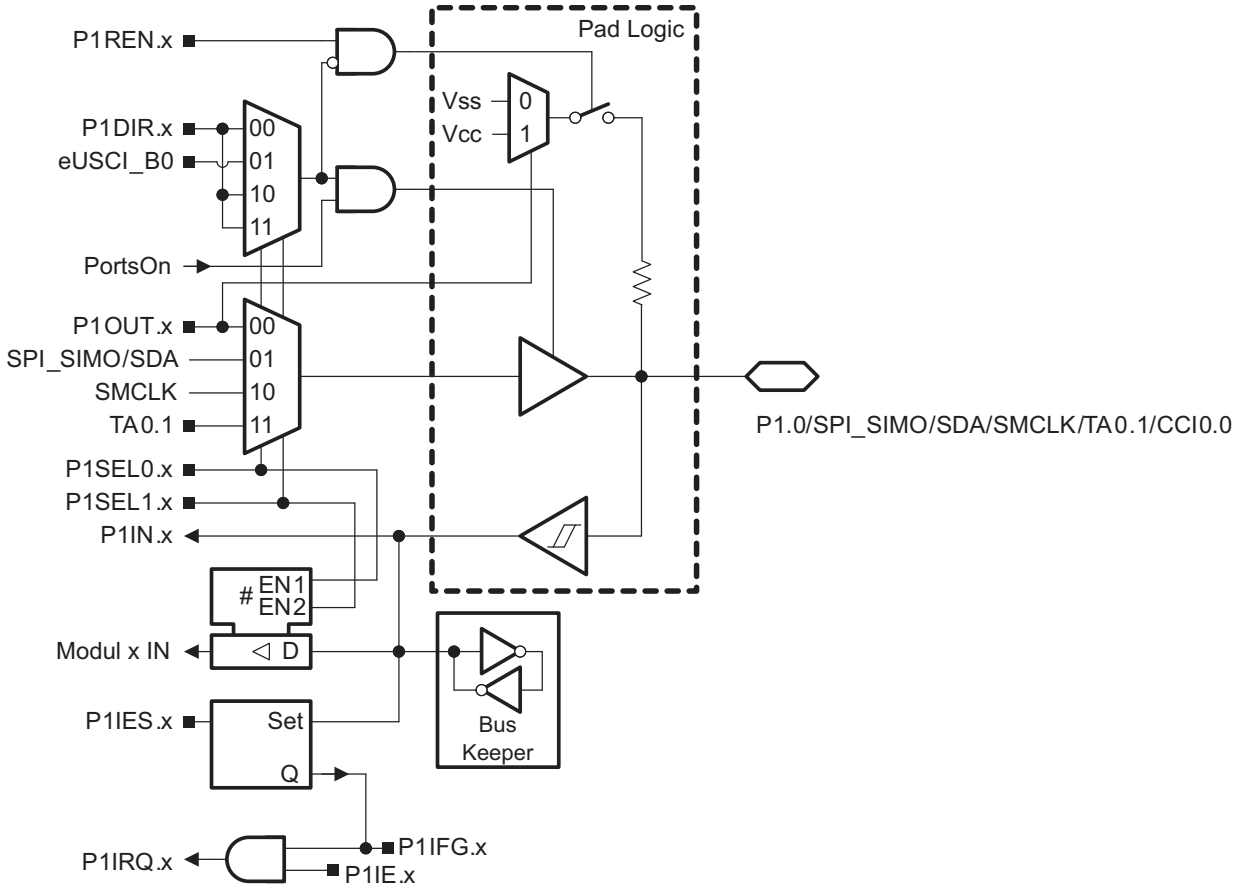


表 6-8. Port P1.0 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	RSELx/ ASELx
P1.0/SPI_SIMO/SDA/SMCLK/TA0.1/CCI0.0	0	P1.0 (I/O)	I:0; O:1	0	0	0
		SPI_SIMO/SDA(2)	1	0	1	0
		SMCLK	1	1	0	0
		TA0.1	1	1	1	0
		Timer A0, CCI0A	0	≠0	≠0	X

(1) X = Don't care
(2) Module controls direction of port, depending on whether RF430 device is master or slave.

6.7.2 Port P1.1 Input/Output

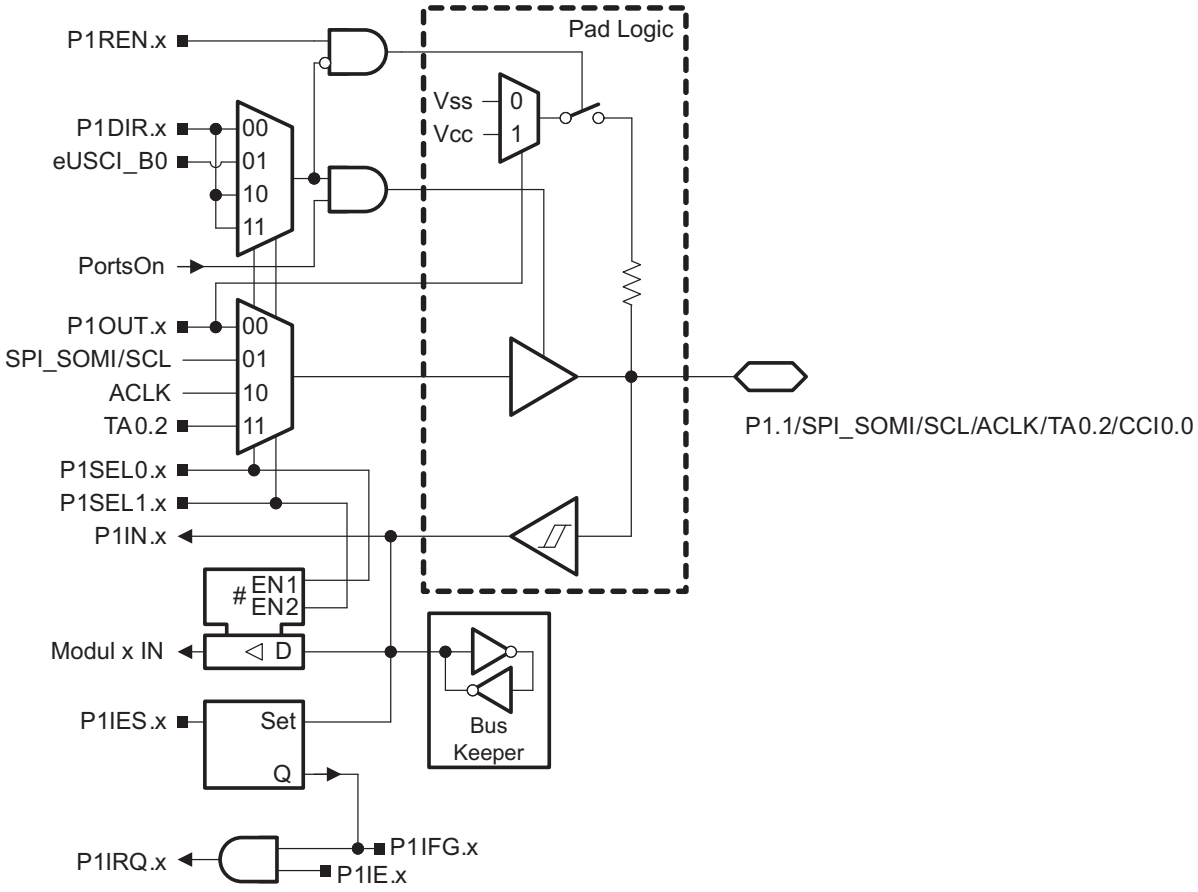


表 6-9. Port P1.1 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	RSELx/ASELx
P1.1/SPI_SOMI/SCL/ACLK/TA0.2/CCI0.0	1	P1.1 (I/O)	I:0; O:1	0	0	0
		SPI_SOMI/SCL(2)	1	0	1	0
		ACLK	1	1	0	0
		TA0.2	1	1	1	0
		Timer A1, CCI0B	0	≠0	≠0	X

(1) X = Don't care
(2) Module controls direction of port, depending on whether RF430 device is master or slave.

6.7.3 Port P1.2 Input/Output

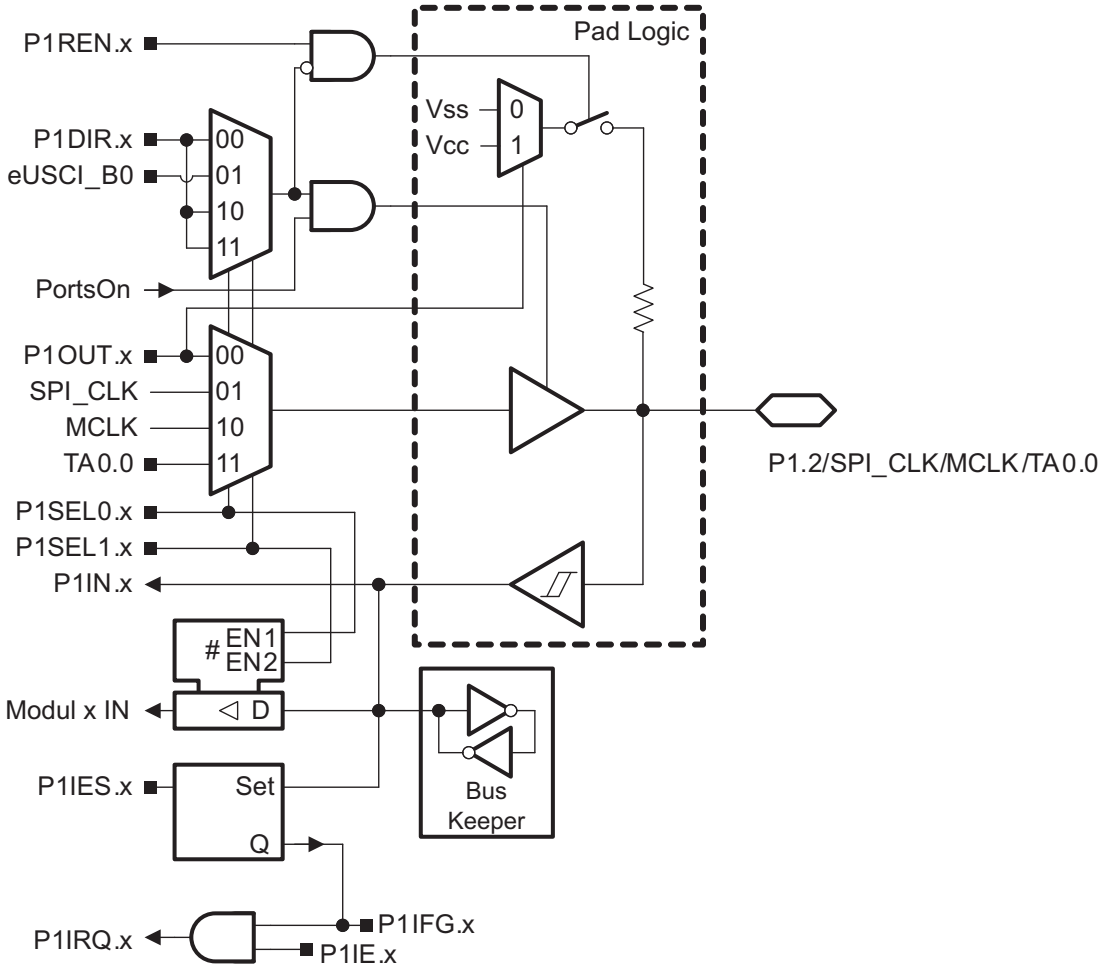


表 6-10. Port P1 (P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	RSELx/ASELx
P1.2/SPI_CLK/MCLK/TA0.0	2	P1.2 (I/O)	I:0; O:1	0	0	0
		SPI_CLK(2)	1	0	1	0
		MCLK	1	1	0	0
		TA0.0	1	1	1	0

(1) X = Don't care
(2) Module controls direction of port, depending on whether RF430 device is master or slave.

6.7.4 Port P1.3 Input/Output

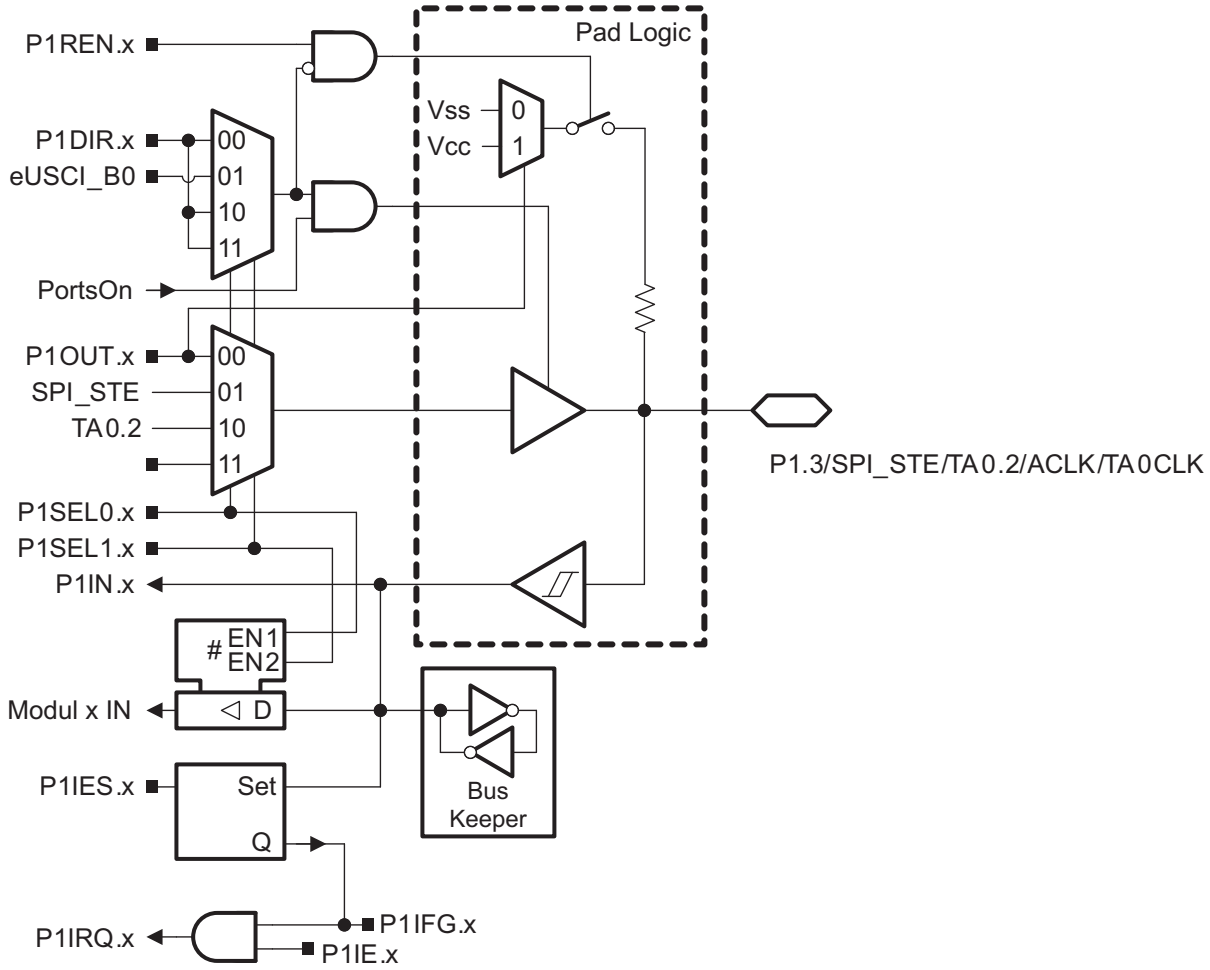


表 6-11. Port P1 (P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	RSELx/ASELx
P1.3/SPI_STE/TA0.2/ACLK/TA0CLK	3	P1.3 (I/O)	I:0; O:1	0	0	0
		SPI_STE(2)	1	0	1	0
		TA0.2	1	1	0	0
		ACLK	1	1	1	0
		TA0CLK	X	≠0	≠0	X

(1) X = Don't care
(2) Module controls direction of port, depending on whether RF430 device is master or slave.

6.7.5 Port P1.4 Input/Output

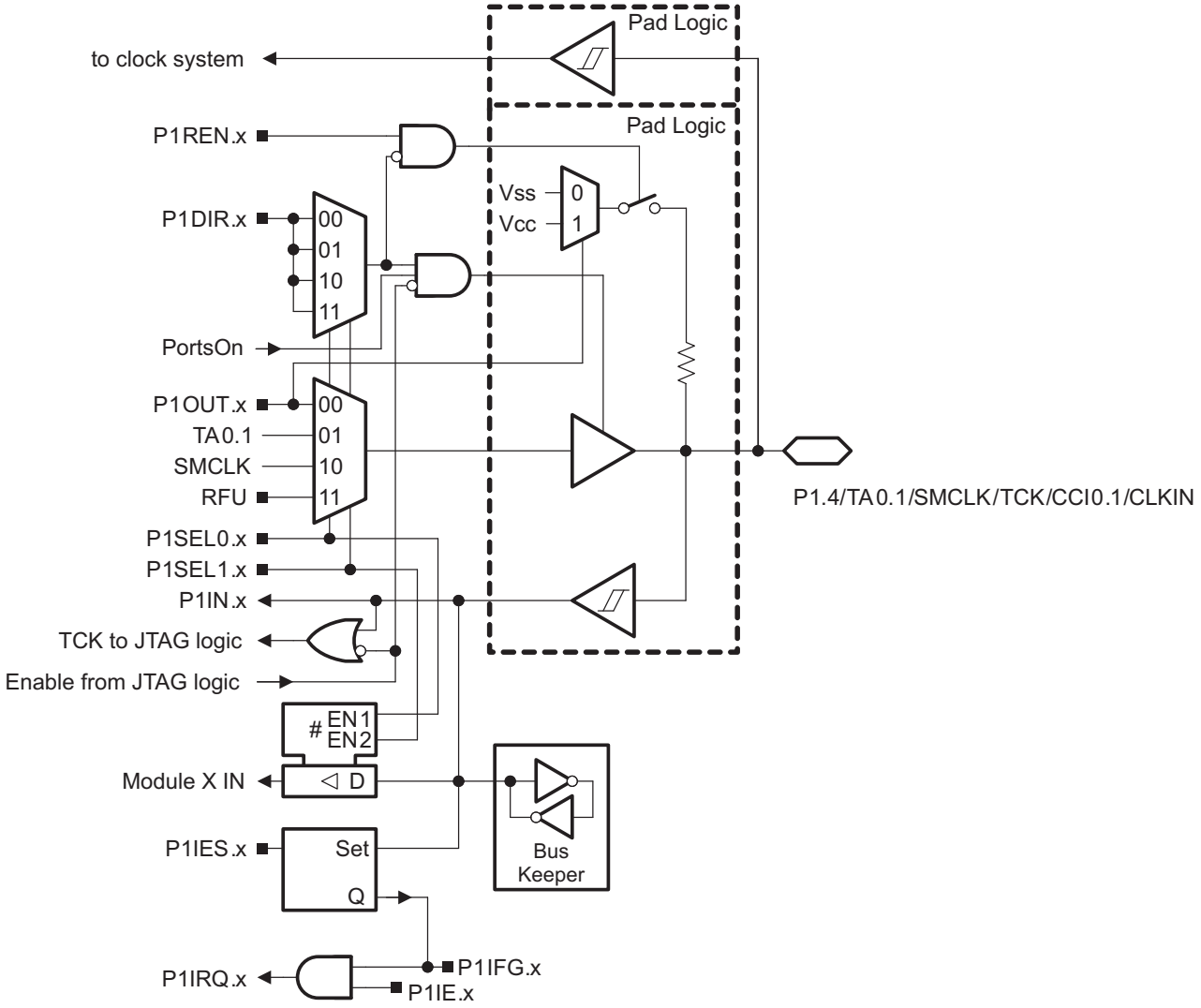


表 6-12. Port P1.4 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	JTAG Mode
TCK/P1.4/TA0.1/SMCLK/CCI0.1	4	P1.4 (I/O)	I:0; O:1	0	0	0
		Timer_A0.1	1	0	1	0
		SMCLK	1	1	0	0
		Reserved	1	1	1	0
		Timer_A0.CCI1A	0	≠0	≠0	0
		JTAG-TCK(2)(3)(4)	X	X	X	1
		CLKIN from bypass	X	X	X	0

(1) X = Don't care
(2) JTAG signals TMS, TCK, and TDI read as 1 when not configured as explicit JTAG terminals.
(3) JTAG overrides digital output control when configured as explicit JTAG terminals.
(4) JTAG function with enabled pullup resistors is default after power up.

6.7.6 Port P1.5 Input/Output

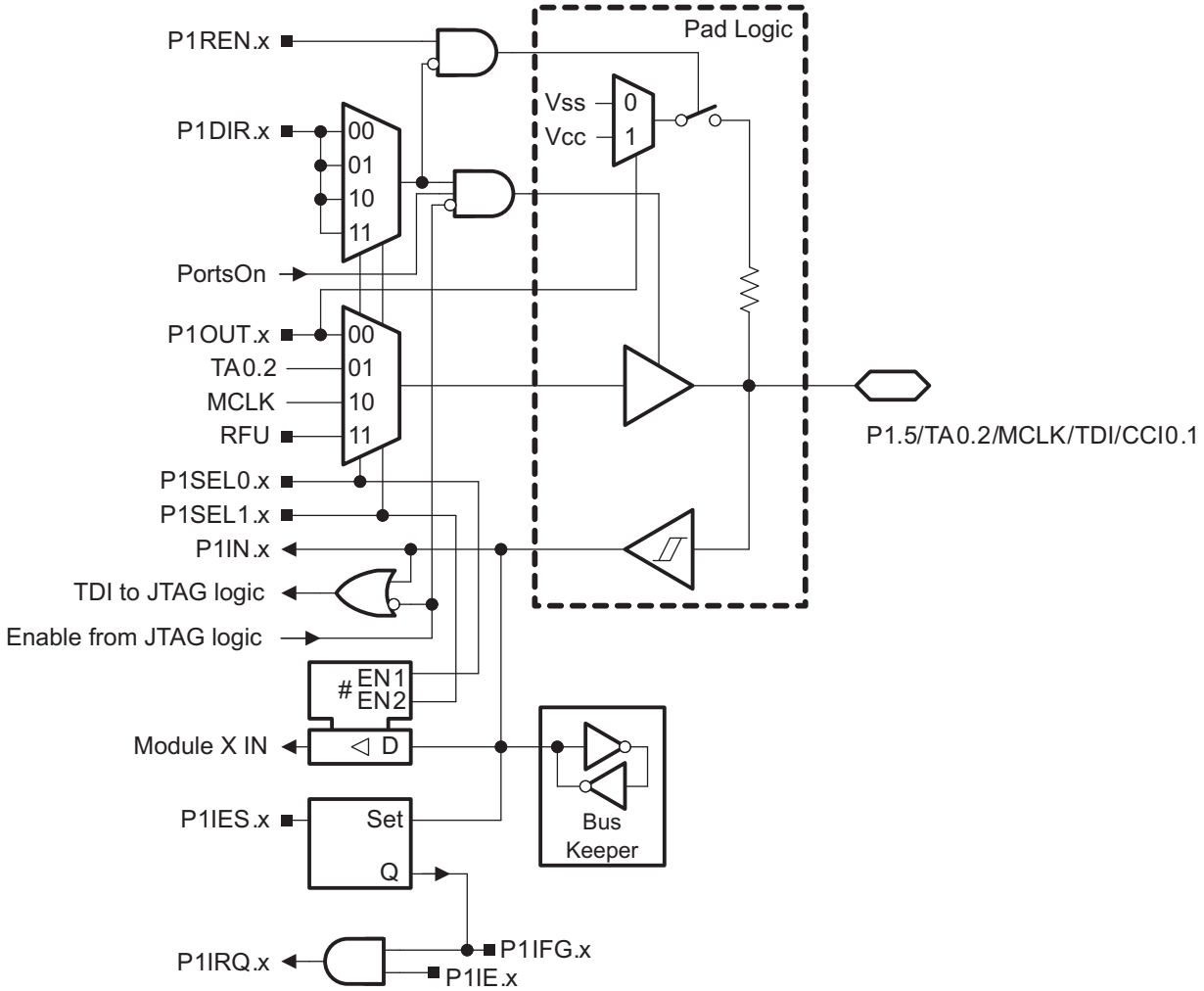


表 6-13. Port P1.5 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	JTAG Mode
TDI/P1.5/TA0.2/MCLK/CCI0.1	5	P1.5 (I/O)	I:0; O:1	0	0	0
		Timer_A0.2	1	0	1	0
		MCLK	1	1	0	0
			1	1	1	0
		Timer_A0 CCI1B	0	≠0	≠0	0
		JTAG-TDI(2)(3)(4)	X	X	X	1

(1) X = Don't care
(2) JTAG signals TMS, TCK, and TDI read as 1 when not configured as explicit JTAG terminals.
(3) JTAG overrides digital output control when configured as explicit JTAG terminals.
(4) JTAG function with enabled pullup resistors is default after power up.

6.7.7 Port P1.6 Input/Output

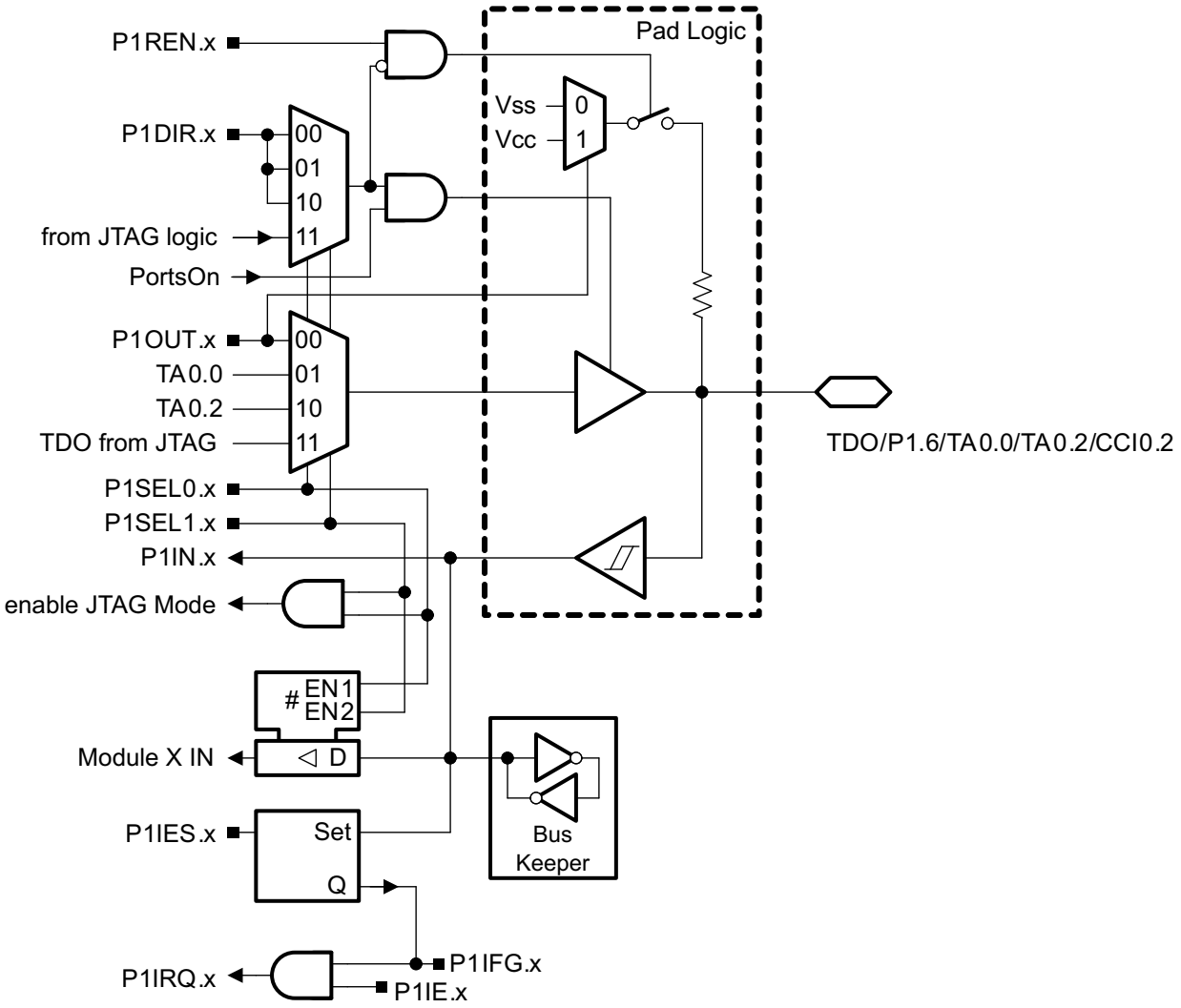


表 6-14. Port P1.6 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P1DIR.x	P1SEL1.x	P1SEL0.x
TDO/P1.6/TA0.0/TA0.2/CCI0.2	6	P1.6 (I/O)	I:0; O:1	0	0
		Timer_A0.0	1	0	1
		Timer_A0.2	1	1	0
		JTAG-TDO(1)(2)	1	1	1
		Timer_A0 CCI2A	0	≠0	≠0

(1) JTAG signals TMS, TCK, and TDI read as 1 when not configured as explicit JTAG terminals.
(2) JTAG overrides digital output control when configured as explicit JTAG terminals.

6.7.8 Port P1.7 Input/Output

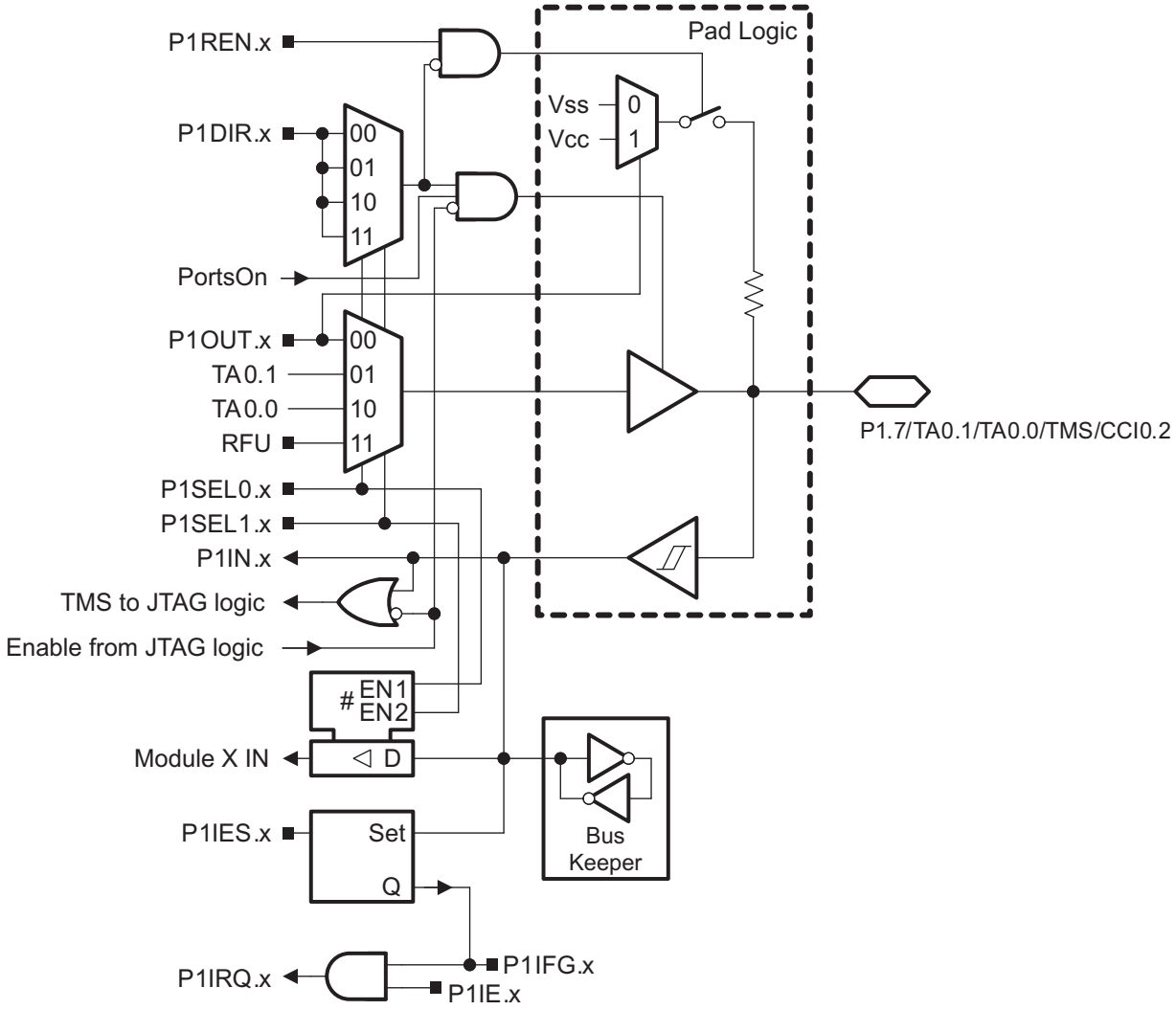


表 6-15. Port P1.7 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	JTAG Mode
TMS/P1.7/TA0.1/TA0.0/CCI0.2	7	P1.7 (I/O)	I:0; O:1	0	0	0
		Timer_A0.1	1	0	1	0
		Timer_A0.0	1	1	0	0
		Reserved	1	1	1	0
		Timer_A0.CCI2B	0	≠0	≠0	0
		JTAG-TMS(2)(3)(4)	X	X	X	1

(1) X = Don't care
(2) JTAG signals TMS, TCK, and TDI read as 1 when not configured as explicit JTAG terminals.
(3) JTAG overrides digital output control when configured as explicit JTAG terminals.
(4) JTAG function with enabled pullup resistors is default after power up.

6.8 Device Descriptors (TLV)

表 6-16 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

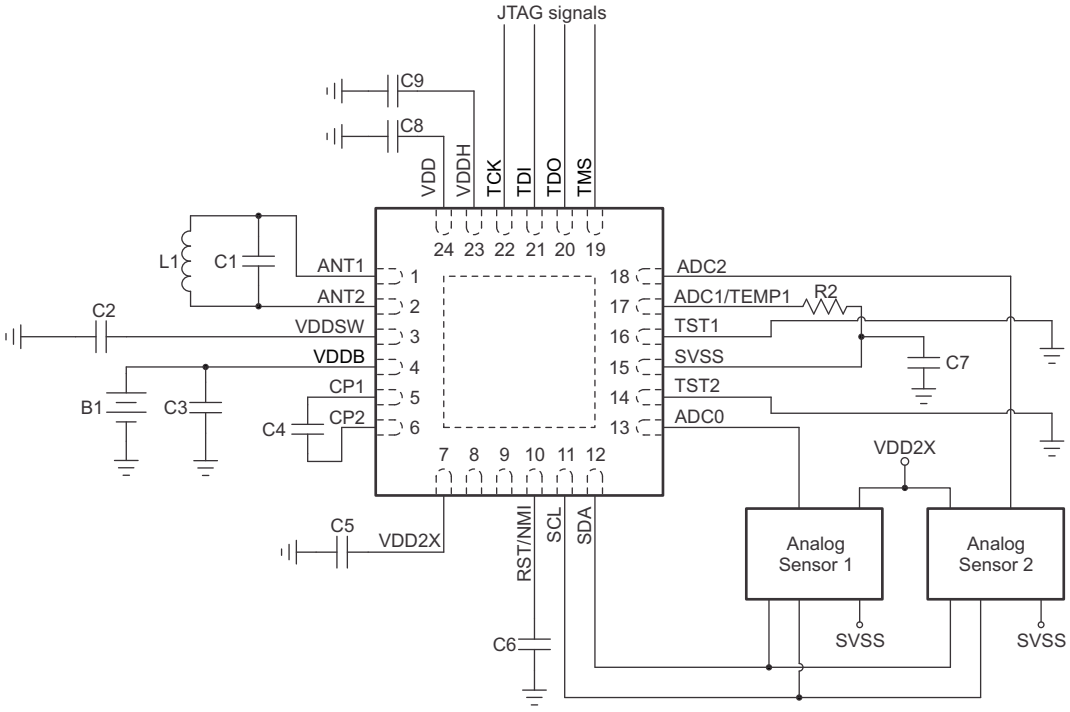
表 6-16. RF430FRL15xH Boot Data and Device Descriptor Table

	Description	Address	Size bytes	FRL152H	FRL153H	FRL154H
Info Block	Boot Data Length	01A00h	1	03h	03h	03h
	CRC length	01A01h	1	03h	03h	03h
	Boot Data CRC value	01A02h	2	per unit	per unit	per unit
	Device ID	01A04h	1	E7h	FBh	FCh
	Device ID	01A05h	1	81h	81h	81h
Die Record	Lot #0	01A06h	1	per unit	per unit	per unit
	Lot #1	01A07h	1	per unit	per unit	per unit
	UID0	01A08h	1	per unit	per unit	per unit
	UID1	01A09h	1	per unit	per unit	per unit
	UID2	01A0Ah	1	per unit	per unit	per unit
	UID3	01A0Bh	1	per unit	per unit	per unit
	UID4	01A0Ch	1	per unit	per unit	per unit
	UID5	01A0Dh	1	A2h / A3h	A2h / A3h	A2h / A3h
	Lot #2	01A0Eh	1	per unit	per unit	per unit
	Fab ID / Wafer Number	01A0Fh	1	per unit	per unit	per unit
	Reserved	01A10h	2	0FFFFh	0FFFFh	0FFFFh
	Reserved	01A12h	2	0FFFFh	0FFFFh	0FFFFh
Calibration	Calibration Pointer	01A14h	2	01A14h	01A14h	01A14h
	Reserved	01A16h	2	per unit	per unit	per unit
	Reserved	01A18h	2	per unit	per unit	per unit
	Reserved	01A1Ah	2	per unit	per unit	per unit
	Reserved	01A1Ch	2	per unit	per unit	per unit
	Reserved	01A1Eh	2	per unit	per unit	per unit
ECC	ECC of previous data	01A3E - 01A20h	32	per unit	per unit	per unit

表 6-17. UID (Unique Identifier) Definition

Description	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Lot ID 0	0x1A06	LotNr[7]	LotNr[6]	LotNr[5]	LotNr[4]	LotNr[3]	LotNr[2]	LotNr[1]	LotNr[0]
Lot ID 1	0x1A07	LotNr[15]	LotNr[14]	LotNr[13]	LotNr[12]	LotNr[11]	LotNr[10]	LotNr[9]	LotNr[8]
UID0	0x1A08	TI[7]	TI[6]	TI[5]	TI[4]	TI[3]	TI[2]	TI[1]	TI[0]
UID1	0x1A09	TI[15]	TI[14]	TI[13]	TI[12]	TI[11]	TI[10]	TI[9]	TI[8]
UID2	0x1A0A	TI[23]	TI[22]	TI[21]	TI[20]	TI[19]	TI[18]	TI[17]	TI[16]
UID3	0x1A0B	TI[31]	TI[30]	TI[29]	TI[28]	TI[27]	TI[26]	TI[25]	TI[24]
UID4	0x1A0C	TI[39]	TI[38]	TI[37]	TI[36]	TI[35]	TI[34]	TI[33]	TI[32]
UID5	0x1A0D	1	0	1	0	0	0	1	TI[40]
Lot ID 2	0x1A0E	LotNr[23]	LotNr[22]	LotNr[21]	LotNr[20]	LotNr[19]	LotNr[18]	LotNr[17]	LotNr[16]
FabID	0x1A0F	Wafer[4]	Wafer[3]	Wafer[2]	Wafer[1]	Wafer[0]	FabNr[2]	FabNr[1]	FabNr[0]

7 Applications, Implementation, and Layout



Two analog sensors connected through I^2C, supplied by VDD2X (≈3 V)

图 7-1. Application Circuit

表 7-1 lists the bill of materials for this application.

表 7-1. Bill of Materials

Name	Value	Description
L1	3 µH	RF inductance (nominal)
C1	8.2 pF	RF tuning capacitor (nominal)
C2	2.2 µF	Decoupling cap at VDDSW
C3	100 nF	Decoupling cap at VDDB
C4	10 nF	Charge pump capacitor
C5	100 nF	Decoupling cap at VDD2X
C6	10 nF	Decoupling cap at RST
C7	1µF	Bypass capacitor between SVSS and V_{SS}
C8	100 nF	Decoupling cap at VDD
C9	100 nF	Decoupling cap at VDDH
B1	1.5 V	Battery
R2	100 kΩ	Reference resistor

8 器件和文档支持

8.1 器件支持

8.1.1 开发支持

TI 提供了大量的开发工具，其中包括评估处理器性能、生成代码、开发算法实现、以及完全集成和调试软件及硬件模块的工具。 工具支持文档以电子文档形式提供，包含在 Code Composer Studio™ 集成开发环境(IDE)中。

有关 NFC 应答器的开发工具和驱动程序的概述，请访问 NFC/RFID 工具和软件页面。

8.1.2 器件和开发工具命名规则

为了指明产品开发周期所处的阶段，TI 为所有 RF430 MCU 器件和支持工具的产品型号分配了前缀。 每个商业系列成员都具有以下三个前缀中的一个：RF、P 或 X（例如，RF430FRL152H）。 德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：RF 和 X。这些前缀代表了产品开发的发展阶段：即从工程原型设计（X 表示器件和工具）直到完全合格的生产器件和工具（RF 表示器件和工具）。

器件开发进化流程：

X - 试验器件不一定代表最终器件的电气技术规格

P - 最终的芯片模型符合器件的电气技术规格，但是未经完整的质量和可靠性验证

RF - 完全合格的生产器件

支持工具开发发展流程：

X - 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。

RF – 完全合格的开发支持产品

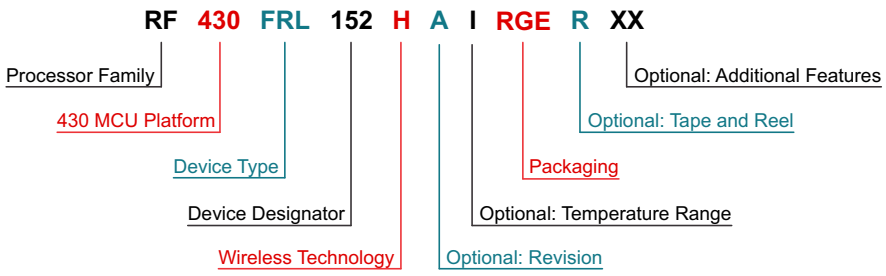
X 和 P 器件和 X 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

RF 器件和 RF 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。 TI 的标准保修证书适用。

预测显示原型器件（X 和 P）的故障率大于标准生产器件。 由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。 只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。 这个后缀包括封装类型（例如，RGE）和温度范围（例如，T）。图 8-1 提供了解读任一系列产品成员完整器件名称的图例。



Processor Family	RF = Embedded RF Radio X = Experimental Silicon P = Prototype Device
430 MCU Platform	TI's Low Power Microcontroller Platform
Device Type	FR = FRAM Memory L = Low-Power Series
Device Designator	Various Levels of Integration Within a Series
Wireless Technology	HF = High Frequency
Optional: Revision	A = Device Revision
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C
Packaging	www.ti.com/packaging
Optional: Tape and Reel	T = Small Reel (7 inch) R = Large Reel (11 inch) No Markings = Tube or Tray
Optional: Additional Features	-EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C)

图 **8-1.** 器件命名规则

8.2 文档支持

下列文档描述了 RF430FRL15xH 器件。

SLAU506 *RF430FRL15xH 系列技术参考手册。* 详细介绍了这款器件系列提供的所有模块和外设。

SLAU603 *RF430FRL15xH 固件用户指南。* 详细介绍了为这些器件提供的固件。

8.3 相关链接

表 8-1 列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **8-1.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
RF430FRL152H	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
RF430FRL153H	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
RF430FRL154H	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.5 商标

MSP430, Code Composer Studio, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

9 机械封装和可订购信息

9.1 封装信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RF430FRL152HCRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	RF430 FRL152H	Samples
RF430FRL153HCRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	RF430 FRL153H	Samples
RF430FRL154HCRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	RF430 FRL154H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

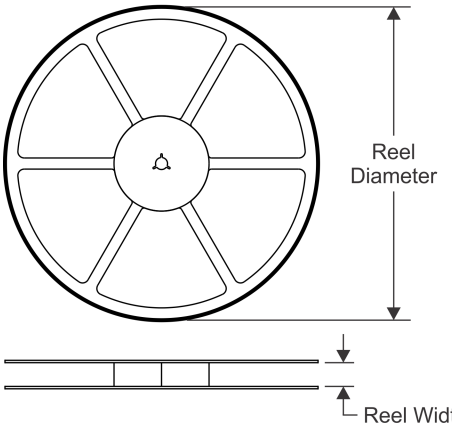
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

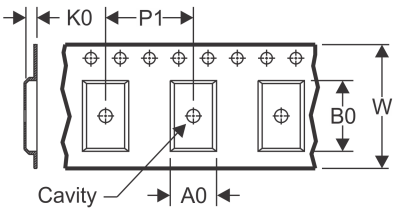
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

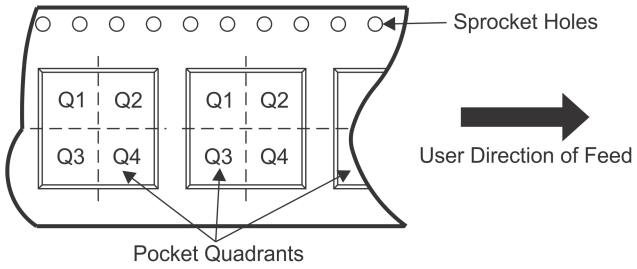


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

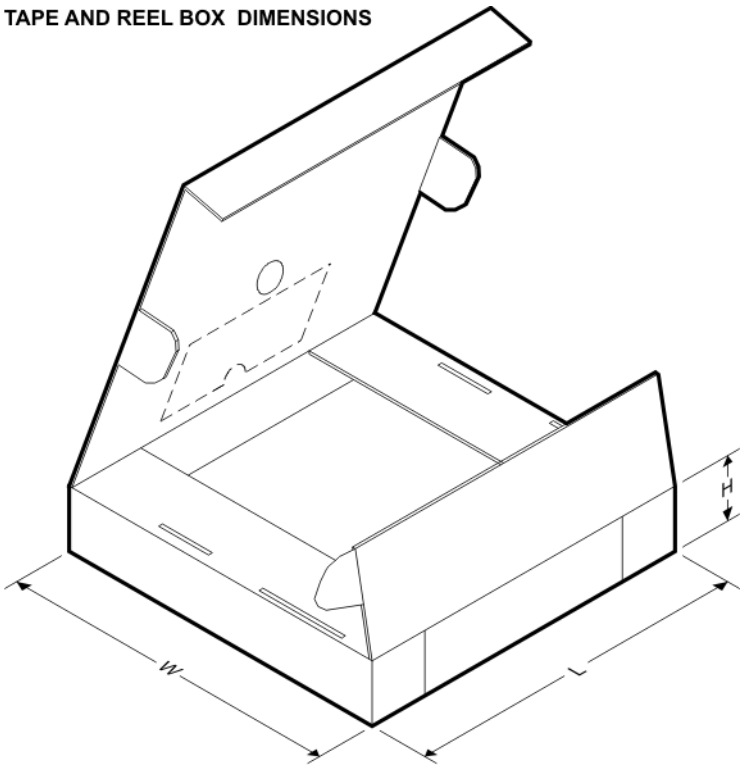
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RF430FRL152HCRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
RF430FRL153HCRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
RF430FRL154HCRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



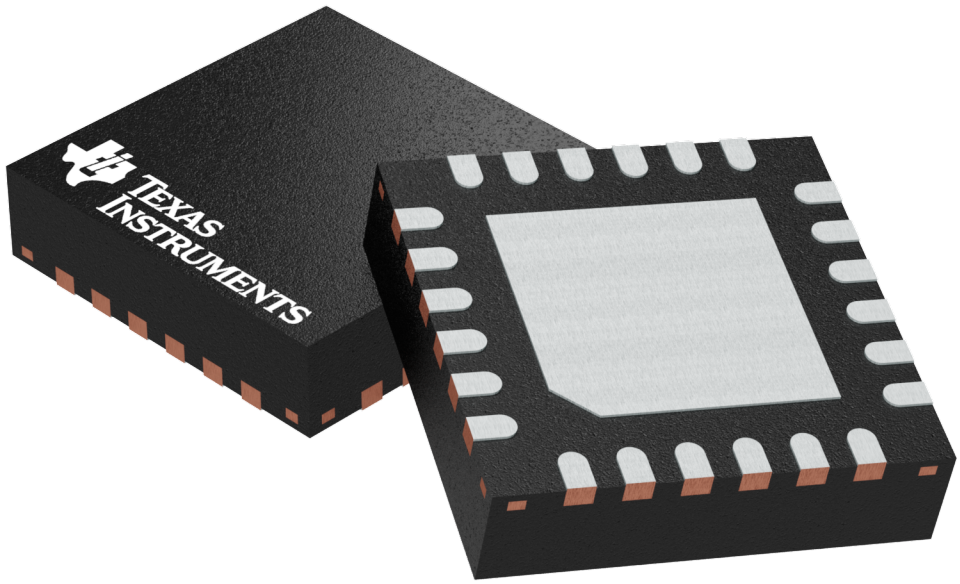
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RF430FRL152HCRGER	VQFN	RGE	24	3000	338.1	338.1	20.6
RF430FRL153HCRGER	VQFN	RGE	24	3000	338.1	338.1	20.6
RF430FRL154HCRGER	VQFN	RGE	24	3000	338.1	338.1	20.6

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

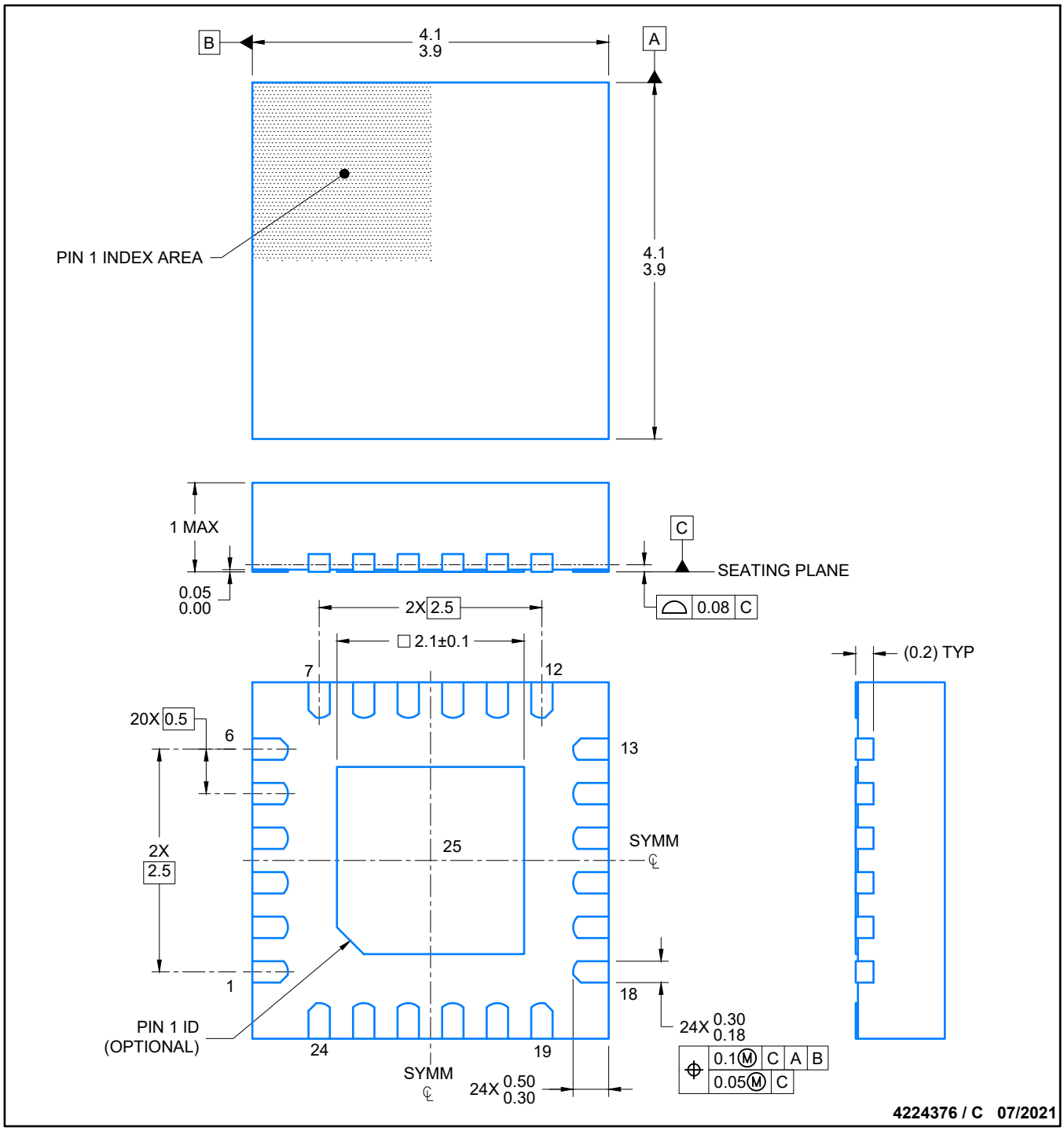
4204104/H

PACKAGE OUTLINE

RGE0024C

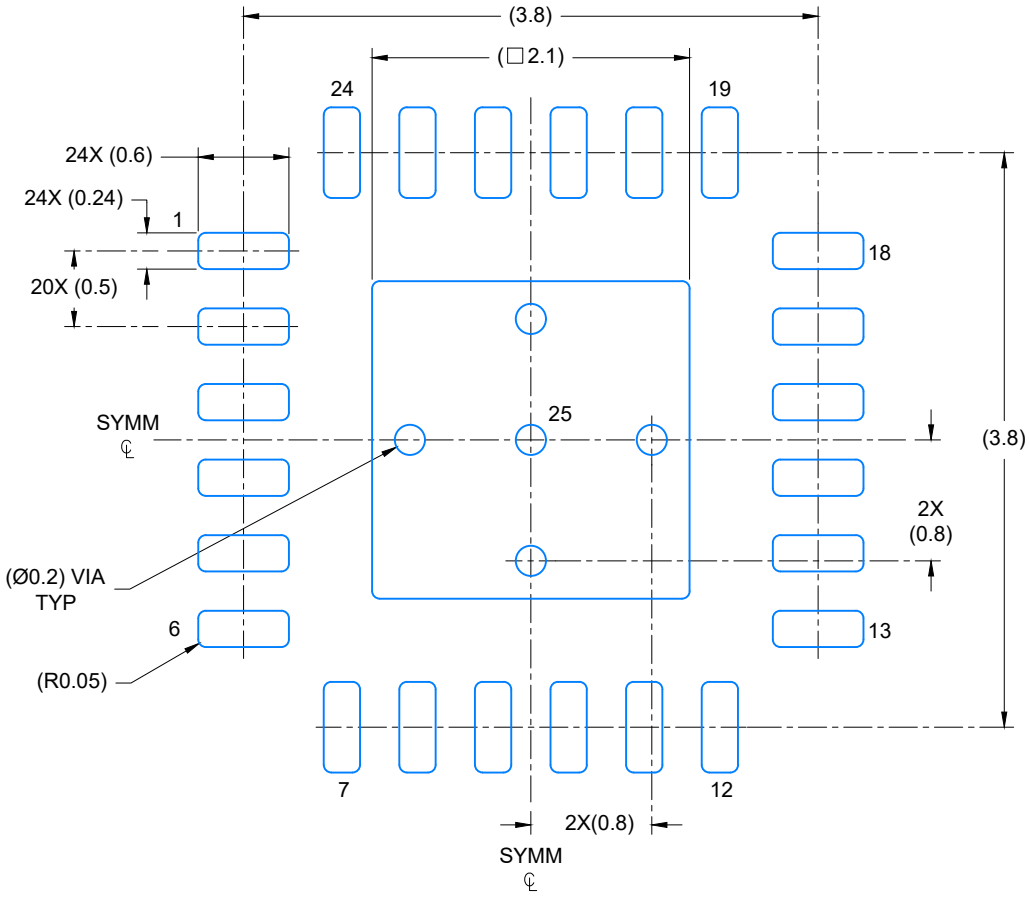
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



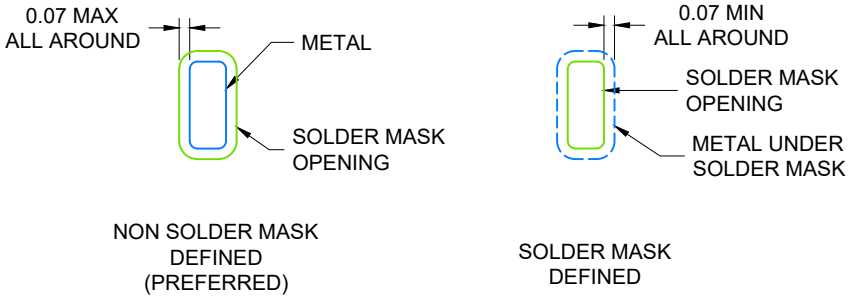
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

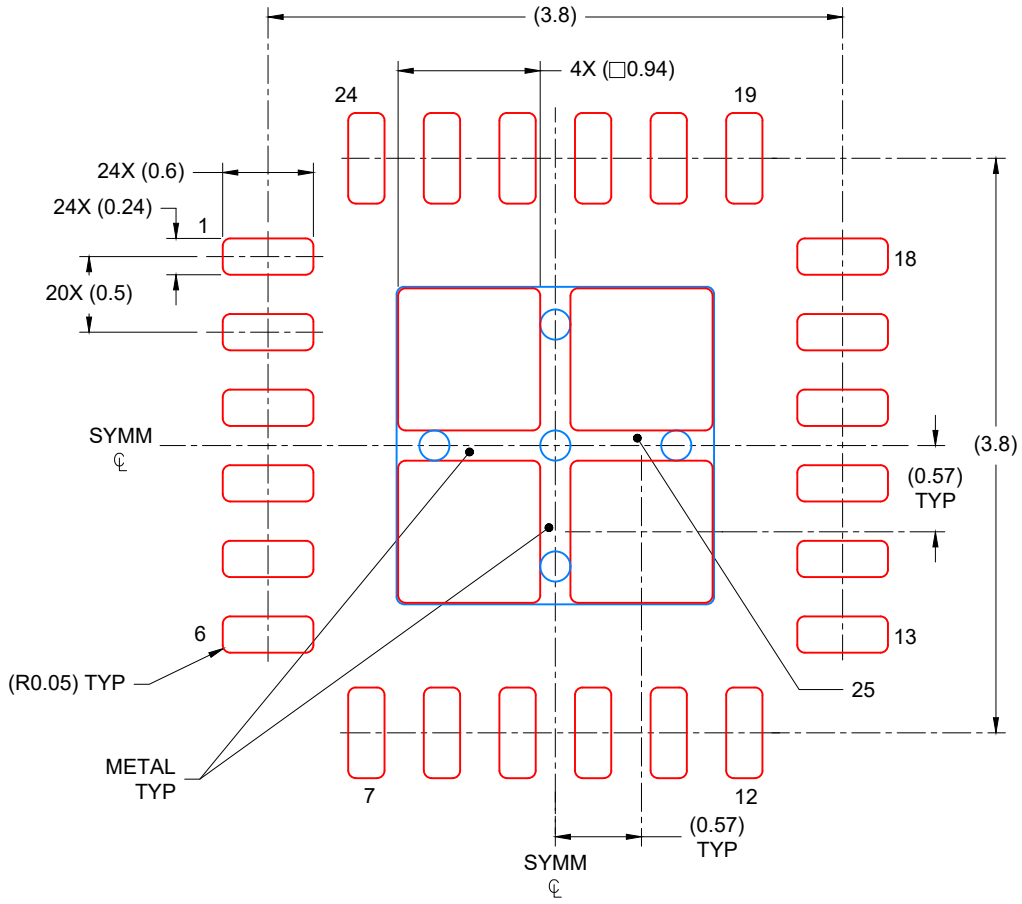


SOLDER MASK DETAILS

4224376 / C 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

4224376 / C 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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