OPAx377-Q1 低噪声、低静态电流、汽车级精密运算放大器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 3A
  - 器件组件充电模式 (CDM) ESD 分类等级 C6
- 低噪声：1kHz 时为 7.5nV/$\sqrt{Hz}$
- 0.1Hz 至 10Hz 噪声：0.8 μV_{PP}
- 静态电流：760μA（典型值）
- 低偏移电压：250μV（典型值）
- 增益带宽积：5.5MHz
- 轨到轨输入和输出
- 单电源供电
- 电源电压：2.2V 至 5.5V
- 小型封装：
  - 小外形尺寸晶体管 (SOT)-23、超薄小外形尺寸 (VSSOP) 和薄型小外形尺寸 (TSSOP)

2 应用

- 主动巡航控制
- 停车辅助
- 轮胎气压监视
- 信息娱乐系统
- 有源滤波
- 传感器信号调节

3 说明

OPAx377-Q1 系列运算放大器属于高带宽 CMOS 放大器，同时拥有超低噪声、低输入偏置电流和低偏移电压特性，静态工作电流低至 0.76mA（典型值）。

OPAx377-Q1 运放针对低电压、单电源应用进行了 优化。其交流和直流性能都非常出色，非常适合 诸如小信号调节、音频和有源滤波器等各类应用。此外，该系列器件还具有较宽的电源范围及优异的电源抑制比 (PSRR)，因此对于不经过稳压而直接由电池供电运行的 应用 而言极具吸引力。

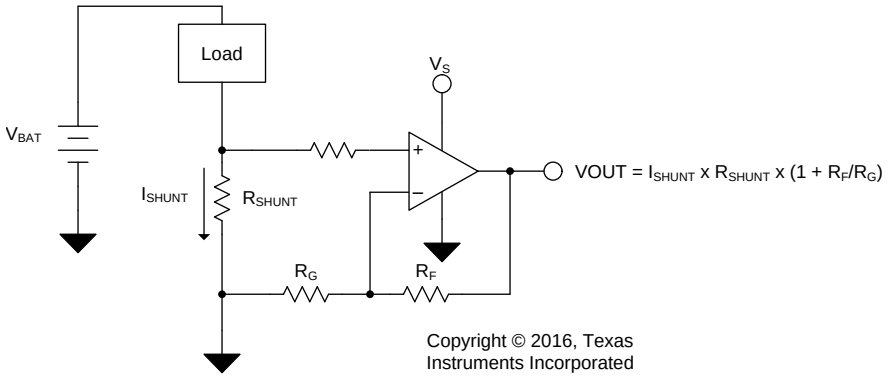
OPA377-Q1 采用 SOT23-5 封装。OPA2377-Q1（双通道版本）采用微型小外形尺寸 (MSOP)-8 封装，OPA4377-Q1（四通道版本）采用 TSSOP-14 封装。所有器件版本的额定工作温度范围均为 -40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA377-Q1	SOT-23 (5)	2.90mm x 1.60mm
OPA2377-Q1	VSSOP (8)	3.00mm × 3.00mm
OPA4377-Q1	TSSOP (14)	5.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

低侧电流感测放大器



目录

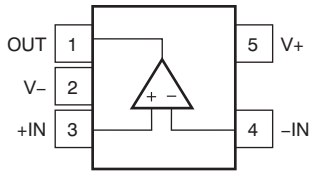
4 修订历史记录

Changes from Original (May 2016) to Revision A **Page**

- 已将器件状态由“*产品预览*”更改为“*量产数据*” ... 1

5 Pin Configuration and Functions

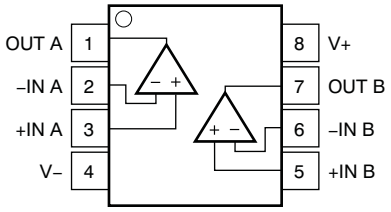
OPA377-Q1: DBV Package
5-Pin SOT23
Top View



Pin Functions: OPA377-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	DBV		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
NC	—	—	No internal connection (can be left floating)
OUT	1	O	Output
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

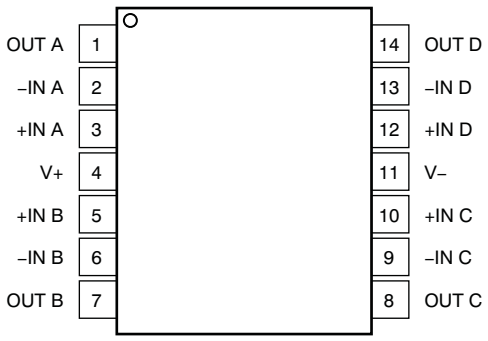
OPA2377-Q1: DGK Package
8-Pin VSSOP and SOIC
Top View



Pin Functions: OPA2377-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	DGK		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

OPA4377-Q1: PW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4377-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	PW		
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S = (V+) – (V–)	Supply voltage		7	V
	Signal input terminal voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Signal input terminal current(2)	–10	10	mA
	Output short-circuit current(3)		Continuous	
T_A	Operating temperature	–40	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Supply voltage	2.2	5.5	V
T_A	Operating temperature	–40	150	°C

6.4 Thermal Information: OPA377-Q1

THERMAL METRIC(1)		OPA377-Q1 DBV (SOT23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	273.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	126.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2377-Q1

THERMAL METRIC(1)		OPA2377-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Thermal Information: OPA2377-Q1 (continued)

THERMAL METRIC(1)		OPA2377-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

6.6 Thermal Information: OPA4377-Q1

THERMAL METRIC(1)		OPA4377-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics: V_S = 2.2 V to 5.5 V

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		0.25	1	mV
	Input offset voltage versus temperature	At T_A = –40°C to +125°C, V_S = 2.2 V to 5.5 V, V_{CM} < (V+) – 1.3 V		5		µV/V
dV_{OS}/dT	Input offset voltage versus drift	At T_A = –40°C to +125°C		0.32	2	µV/°C
PSRR	Input offset voltage versus power supply	At T_A = 25°C, V_S = 2.2 V to 5.5 V, V_{CM} < (V+) – 1.3 V		5	28	µV/V
	Channel separation, dc (dual, quad)			0.5		µV/V
INPUT BIAS CURRENT						
I_{IB}	Input bias current			±0.2	±10	pA
	Input bias current versus temperature			See *Typical Characteristics*		pA
I_{OS}	Input offset current			±0.2	±10	pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		0.8		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		7.5		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.3 V	70	90		dB
INPUT CAPACITANCE						
	Differential			6.5		pF
	Common-mode			13		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	50 mV < V_O < (V+) – 50 mV, R_L = 10 kΩ	112	134		dB
		100 mV < V_O < (V+) – 100 mV, R_L = 2 kΩ		126		dB
FREQUENCY RESPONSE, V_S = 5.5 V						

Electrical Characteristics: V_S = 2.2 V to 5.5 V (continued)

At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GBW	Gain-bandwidth product			5.5		MHz
SR	Slew rate	G = +1		2		V/µs
t_S	Settling time	At 0.1%, 2-V step, G = +1		1.6		µs
		At 0.01%, 2-V step, G = +1		2		µs
	Overload recovery time	V_{IN} × Gain > V_S		0.33		µs
THD+N	Total harmonic distortion + noise	V_O = 1 V_{RMS}, G = +1, f = 1 kHz, R_L = 10 kΩ		0.00027%		
OUTPUT						
	Voltage output swing from rail	At T_A = 25°C, R_L = 10 kΩ		10	20	mV
		At T_A = –40°C to +125°C, R_L = 10 kΩ			40	mV
I_{SC}	Short-circuit current			+30/–50		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		
R_O	Open-loop output impedance			150		Ω
POWER SUPPLY						
V_S	Specified voltage		2.2		5.5	V
I_Q	Quiescent current (per amplifier)	At T_A = 25°C, I_O = 0, V_S = 5.5 V		0.76	1.05	mA
		At T_A = –40°C to +125°C			1.2	mA
TEMPERATURE						
	Specified temperature		–40		+125	°C

6.8 Typical Characteristics

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

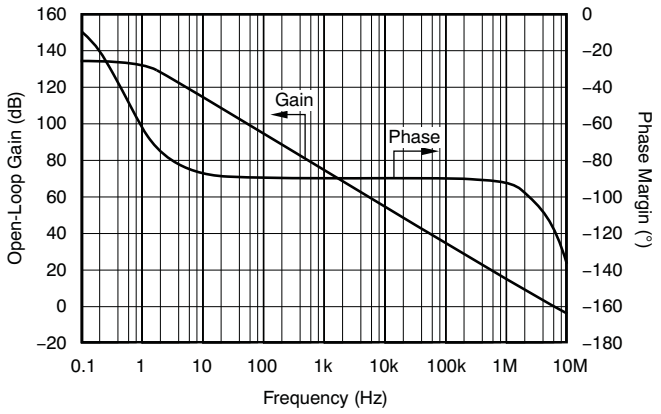


Figure 1. Open-Loop Gain and Phase vs Frequency

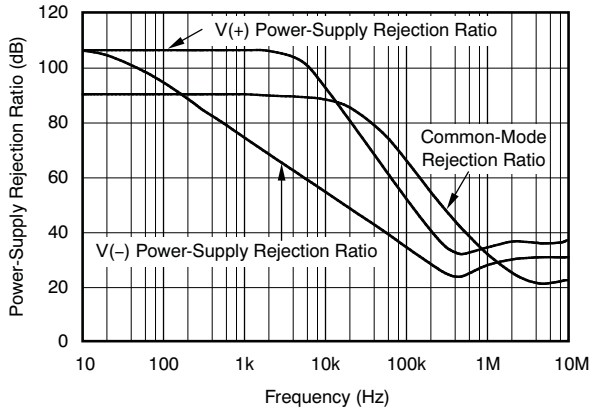


Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

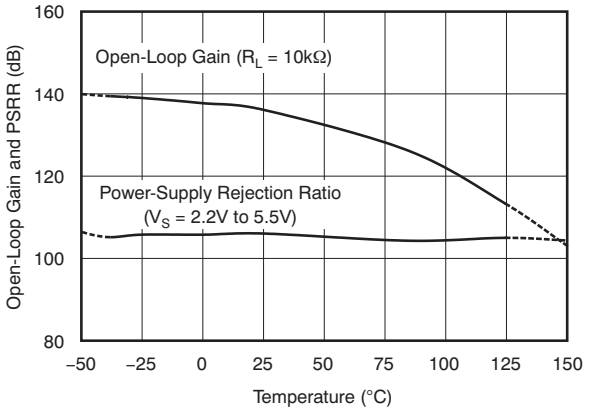


Figure 3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

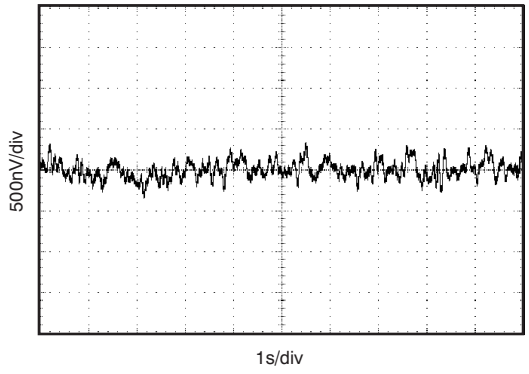


Figure 4. 0.1-Hz to 10-Hz Input Voltage Noise

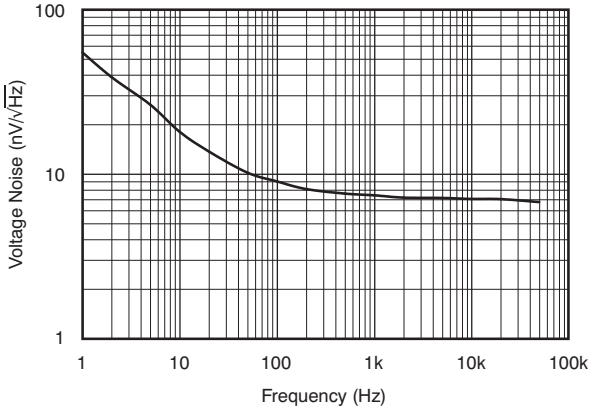


Figure 5. Input Voltage Noise Spectral Density

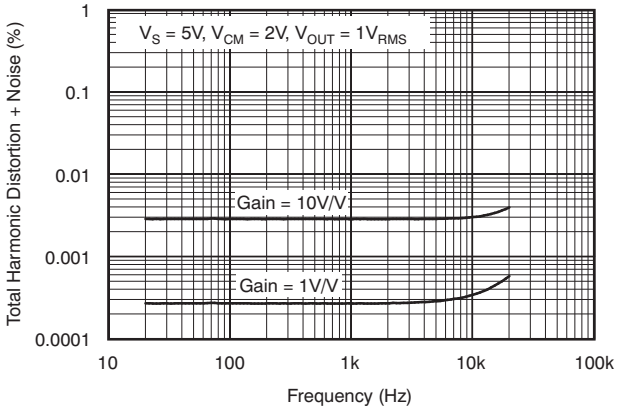


Figure 6. Total Harmonic Distortion and Noise vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

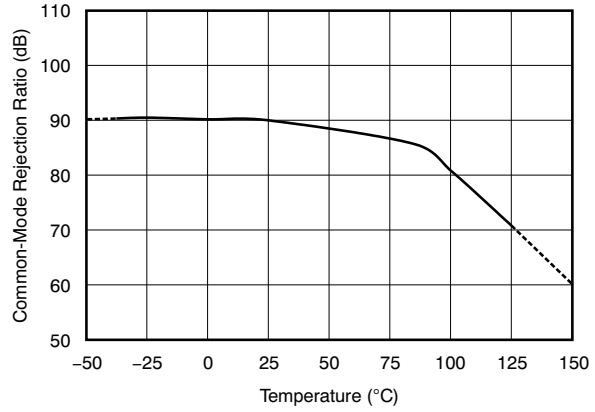


Figure 7. Common-Mode Rejection Ratio vs Temperature

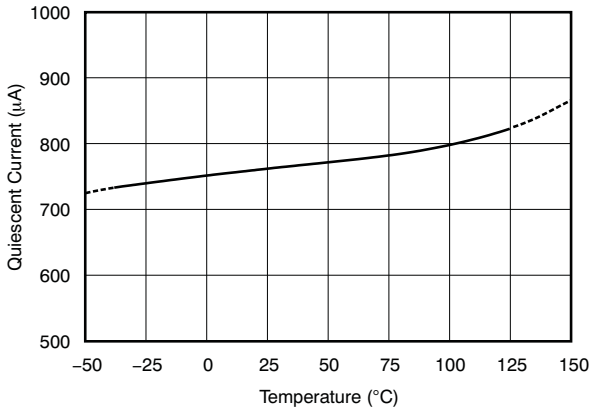


Figure 8. Quiescent Current vs Temperature

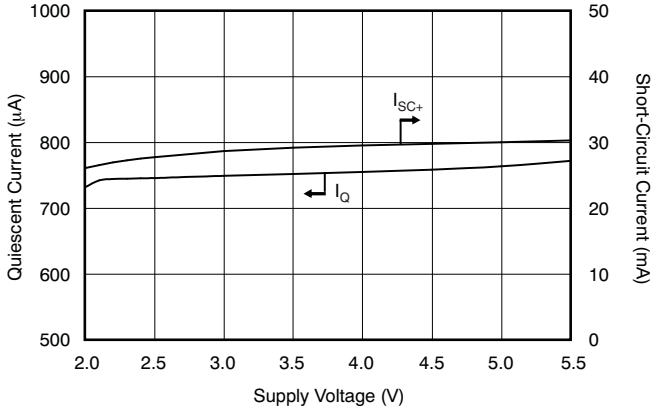


Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage

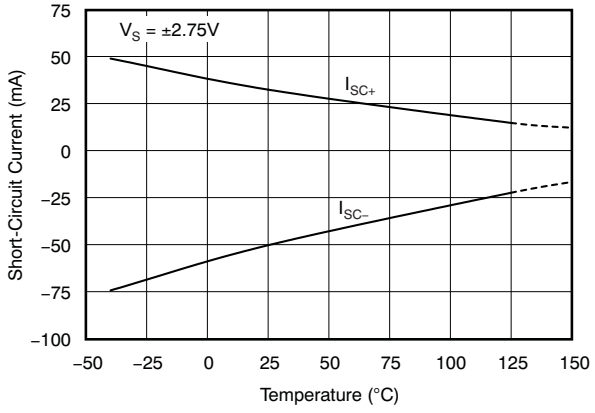


Figure 10. Short-Circuit Current vs Temperature

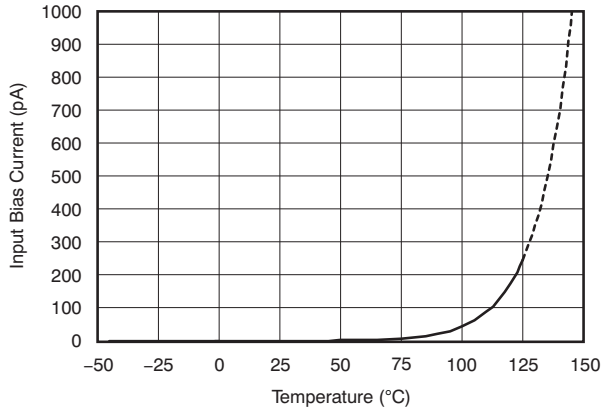


Figure 11. Input Bias Current vs Temperature

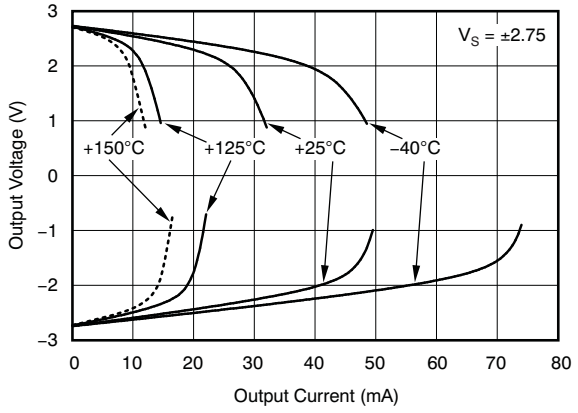


Figure 12. Output Voltage vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

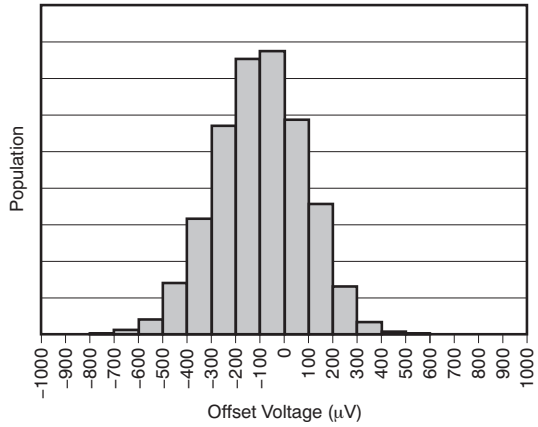


Figure 13. Offset Voltage Production Distribution

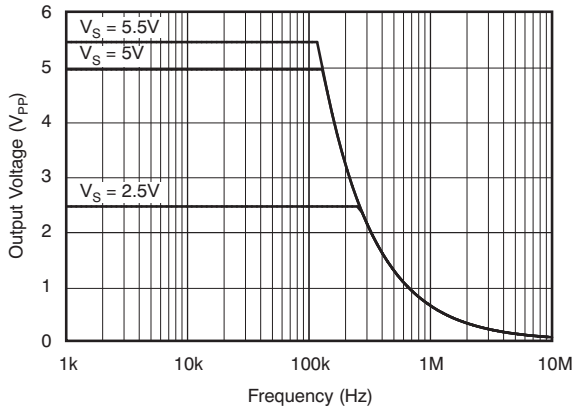


Figure 14. Maximum Output Voltage vs Frequency

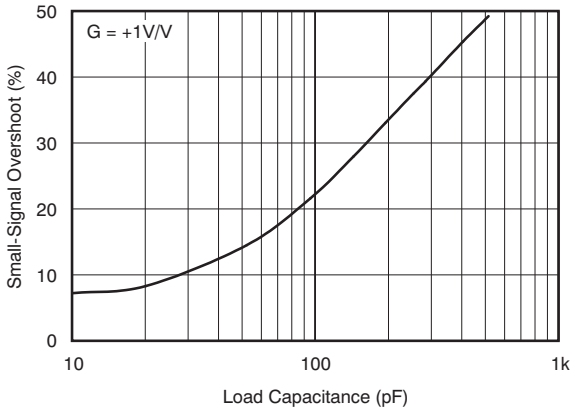


Figure 15. Small-Signal Overshoot vs Load Capacitance

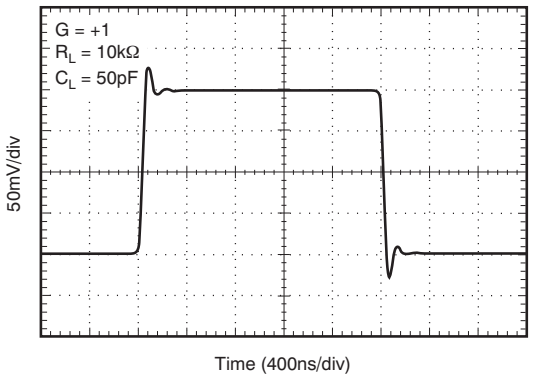


Figure 16. Small-Signal Pulse Response

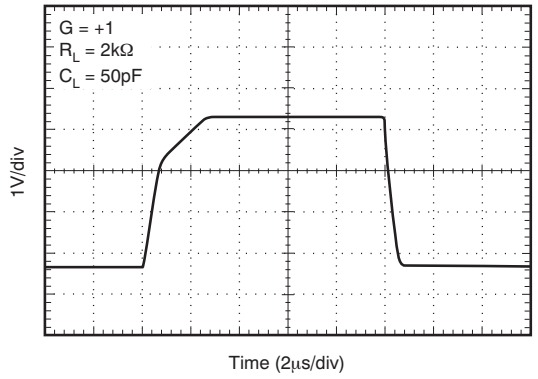


Figure 17. Large-Signal Pulse Response

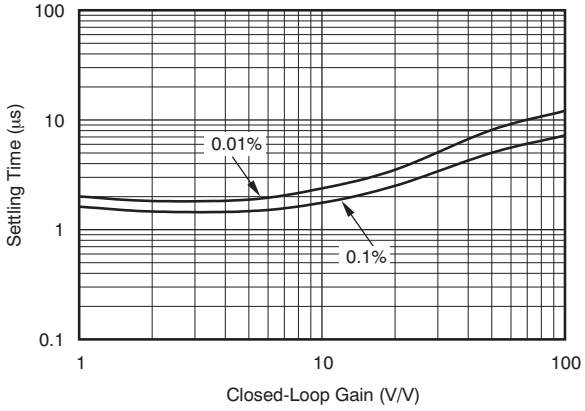


Figure 18. Settling Time vs Closed-Loop Gain

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

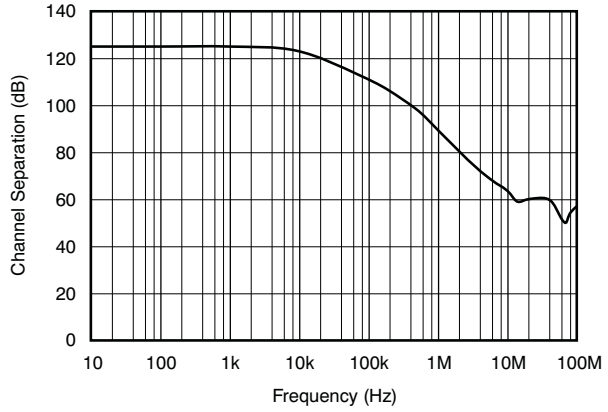


Figure 19. Channel Separation vs Frequency

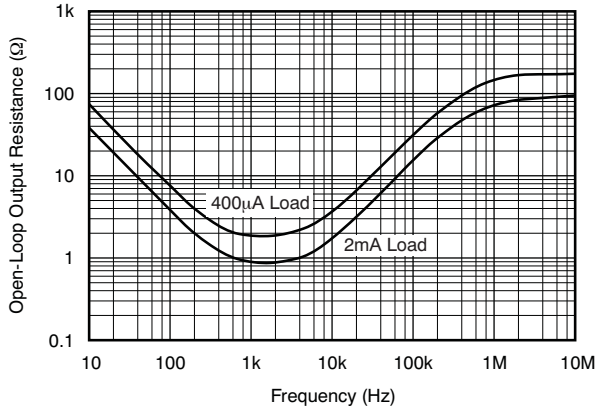


Figure 20. Open-Loop Output Resistance vs Frequency

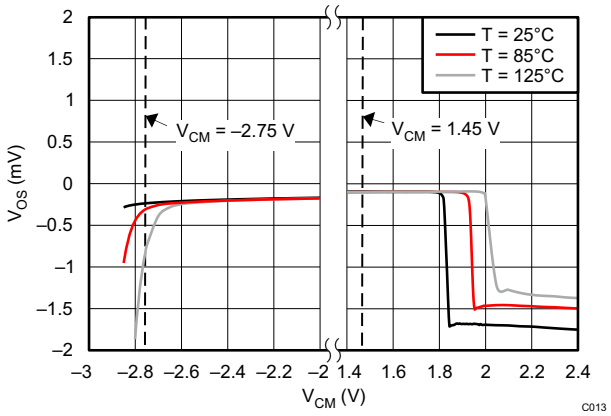


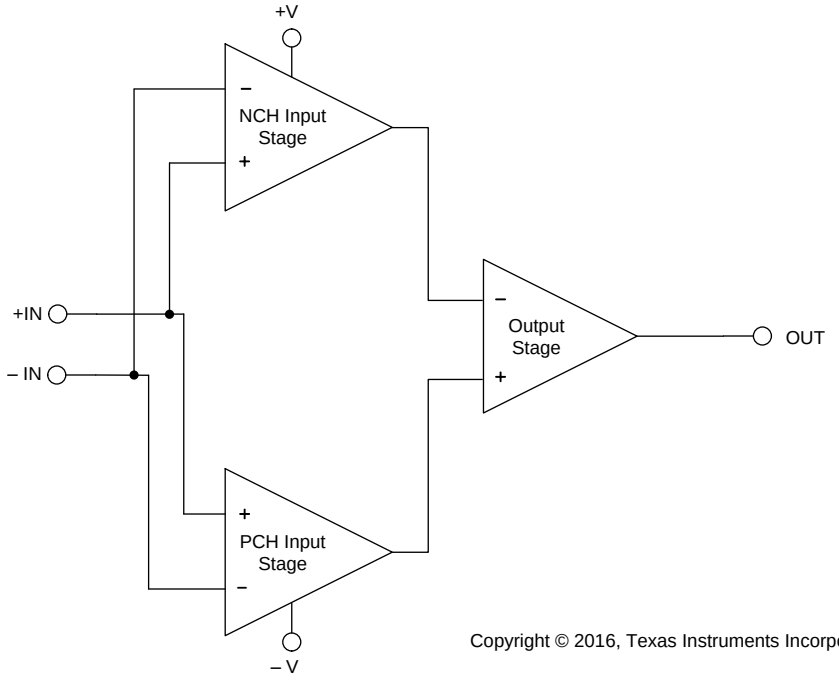
Figure 21. Input Offset Voltage vs Common-Mode Voltage

7 Detailed Description

7.1 Overview

The OPAx377-Q1 family belongs to a new generation of low-noise operational amplifiers, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this device has a wide supply range with excellent PSRR, making it a suitable option for applications that are battery-powered without regulation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx377-Q1 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx377-Q1 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is low, from approximately (V–) to (V+) – 1 V, as shown in Figure 22. The offset voltage increases as common-mode voltage exceeds (V+) – 1 V. Common-mode rejection is specified from (V–) to (V+) – 1.3 V.

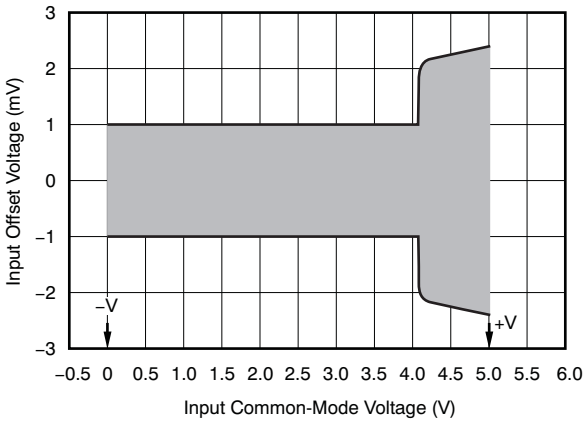


Figure 22. Offset and Common-Mode Voltage

7.3.3 Input and ESD Protection

The OPAx377-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table.

Figure 23 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.

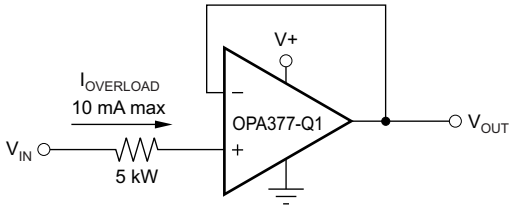


Figure 23. Input Current Protection

Feature Description (continued)

7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from the nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx377-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 75 MHz (–3 dB), with a roll-off of 20 dB per decade.

7.3.5 Capacitive Load and Stability

The OPAx377-Q1 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx377-Q1 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

The OPAx377-Q1 in a unity-gain configuration can directly drive up to 250-pF pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic plot, Figure 15. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 24. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L, and is generally negligible at low output current levels.

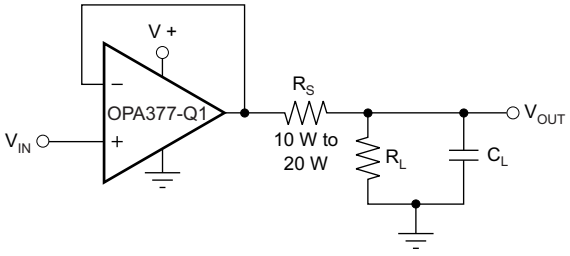


Figure 24. Improving Capacitive Load Drive

7.4 Device Functional Modes

The OPAx377-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the OPAx376-Q1 is 5.5 V (±2.75 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx377-Q1 family of operational amplifiers is built on a precision analog CMOS technology featuring low noise and low offset voltage. The OPAx377-Q1 family delivers excellent offset voltage (250 µV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. These 5.5-MHz CMOS op amps operate on 760 µA (typical) quiescent current.

8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA377-Q1 is ideally suited to construct high-speed, high-precision active filters. Figure 25 shows a second-order, low-pass filter commonly encountered in signal processing applications.

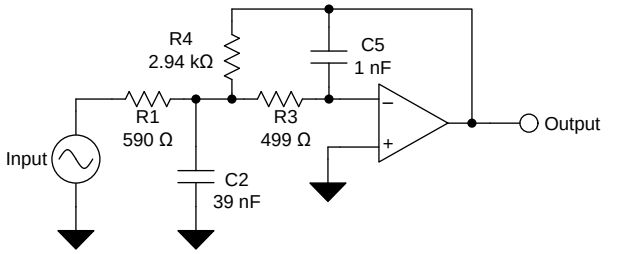


Figure 25. Typical Application Schematic

8.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 25. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Typical Application (continued)

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

8.2.3 Application Curve

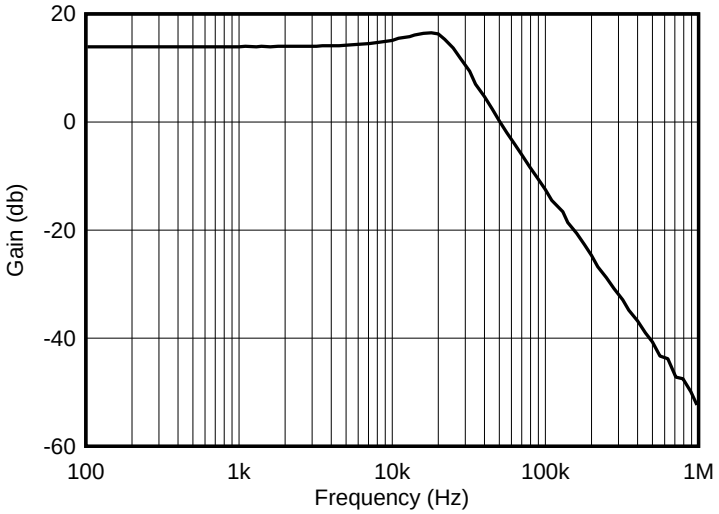


Figure 26. Low-Pass Filter Transfer Function

9 Power Supply Recommendations

The OPAx377-Q1 family of devices is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to the application report, *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 28, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

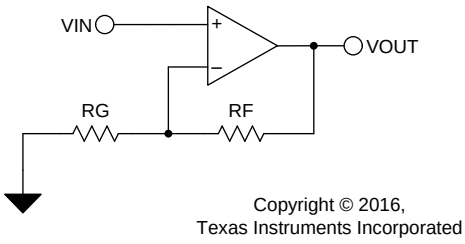


Figure 27. Typical Schematic for PCB Layout Example

Layout Example (continued)

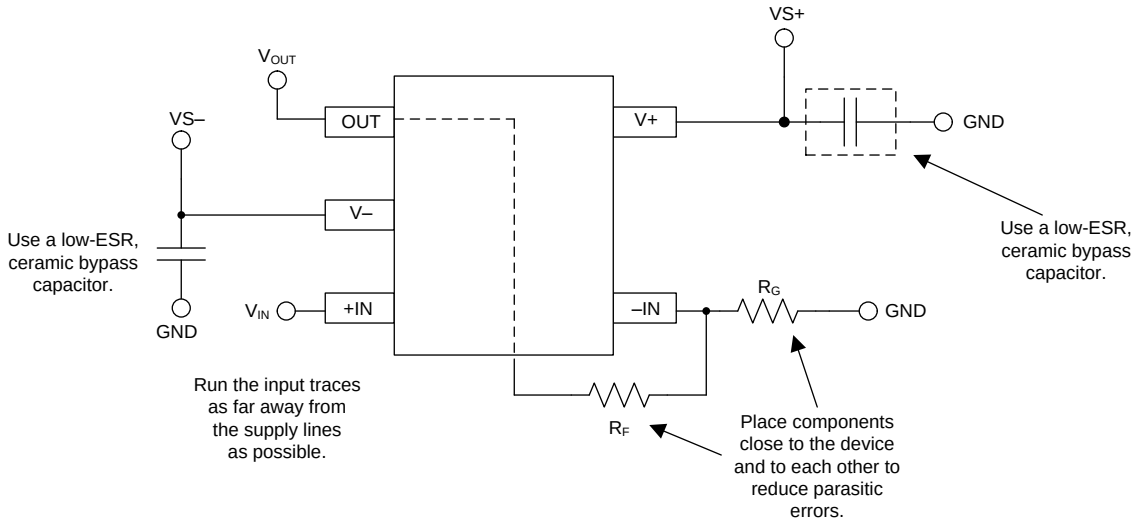


Figure 28. Typical PCB Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

11.1.1.2 DIP 适配器 EVM

DIP 适配器 EVM 工具提供了一种简单而低成本的方式来针对小型表面贴装 IC 进行原型设计。评估工具适用于以下 TI 封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (MSOP-8)、DBV（SOT23-6、SOT23-5 和 SOT23-3）、DCK（SC70-6 和 SC70-5）和 DRL (SOT563-6)。DIP 适配器 EVM 也可搭配引脚排使用或直接与现有电路相连。

11.1.1.3 通用运放 EVM

通用运放 EVM 是一系列通用空白电路板，可简化采用各种 IC 封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、MSOP、TSSOP 和 SOT23 封装。

注

这些电路板均为空白电路板，用户必须自行提供 IC。TI 建议您在订购通用运放 EVM 时申请几个运放器件样品。

11.1.1.4 TI 高精度设计

TI 高精度设计是由 TI 公司的高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整 PCB 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

11.1.1.5 WEBENCH®滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。WEBENCH Filter Designer 通过选择 TI 运算放大器以及 TI 供应商合作伙伴的无源组件来构建优化滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® Filter Designer。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- *《电路板布局布线技巧》*，SLOA089
- *《运算放大器增益稳定性，第 3 部分：交流增益误差分析》*，SLYT383
- *《运算放大器增益稳定性，第 2 部分：直流增益误差分析》*，SLYT374
- *《运算放大器性能分析》*，SBOS054
- *《无铅组件涂层的保存期评估》*，SZZA046
- *《运算放大器的单电源运行》*，SBOA059
- *《调整放大器》*，SBOA067
- *《在全差分有源滤波器中使用无限增益、MFB 滤波器拓扑》*，SLYT343

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2377QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2377	Samples
OPA377QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	377Q	Samples
OPA4377AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4377Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

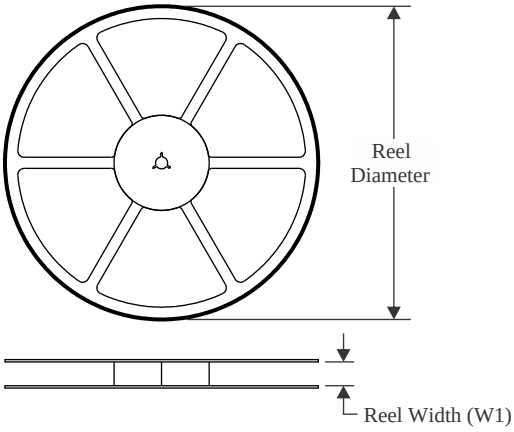
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

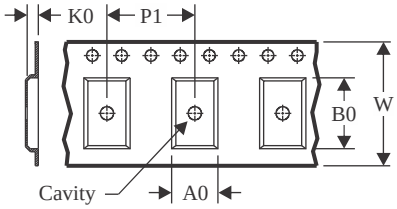
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

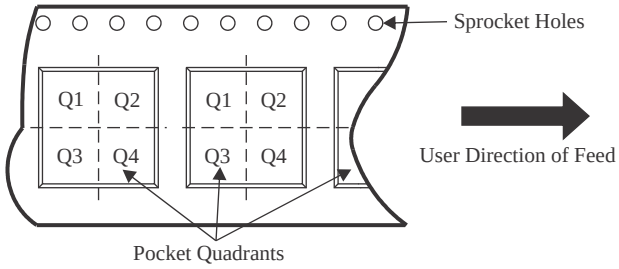


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

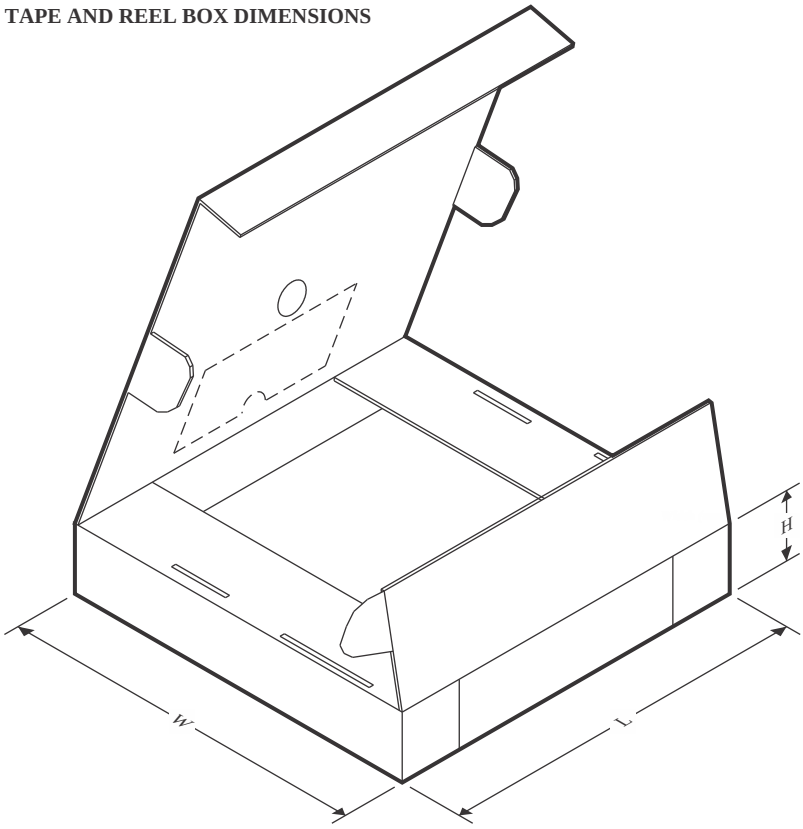
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2377QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA377QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA4377AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

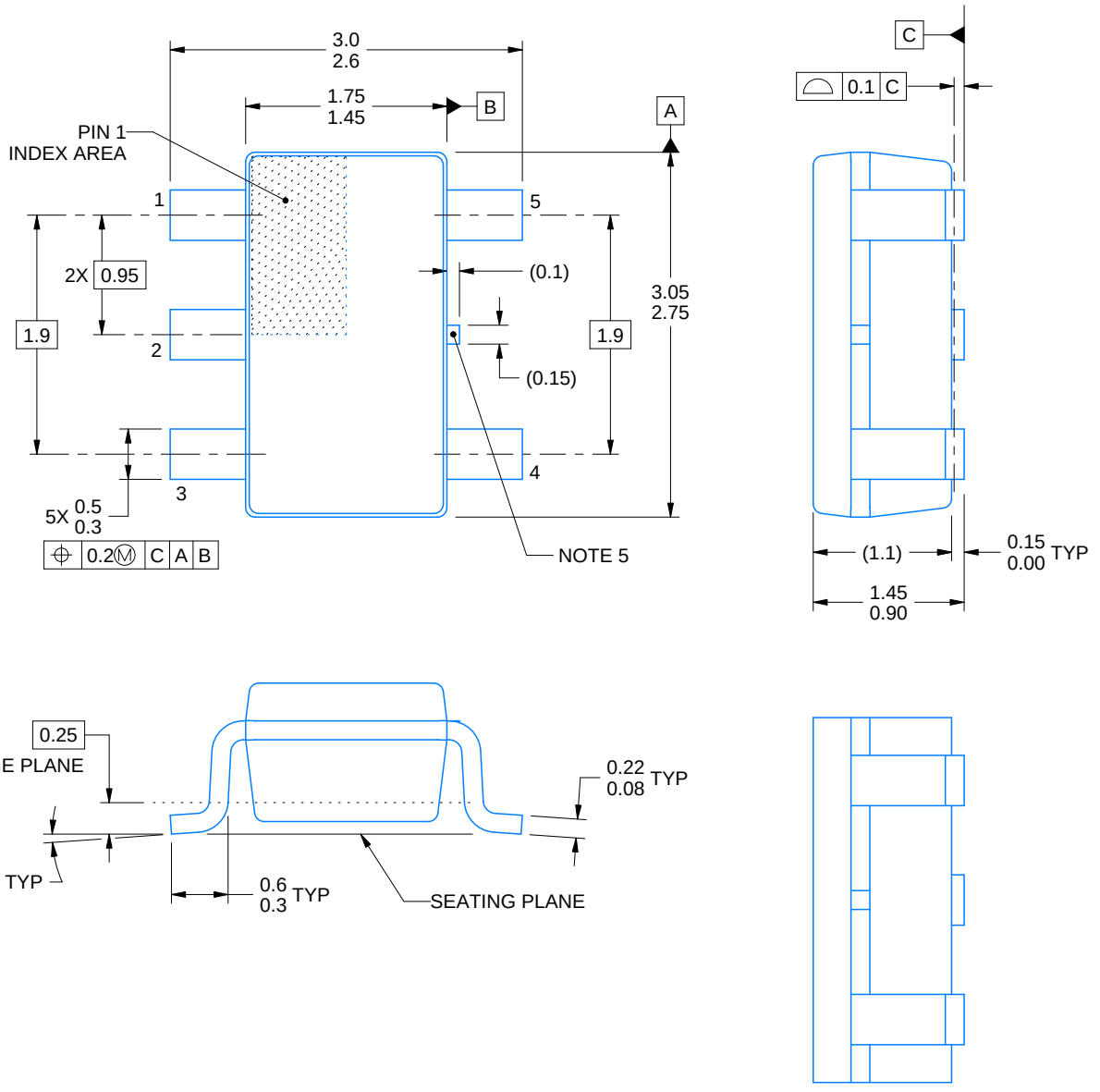
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2377QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA377QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA4377AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

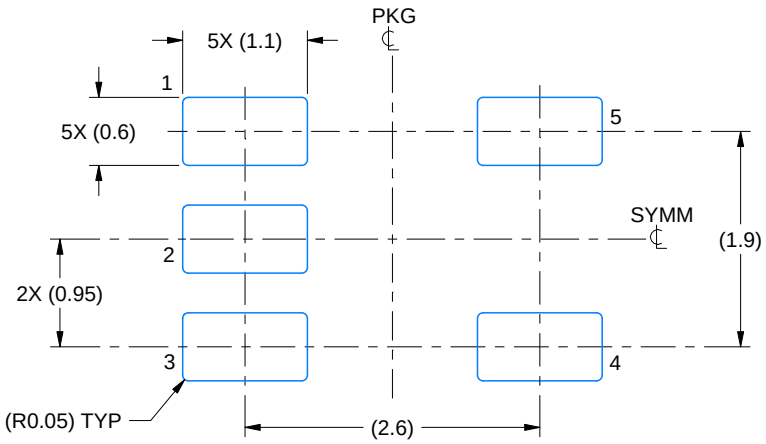


ALTERNATIVE PACKAGE SINGULATION VIEW

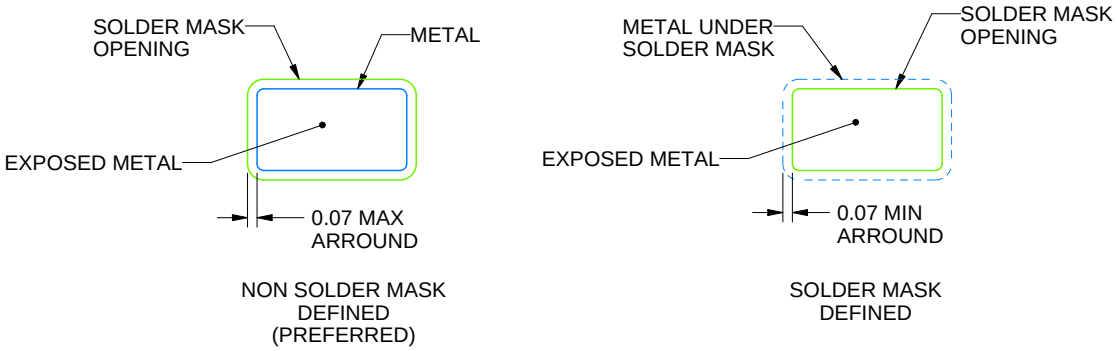
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

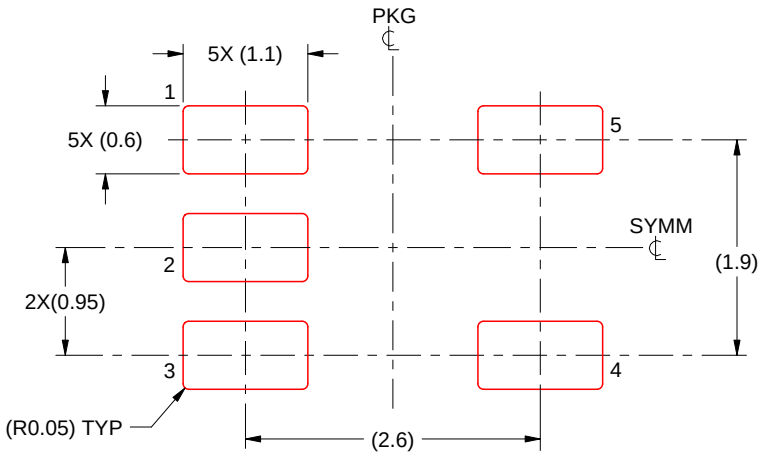


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



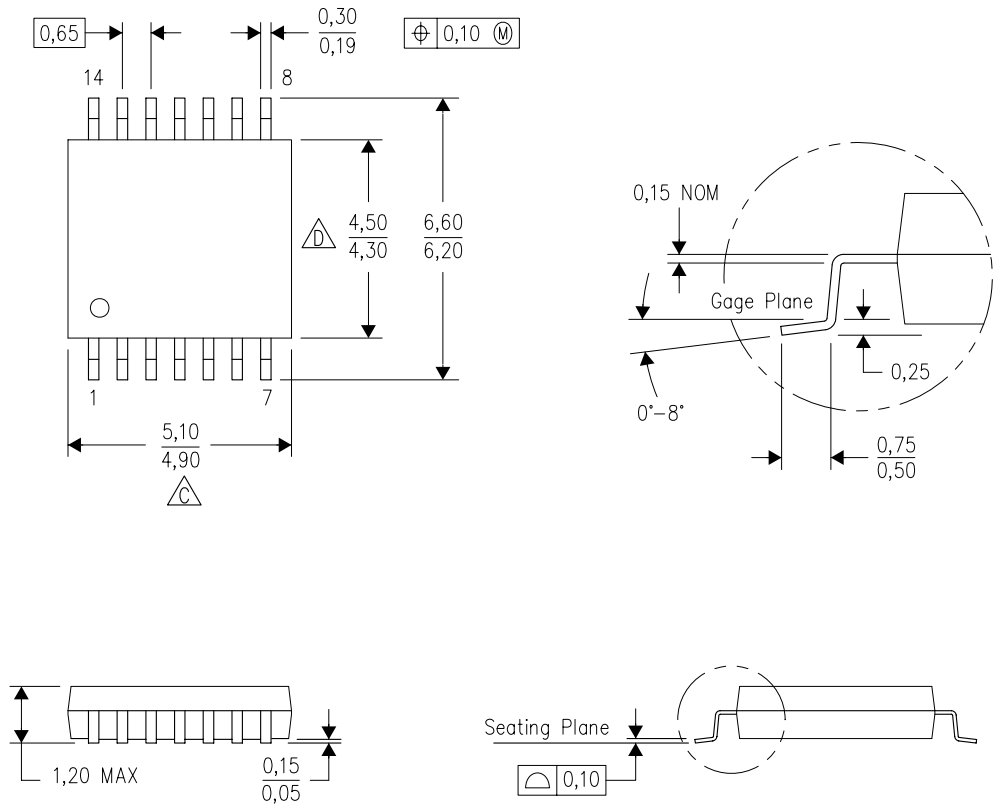
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

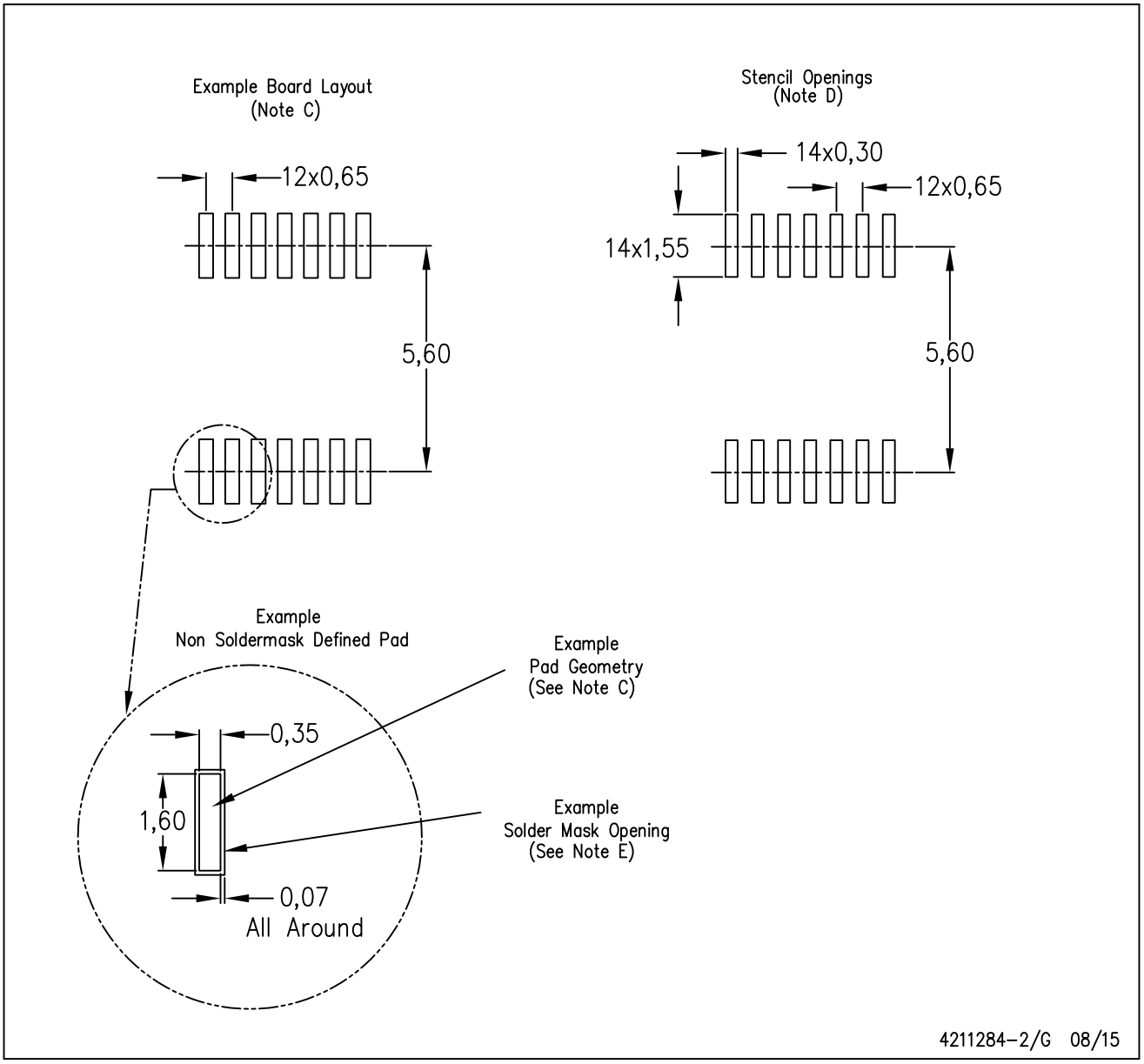
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

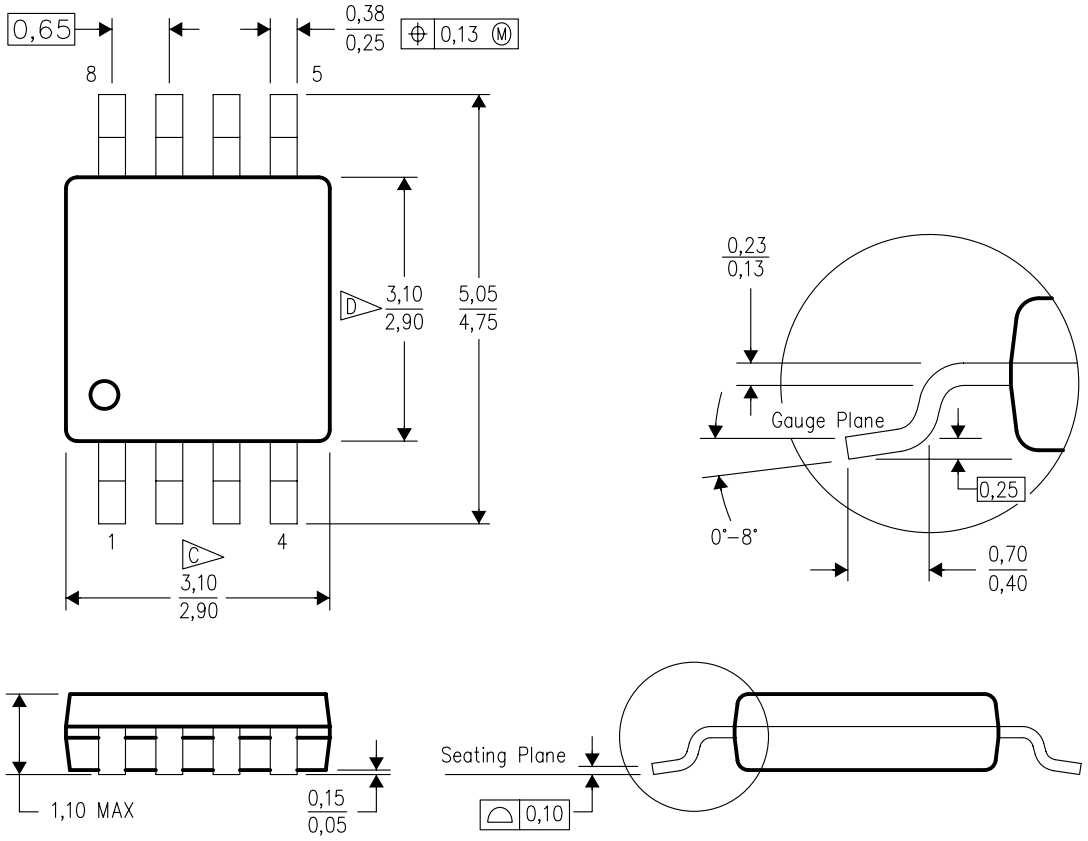
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

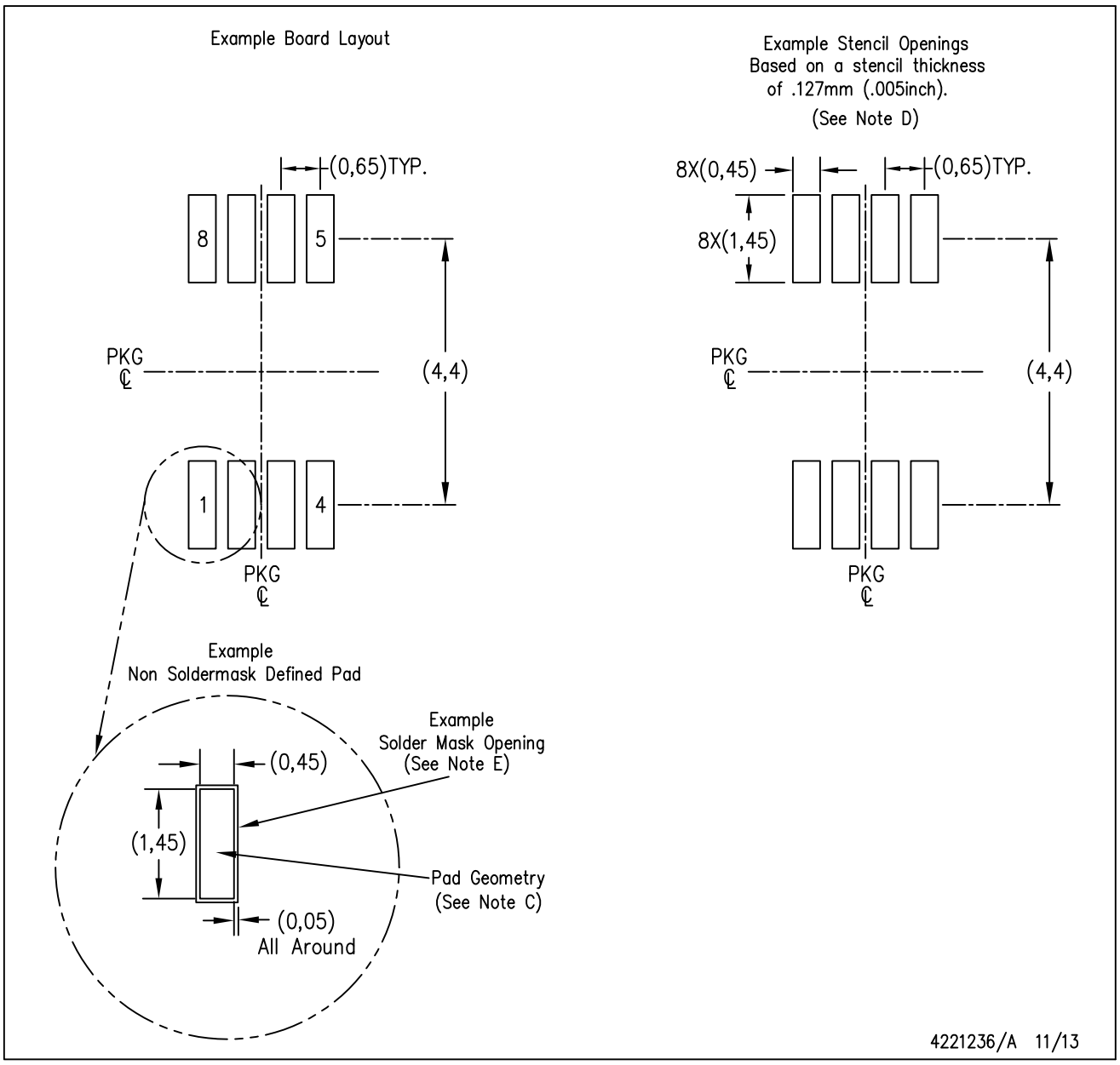
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265