具有停机模式的 20-MHz、低噪声、1.8-V、RRI/O, CMOS 运算放大器

查询样品: OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S

特性

- 增益带宽： **20 MHz**
- 低噪声： **8.5 nV/√Hz** （在 **1 kHz** 频率条件下）
- 转换速率： **10 V/μs**
- 低 **THD + N： 0.0005%**
- 轨至轨输入输出 **(I/O)**
- 失调电压： **2 mV** （最大值）
- 电源电压： **1.8 V** 至 **5.5 V**
- 电源电流： 每通道 **1.5 mA**
  - 停机模式： 每个通道的静态电流为 **0.1 μA**
- 具有稳定的单位增益
- 小外形封装：
  - **SOT23, DFN, MSOP, TSSOP**

应用范围

- 传感器信号调节
- 消费类音频
- 多极点有源滤波器
- 控制环路放大器
- 通信
- 安全
- 扫描仪

说明

OPA322 系列包含具有低噪声和轨至轨输入/输出的单通道、双通道和四通道 CMOS 运算放大器，专为低功耗、单电源应用而优化。 1.8 V 至 5.5 V 的宽电源范围以及每通道仅 1.5 mA 的低静态电流，使得这些器件非常适合于功耗敏感型应用。

由于兼具超低的噪声（在 1 kHz 频率下为 8.5 nV/√Hz ）、高的增益带宽 (20 MHz) 和高转换速率 (10 V/μs)，因而使得 OPA322 系列成为众多应用的理想选择，包括信号调节及需要高增益的传感器放大。 另外，OPA322 系列还拥有很低的 THD + N，因此同样极为适合于消费类音频应用，尤其是单电源系统。

OPAx322S 型号的器件具有一种停机模式，该模式允许将放大器从正常操作状态切换至待机状态 （待机电流通常小于 0.1 μA）。

OPA322 （单通道版本） 采用 SOT23-5 和 SOT23-6 封装，而 OPA2322 （双通道版本） 则可提供 MSOP-8、MSOP-10、SO-8 和 DFN-8 封装。 四通道版本 OPA4322 采用 TSSOP-14 和 TSSOP-16 封装。 所有器件版本的规定工作温度范围均为 —40℃ 至 +125℃

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA322	SOT23-5	DBV	RAD
OPA322S	SOT23-6	DBV	RAF
OPA2322	SO-8	D	O2322A
	MSOP-8	DGK	OOZI
	DFN-8	DRG	OPCI
OPA2322S	MSOP-10	DGS	OPBI
OPA4322	TSSOP-14	PW	O4322
OPA4322S	TSSOP-16	PW	O4322SA

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S	UNIT
Supply voltage, V_S = (V+) – (V–)		6	V
Signal input pins	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short-circuit current(3)		Continuous	mA
Operating temperature, T_A		–40 to +150	°C
Storage temperature, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
ESD ratings	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

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ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V, or ±0.9 V to ±2.75 V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2, and $\overline{SHDN_x}$ = V_S+, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			0.5	2	mV
vs Temperature	**dV_{OS}/dT**	**V_S = +5.5 V**		**1.8**	**6**	**µV/°C**
vs Power supply	PSR	V_S = +1.8 V to +5.5 V		10	50	µV/V
Over temperature		**V_S = +1.8 V to +5.5 V**		**20**	**65**	**µV/V**
Channel separation		At 1 kHz		130		dB
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-mode rejection ratio	CMRR	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	90	100		dB
Over temperature			**90**			**dB**
INPUT BIAS CURRENT						
Input bias current	I_B			±0.2	±10	pA
Over temperature		**T_A = –40°C to +85°C**			**±50**	**pA**
		OPA322, OPA322S, T_A = –40°C to +125°C			**±800**	**pA**
		OPA2322, OPA2322S, T_A = –40°C to +125°C			**±400**	**pA**
		OPA4322, OPA4322S, T_A = –40°C to +125°C			**±400**	**pA**
Input offset current	I_{OS}			±0.2	±10	pA
Over temperature		**T_A = –40°C to +85°C**			**±50**	**pA**
		T_A = –40°C to +125°C			**±400**	**pA**
NOISE						
Input voltage noise		f = 0.1 Hz to 10 Hz		2.8		μV_{PP}
Input voltage noise density	e_n	f = 1 kHz		8.5		nV/√Hz
		f = 10 kHz		7		nV/√Hz
Input current noise density	i_n	f = 1 kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
Differential				5		pF
Common-mode				4		pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{OL}	0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ	100	130		dB
		0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ	**94**			**dB**
Phase margin	PM	V_S = 5 V, C_L = 50 pF		47		Degrees
FREQUENCY RESPONSE		**V_S = 5.0 V, C_L = 50 pF**				
Gain bandwidth product	GBP	Unity gain		20		MHz
Slew rate	SR	G = +1		10		V/µs
Settling time	t_S	To 0.1%, 2-V step, G = +1		0.25		µs
		To 0.01%, 2-V step, G = +1		0.32		µs
Overload recovery time		V_{IN} × G > V_S		100		ns
Total harmonic distortion + noise(1)	THD+N	V_O = 4 V_{PP}, G = +1, f = 10 kHz, R_L = 10 kΩ		0.0005		%
		V_O = 2 V_{PP}, G = +1, f = 10 kHz, R_L = 600 Ω		0.0011		%

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

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ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V, or ±0.9 V to ±2.75 V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2, and $\overline{SHDN_x}$ = V_S+, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage output swing from both rails	V_O	R_L = 10 kΩ		10	20	mV
Over temperature		**R_L = 10 kΩ**			**30**	**mV**
Short-circuit current	I_{SC}	V_S = 5.5 V		±65		mA
Capacitive load drive	C_L		See Typical Characteristics			
Open-loop output resistance	R_O	I_O = 0 mA, f = 1 MHz		90		Ω
POWER SUPPLY						
Specified voltage range	V_S		1.8		5.5	V
Quiescent current per amplifier	I_Q	I_O = 0 mA, V_S = +5.5 V				
OPA322, OPA322S		I_O = 0 mA, V_S = +5.5 V		1.6	1.9	mA
Over temperature		**I_O = 0 mA, V_S = +5.5 V**			**2**	**mA**
OPA2322, OPA2322S		I_O = 0 mA, V_S = +5.5 V		1.5	1.75	mA
Over temperature		**I_O = 0 mA, V_S = +5.5 V**			**1.85**	**mA**
OPA4322, OPA4322S		I_O = 0 mA, V_S = +5.5 V		1.4	1.65	mA
Over temperature		**I_O = 0 mA, V_S = +5.5 V**			**1.75**	**mA**
Power-on time		V_{S+} = 0 V to 5 V, to 90% I_Q level		28		µs
SHUTDOWN(2)		V_S = 1.8 V to 5.5 V				
Quiescent current, per amplifier	I_{QSD}	All amplifiers disabled, $\overline{SHDN}$ = V_{S-}		0.1	0.5	µA
High voltage (enabled)	V_{IH}	Amplifier enabled	(V+) - 0.1			V
Low voltage (disabled)	V_{IL}	Amplifier disabled			(V-) + 0.1	V
Amplifier enable time (full shutdown)(3)	t_{ON}	Full shutdown; G = 1, V_{OUT} = 0.9 × V_S/2 (4)		10		µs
Amplifier enable time (partial shutdown) (3)	t_{ON}	Partial shutdown; G = 1, V_{OUT} = 0.9 × V_S/2 (4)		6		µs
Amplifier disable time(3)	t_{OFF}	G = 1, V_{OUT} = 0.1 × V_S/2		3		µs
$\overline{SHDN}$ pin input bias current (per pin)		V_{IH} = 5.0 V		0.13		µA
		V_{IL} = 0 V		0.04		µA
TEMPERATURE						
Specified range			–40		+125	°C
Operating range			–40		+150	°C

(2) Ensured by design and characterization; not production tested.
(3) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(4) Full shutdown refers to the dual OPA2322S having both channels A and B disabled ($\overline{SHDN_A}$ = $\overline{SHDN_B}$ = V_{S-}) and the quad OPA4322S having all channels A to D disabled ($\overline{SHDN_A/B}$ = $\overline{SHDN_C/D}$ = V_{S-}). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in this mode, the internal biasing and oscillator remain operational and the enable time is shorter.

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THERMAL INFORMATION: OPA322

THERMAL METRIC(1)		OPA322	OPA322S	UNITS
		DBV	DBV	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	219.3	177.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	107.5	108.9	
θ_{JB}	Junction-to-board thermal resistance	57.5	27.4	
ψ_{JT}	Junction-to-top characterization parameter	7.4	13.3	
ψ_{JB}	Junction-to-board characterization parameter	56.9	26.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：SPRA953）。

THERMAL INFORMATION: OPA2322

THERMAL METRIC(1)		OPA2322			OPA2322S	UNITS
		D	DRG	DGK	DGS	
		8 PINS	8 PINS	8 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	122.6	50.6	174.8	171.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	67.1	54.9	43.9	43.0	
θ_{JB}	Junction-to-board thermal resistance	64.0	25.2	95.0	91.4	
ψ_{JT}	Junction-to-top characterization parameter	13.2	0.6	2.0	1.9	
ψ_{JB}	Junction-to-board characterization parameter	63.4	25.3	93.5	89.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	5.7	n/a	n/a	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：SPRA953）。

THERMAL INFORMATION: OPA4322

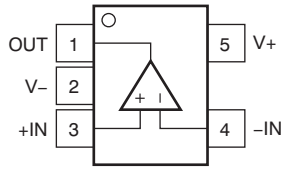
THERMAL METRIC(1)		OPA4322	OPA4322S	UNITS
		PW	PW	
		14 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	109.8	105.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	34.9	28.1	
θ_{JB}	Junction-to-board thermal resistance	52.5	51.1	
ψ_{JT}	Junction-to-top characterization parameter	2.2	0.8	
ψ_{JB}	Junction-to-board characterization parameter	51.8	50.4	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：SPRA953）。

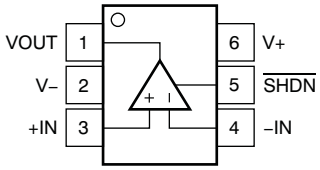
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PIN CONFIGURATIONS

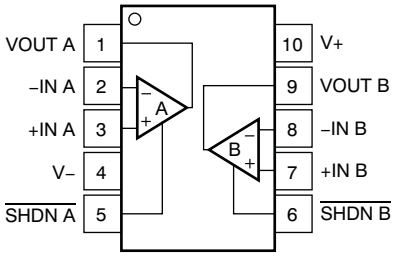
DBV PACKAGE
SOT23-5
(TOP VIEW)



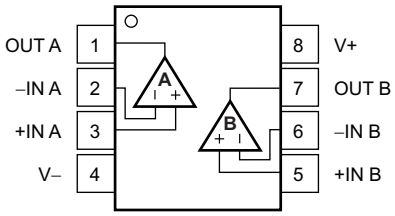
DBV PACKAGE
SOT23-6
(TOP VIEW)



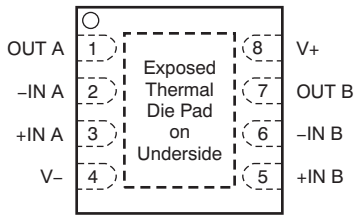
DGS PACKAGE
MSOP-10
(TOP VIEW)



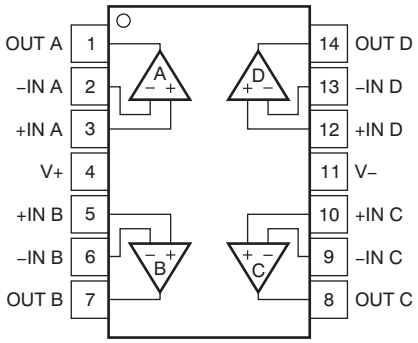
D, DGK PACKAGES
SO-8, MSOP-8
(TOP VIEW)



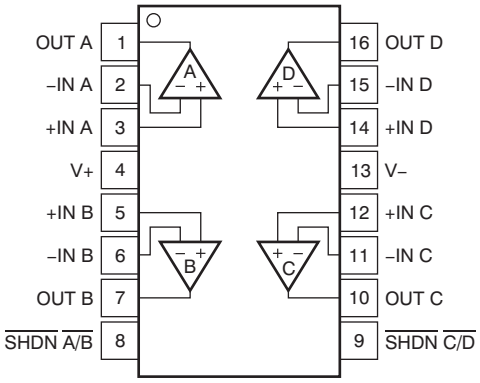
DRG PACKAGE(1)(2)
DFN-8
(TOP VIEW)



PW PACKAGE
TSSOP-14
(TOP VIEW)



PW PACKAGE
TSSOP-16
(TOP VIEW)



(1) Connect thermal pad to V–.

(2) Pad size: 2mm × 1.2mm.

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

OPEN-LOOP GAIN/PHASE vs FREQUENCY

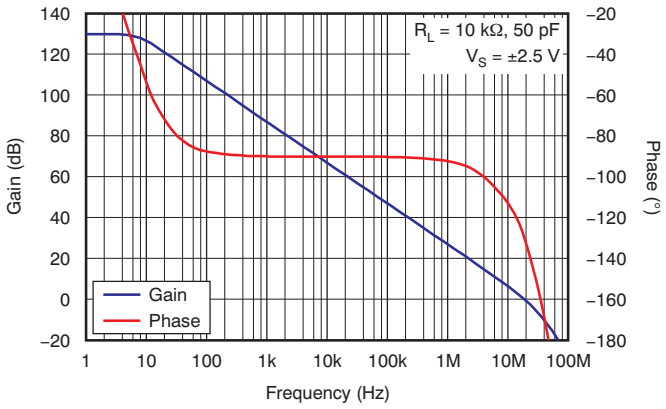


Figure 1.

OPEN-LOOP GAIN vs TEMPERATURE

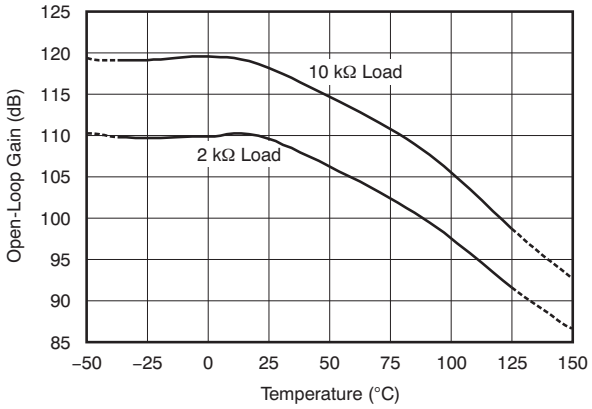


Figure 2.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

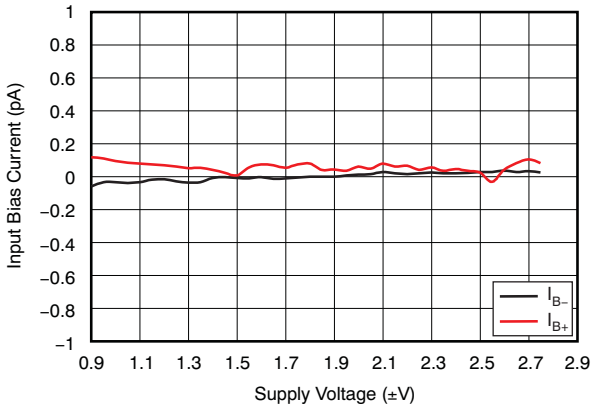


Figure 3.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

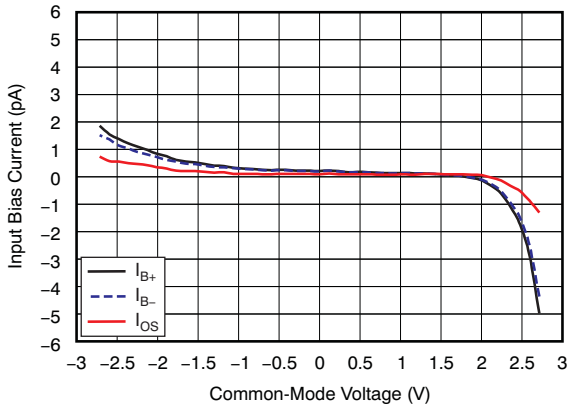


Figure 4.

INPUT BIAS CURRENT vs TEMPERATURE

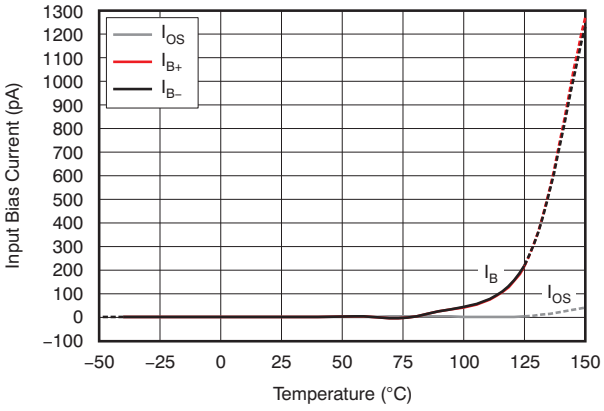


Figure 5.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

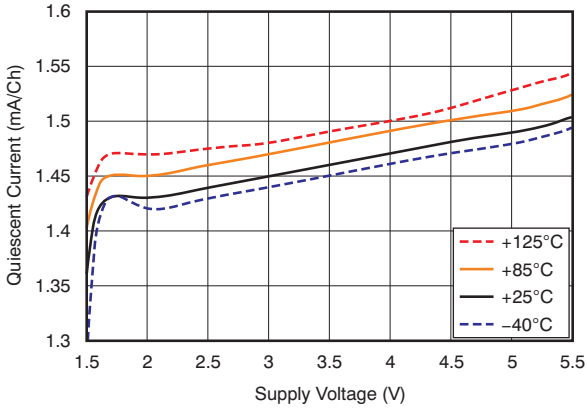


Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION HISTOGRAM

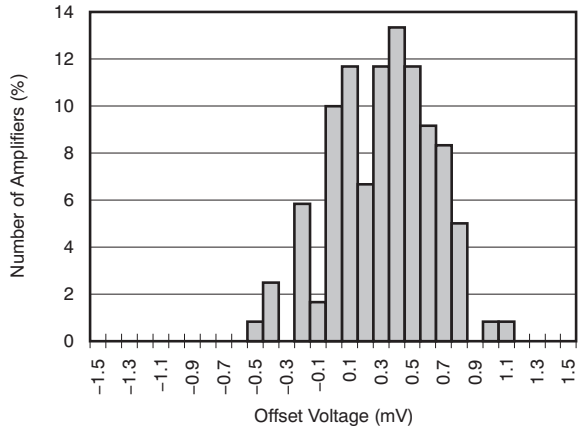


Figure 7.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

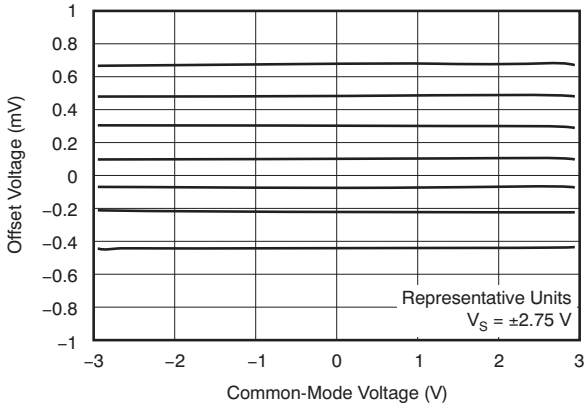


Figure 8.

INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

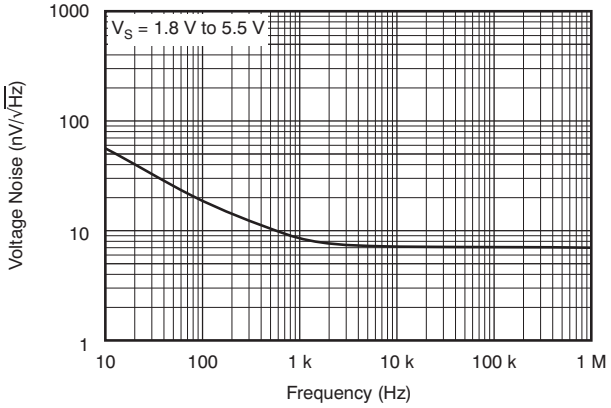


Figure 9.

0.1 Hz TO 10 Hz INPUT VOLTAGE NOISE

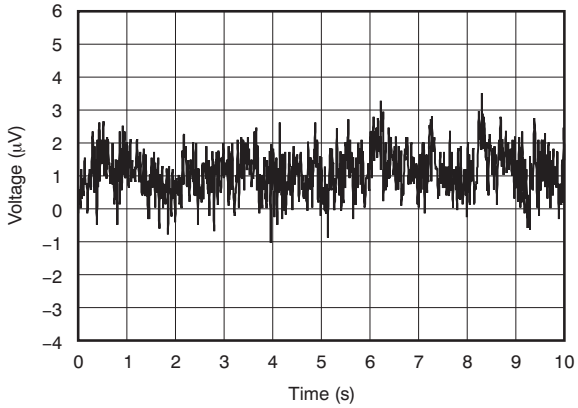


Figure 10.

CLOSED-LOOP GAIN vs FREQUENCY

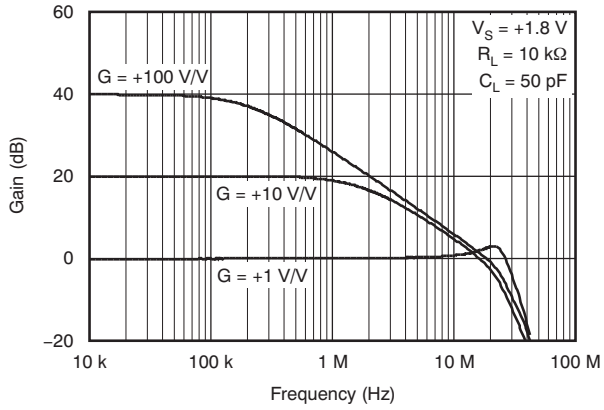


Figure 11.

CLOSED-LOOP GAIN vs FREQUENCY

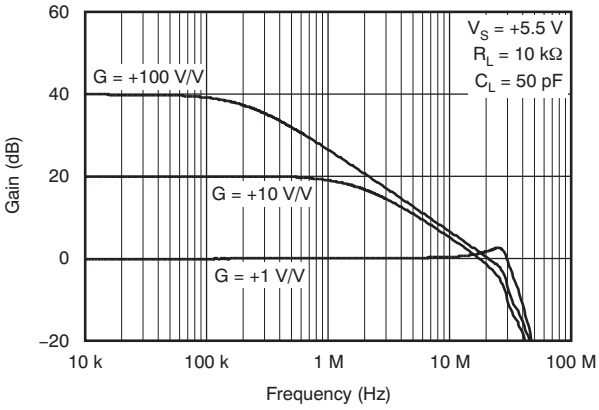


Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

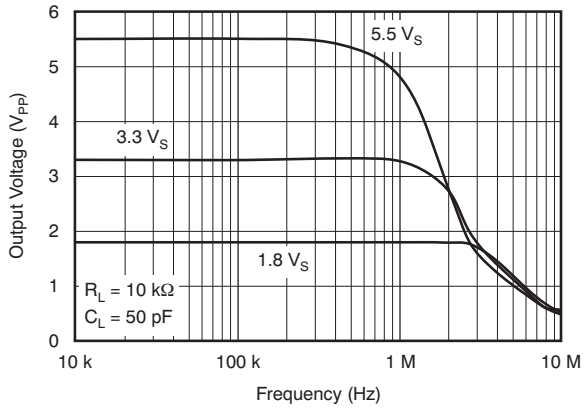


Figure 13.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

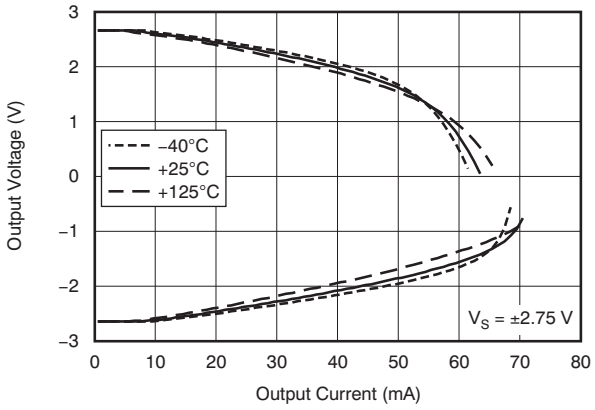


Figure 14.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

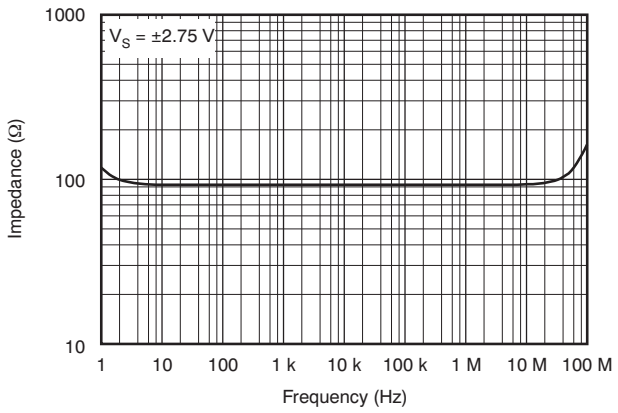


Figure 15.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

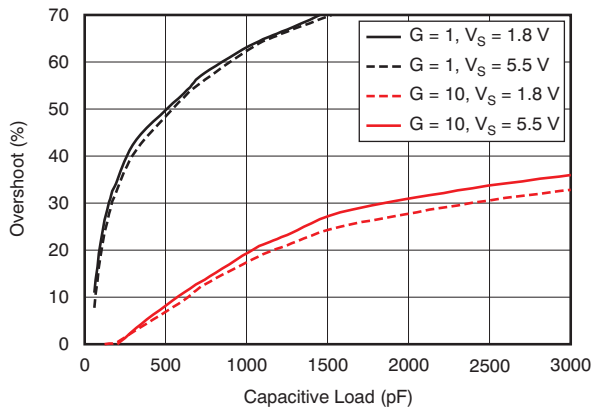


Figure 16.

THD+N vs AMPLITUDE

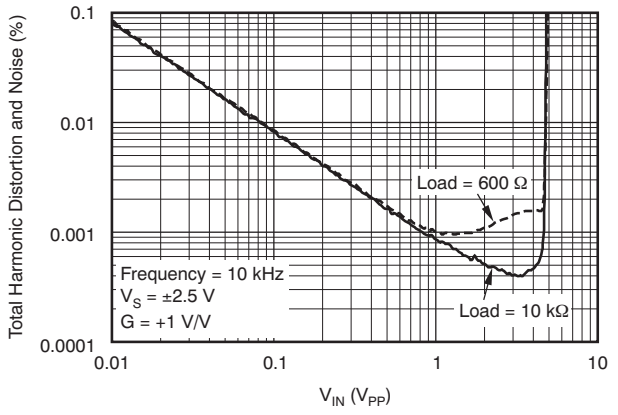


Figure 17.

THD+N vs FREQUENCY

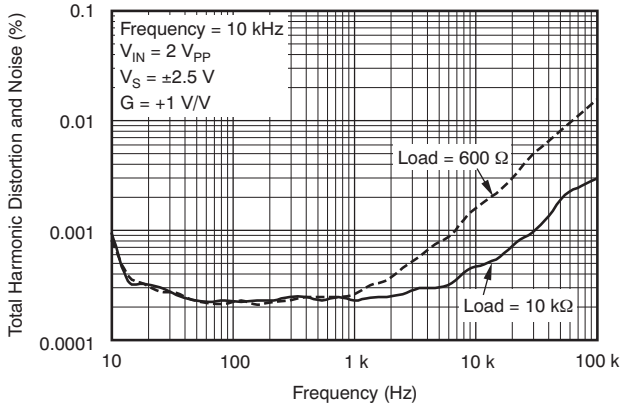


Figure 18.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

THD+N vs FREQUENCY

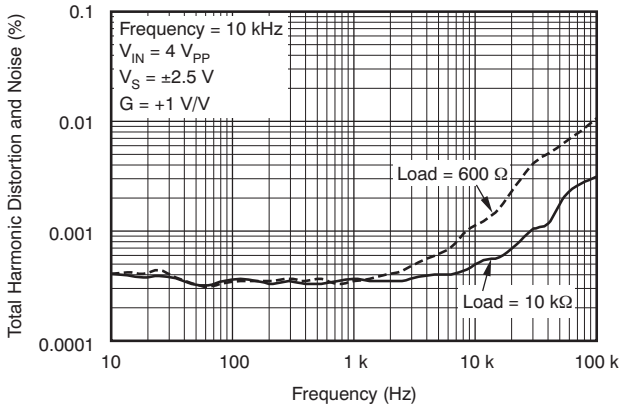


Figure 19.

CHANNEL SEPARATION vs FREQUENCY (for Dual)

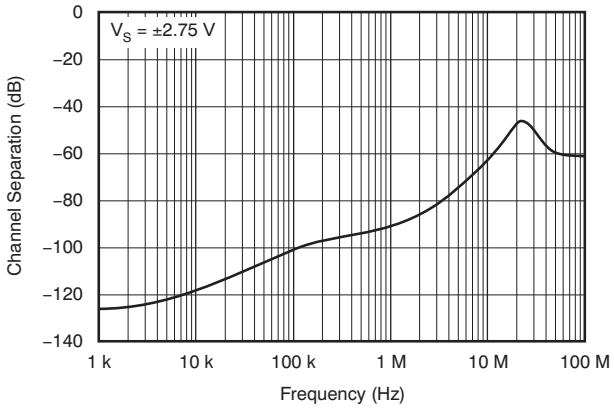


Figure 20.

SLEW RATE vs SUPPLY VOLTAGE

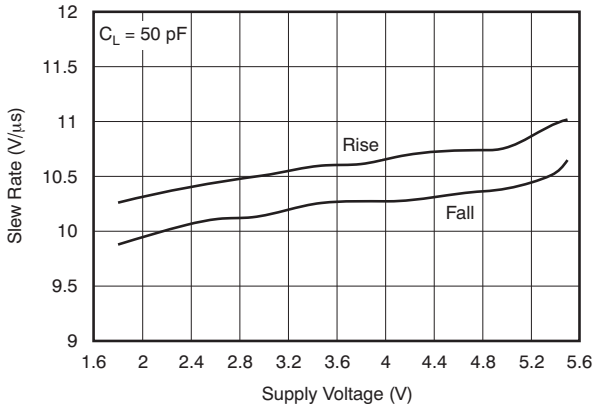


Figure 21.

SMALL-SIGNAL STEP RESPONSE

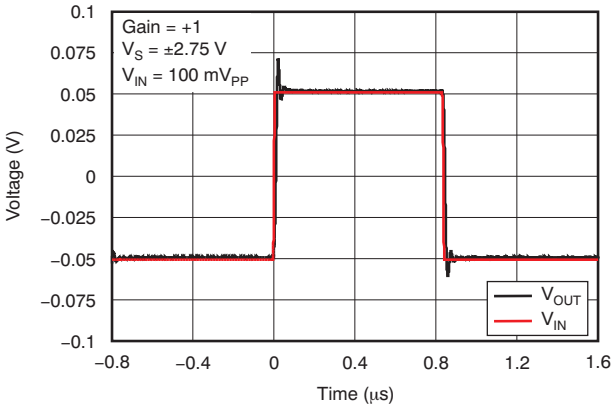


Figure 22.

SMALL-SIGNAL STEP RESPONSE

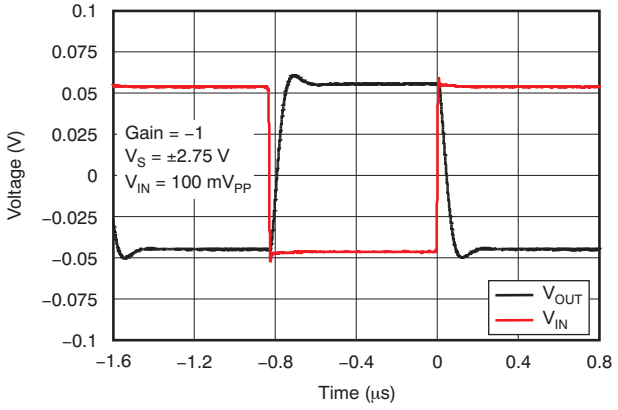


Figure 23.

LARGE-SIGNAL STEP RESPONSE vs TIME

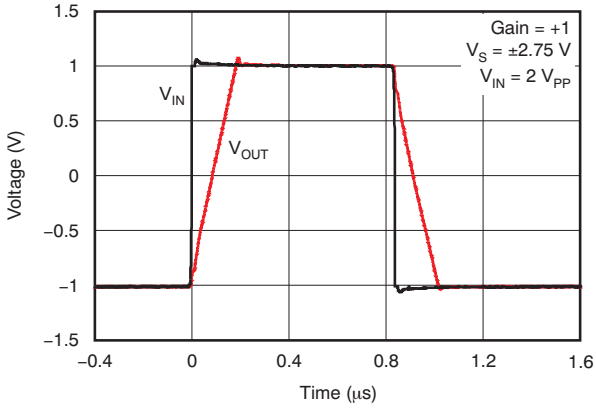


Figure 24.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

CMRR AND PSRR vs FREQUENCY

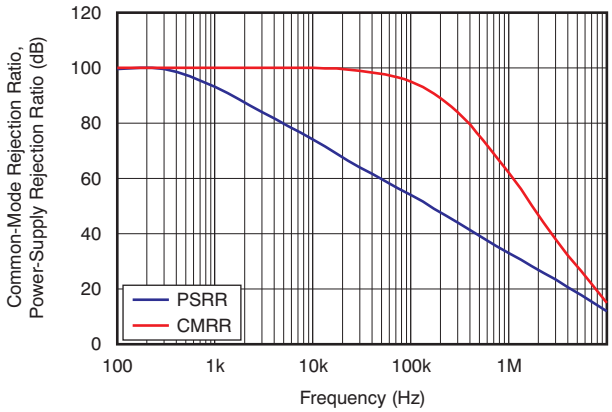


Figure 25.

TURN-OFF TRANSIENT

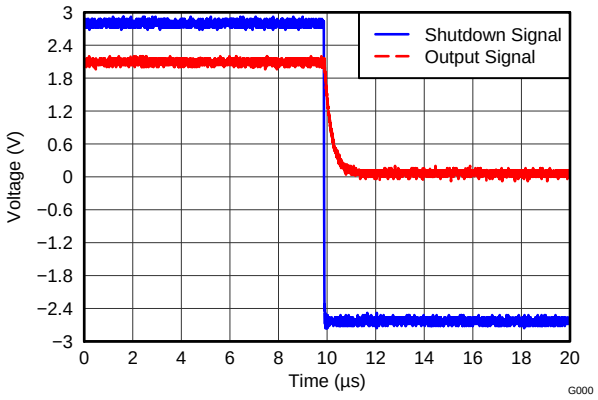


Figure 26.

TURN-ON TRANSIENT

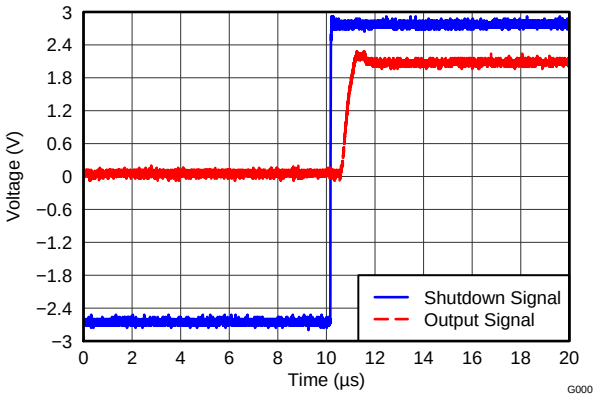


Figure 27.

TURN-ON AND TURN-OFF TRANSIENT 5.5V (High Supply)

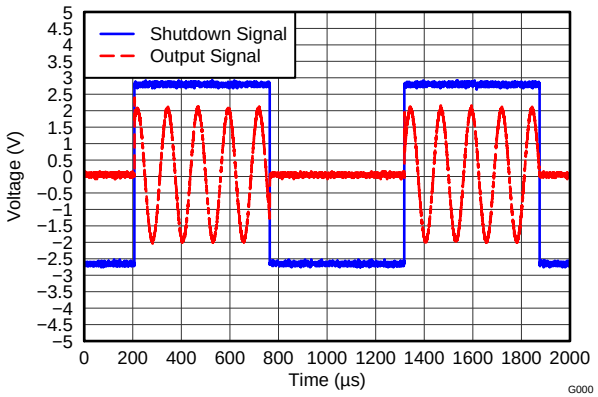


Figure 28.

TURN-ON AND TURN-OFF TRANSIENT 1.8V (Low Supply)

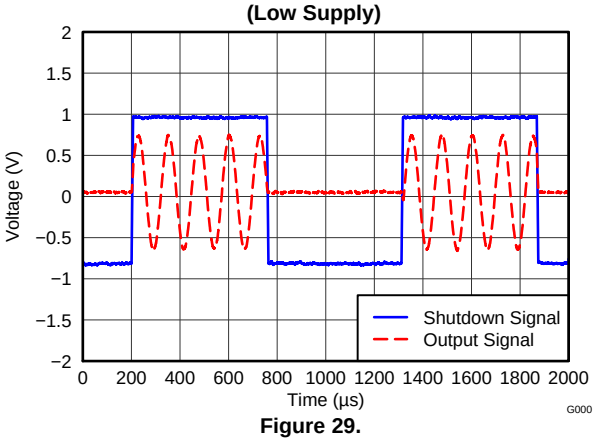


Figure 29.

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APPLICATION INFORMATION

OPERATING VOLTAGE

The OPA322 series op amps are unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (±0.9 V to ±2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 µF to 0.1 µF). These amplifiers are fully specified from +1.8 V to +5.5 V and over the extended temperature range of –40°C to +125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

INPUT AND ESD PROTECTION

The OPA322 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings table. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 30 shows how a series input resistor (R_S) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

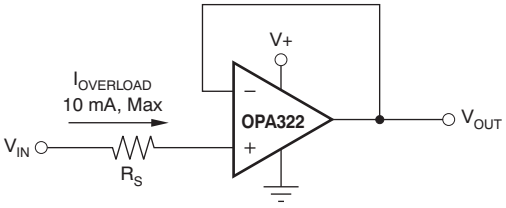


Figure 30. Input Current Protection

PHASE REVERSAL

The OPA322 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. Figure 31 shows the input voltage exceeding the supply voltage without any phase reversal.

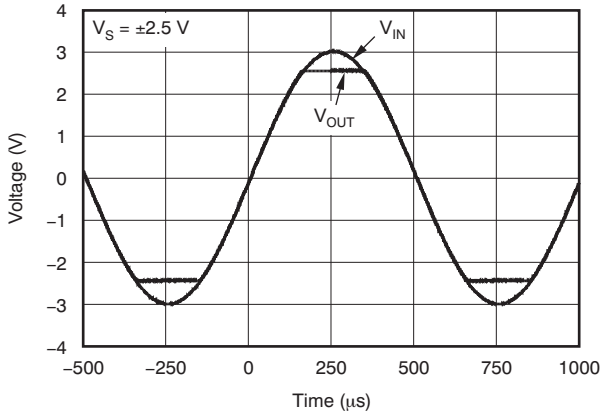
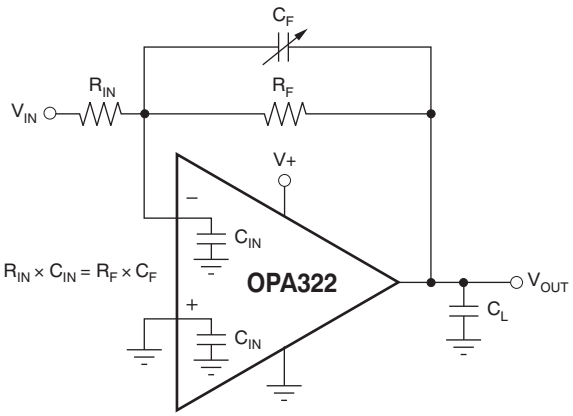


Figure 31. No Phase Reversal

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FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 32. This capacitor compensates for the zero created by the feedback network impedance and the OPA322 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.



NOTE: Where C_{IN} is equal to the OPA322 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 32. Feedback Capacitor Improves Dynamic Performance

It is suggested that a variable capacitor be used for the feedback capacitor because input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 32, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA322 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$R_{IN} \times C_{IN} = R_F \times C_F$

Where:

C_{IN} is equal to the OPA322 input capacitance (sum of differential and common-mode) plus the layout capacitance.

The capacitor value can be adjusted until optimum performance is obtained.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the device, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA322 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 580 MHz (–3 dB), with a roll-off of 20 dB per decade.

OUTPUT IMPEDANCE

The open-loop output impedance of the OPA322 common-source output stage is approximately 90 Ω. When the op amp is connected with feedback, this value is reduced significantly by the loop gain. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPA322 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This characteristic, in turn, prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA322 has excellent capacitive load drive capability for an op amp with its bandwidth.

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CAPACITIVE LOAD AND STABILITY

The OPA322 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA322 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (+1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA322 remains stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors (C_L > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 33. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor (R_S), typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 34.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider, however, may be insignificant. For instance, with a load resistance, R_L = 10 kΩ and R_S = 20 Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600 Ω, which the OPA322 is able to drive, the error increases to 7.5%.

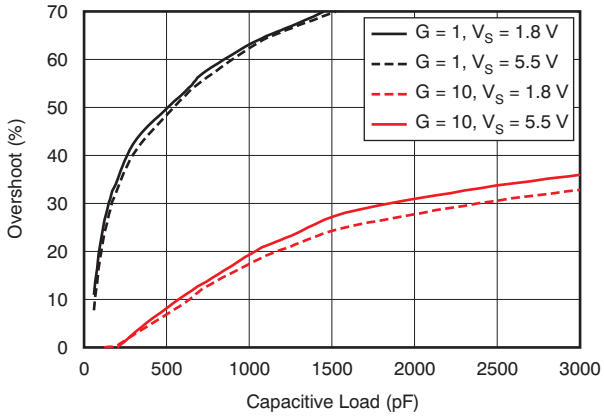


Figure 33. Small-Signal Overshoot versus Capacitive Load (100-mV_{PP} output step)

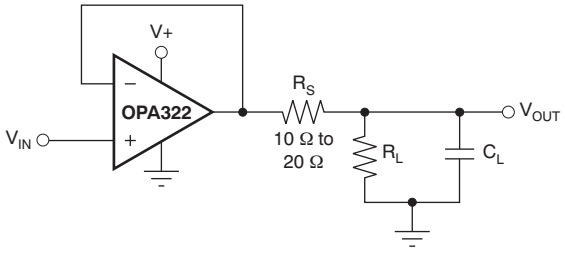


Figure 34. Improving Capacitive Load Drive

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OVERLOAD RECOVERY TIME

Overload recovery time is the time required for the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 35 and Figure 36 show the positive and negative overload recovery times of the OPA322, respectively. In both cases, the time elapsed before the OPA322 comes out of saturation is less than 100 ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

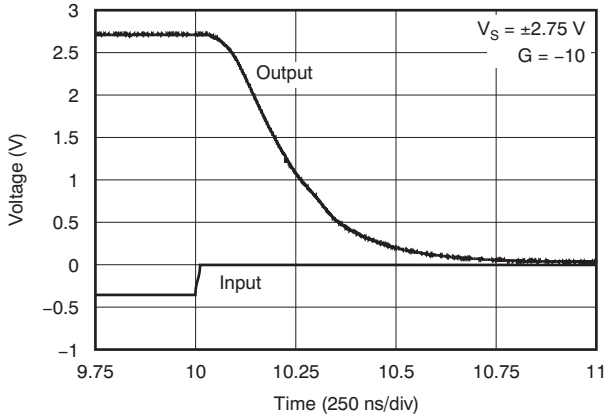


Figure 35. Positive Recovery Time

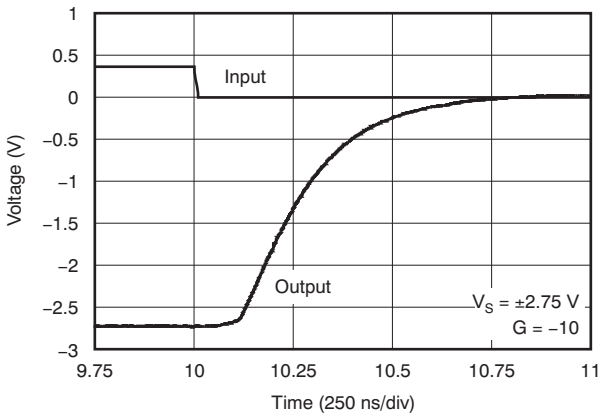


Figure 36. Negative Recovery Time

SHUTDOWN FUNCTION

The SHDN (enable) pin function of the OPAx322S is referenced to the negative supply voltage of the operational amplifier. A logic level high enables the op amp. A valid logic high is defined as voltage [(V+) – 0.1 V], up to (V+), applied to the SHDN pin. A valid logic low is defined as [(V–) + 0.1 V], down to (V–), applied to the enable pin. The maximum allowed voltage applied to SHDN is 5.5 V with respect to the negative supply, independent of the positive supply voltage. This pin should either be connected to a valid high or a low voltage or driven, and not left as an open circuit.

The logic input is a high-impedance CMOS input. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 µs for full shutdown of all channels; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx322S to be operated as a *gated* amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases with increased load resistance. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to mid-supply (V_S / 2) is required. If using the OPAx322S without a load, the resulting turn-off time is significantly increased.

GENERAL LAYOUT GUIDELINES

The OPA322 is a wideband amplifier. To realize the full operational performance of the device, follow good high-frequency printed circuit board (PCB) layout practices. The bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

LEADLESS DFN PACKAGE

The OPA2322 uses the DFN style package (also known as SON), which is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes PCB space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low height (0,8 mm).

DFN packages are physically small, and have a smaller routing area. Additionally, they offer improved thermal performance, reduced electrical parasitics, and a pinout scheme that is consistent with other commonly-used packages (such as SO and MSOP). The absence of external leads also eliminates bent-lead issues.

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The DFN package can easily be mounted using standard PCB assembly techniques. See the application reports, *QFN/SON PCB Attachment* (SLUA271) and *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com. **The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V–).** The dimension of the exposed thermal die pad is 2 mm × 1,2 mm and is centered.

APPLICATION EXAMPLES

ACTIVE FILTER

The OPA322 is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 37 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

1. adding an inverting amplifier;
2. adding an additional second-order MFB stage; or
3. using a noninverting filter topology, such as the Sallen-Key (shown in Figure 38).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

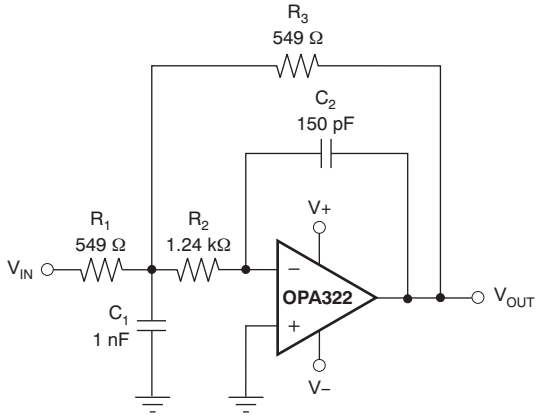


Figure 37. Second-Order Butterworth 500-kHz Low-Pass Filter

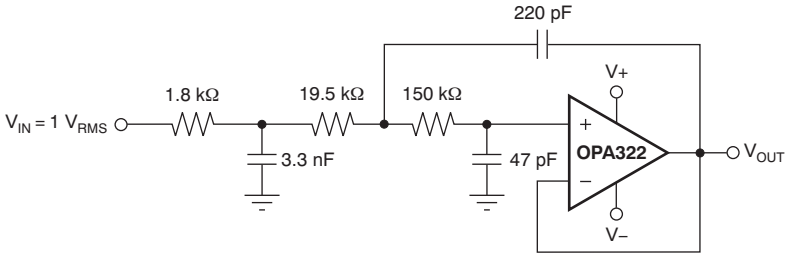


Figure 38. OPA322 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2012) to Revision E — **Page**

- Changed product status from Production Data to Mixed Status 1
- Updated D, DGK pinout drawing 6
- Added Figure 26 to Figure 29 11
- Added *Shutdown Function* section 15

Changes from Revision C (November 2011) to Revision D — **Page**

- Changed product status from Mixed Status to Production Data 1
- Deleted shading and footnote 2 from Package/Ordering Information table 2
- Added OPA4322, OPA4322S to the Input Bias Current, *Input bias current, Over temperature* parameter in Electrical Characteristics table 3
- Changed Power Supply, OPA4322, OPA4322S *Over temperature* parameter maximum specification in the Electrical Characteristics table 4

Changes from Revision B (July 2011) to Revision C — **Page**

- Changed status of OPA2322 SO-8 (D) to production data from product preview 2

Changes from Revision A (May 2011) to Revision B — **Page**

- Updated OPA322 SOT23-5 device status from product preview to production data in Package/Ordering Information table 2
- Changed Input Bias Current *Input bias current, Over temperature* parameter in Electrical Characteristics table 3
- Changed Open-Loop Gain, *Open-loop voltage gain* parameter typical specification in the Electrical Characteristics table 3
- Changed Open-Loop Gain, *Phase margin* parameter test conditions in the Electrical Characteristics table 3
- Added test conditions to *Power Supply* section in Electrical Characteristics table 4
- Changed Power Supply, Quiescent current per amplifier OPA322/S parameter maximum specification in the Electrical Characteristics 4
- Changed Power Supply, OPA322 *Over temperature* parameter maximum specification in the Electrical Characteristics table 4
- Changed Power Supply, Quiescent current per amplifier OPA4322/S parameter typical specification in the Electrical Characteristics 4
- Changed Shutdown, *Quiescent current, per amplifier* parameter maximum specification in Electrical Characteristics table 4
- Added OPA322S thermal information to Thermal Information: OPA322 table 5
- Added OPA2322S thermal information to Thermal Information: OPA2322 table 5
- Added OPA4322S thermal information to Thermal Information: OPA4322 table 5
- Updated Figure 1 7
- Added Figure 25 11
- Changed *Overload Recovery Time* section 15

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2322AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2322A	Samples
OPA2322AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOZI	Samples
OPA2322AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OOZI	Samples
OPA2322AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2322A	Samples
OPA2322AIDRGR	ACTIVE	SON	DRG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPCI	Samples
OPA2322AIDRGT	ACTIVE	SON	DRG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPCI	Samples
OPA2322SAIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPBI	Samples
OPA2322SAIDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPBI	Samples
OPA322AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAD	Samples
OPA322AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAD	Samples
OPA322SAIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAF	Samples
OPA322SAIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAF	Samples
OPA4322AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322A	Samples
OPA4322AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322A	Samples
OPA4322SAIPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322SA	Samples
OPA4322SAIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322SA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2322, OPA322, OPA4322 :

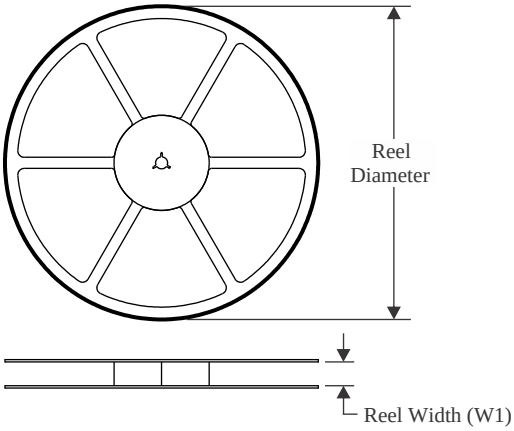
- Automotive : OPA2322-Q1, OPA322-Q1, OPA4322-Q1

NOTE: Qualified Version Definitions:

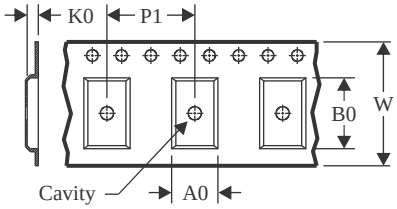
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

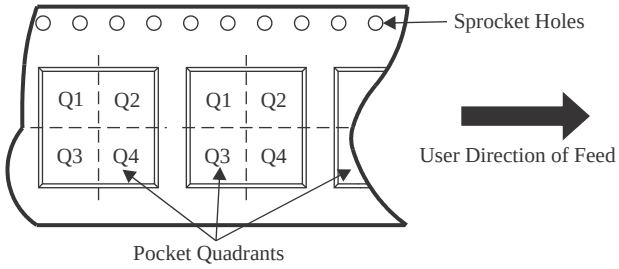


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

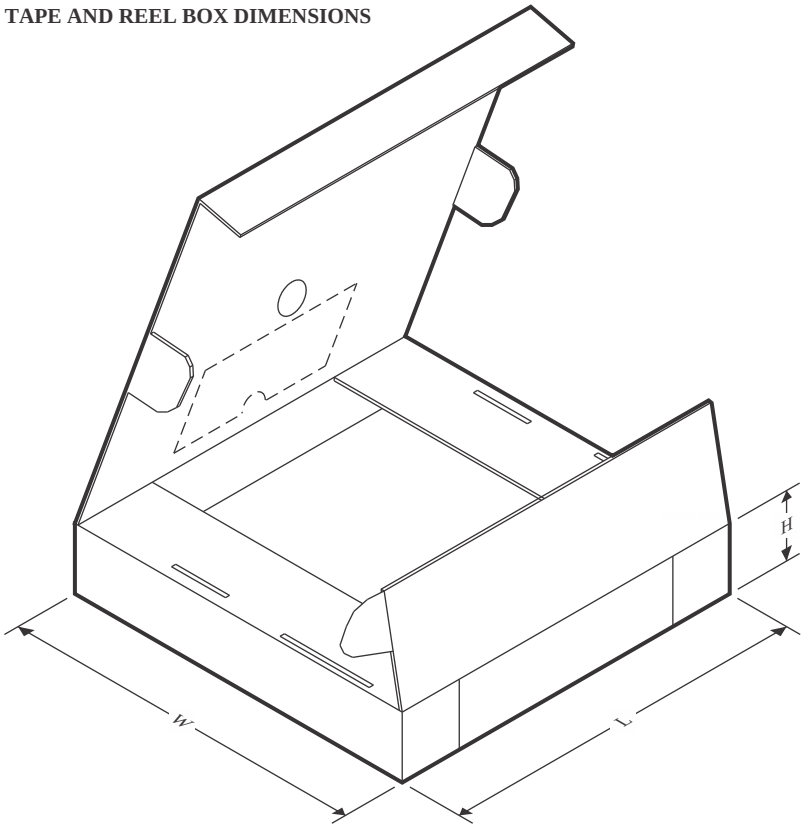
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2322AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2322AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2322AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2322SAIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322SAIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA322AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA322AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA322AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA322SAIDBVT	SOT-23	DBV	6	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA4322AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4322SAIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

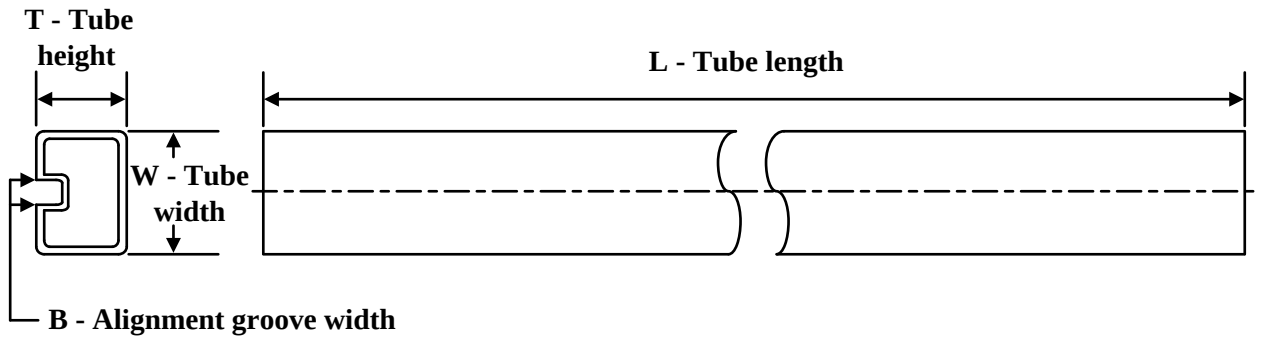
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2322AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2322AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2322AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2322AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2322AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2322AIDRGR	SON	DRG	8	3000	356.0	356.0	35.0
OPA2322AIDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA2322SAIDGSR	VSSOP	DGS	10	2500	356.0	356.0	35.0
OPA2322SAIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA322AIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA322AIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA322AIDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA322SAIDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
OPA4322AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
OPA4322SAIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

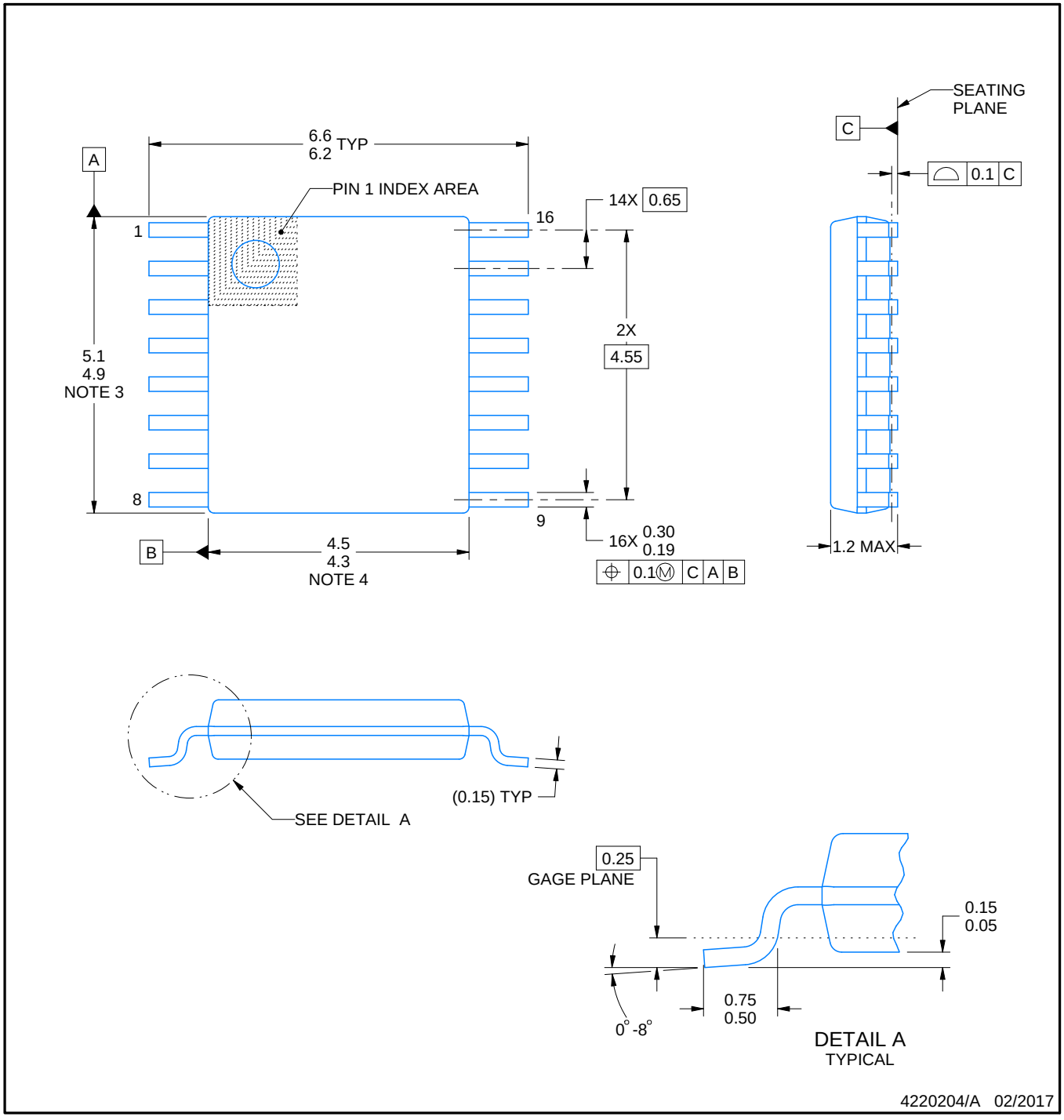
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2322AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4322AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
OPA4322SAIPW	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

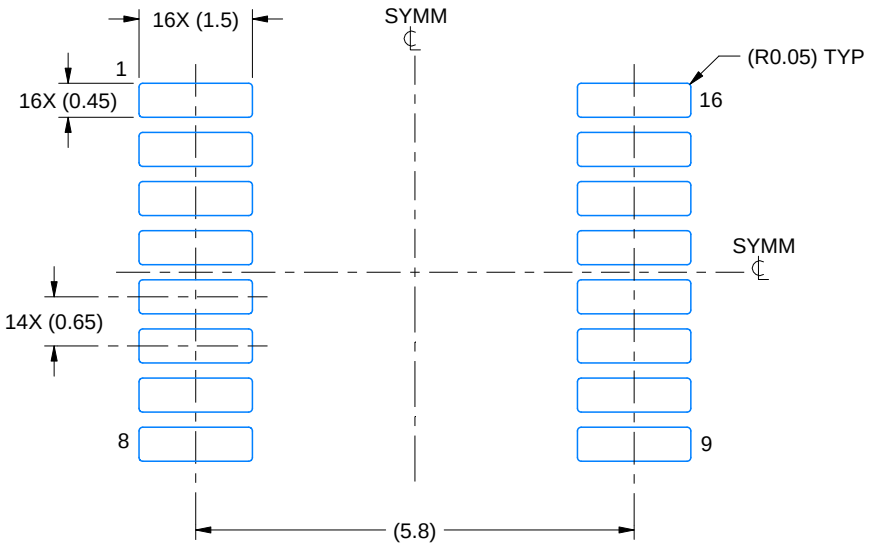
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

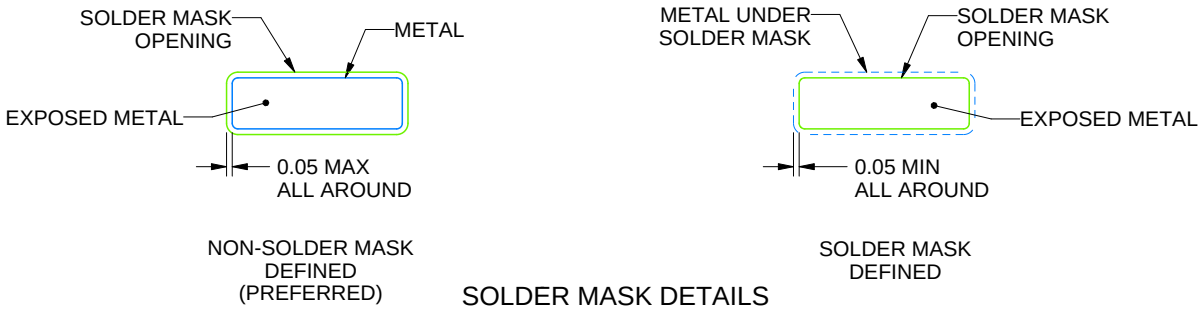


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

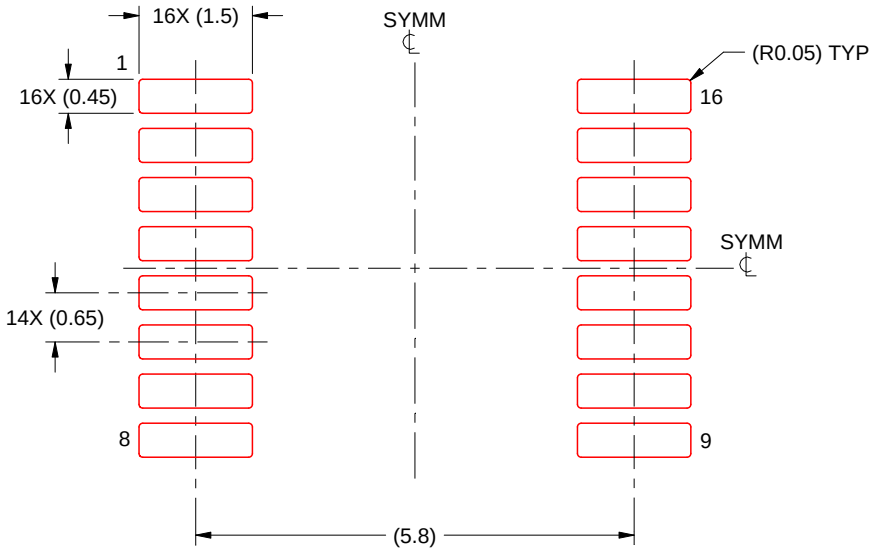


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

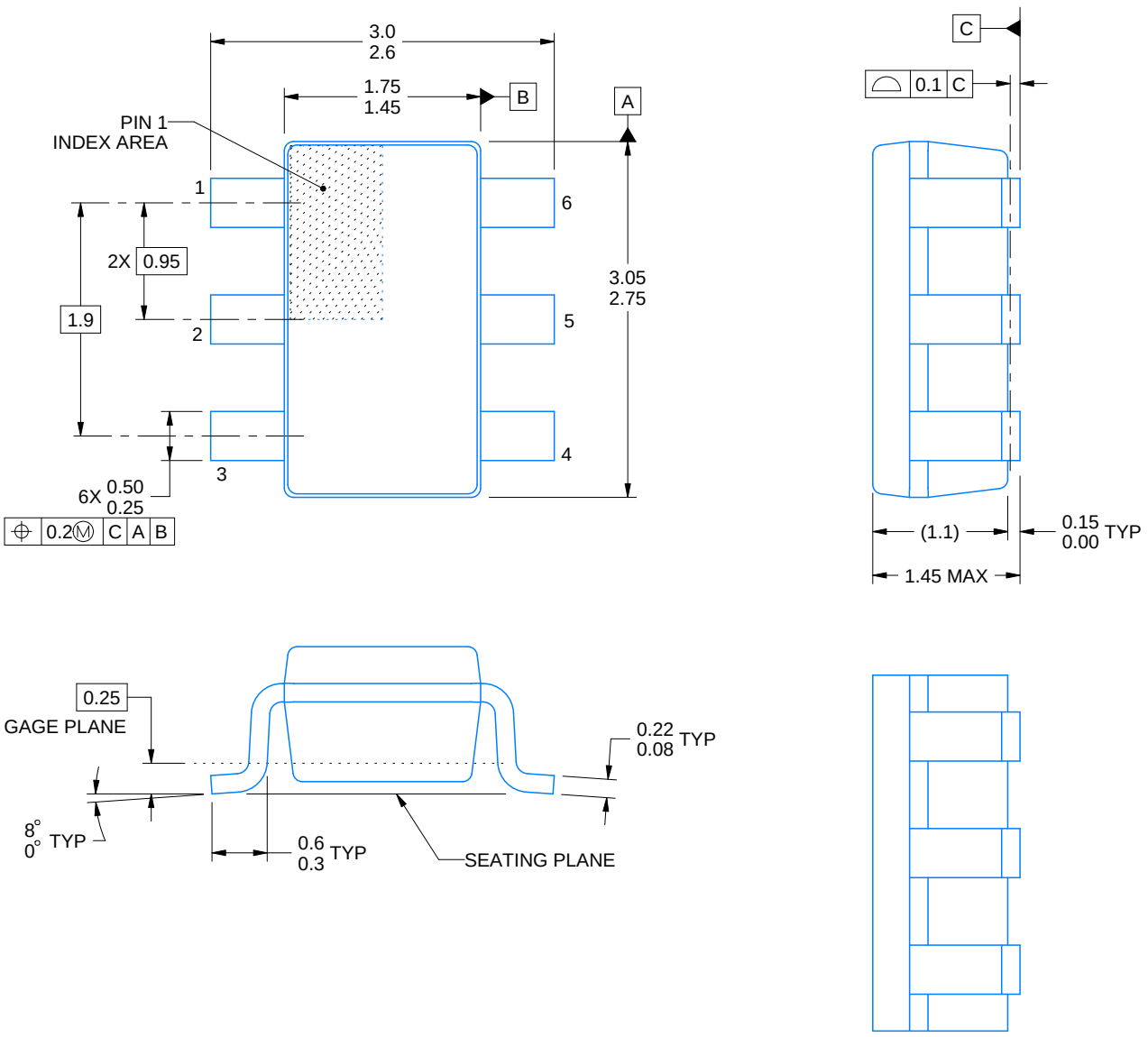
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

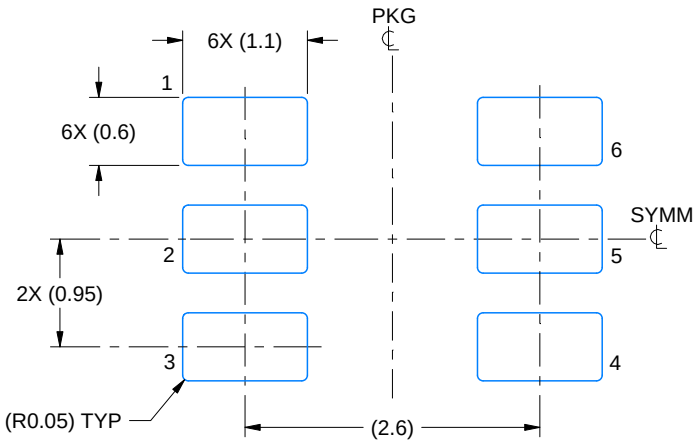


ALTERNATIVE PACKAGE SINGULATION VIEW

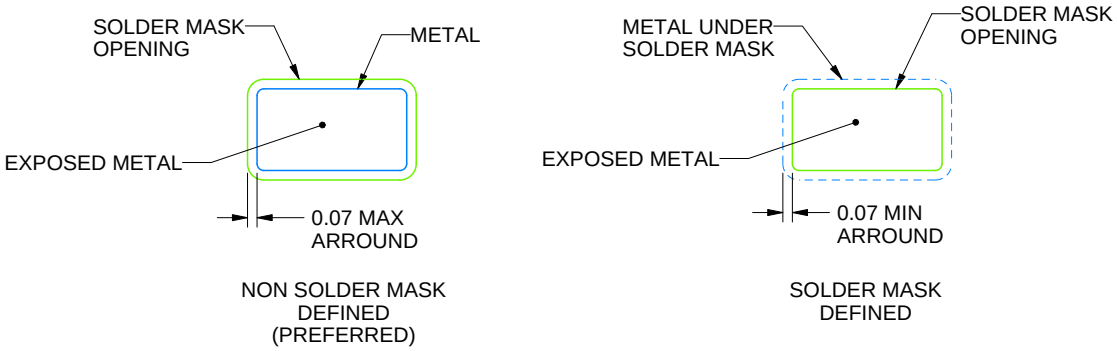
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

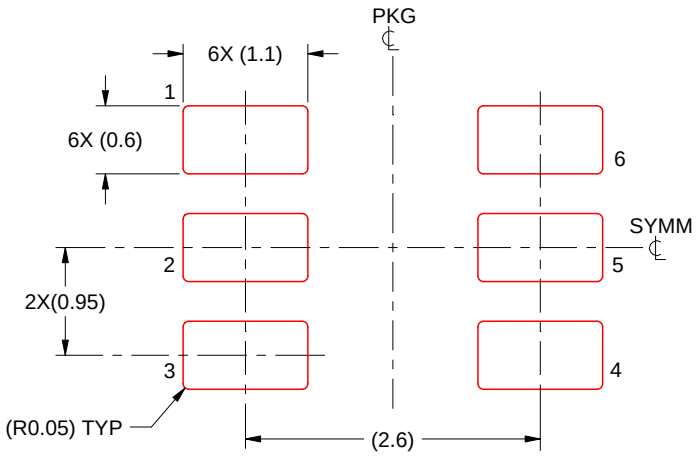


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

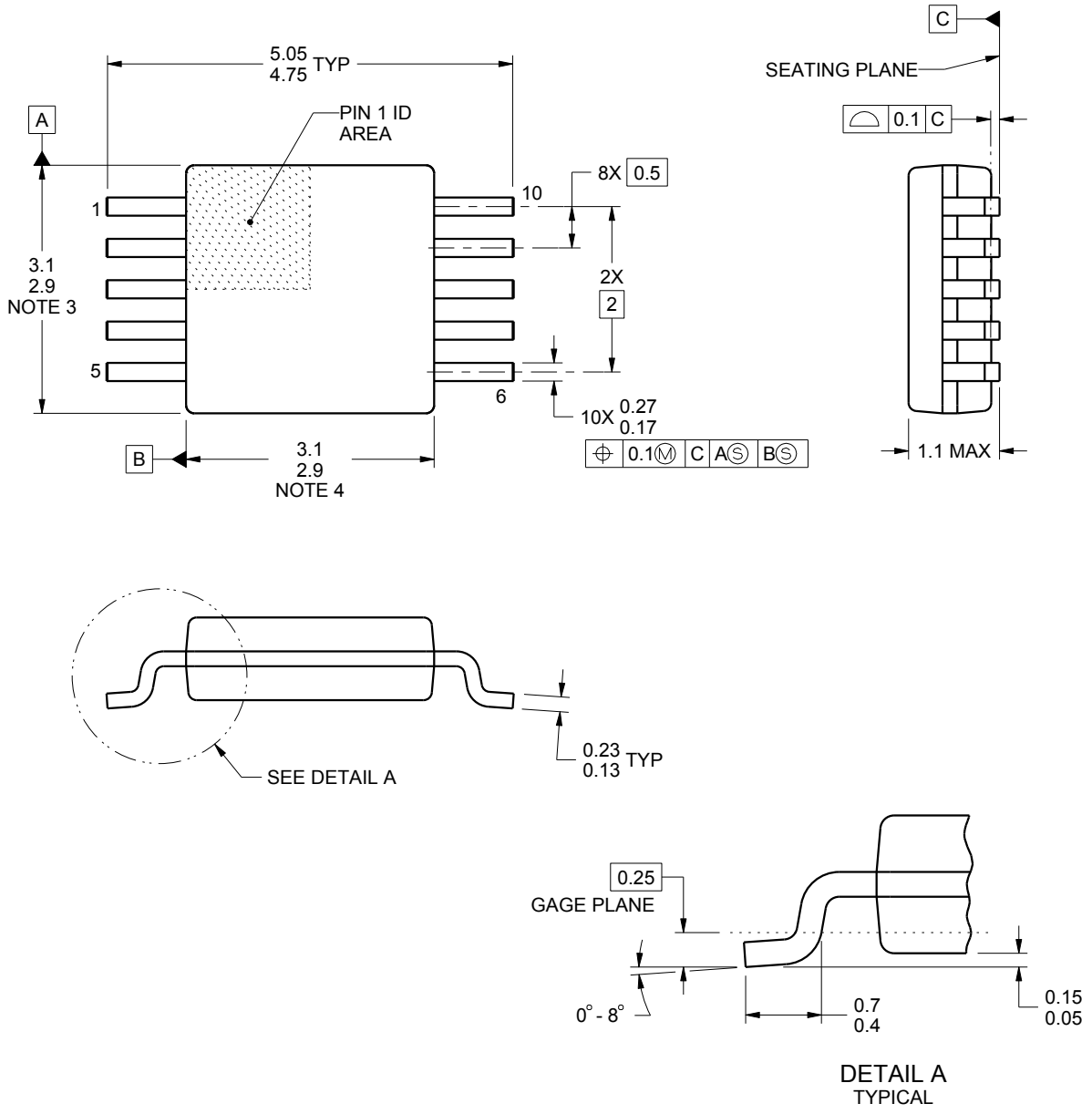
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

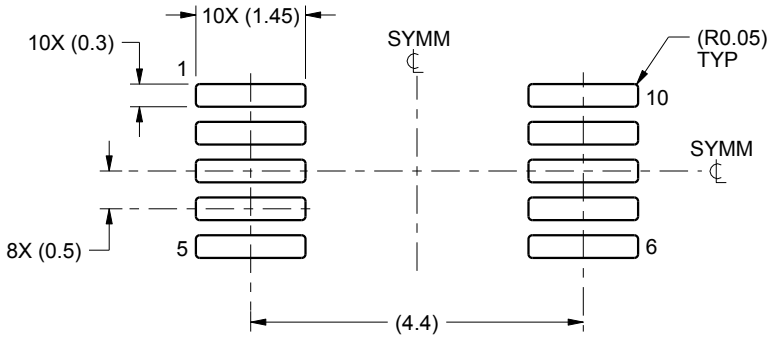
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

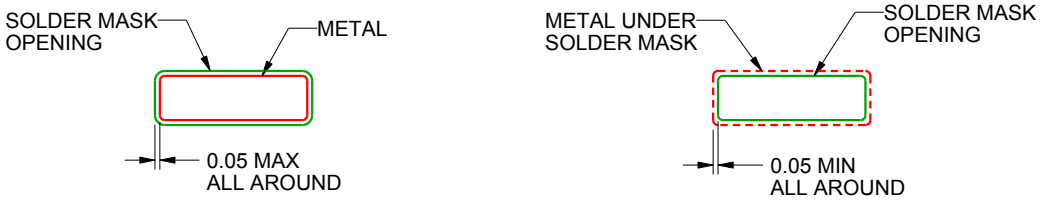


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

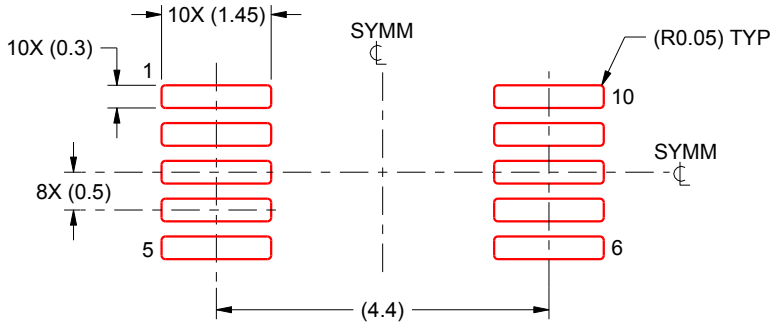


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

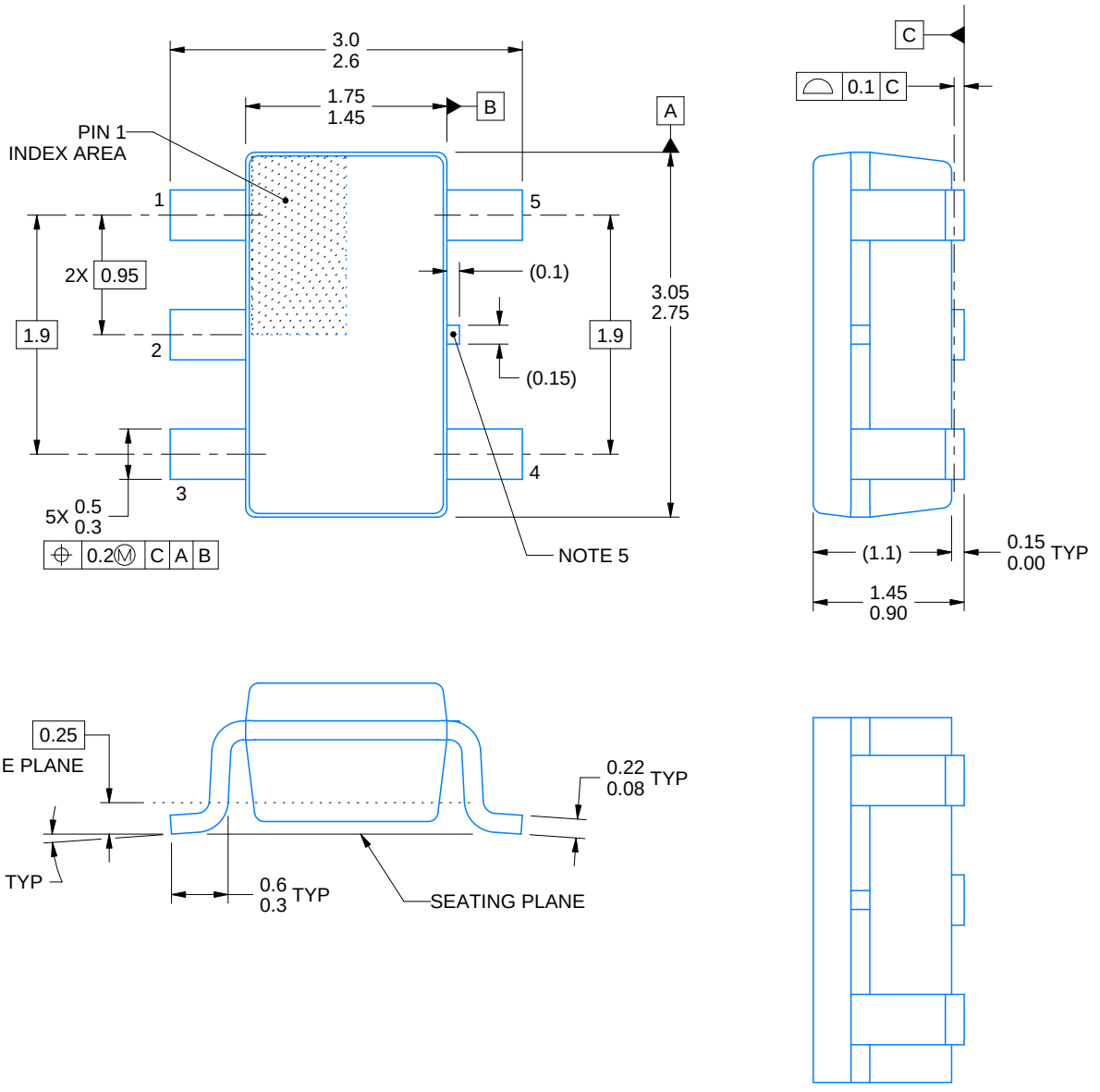
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

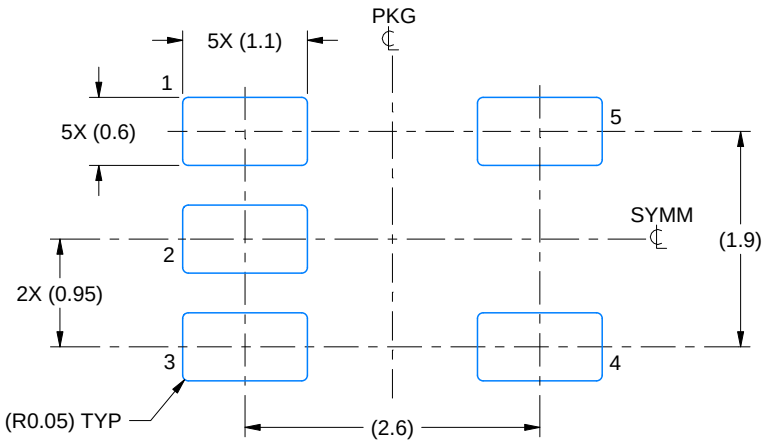


ALTERNATIVE PACKAGE SINGULATION VIEW

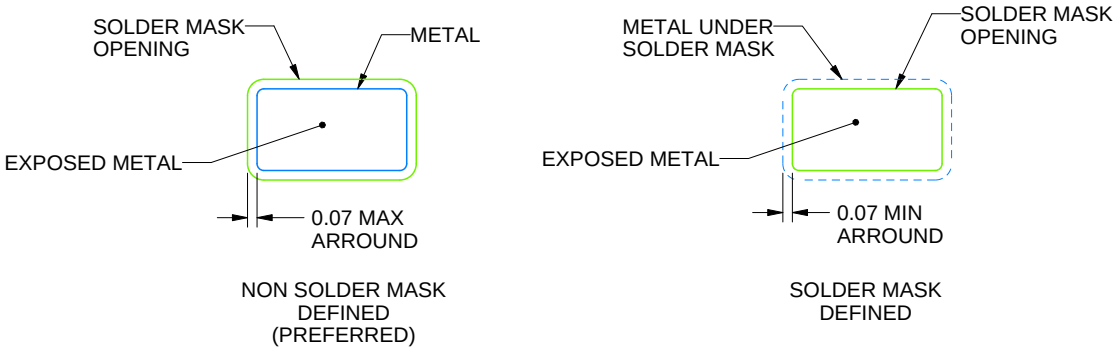
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

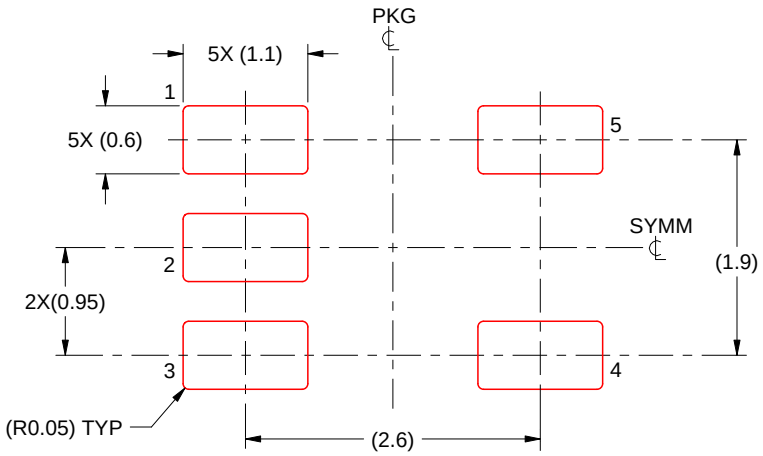


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



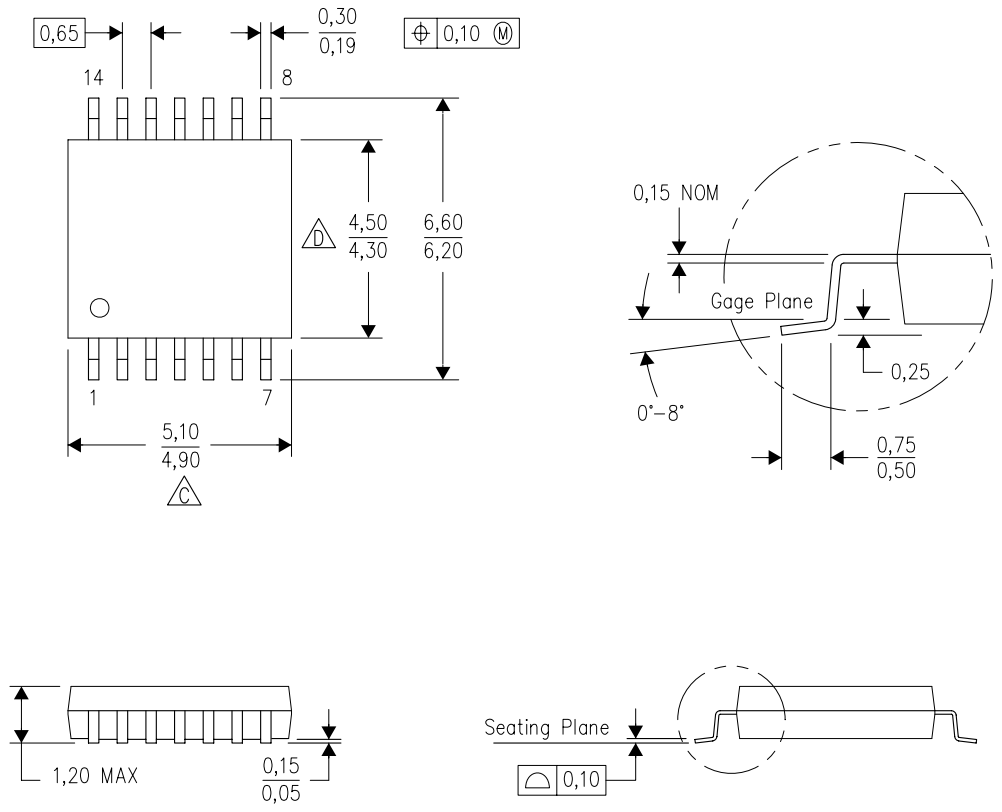
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

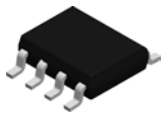
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

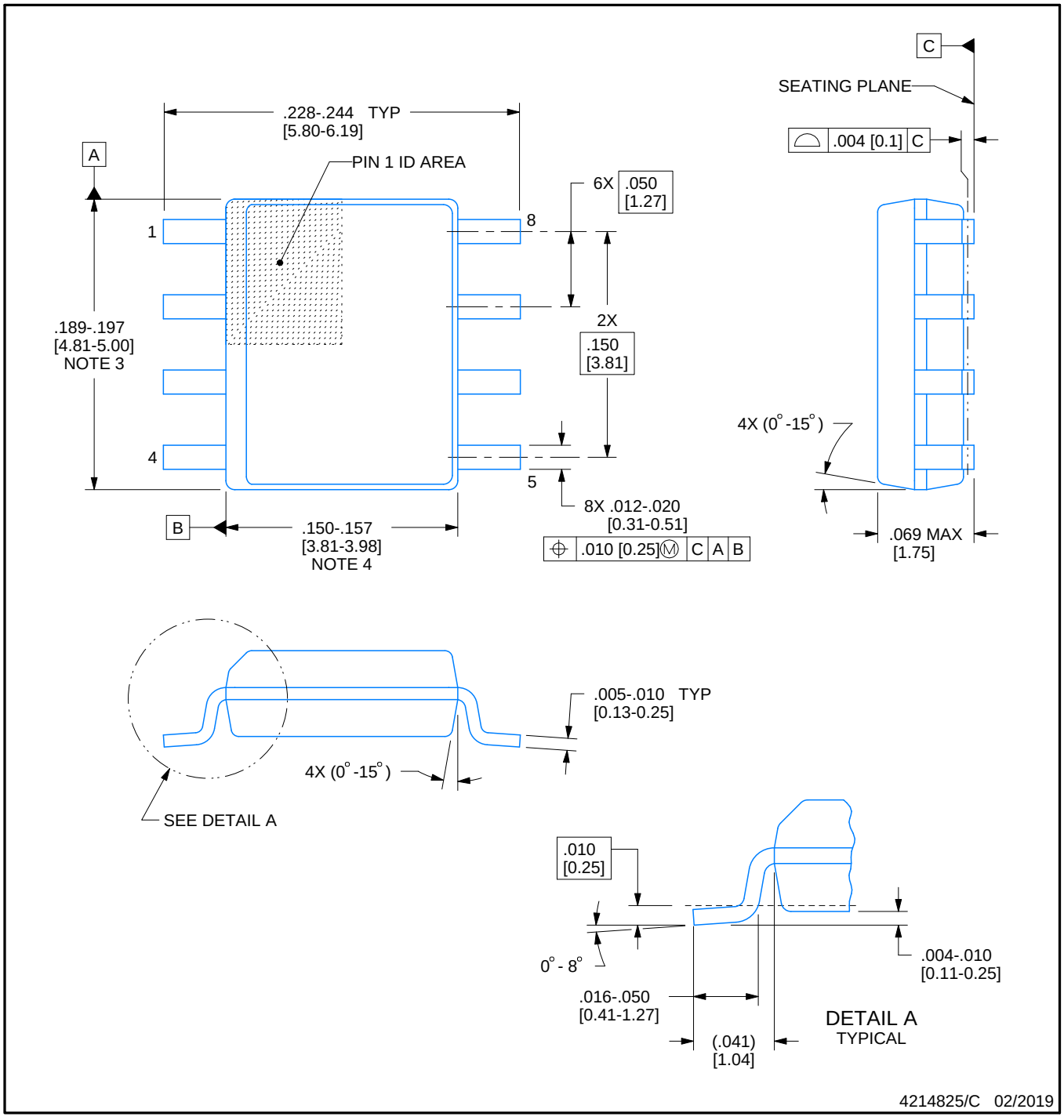


PACKAGE OUTLINE

D0008A

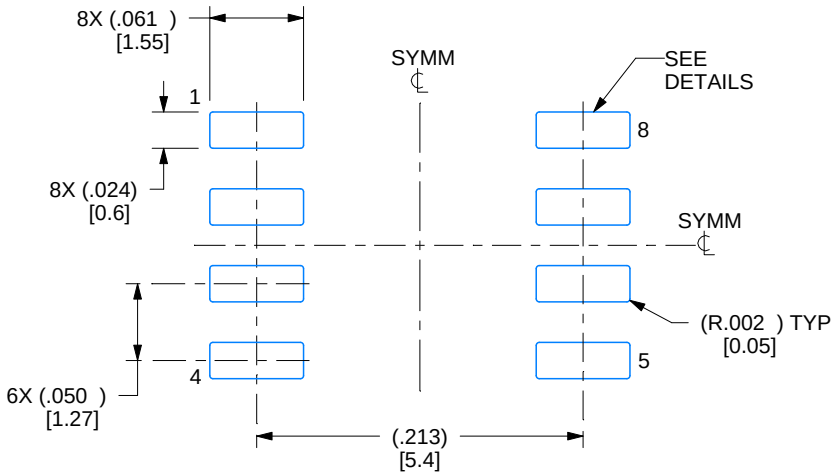
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

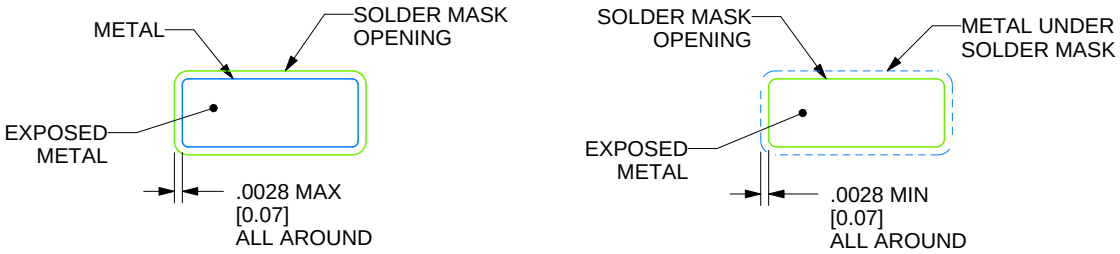


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

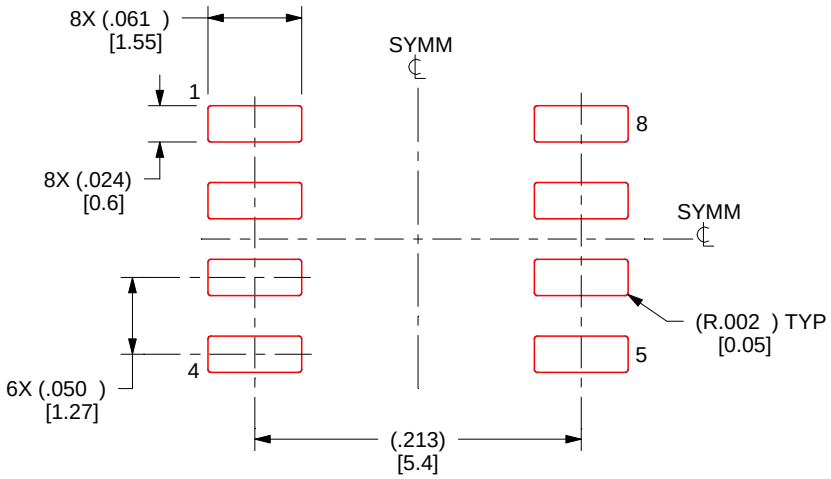
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



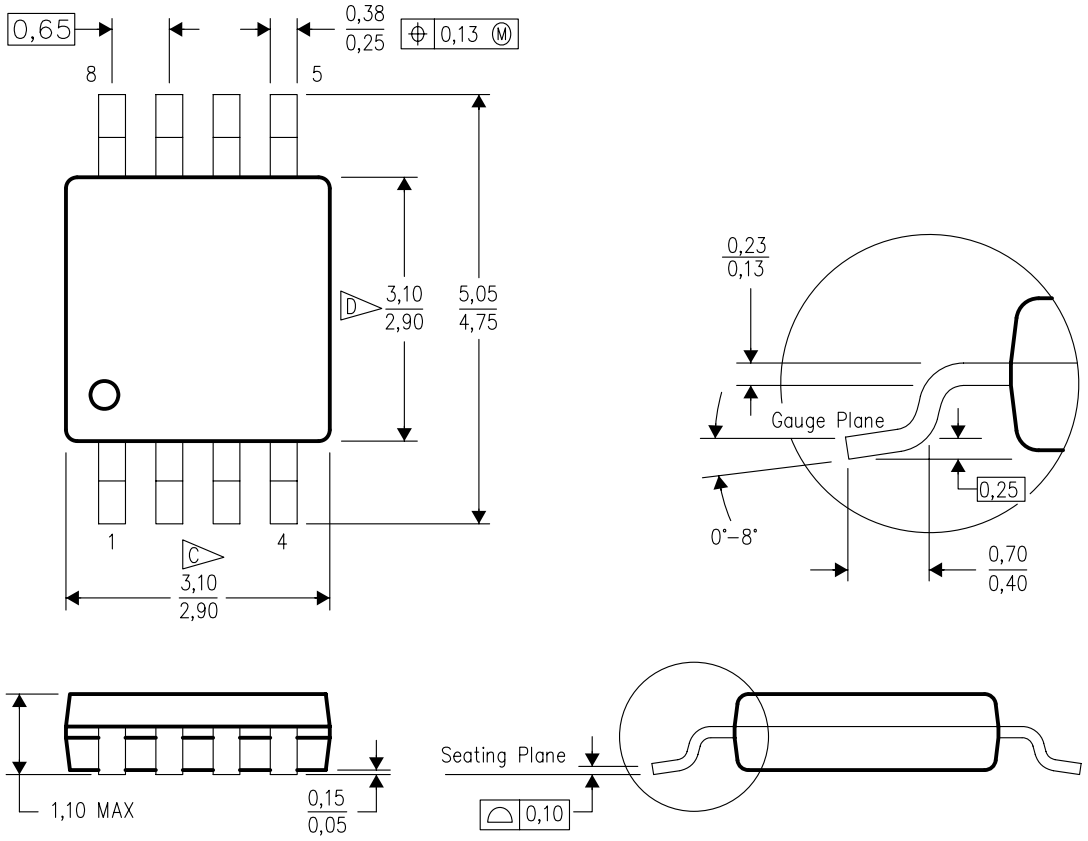
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

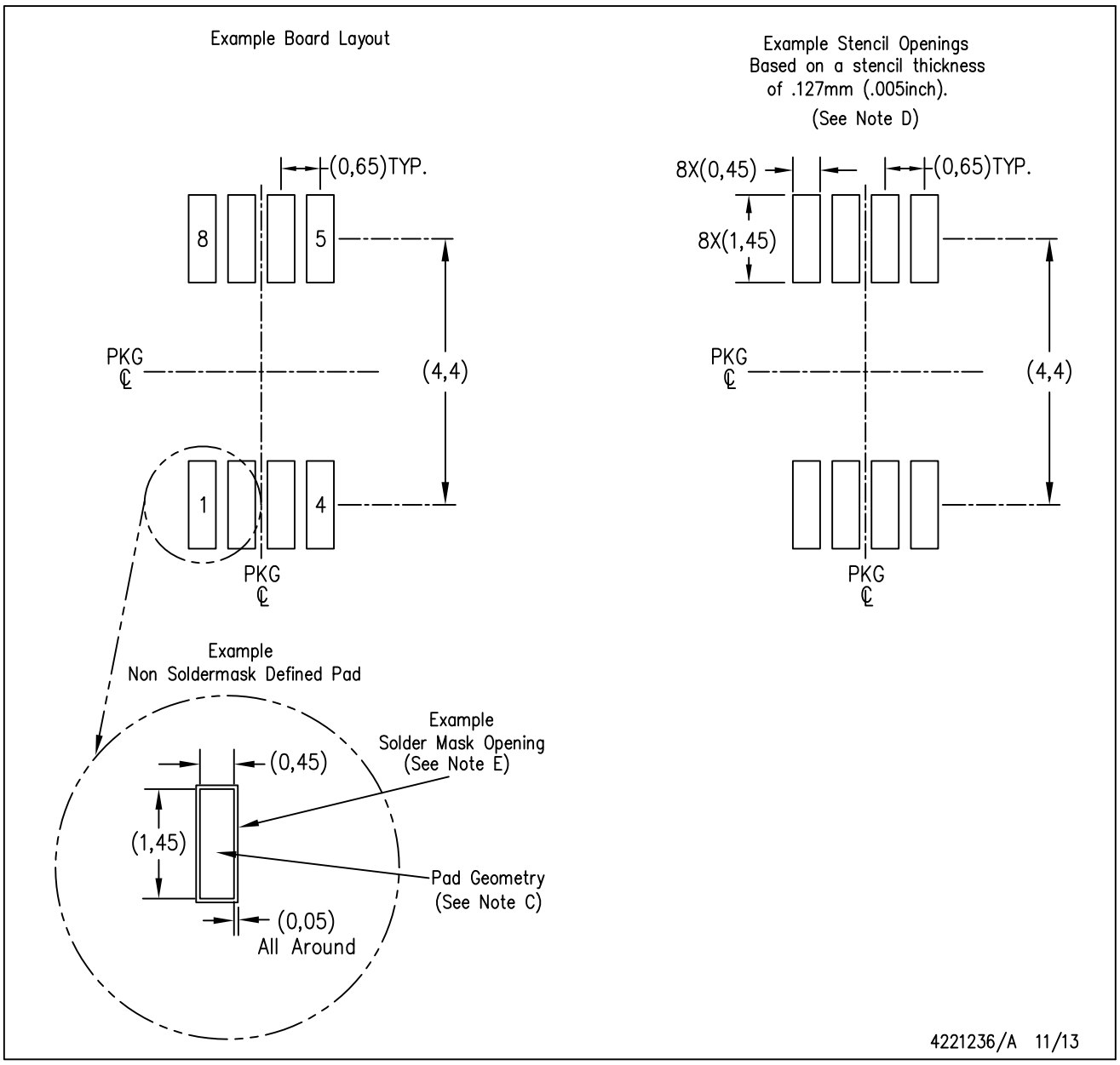
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

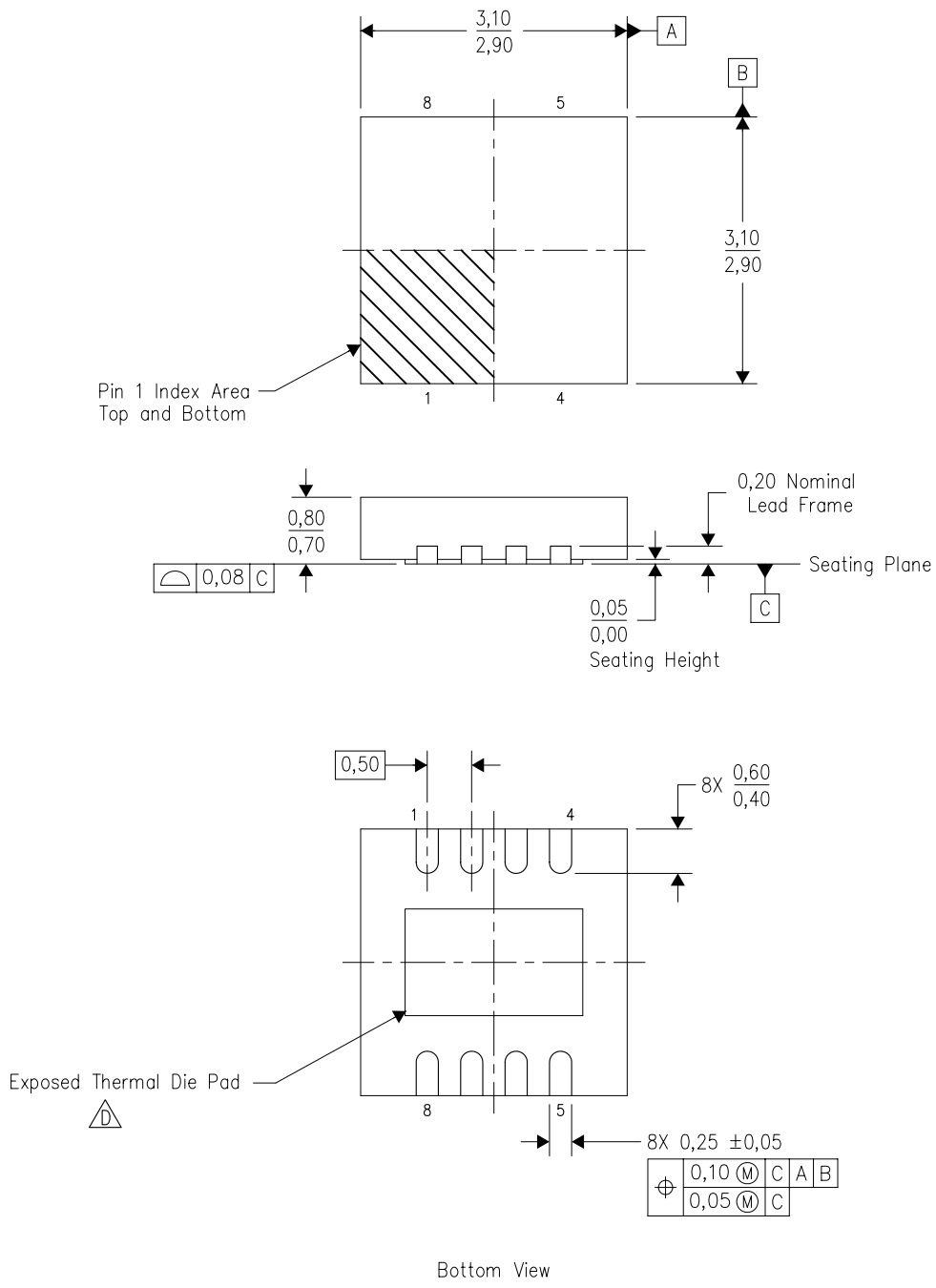
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



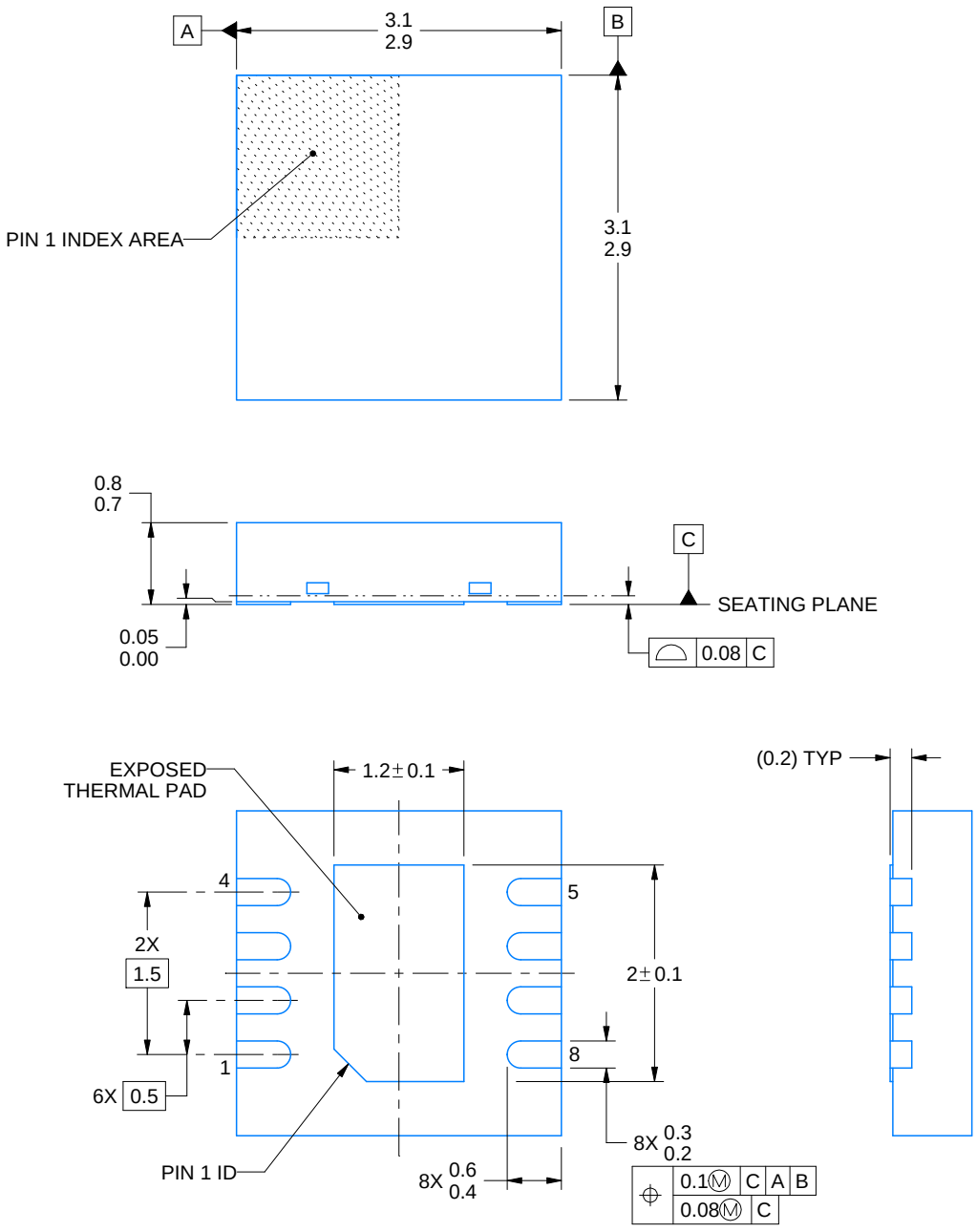
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

PACKAGE OUTLINE

DRG0008A

WSON - 0.8 mm max height

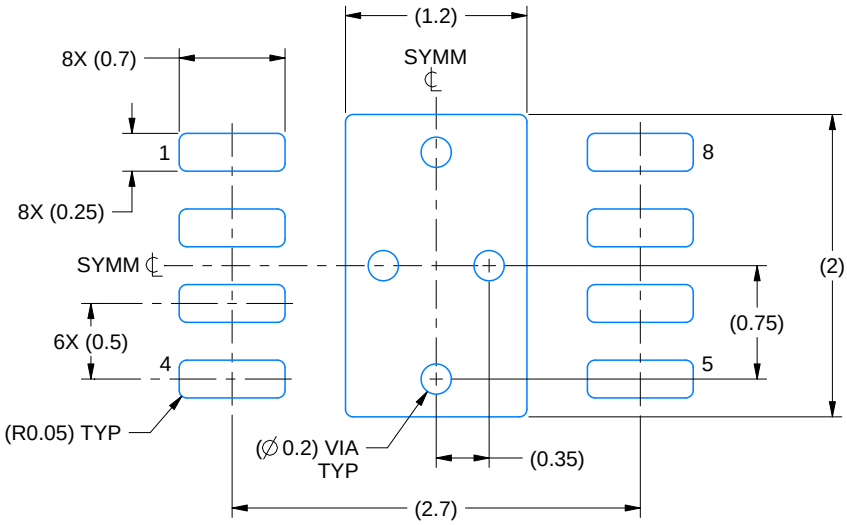
PLASTIC SMALL OUTLINE - NO LEAD



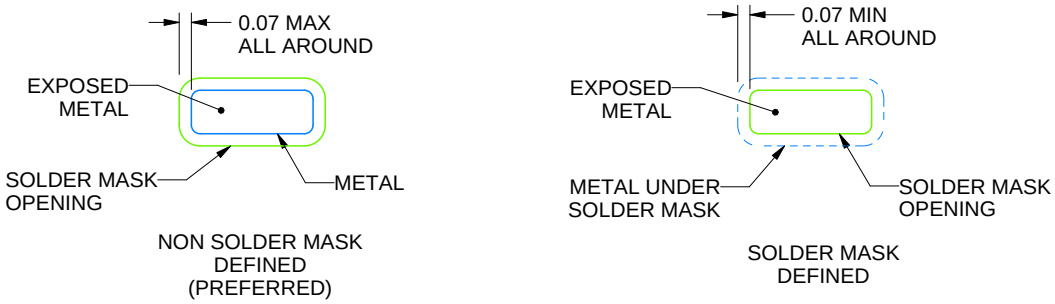
4218885/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

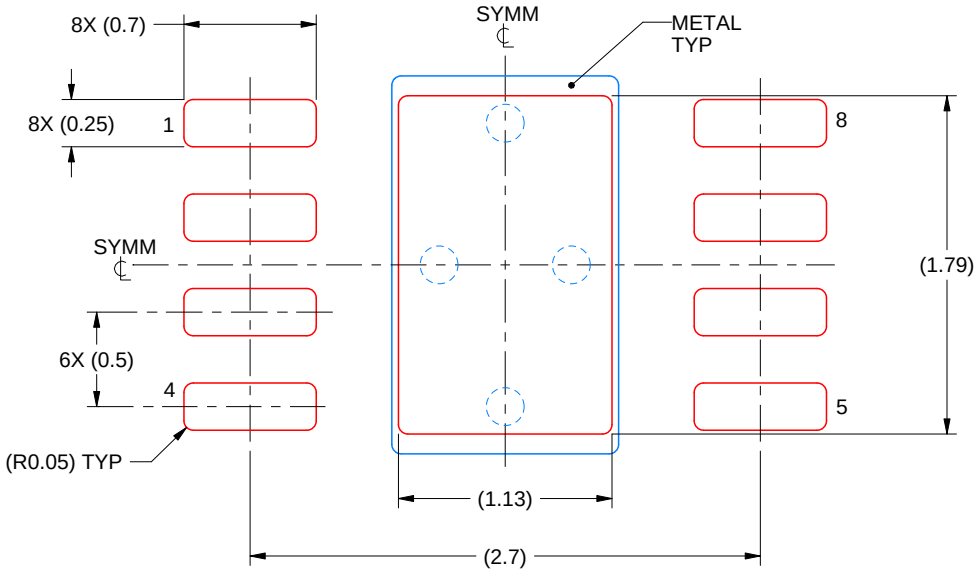


SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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