5MHz, Low-Noise, Single, Dual, Quad CMOS Operational Amplifiers

Check for Samples: OPA377, OPA2377, OPA4377

FEATURES

- **GAIN BANDWIDTH PRODUCT: 5.5MHz**
- **LOW NOISE: 7.5nV/√Hz at 1kHz**
- **OFFSET VOLTAGE: 1mV (max)**
- **INPUT BIAS CURRENT: 0.2pA**
- **RAIL-TO-RAIL OUTPUT**
- **UNITY-GAIN STABLE**
- **EMI INPUT FILTERING**
- **QUIESCENT CURRENT: 0.76mA/ch**
- **SUPPLY VOLTAGE: 2.2V to 5.5V**
- **SMALL PACKAGES: SC70, SOT23, and MSOP**

APPLICATIONS

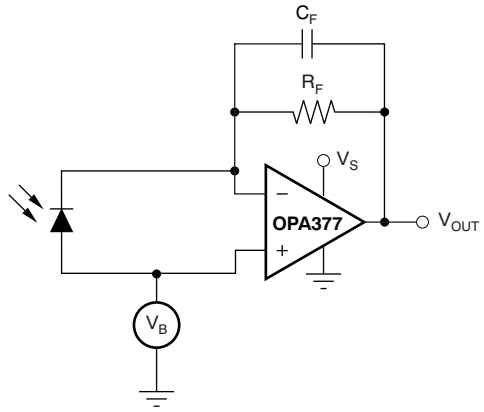
- **PHOTODIODE PREAMP**
- **PIEZOELECTRIC SENSOR PREAMP**
- **SENSOR SIGNAL CONDITIONING**
- **AUDIO EQUIPMENT**
- **ACTIVE FILTERS**

DESCRIPTION

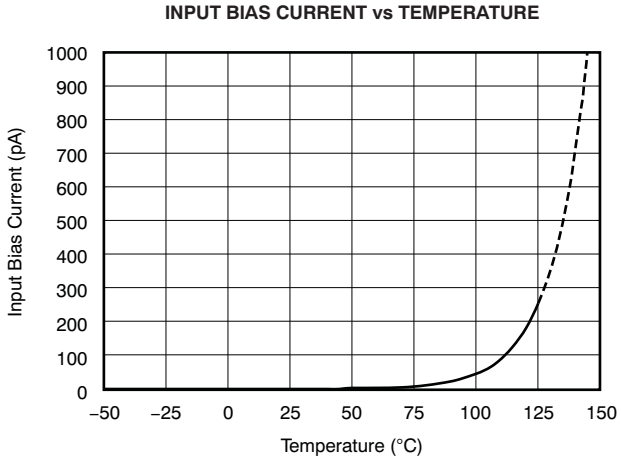
The OPA377 family of operational amplifiers are wide-bandwidth CMOS amplifiers that provide very low noise, low input bias current, and low offset voltage while operating on a low quiescent current of 0.76mA (typ).

The OPA377 op amps are optimized for low-voltage, single-supply applications. The exceptional combination of ac and dc performance make them ideal for a wide range of applications, including small signal conditioning, audio, and active filters. In addition, these parts have a wide supply range with excellent PSRR, making them attractive for applications that run directly from batteries without regulation.

The OPA377 is available in the SC70-5, SOT23-5, and SO-8 packages. The dual OPA2377 is offered in the SO-8 and MSOP-8, and the quad OPA4377 in the TSSOP-14 packages. All versions are specified for operation from –40°C to +125°C.



Photodiode Preamplifier



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATING(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA377, OPA2377, OPA4377	UNIT
Supply Voltage	V_S = (V+) – (V–)	+7	V
Signal Input Terminals	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output Short-Circuit(3)		Continuous	
Operating Temperature	T_A	–40 to +150	°C
Storage Temperature	T_A	–65 to +150	°C
Junction Temperature	T_J	+150	°C
ESD Rating	Human Body Model	4000	V
	Charged Device Model	1000	V
	Machine Model	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA377	SC70-5	DCK	OP377A
	SOT23-5	DBV	OP377A
	SO-8	D	OP377A
OPA2377	SO-8	D	O2377A
	MSOP-8	DGK	OTAQ
OPA4377	TSSOP-14	PW	O4377A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

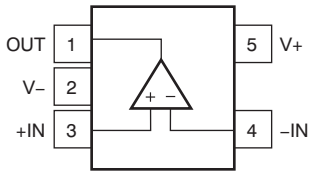
ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V

Boldface limits apply over the specified temperature range: **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

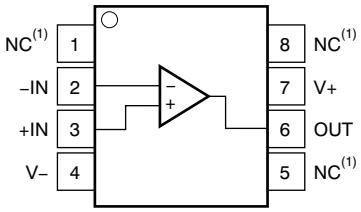
PARAMETERS		CONDITIONS	OPA377, OPA2377, OPA4377			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = +5V		0.25	1	mV
vs Temperature	**dV_{OS}/dT**	**–40°C to +125°C**		**0.32**	**2**	**µV/°C**
vs Power Supply	PSRR	V_S = +2.2V to +5.5V, V_{CM} < (V+) – 1.3V		5	28	µV/V
Over Temperature		**V_S = +2.2V to +5.5V, V_{CM} < (V+) – 1.3V**		**5**		**µV/V**
Channel Separation, dc (dual, quad)				0.5		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.2	±10	pA
Over Temperature			**See Typical Characteristics**			**pA**
Input Offset Current	I_{OS}			±0.2	±10	pA
NOISE						
Input Voltage Noise,	e_n	f = 0.1Hz to 10Hz		0.8		μV_{PP}
Input Voltage Noise Density	e_n	f = 1kHz		7.5		$nV/\sqrt{Hz}$
Input Current Noise	i_n	f = 1kHz		2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	(V–) < V_{CM} < (V+) – 1.3 V	70	90		dB
INPUT CAPACITANCE						
Differential				6.5		pF
Common-Mode				13		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	50mV < V_O < (V+) – 50mV, R_L = 10kΩ	112	134		dB
		100mV < V_O < (V+) – 100mV, R_L = 2kΩ		126		dB
FREQUENCY RESPONSE		V_S = 5.5V				
Gain-Bandwidth Product	GBW			5.5		MHz
Slew Rate	SR	G = +1		2		V/µs
Settling Time 0.1%	t_S	2V Step , G = +1		1.6		µs
Settling Time 0.01%	t_S	2V Step , G = +1		2		µs
Overload Recovery Time		V_{IN} × Gain > V_S		0.33		µs
THD + Noise	THD+N	V_O = 1V_{RMS}, G = +1, f = 1kHz, R_L = 10kΩ		0.00027		%
OUTPUT						
Voltage Output Swing from Rail		R_L = 10kΩ		10	20	mV
Over Temperature		**R_L = 10kΩ**			**40**	**mV**
Short-Circuit Current	I_{SC}			+30/–50		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			
Open-Loop Output Impedance	R_O			150		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.2		5.5	V
Quiescent Current per amplifier	I_Q	I_O = 0, V_S = +5.5V		0.76	1.05	mA
Over Temperature					**1.2**	**mA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Thermal Resistance	θ_{JA}					°C/W
SC70-5				250		°C/W
SOT23-5				200		°C/W
MSOP-8, SO-8, TSSOP-14				150		°C/W

PIN CONFIGURATIONS

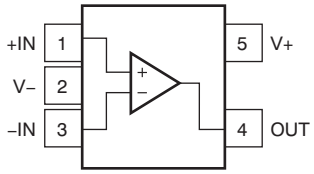
OPA377
SOT23-5
(TOP VIEW)



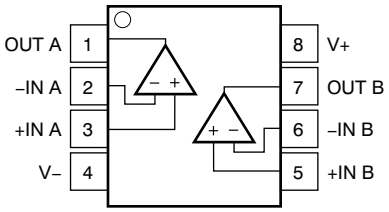
OPA377
SO-8
(TOP VIEW)



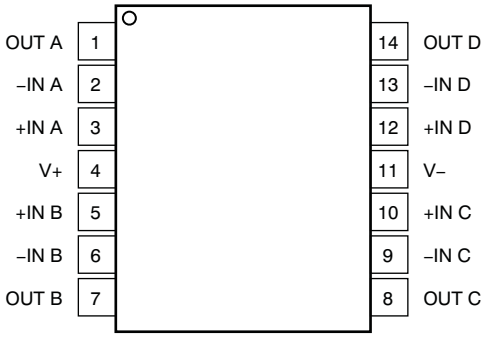
OPA377
SC70-5
(TOP VIEW)



OPA2377
SO-8, MSOP-8
(TOP VIEW)



OPA4377
TSSOP-14
(TOP VIEW)



(1) NC denotes no internal connection.

(2) Connect thermal die to V–.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and V_{OUT} = $V_S/2$, unless otherwise noted.

OPEN-LOOP GAIN/PHASE vs FREQUENCY

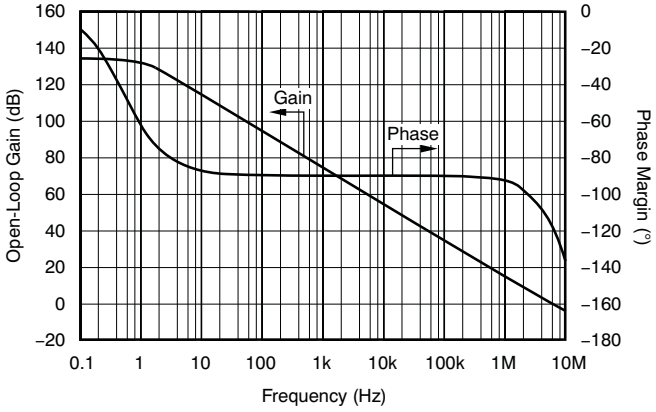


Figure 1.

POWER-SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY

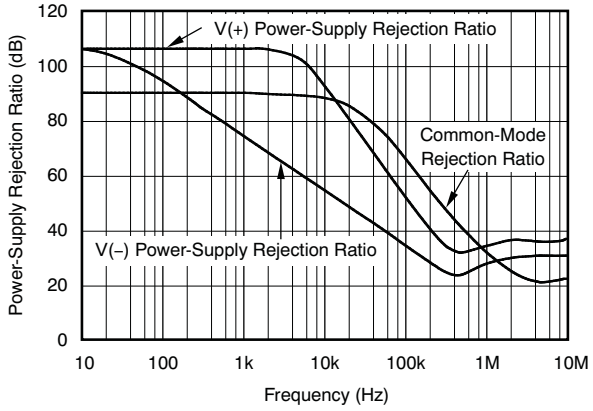


Figure 2.

OPEN-LOOP GAIN AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE

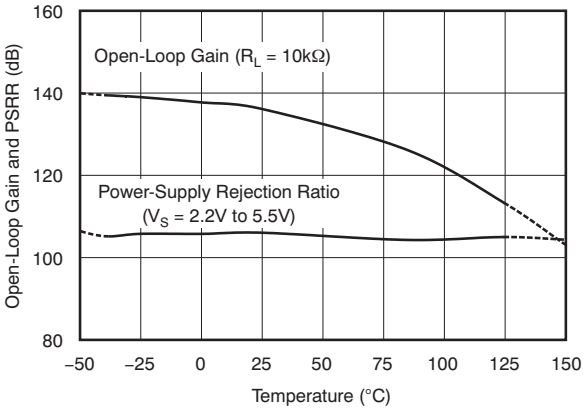


Figure 3.

0.1Hz to 10Hz INPUT VOLTAGE NOISE

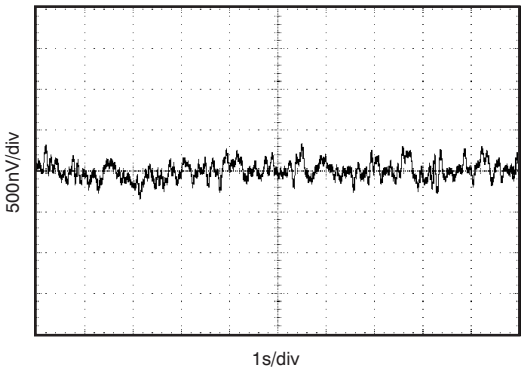


Figure 4.

INPUT VOLTAGE NOISE SPECTRAL DENSITY

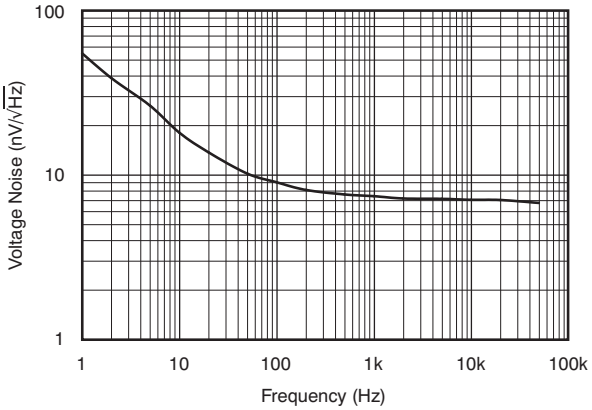


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

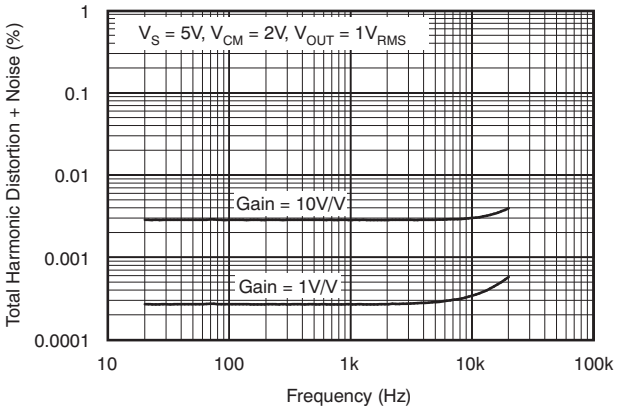


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and V_{OUT} = $V_S/2$, unless otherwise noted.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

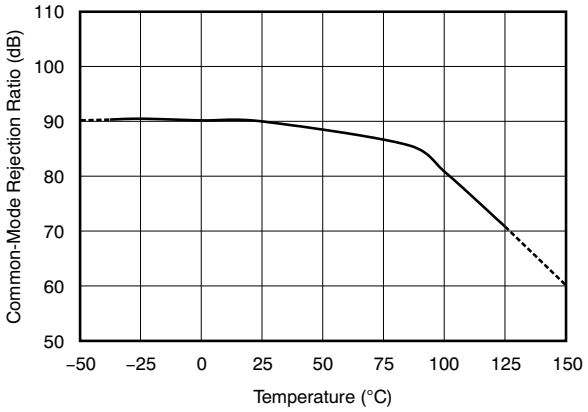


Figure 7.

QUIESCENT CURRENT vs TEMPERATURE

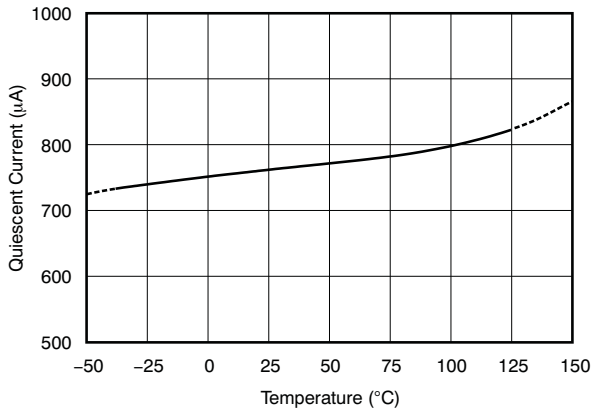


Figure 8.

QUIESCENT AND SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE

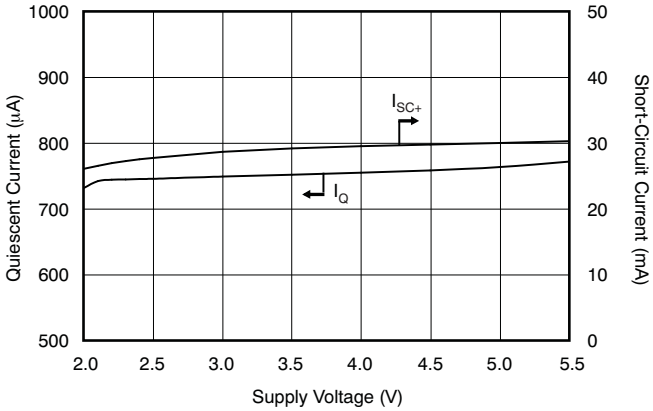


Figure 9.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

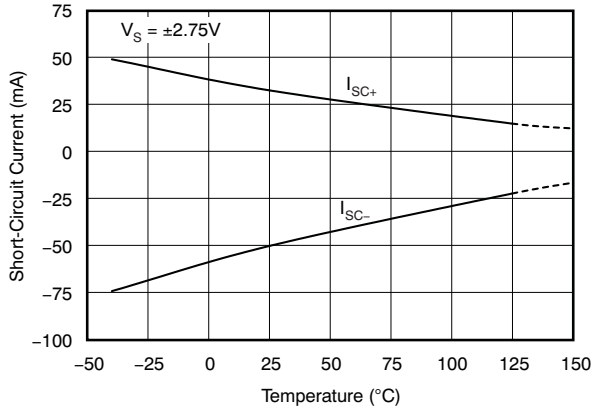


Figure 10.

INPUT BIAS CURRENT vs TEMPERATURE

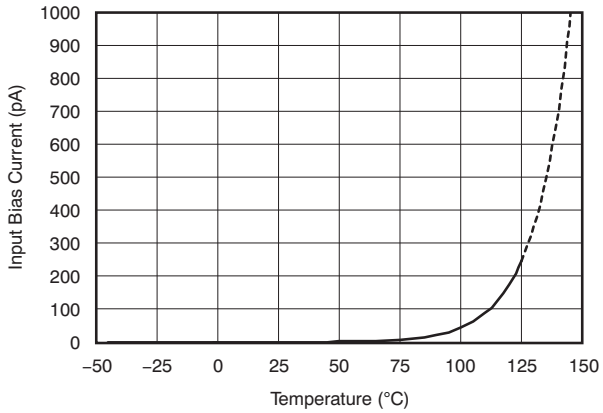


Figure 11.

OUTPUT VOLTAGE vs OUTPUT CURRENT

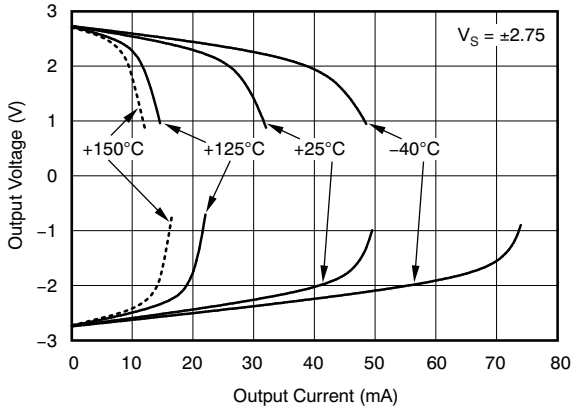


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and V_{OUT} = $V_S/2$, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

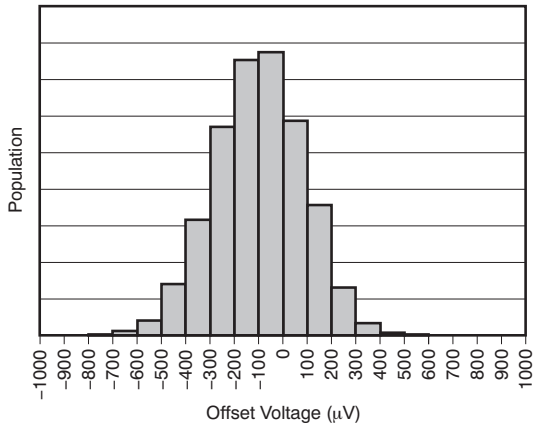


Figure 13.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

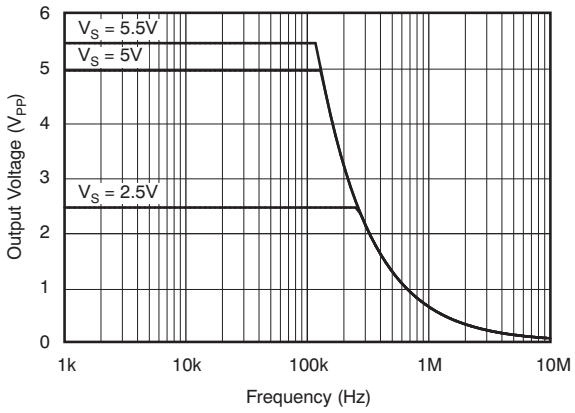


Figure 14.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

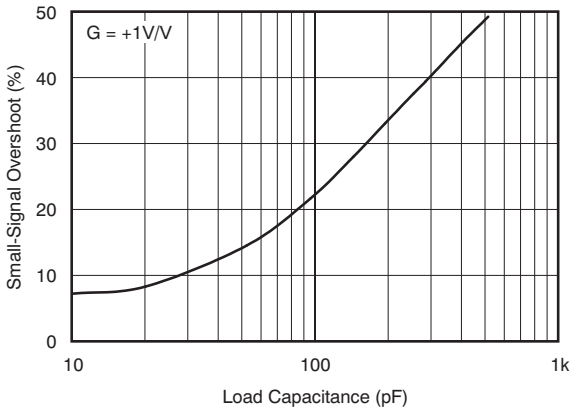


Figure 15.

SMALL-SIGNAL PULSE RESPONSE

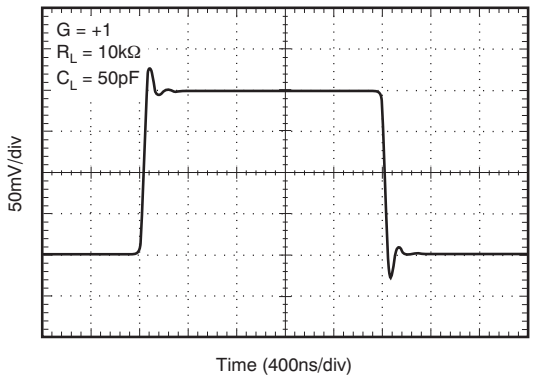


Figure 16.

LARGE-SIGNAL PULSE RESPONSE

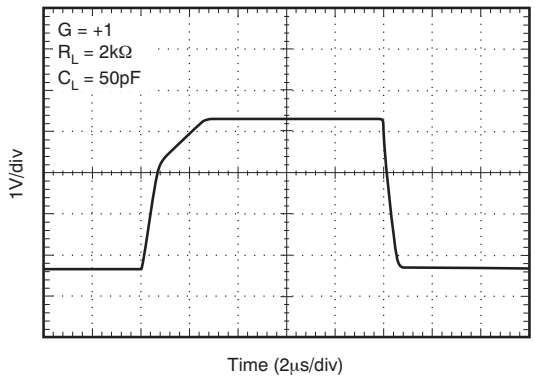


Figure 17.

SETTLING TIME vs CLOSED-LOOP GAIN

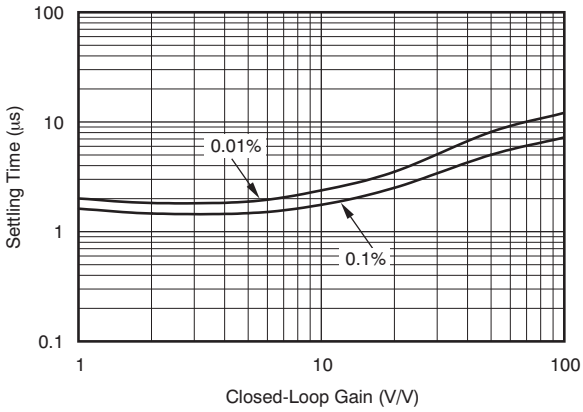


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to $V_S/2$, V_{CM} = $V_S/2$, and V_{OUT} = $V_S/2$, unless otherwise noted.

CHANNEL SEPARATION vs FREQUENCY

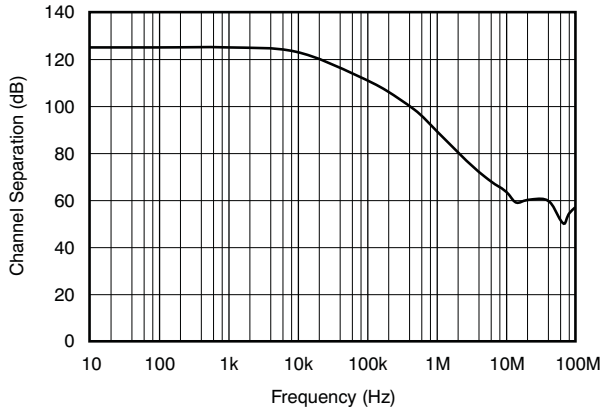


Figure 19.

OPEN-LOOP OUTPUT RESISTANCE vs FREQUENCY

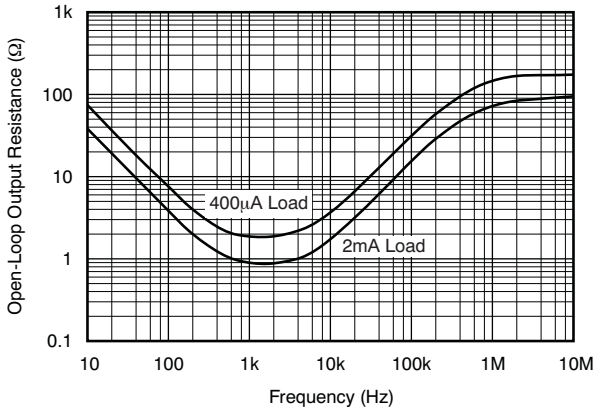


Figure 20.

APPLICATION INFORMATION

OPERATING CHARACTERISTICS

The OPA377 family of amplifiers has parameters that are fully specified from 2.2V to 5.5V (±1.1V to ±2.75V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are required. Low-loss, 0.1μF bypass capacitors must be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

BASIC AMPLIFIER CONFIGURATIONS

The OPA377 family is unity-gain stable. It does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 21. The OPA377 is configured as a basic inverting amplifier with a gain of –10V/V. This single-supply connection has an output centered on the common-mode voltage, V_{CM}. For the circuit shown, this voltage is 2.5V, but may be any value within the common-mode input voltage range.

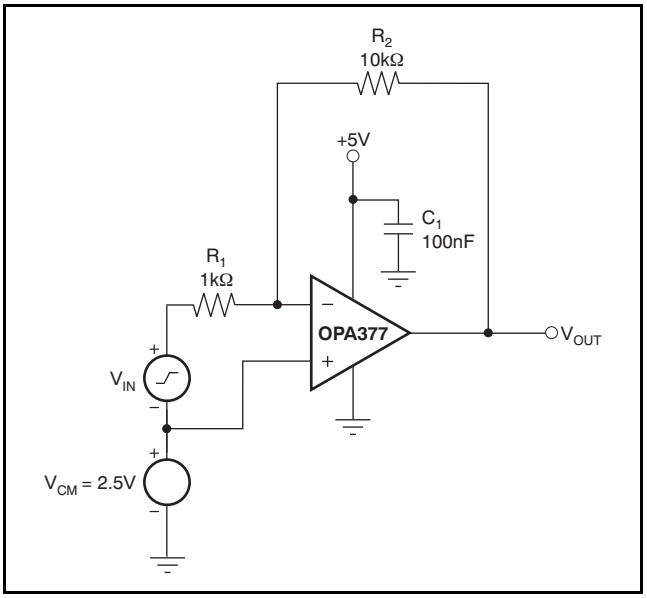


Figure 21. Basic Single-Supply Connection

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA377 series extends 100mV beyond the supply rails. The offset voltage of the amplifier is low, from approximately (V–) to (V+) – 1V, as shown in Figure 22. The offset voltage increases as common-mode voltage exceeds (V+) –1V. Common-mode rejection is specified from (V–) to (V+) – 1.3V.

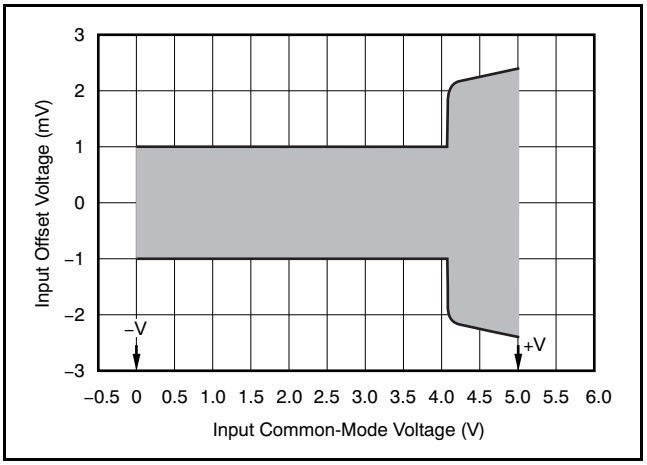


Figure 22. Offset and Common-Mode Voltage

INPUT AND ESD PROTECTION

The OPA377 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the Absolute Maximum Ratings. Figure 23 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

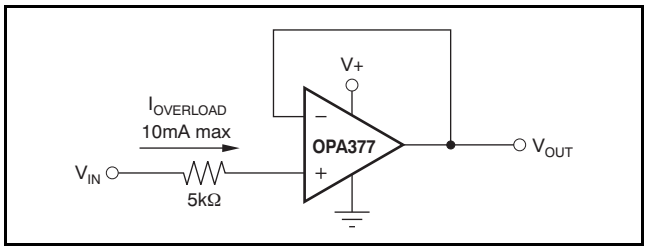


Figure 23. Input Current Protection

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from the nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA377 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 75MHz (–3dB), with a roll-off of 20dB per decade.

CAPACITIVE LOAD AND STABILITY

The OPA377 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx377 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (+1V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

The OPAx377 in a unity-gain configuration can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic plot, *Small-Signal Overshoot vs Capacitive Load*. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10Ω to 20Ω) resistor, R_S, in series with the output, as shown in Figure 24. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L, and is generally negligible at low output current levels.

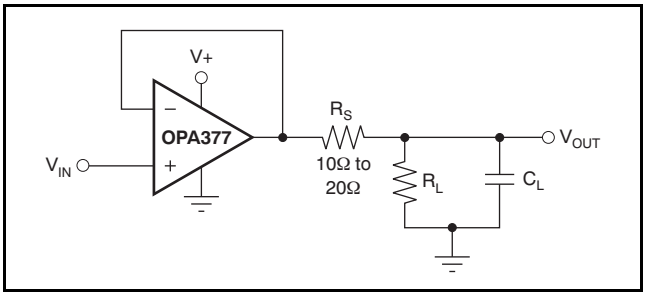


Figure 24. Improving Capacitive Load Drive

ACTIVE FILTERING

The OPA377 series is well-suited for filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 25 shows a 50kHz, 2nd-order, low-pass filter. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an analog-to-digital converter (ADC).

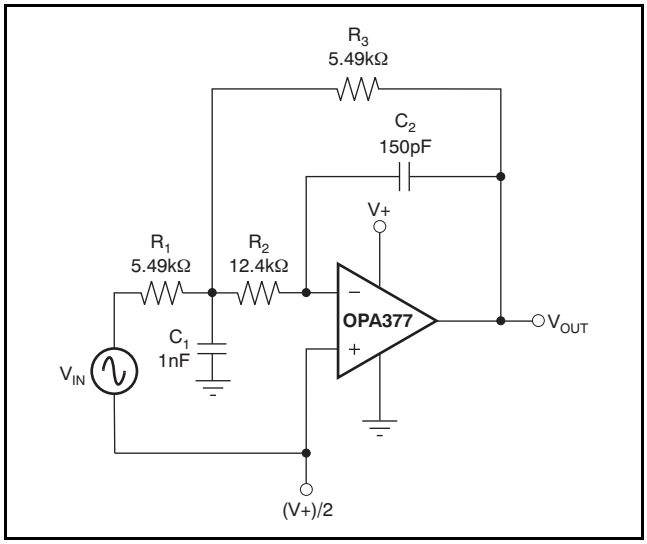
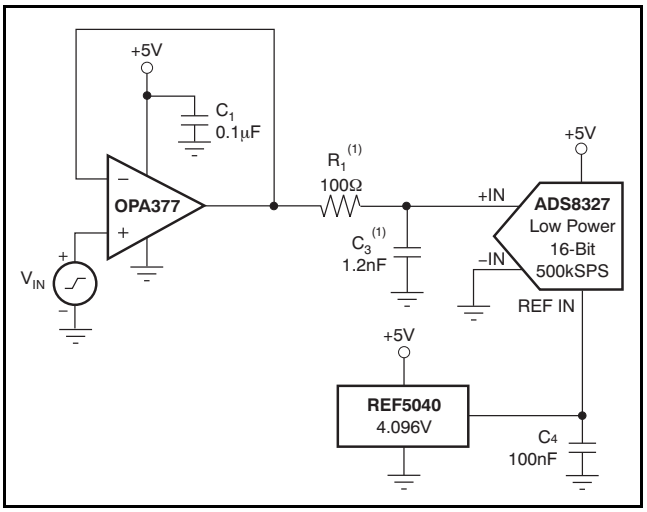


Figure 25. Second-Order Butterworth 50kHz Low-Pass Filter

DRIVING AN ANALOG-TO-DIGITAL CONVERTER

The low noise and wide gain bandwidth of the OPA377 family make it an ideal driver for ADCs. Figure 26 illustrates the OPA377 driving an ADS8327, 16-bit, 250kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer.



(1) Suggested value; may require adjustment based on specific application.

(2) Initial calibration recommended.

Figure 26. Driving an ADS8327(2)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2010) to Revision B **Page**

- Changed document status to production data 1
- Deleted cross-reference to note 2 and shading from DCK package in Package Information table 2
- Updated Figure 22 9

Changes from Original (February 2010) to Revision A **Page**

- Deleted DFN from list of packages in final *Features* bullet 1
- Deleted DFN package from *Description* section 1
- Updated *Input Bias Current vs Temperature* plot 1
- Deleted cross-reference to note 2 and shading from all packages except SC70-5 in Package Information table 2
- Deleted DFN-8 package from Package Information table 2
- Deleted Temperature Range, *DFN-8* parameter from Electrical Characteristics table 3
- Deleted DFN-8 pin configuration 4
- Updated Figure 11 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2377AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2377A	Samples
OPA2377AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OTAQ	Samples
OPA2377AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OTAQ	Samples
OPA2377AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2377A	Samples
OPA377AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP377A	Samples
OPA377AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PAG	Samples
OPA377AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PAG	Samples
OPA377AIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PAF	Samples
OPA377AIDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PAF	Samples
OPA377AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP377A	Samples
OPA4377AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP4377A	Samples
OPA4377AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP4377A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2377, OPA377, OPA4377 :

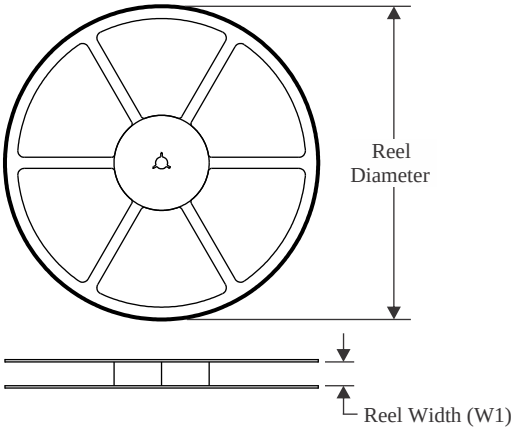
- Automotive : OPA2377-Q1, OPA377-Q1, OPA4377-Q1

NOTE: Qualified Version Definitions:

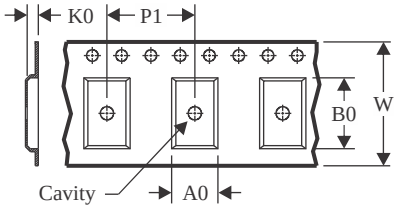
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

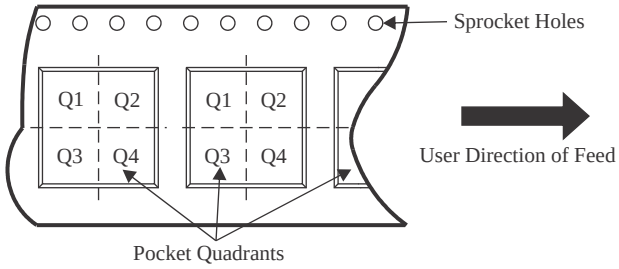


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

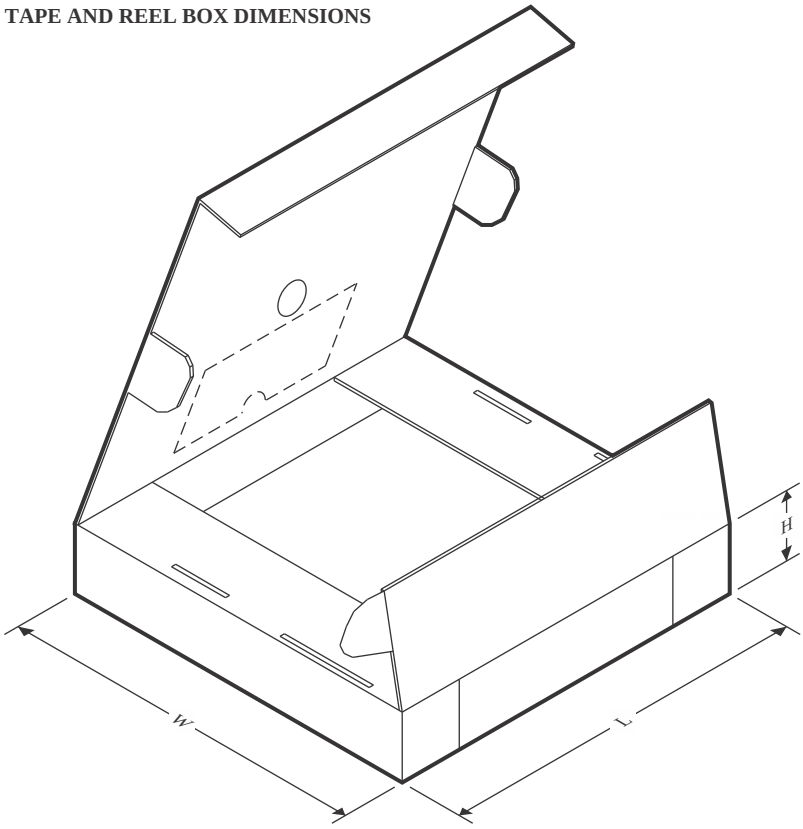
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2377AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2377AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2377AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA377AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA377AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA377AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA377AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA377AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA377AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA377AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4377AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

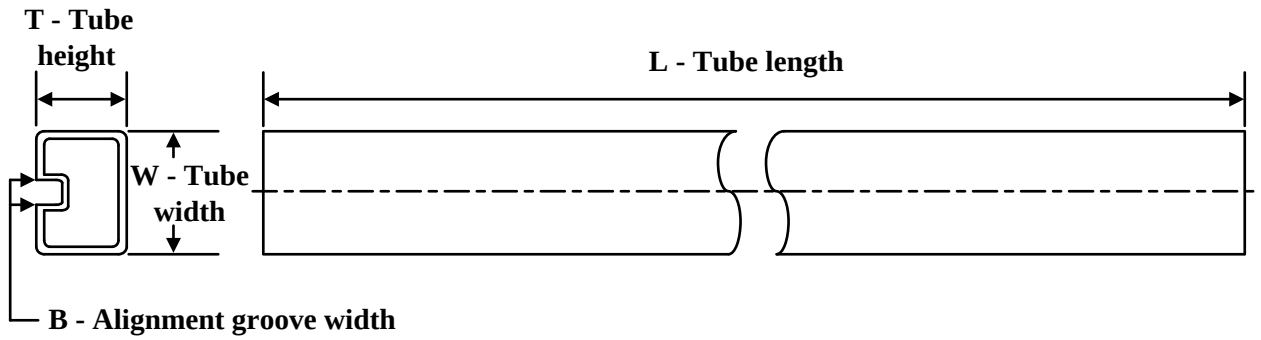
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2377AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2377AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2377AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA377AIDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA377AIDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA377AIDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA377AIDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA377AIDCKR	SC70	DCK	5	3000	213.0	191.0	35.0
OPA377AIDCKT	SC70	DCK	5	250	213.0	191.0	35.0
OPA377AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4377AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

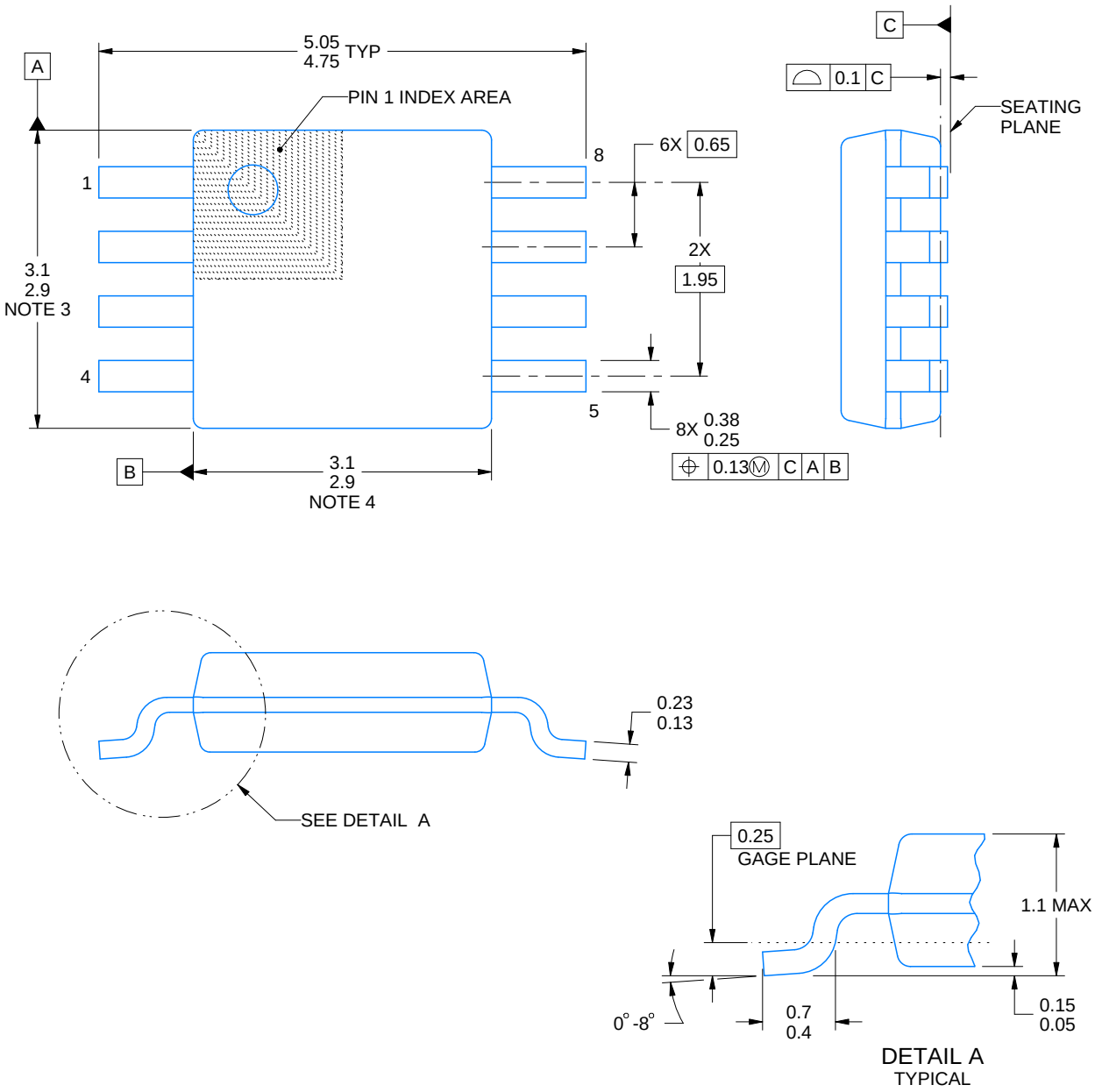
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2377AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA377AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4377AIPW	PW	TSSOP	14	90	508	8.5	3250	2.8

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

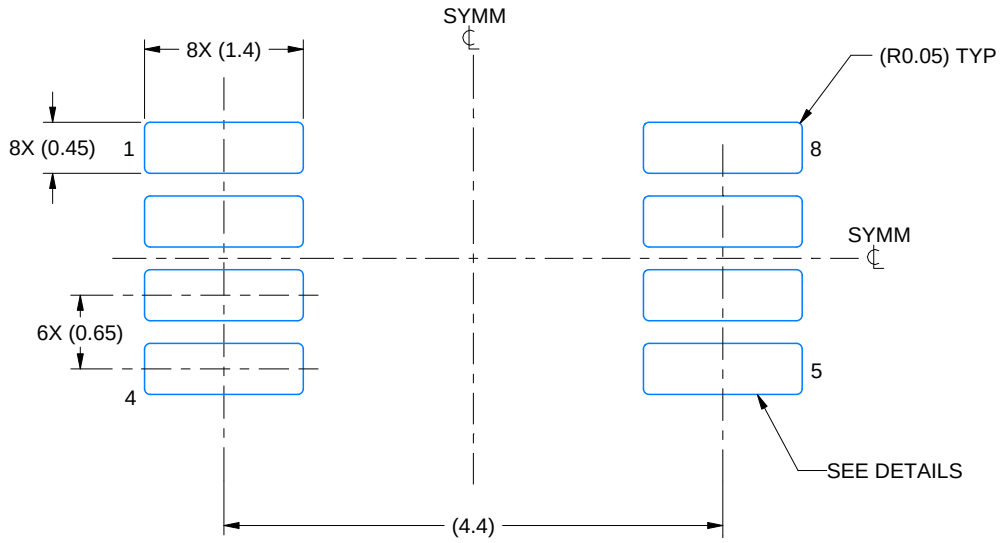
SMALL OUTLINE PACKAGE



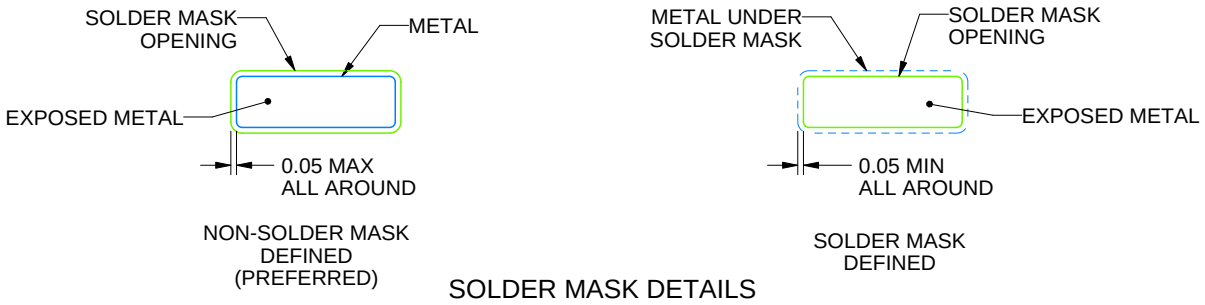
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

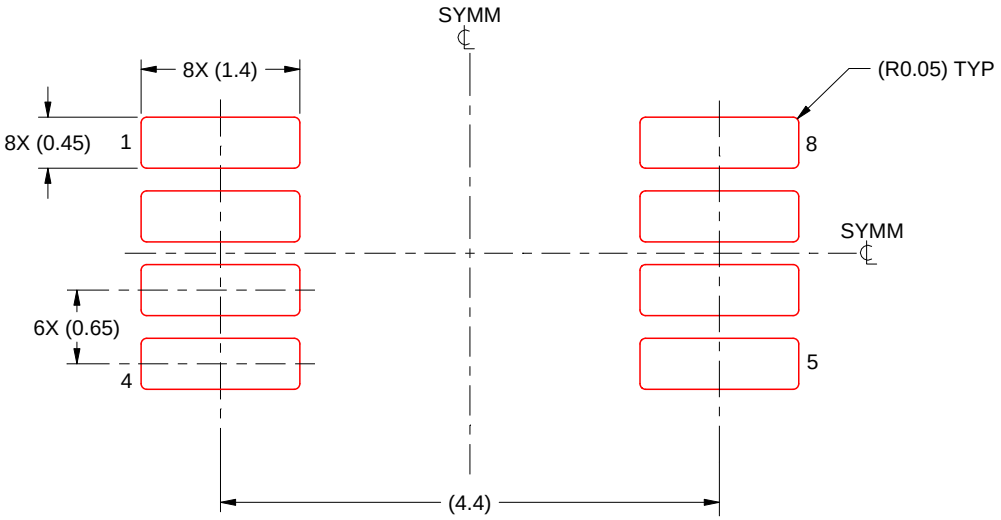


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

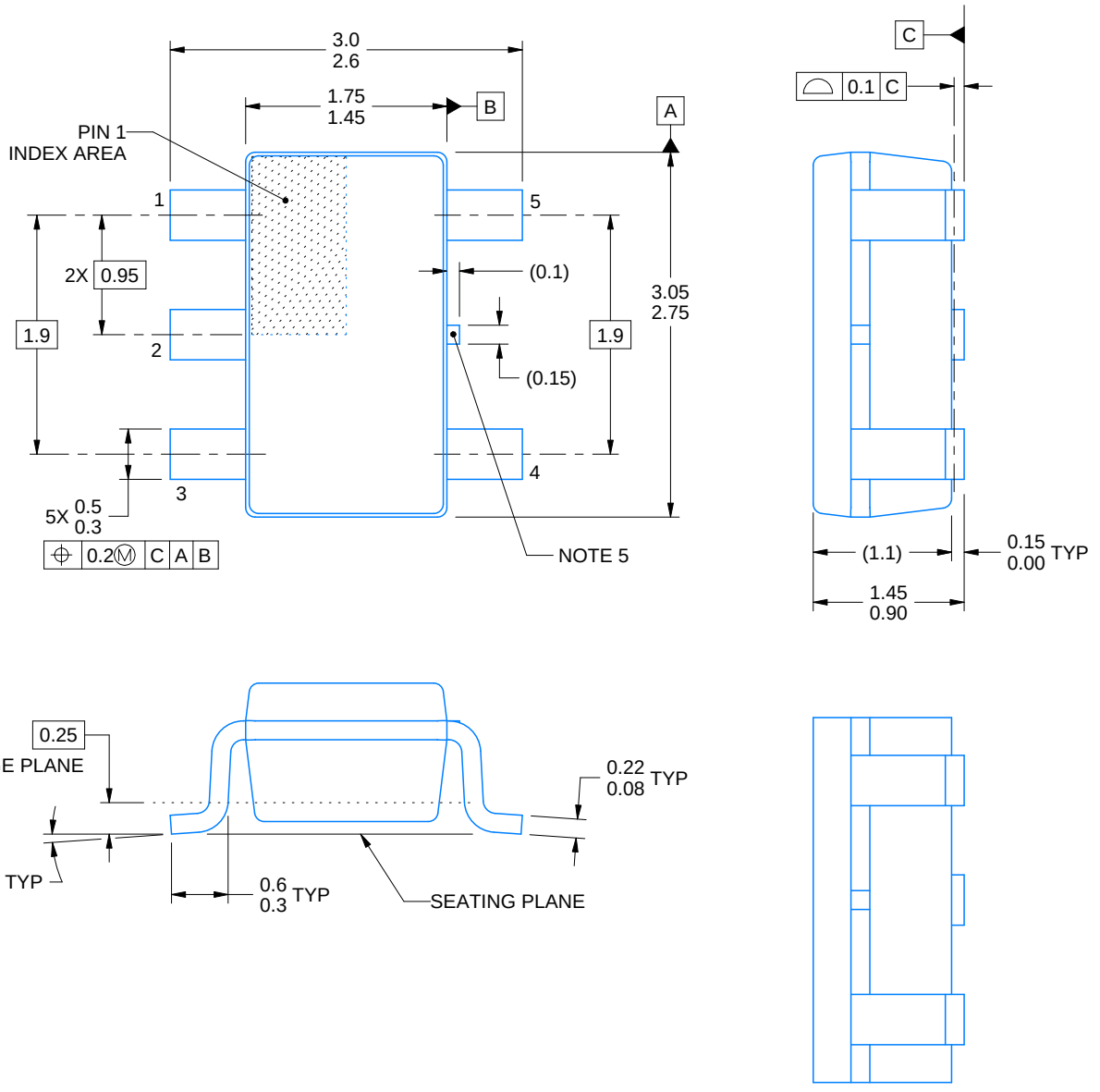
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

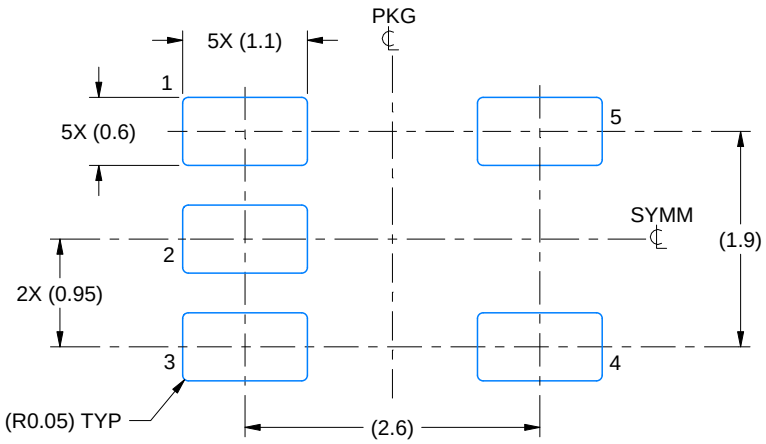


ALTERNATIVE PACKAGE SINGULATION VIEW

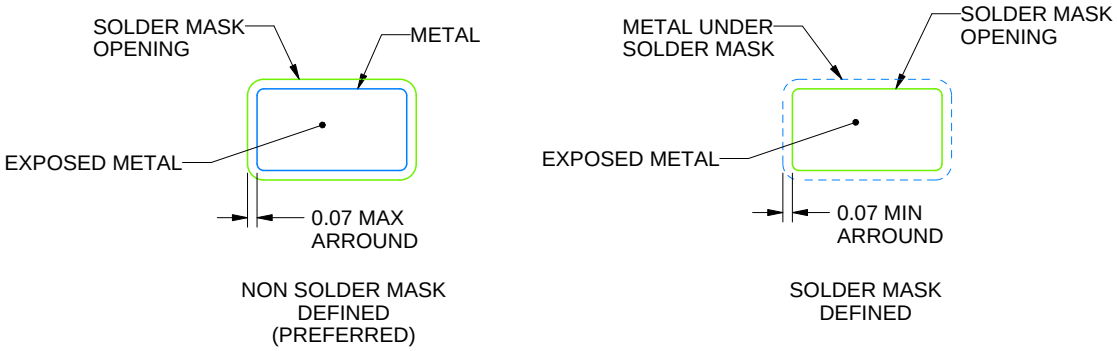
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

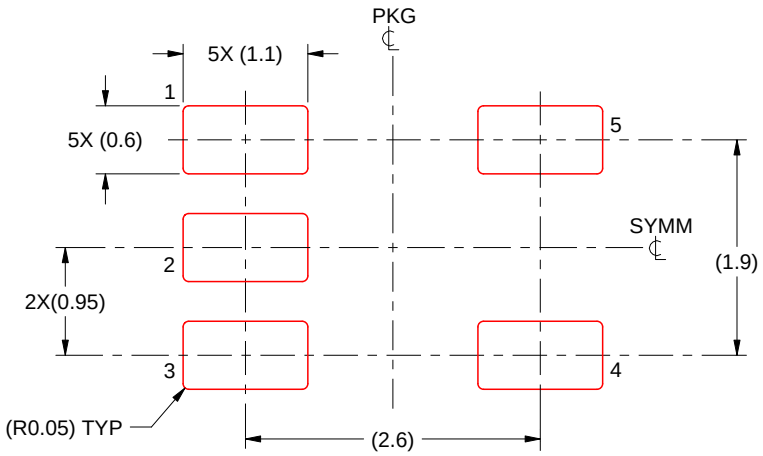


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

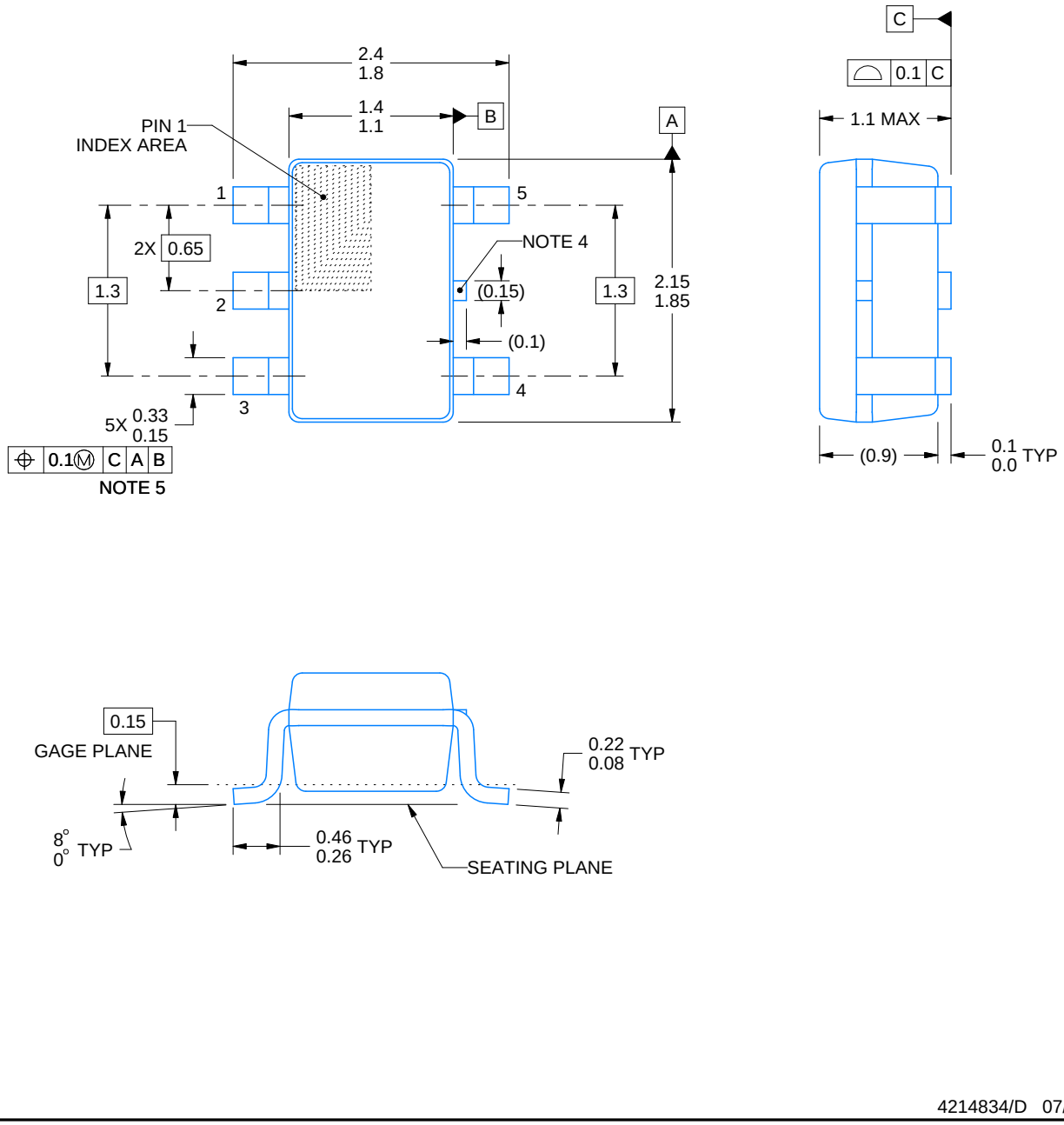
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

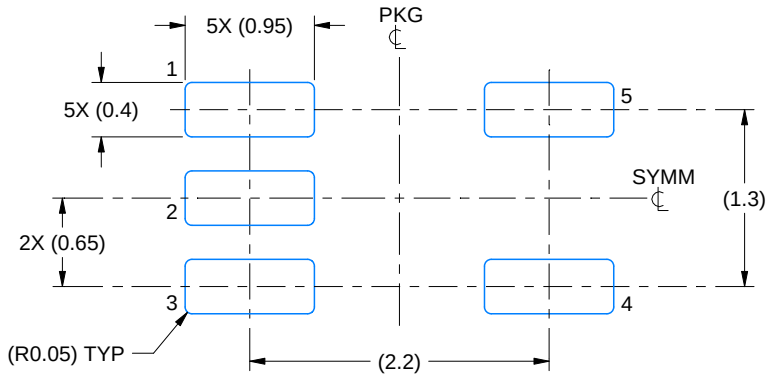
SMALL OUTLINE TRANSISTOR



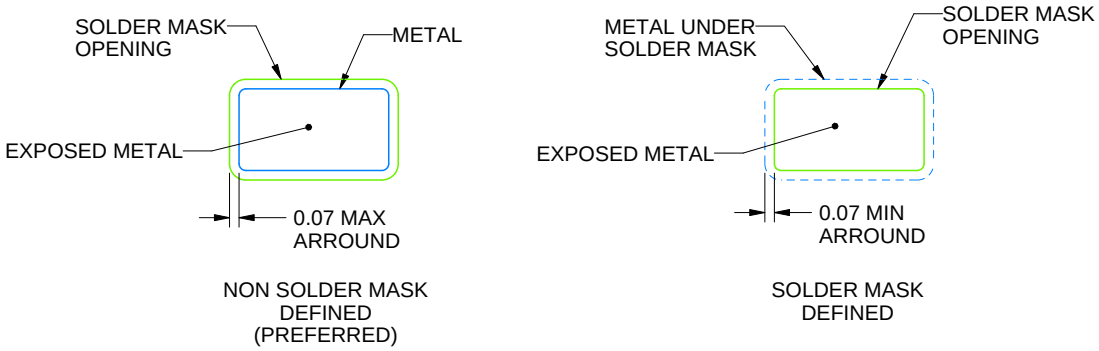
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

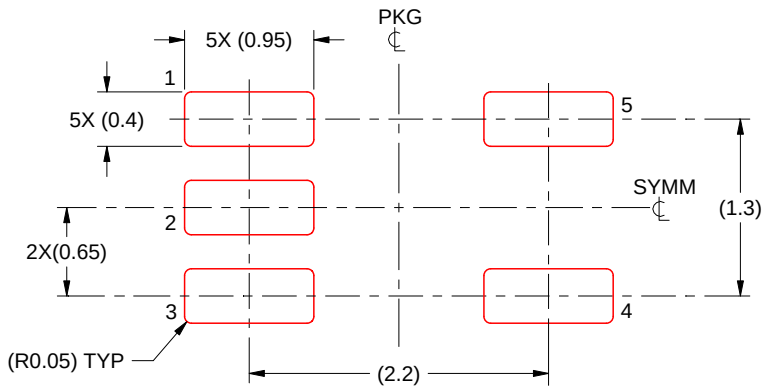


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



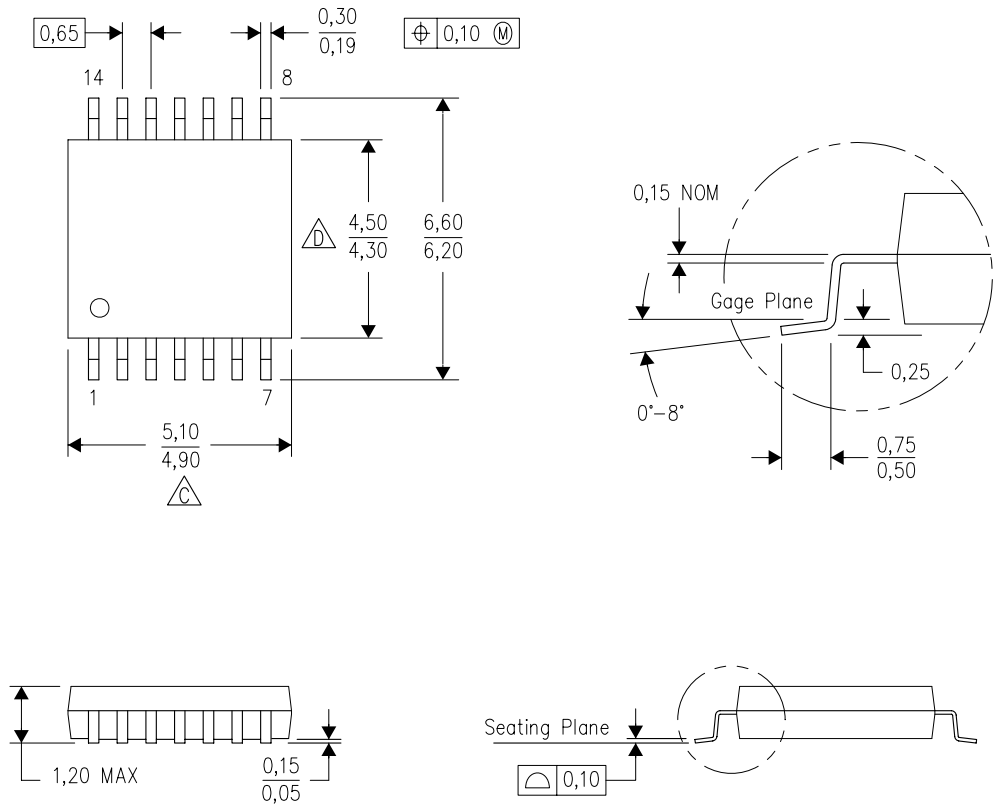
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

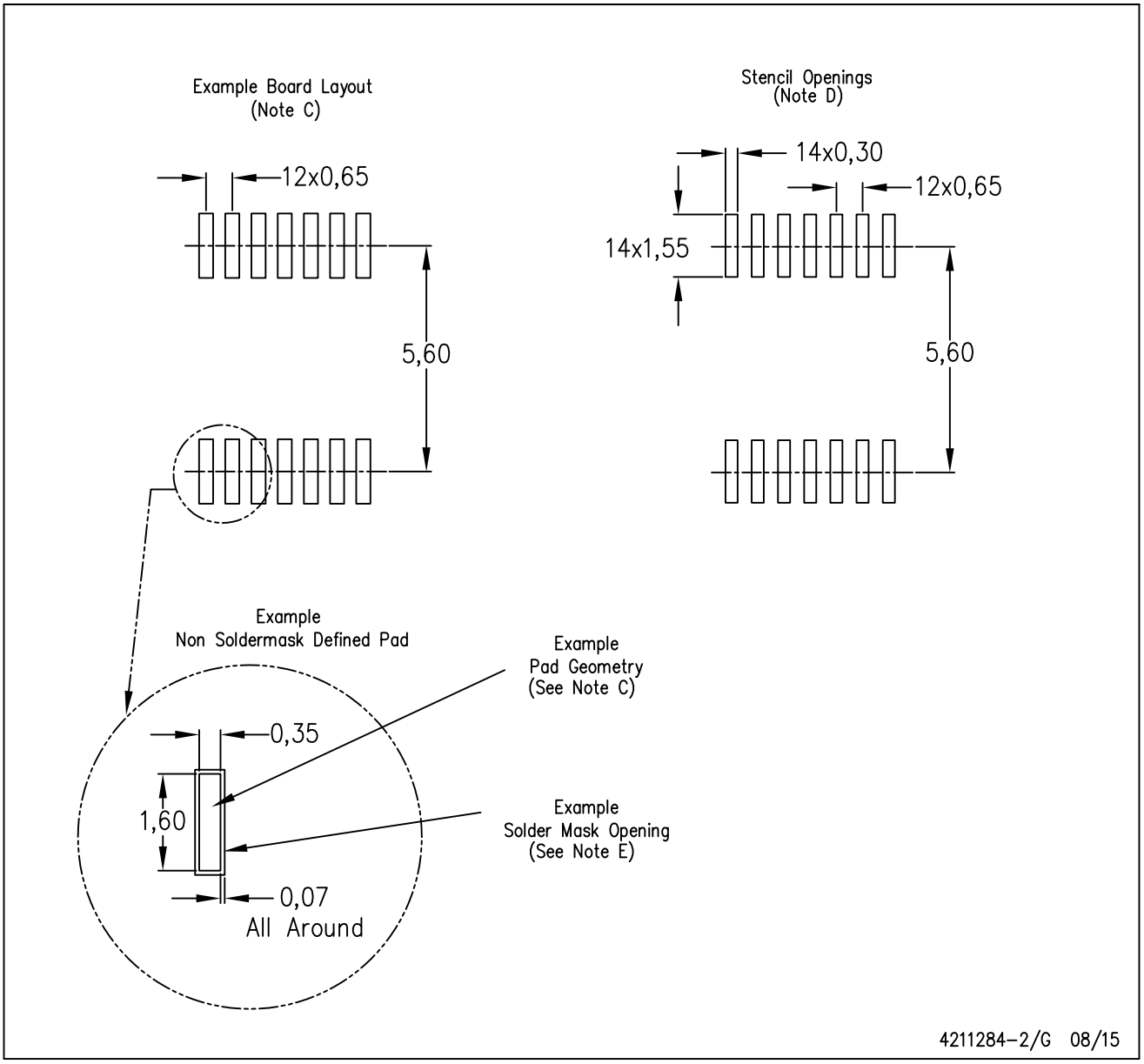
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



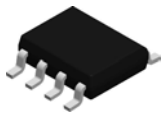
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

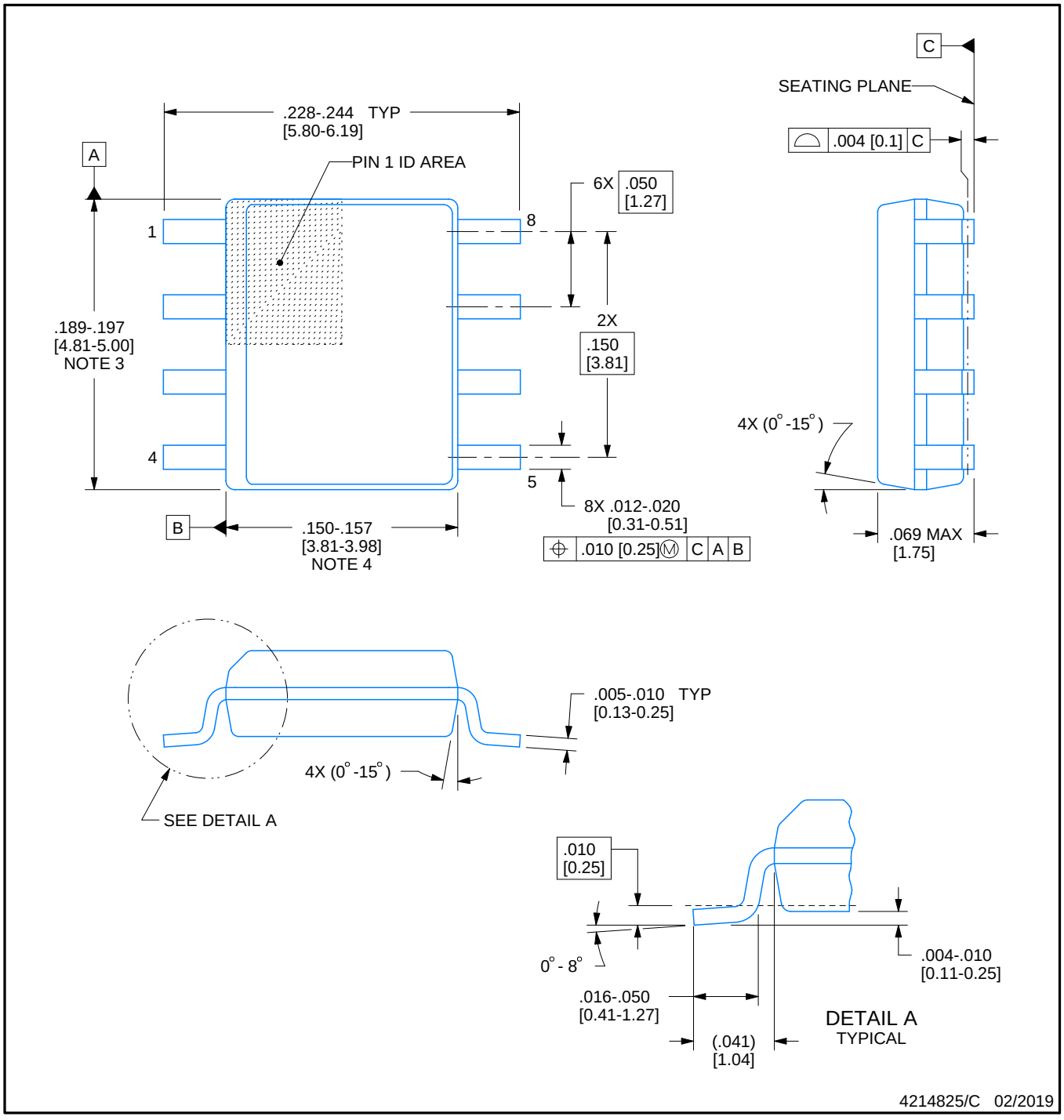


PACKAGE OUTLINE

D0008A

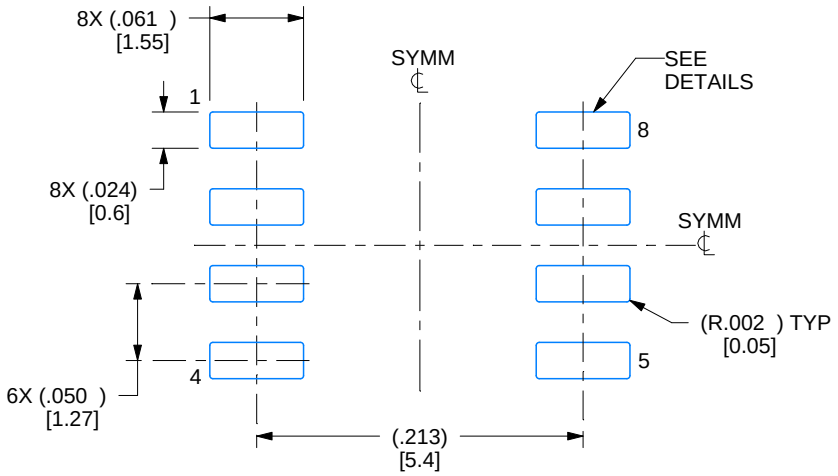
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

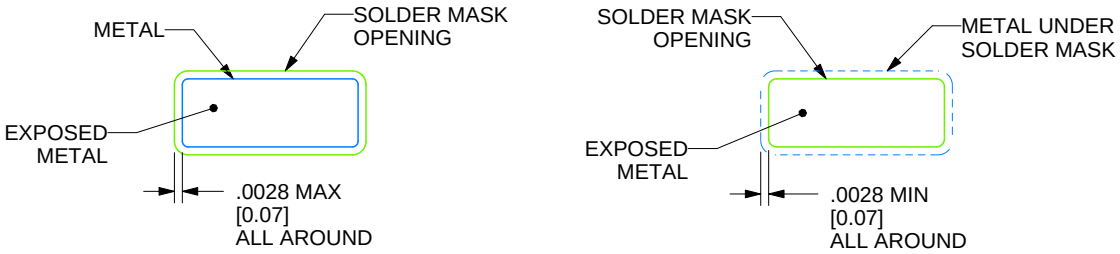


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

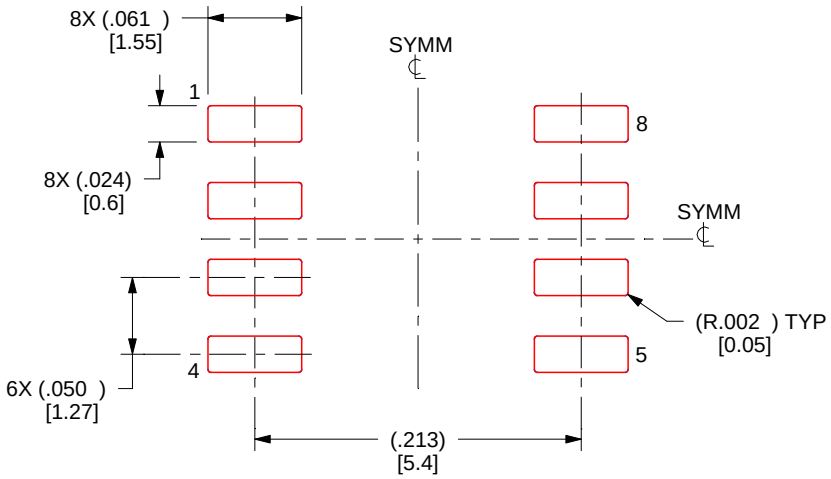
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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