TEXAS INSTRUMENTS

ISO7741TA-Q1, ISO7741TB-Q1
SLLSFW9 – APRIL 2024

ISO7741Tx-Q1 Automotive, High-Speed, Reinforced Quad-Channel Digital Isolator With Integrated Transformer Driver

1 Features

- Qualified for automotive applications AEC-Q100 qualified with the following results:
- Device temperature Grade 1: –40°C to 125°C ambient operating temperature
- Functional Safety-Capable
- 100Mbps data rate
- Robust isolation barrier:
  – >30-year projected lifetime at $1500V_{RMS}$ working voltage
  – $5000V_{RMS}$ rating
  – Up to 12.8kV surge capability
  – ±100kV/µs typical CMTI for digital isolator
- Wide supply range: 2.25V to 5.5V
- 2.25V to 5.5V level translation
- Default output *high* (ISO7741T) and *low* (ISO7741FT) options
- Low power consumption, typical 1.5mA per channel at 1Mbps
- Low propagation delay: 10.7ns typical (5V Supplies)
- Robust electromagnetic compatibility (EMC)
  – System-level ESD, EFT, and surge immunity
  – ±8kV IEC 61000-4-2 contact discharge protection across isolation barrier
- Safety-related certifications (Pending):
  – DIN EN IEC 60747-17 (VDE 0884-17)
  – UL 1577 component recognition program
  – IEC 61010-1, IEC 62368-1, IEC 60601-1, and GB 4943.1 certifications
- Push-pull driver for transformers
- High output drive: 0.7A at 5V supply
- Low R_{ON} 0.4Ω max at 4.5V supply
- Spread spectrum clocking
- 1.7A Current-limit

2 Applications

Hybrid, electric and powertrain system (EV/HEV)
- Battery management system (BMS)
- On-board charger
- Traction inverter and motor control
- DC/DC converter

Body electronics
- Automotive parking heater module
- HVAC control module

3 Description

The ISO7741T-Q1 is a grade 1, high-performance, quad-channel digital isolator with integrated transformer driver with $5000V_{RMS}$ isolation ratings per UL 1577. This reinforced insulation ratings according to VDE, CSA, TUV and CQC.

The ISO7741T-Q1 device provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. If the input power or signal is lost, default output is *high* for devices without suffix F and *low* for devices with suffix F. See the Device Functional Modes section for further details.

The ISO7741T-Q1 has a low-noise, low-EMI push-pull transformer driver, specifically designed for small form factor, isolated power supplies. The device drives low-profile, center-tapped transformers from a 2.25V to 5.5V DC power supply. Very low noise and EMI are achieved by slew rate control of the output switch voltage and through Spread Spectrum Clocking (SSC). The ISO7741T-Q1 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive ground-referenced N-channel power switches. The device includes two 1A Power-MOSFET switches to provide start-up under heavy loads. The internal protection features include a 1.7A current limiting, under-voltage lockout, thermal shutdown, and break-before-make circuitry. ISO7741T-Q1 include a soft-start feature that prevents high inrush current during power up with large load capacitors. ISO7741TA-Q1 has a 160kHz internal oscillator for applications that need to minimize emissions whereas ISO7741TB-Q1 has a 420kHz internal oscillators for applications that require higher efficiency and smaller transformer size.

The ISO7741Tx-Q1 is available in a 16-pin DW package. The device operation is characterized for a temperature range from -40°C to 125°C.

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Package Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)	PACKAGE SIZE[2]
ISO7741Tx-Q1	DW (16)	10.30mm × 7.50mm	10.30mm × 10.30mm

(1) For all available packages, see Section 10.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.
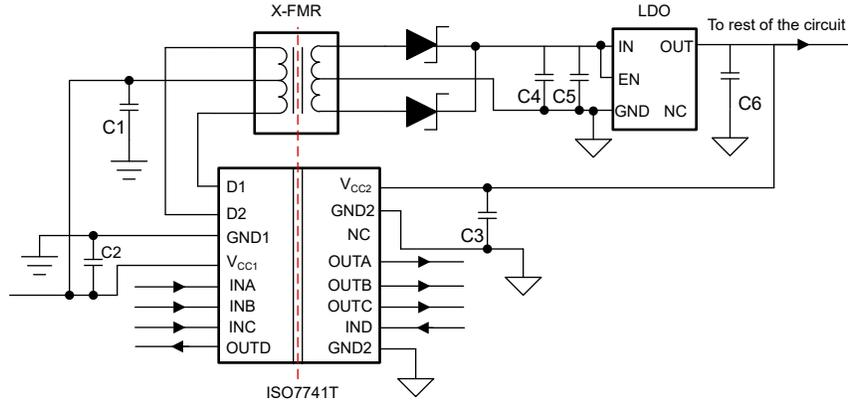
Simplified Schematic

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Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

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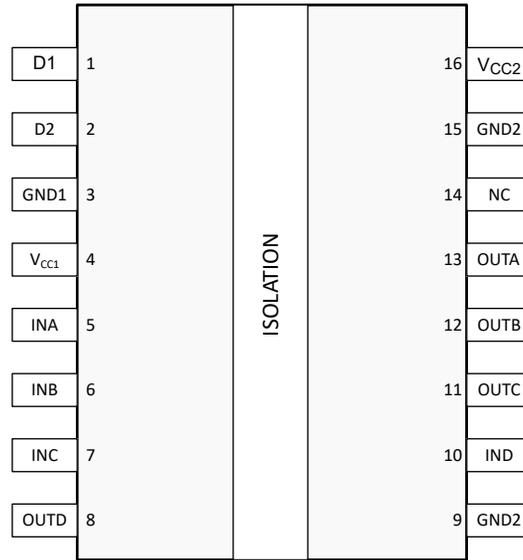
Figure 4-1. ISO7741T DW Package Top View

Pin Functions

NAME	PIN	Type[(1)]	DESCRIPTION
D1	1	O	Open drain output of the first power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, the external traces must be kept short.
D2	2	O	Open drain output of the second power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, the external traces must be kept short.
GND1	3	—	Ground connection for V_{CC1}
GND2	9	—	Ground connection for V_{CC2}
	15		
INA	5	I	Input, channel A
INB	6	I	Input, channel B
INC	7	I	Input, channel C
IND	10	I	Input, channel D
NC	14	—	Not connected
OUTA	13	O	Output, channel A
OUTB	12	O	Output, channel B
OUTC	11	O	Output, channel C
OUTD	8	O	Output, channel D
V_{CC1}	4	—	Power supply, side 1
V_{CC2}	16	—	Power supply, side 2

(1)   I = Input, O = Output

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

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5 Specifications

5.1 Absolute Maximum Ratings

See[1]

				MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage [2]			-0.5	6	V
V	Voltage at INx, OUTx			-0.5	V_{CCX} + 0.5 [3]	V
D1, D2	Output switch voltage	D1, D2			16	V
$I_{(D1)Pk}$, $I_{(D2)Pk}$	Peak output switch current	$I_{(D1)Pk}$, $I_{(D2)Pk}$			2.4	A
I_O	Output current			-15	15	mA
T_J	Junction temperature			-40	150	°C
T_{stg}	Storage temperature			-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

(3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 HBM ESD Classification Level 3A [1]	±6000	V
		Charged-device model (CDM), per AEC Q100-011 V CDM ESD Classification Level C6	±1500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply Voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{D1}, I_{D2}	Output switch current - Primary side	$2.25V \le V_{CC} \le 2.8V$			0.7	A
I_{D1}, I_{D2}	Output switch current - Primary side	$2.8V < V_{CC} \le 5.5V$			0.7	A
I_{OH}	High level output current	V_{CCO} = 5V [1]	-4			mA
		V_{CCO} = 3.3V	-2			
		V_{CCO} = 2.5V	-1			
I_{OL}	Low level output current	V_{CCO} = 5V			4	mA
		V_{CCO} = 3.3V			2	
		V_{CCO} = 2.5V			1	
V_{IH}	High level Input voltage		$0.7 \times V_{CCI}$ [1]		V_{CCI}	V
V_{IL}	Low level Input voltage		0		$0.3 \times V_{CCI}$	V
DR	Data Rate[2]		0		100	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2)   100Mbps is the maximum specified data rate, although higher data rates are possible.

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Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

5.4 Thermal Information

THERMAL METRIC[1]		ISO7741T-Q1	UNIT
		DW (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7741T-Q1						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5V$, $T_J = 150°C$, $C_L =$ 15pF, Input a 50-MHz 50% duty cycle square wave, $I_{D1,}$ $I_{D2}= 700mA$			401	mW
P_{D1}	Maximum power dissipation (side-1)	$V_{CC1} = 5.5V$, $T_J = 150°C$, $C_L = 15pF$, Input a 50-MHz 50% duty cycle square wave, $I_{D1,}$ $I_{D2}= 700mA$			266	mW
P_{D2}	Maximum power dissipation (side-2)	$V_{CC2} = 5.5V$, $T_J = 150°C$, $C_L = 15pF$, Input a 50-MHz 50% duty cycle square wave, $I_{D1,}$ $I_{D2}= 700mA$			135	mW

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE DW-16	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) [2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After Input output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤5	
		Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1MHz	~1	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}	
		V_{IO} = 500V at T_S = 150°C	>10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-terminal device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 7071 V_{PK} (DW-16, Reinforced); Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW-16, Reinforced); Maximum surge isolation voltage, 12800 V_{PK} (DW-16, Reinforced)	Reinforced insulation per CSA 62368-1 and IEC 62368-1, 600 V_{RMS} (DW-16) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V_{RMS} (DW-16) max working voltage	DW-16: Single protection, 5000 V_{RMS};	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage;	5000 V_{RMS} (DW-16) Reinforced insulation per EN 61010-1 up to working voltage of 600 V_{RMS} (DW-16); 5000 V_{RMS} (DW-16) Reinforced insulation per EN 62368-1 up to working voltage of 600 V_{RMS} (DW-16)
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

5.8 Safety Limiting Values

Safety limiting[1] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 64°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C, I_L = 700mA			319	mA
		$R_{\theta JA}$ = 64°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C, I_L = 700mA			480	
		$R_{\theta JA}$ = 64°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C, I_L = 700mA			630	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 64°C/W, T_J = 150°C, T_A = 25°C			1953	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in Section 5.4 is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

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5.9 Electrical Characteristics Transformer

over full-range of recommended operating conditions, unless otherwise noted. All typical values are at T_A = 25°C, V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLK						
F_{SW}	D1, D2 average switching Frequency (ISO7741TA-Q1)	R_L = 50Ω to V_{CC};	138	160	203	kHz
	D1, D2 average switching Frequency (ISO7741TB-Q1)	R_L = 50Ω to V_{CC} .	363	424	517	kHz
OUTPUT STAGE						
DMM	Average ON time mismatch between D1 and D2	R_L = 50Ω		0%		
$R_{(ON)}$	Output switch on resistance	V_{CC} = 4.5V, I_{D1}, I_{D2} = 700mA		0.22	0.4	Ω
		V_{CC} = 2.8V, I_{D1}, I_{D2} = 700mA		0.24	0.45	Ω
		V_{CC} = 2.25V, I_{D1}, I_{D2} = 0.5 A		0.26	0.5	Ω
$V_{(SLEW)}$	Voltage slew rates on D1 and D2 for ISO7741TA-Q1	R_L = 50 Ω to V_{CC}		48		V/μs
$I_{(SLEW)}$	Current slew rates at D1 and D2 for ISO7741TA-Q1	R_L = 5 Ω through transformer		11		A/μs
$V_{(SLEWHF)}$	Voltage slew rates on D1 and D2 for ISO7741TB-Q1	R_L = 50 Ω to V_{CC}		152		V/μs
$I_{(SLEWHF)}$	Current slew rates at D1 and D2 for ISO7741TB-Q1	R_L = 5 Ω through transformer		41		A/μs
I_{LIM}	Current clamp limit (2.8V < V_{CC} ≤ 5.5V)		1.42	1.75	2.15	A
	Current clamp limit (2.25V ≤ V_{CC} ≤ 2.8V)		0.65		1.85	A
THERMAL SHUT DOWN						
T_{SD+}	T_{SD} turn on temperature		154	168	181	°C
T_{SD-}	T_{SD} turn off temperature		135	150	166	°C
T_{SD-}	T_{SD} hysteresis		13	17		°C

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Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

5.10 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4mA	V_{CCO} - 0.4 [1]	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} [1] at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
CMTI[3]	Common mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1200V	85	100		kV/µs
C_I	Input Capacitance [2]	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2)   Measured from input pin to same side ground.
(3)   CMTI is measured only on digital isolator independent of transformer driver

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Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

5.11 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V ±10%, $R_L = 50$ Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7741TA-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7741T)[1] $V_I = 0V$ (ISO7741FT)		I_{CC1}		3	4.2	mA
			I_{CC2}		2.4	3.7	
	$V_I = 0V_I$ (ISO7741T) $V_I = V_{CCI}$ (ISO7741FT)		I_{CC1}		6.3	7.8	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15pF$	1Mbps	I_{CC1}		4.7	6.1	
			I_{CC2}		3.2	4.6	
		10Mbps	I_{CC1}		5.4	6.8	
			I_{CC2}		4.8	6.5	
		100Mbps	I_{CC1}		11.5	13.7	
			I_{CC2}		20	23.5	
ISO7741TB-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7741T)[1] $V_I = 0V$ (ISO7741FT)		I_{CC1}		3.6	5	mA
			I_{CC2}		2.4	3.7	
	$V_I = 0V_I$ (ISO7741T) $V_I = V_{CCI}$ (ISO7741FT)		I_{CC1}		6.9	8.6	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15pF$	1Mbps	I_{CC1}		5.3	6.9	mA
			I_{CC2}		3.2	4.6	
		10Mbps	I_{CC1}		5.9	7.7	
			I_{CC2}		4.8	6.5	
		100Mbps	I_{CC1}		12.1	14.6	
			I_{CC2}		20	23.5	

(1) V_{CCI} = Input-side V_{CC}

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

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5.12 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA	V_{CCO} - 0.3 [1]	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA		0.1	0.3	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI} [1]	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} [1] at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-10			µA
CMTI[2]	Common mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1200V	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) CMTI is measured only on digital isolator independent of transformer driver

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Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

5.13 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$, $R_L = 50\ \Omega$ to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7741TA-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7741T)[1] $V_I = 0V$ (ISO7741FT)		I_{CC1}		2.8	3.9	mA
			I_{CC2}		2.3	3.7	
	$V_I = 0V_I$ (ISO7741T)[1] $V_I = V_{CCI}$ (ISO7741FT)		I_{CC1}		6.1	7.5	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{pF}$	1Mbps	I_{CC1}		4.5	5.7	
			I_{CC2}		3.1	4.5	
		10Mbps	I_{CC1}		4.9	6.3	
			I_{CC2}		4.2	5.9	
		100Mbps	I_{CC1}		9.2	11.1	
			I_{CC2}		15.1	18.2	
ISO7741TB-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7741T)[1] $V_I = 0V$ (ISO7741FT)		I_{CC1}		3.1	4.4	mA
			I_{CC2}		2.3	3.7	
	$V_I = 0V_I$ (ISO7741T)[1] $V_I = V_{CCI}$ (ISO7741FT)		I_{CC1}		6.5	8	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{pF}$	1Mbps	I_{CC1}		4.9	6.3	
			I_{CC2}		3.1	4.5	
		10Mbps	I_{CC1}		5.3	6.9	
			I_{CC2}		4.2	5.9	
		100Mbps	I_{CC1}		9.6	11.7	
			I_{CC2}		15.1	18.2	

(1) V_{CCI} = Input-side V_{CC}

5.14 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA	V_{CCO} - 0.2[1]	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA		0.05	0.2	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} [1] at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-10			µA
$CMTI$[2]	Common mode transient immunity	V_I = V_{CCI} or 0V, V_{CM} = 1200V	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2)   CMTI is measured only on digital isolator independent of transformer driver

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Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

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5.15 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5$ V ±10%, $R_L = 50$ Ω to V_{CC1}, (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7741TA-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7741T)[1] $V_I = 0V$ (ISO7741FT)		I_{CC1}		2.7	3.7	mA
			I_{CC2}		2.3	3.7	
	$V_I = 0V_I$ (ISO7741T)[1] $V_I = V_{CCI}$ (ISO7741FT)		I_{CC1}		6	7.3	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15pF$	1Mbps	I_{CC1}		4.4	5.6	
			I_{CC2}		3	4.5	
		10Mbps	I_{CC1}		4.7	6.1	
			I_{CC2}		3.9	5.5	
		100Mbps	I_{CC1}		8	9.7	
			I_{CC2}		12.1	14.7	
ISO7741TB-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7741T)[1] $V_I = 0V$ (ISO7741FT)		I_{CC1}		3	4.2	mA
			I_{CC2}		2.3	3.7	
	$V_I = 0V_I$ (ISO7741T)[1] $V_I = V_{CCI}$ (ISO7741FT)		I_{CC1}		6.3	7.8	
			I_{CC2}		3.6	5.1	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15pF$	1Mbps	I_{CC1}		4.7	6	
			I_{CC2}		3	4.5	
		10Mbps	I_{CC1}		5	6.5	
			I_{CC2}		3.9	5.5	
		100Mbps	I_{CC1}		8.3	10.1	
			I_{CC2}		12.1	14.7	

(1) V_{CCI} = Input-side V_{CC}

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

5.16 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		6	10.7	17	ns
PWD	Pulse width distortion[1] $\|t_{PHL} - t_{PLH}\|$			0	6.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time[2]	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time[3]				4.4	ns
t_r	Output signal rise time			2.4	3.9	ns
t_f	Output signal fall time			2.4	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V.		0.1	0.3	µs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.8		ns
t_{BBM}	Break-before-make time (ISO7741TA-Q1)	Measured as voltage with $R_L = 50$ Ω to V_{CC}		115		ns
t_{BBM}	Break-before-make time (ISO7741TB-Q1)	Measured as voltage with $R_L = 50$ Ω to V_{CC}		90		ns
t_{SS}	Soft-start time (SN6505A-Q1)	10% to 90% transition time on V_{OUT} With transformer $C_{LOAD} = 40$µF $R_L = 5$Ω	1	2.2	8	ms
t_{SS}	Soft-start time (SN6505B-Q1)	10% to 90% transition time on V_{OUT} With transformer $C_{LOAD} = 40$µF $R_L = 5$Ω	1	4.25	8	ms
$t_{SSdelay}$	Soft-start time delay	From power up to 90% transition time on V_{OUT} With transformer $C_{LOAD} = 40$µF $R_L = 5$Ω	3.5	8.5	18	ms

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.17 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3$ V ±10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		6	12	18.5	ns
PWD	Pulse width distortion[1] |$t_{PHL} - t_{PLH}$|			0.1	6.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time[2]	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time[3]				5	ns
t_r	Output signal rise time			1.3	3	ns
t_f	Output signal fall time			1.3	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V.		0.1	0.3	µs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.9		ns
t_{BBM}	Break-before-make time (ISO7741TA-Q1)	Measured as voltage with $R_L = 50$ Ω to V_{CC}		115		ns
t_{BBM}	Break-before-make time (ISO7741TB-Q1)	Measured as voltage with $R_L = 50$ Ω to V_{CC}		90		ns
t_{SS}	Soft-start time (SN6505A-Q1)	10% to 90% transition time on V_{OUT} With transformer $C_{LOAD} = 40µF$ $R_L = 5Ω$	1	2.2	8	ms
t_{SS}	Soft-start time (SN6505B-Q1)	10% to 90% transition time on V_{OUT} With transformer $C_{LOAD} = 40µF$ $R_L = 5Ω$	1	4.25	8	ms
$t_{SSdelay}$	Soft-start time delay	From power up to 90% transition time on V_{OUT} With transformer $C_{LOAD} = 40µF$ $R_L = 5Ω$	3.5	8.5	18	ms

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

5.18 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		7.5	13	21	ns
PWD	Pulse width distortion[1] |t_{PHL} – t_{PLH}|			0.2	6.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time[2]	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time[3]				5.3	ns
t_r	Output signal rise time			1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V.		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.7		ns
t_{BBM}	Break-before-make time (ISO7741TA-Q1)	Measured as voltage with R_L = 50 Ω to V_{CC},		115		ns
t_{BBM}	Break-before-make time (ISO7741TB-Q1)	Measured as voltage with R_L = 50 Ω to V_{CC}		90		ns
t_{SS}	Soft-start time (SN6505A-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	1	2.2	8	ms
t_{SS}	Soft-start time (SN6505B-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	1	4.25	8	ms
$t_{SSdelay}$	Soft-start time delay	From power up to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40µF R_L = 5Ω	3.5	8.5	18	ms

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6 Detailed Description

6.1 Overview

The ISO7741T devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO7741T also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching.

The transformer driver in ISO7741T is designed for low-cost, small form-factor, isolated DC/DC converters utilizing the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off. The output frequency of the oscillator is divided down by two. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. Before either one of the gates can assume logic high, the BBM logic provides a short time period during which both signals are low and both transistors are high-impedance. This short period, is required to avoid shorting out both ends of the primary. The resulting output signals, present the gate-drive signals for the output transistors.

The conceptual block diagram of a digital capacitive isolator with integrated transformer driver, Figure 6-1 and Figure 6-2, shows a functional block diagram of a typical channel and transformer driver.

6.2 Functional Block Diagram
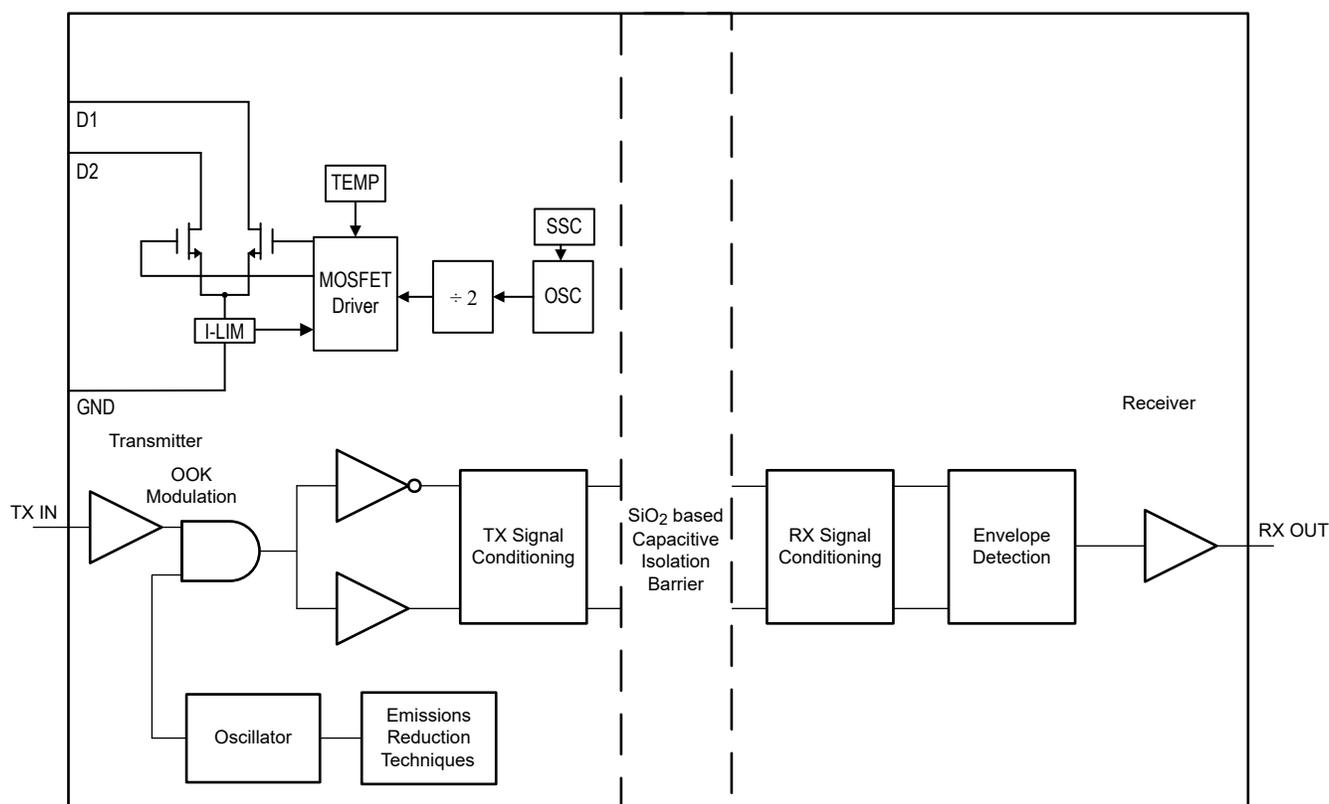
Figure 6-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 6-2 shows a conceptual detail of how the ON-OFF keying scheme works.
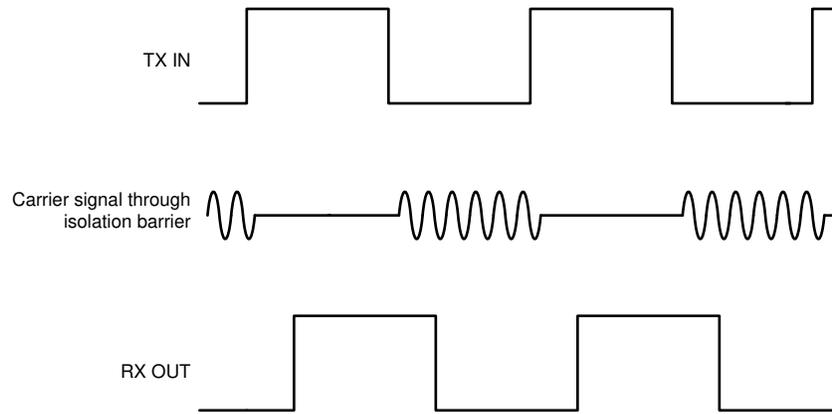
**Figure 6-2. On-Off Keying (OOK) Based Modulation Scheme**

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6.3 Feature Description

Table 6-1. Device Features

PART NUMBER	TYPICAL SWITCHING FREQUENCY	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION
ISO7741TA	160kHz	100Mbps	High	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7741FTA	160kHz	100Mbps	Low	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7741TB	424kHz	100Mbps	High	DW-16	$5000V_{RMS}$ / $7071V_{PK}$
ISO7741FTB	424kHz	100Mbps	Low	DW-16	$5000V_{RMS}$ / $7071V_{PK}$

See *Section 5.7* for detailed isolation ratings.

6.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7741T devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

6.3.2 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary (see *Figure 6-3*).
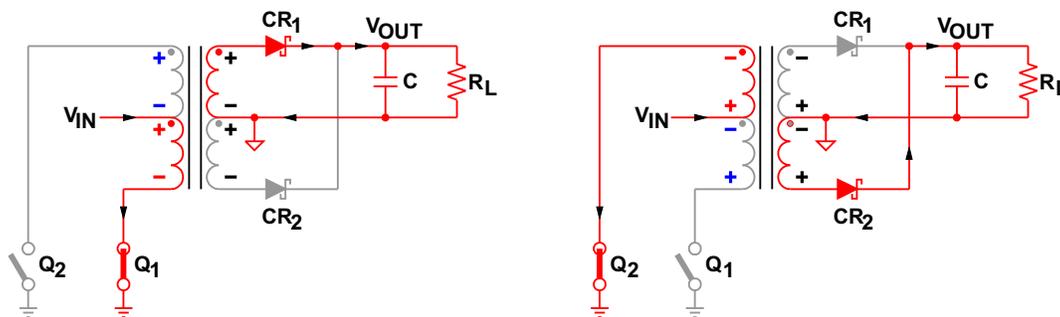

Figure 6-3. Switching Cycles of a Push-Pull Converter

When Q_1 conducts, V_{IN} drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the V_{IN} potential at the center-tap.

At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap to maintain the previously established current flow through Q_2, which now has turned high-impedance. The two voltage sources, each of which equaling V_{IN}, appear in series and cause a voltage potential at the open end of the primary of $2 \times V_{IN}$ with regards to ground.

Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode CR_1. The secondary current

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starting from the upper secondary end flows through CR_1, charges capacitor C, and returns through the load impedance R_L back to the center-tap.

When Q_2 conducts, Q_1 goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a $2 \times V_{IN}$ potential against ground. In this case CR_2 is forward biased while CR_1 is reverse biased and current flows from the lower secondary end through CR_2, charging the capacitor and returning through the load to the center-tap.

6.3.3 Core Magnetization

Figure 6-4 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q_1 conducts the magnetic flux is pushed from A to A', and when Q_2 conducts the flux is pulled back from A' to A. The difference in flux and thus in flux density is proportional to the product of the primary voltage, V_P, and the time, t_{ON}, the voltage is applied to the primary: $B \cong V_P \times t_{ON}$.
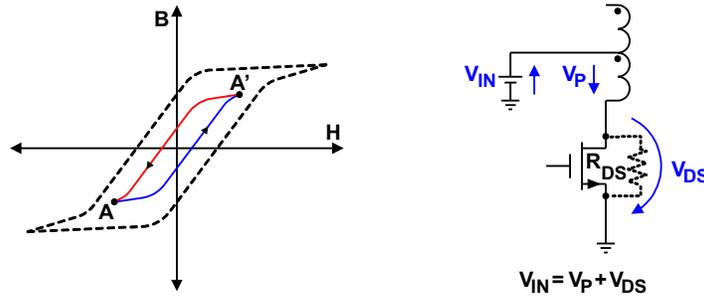
Figure 6-4. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of $R_{DS(on)}$

This volt-seconds (V-t) product is important as the product determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

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6.4 Device Functional Modes

Table 6-2 lists the functional modes for the ISO7741T devices.

Table 6-2. Function Table

V_{CCI} [1]	V_{CCO}	INPUT (INx)[3]	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is *High* for ISO7741Tx and *Low* for ISO7741FTx.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO7741Tx and *Low* for ISO7741FTx. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined[2]. When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

1. V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geq 2.25V$); PD = Powered down ($V_{CC} \leq 1.7V$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance
2. The outputs are in undetermined state when $1.7V < V_{CCI}, V_{CCO} < 2.25V$.
3. A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

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Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

6.4.1 Device I/O Schematics
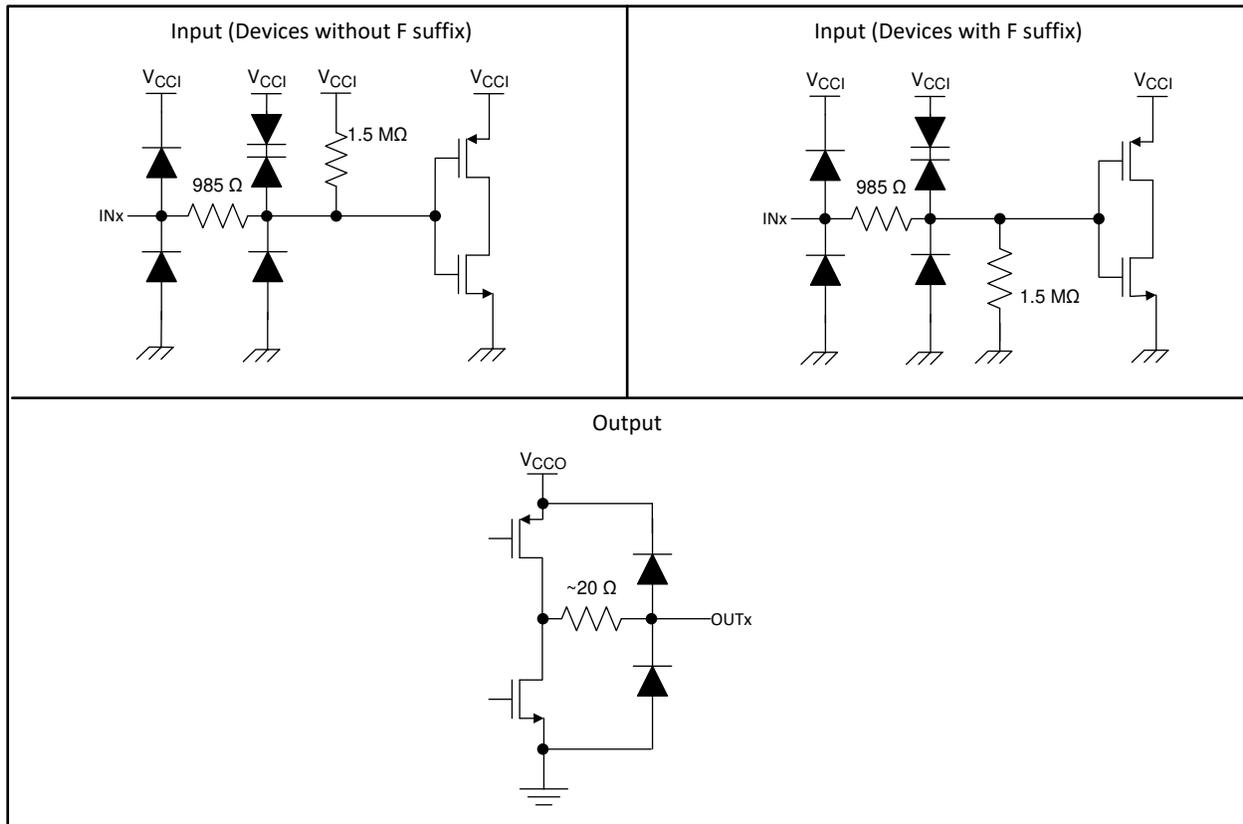
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Figure 6-5. Device I/O Schematics

6.4.2 Start-Up Mode

When the supply voltage at V_{CC} ramps up to 2.25V, the internal oscillator starts operating. The output stage begins switching but the amplitude of the drain signals at D1 and D2 has not reached the full maximum yet.

ISO7741T-Q1 devices support soft-start feature. Upon power up, the gate drive of the output power-MOSFET is gradually increased over a period of time from 0V to V CC. Soft-start prevents high inrush current from V CC while charging large secondary side decoupling capacitors, and also prevents overshoot in secondary voltage during power-up.

6.4.3 Operating Mode

When the device supply has reached the nominal value ±10% the oscillator is fully operating. However variations over supply voltage and operating temperature can vary the switching frequencies at D1 and D2.

6.4.4 Spread Spectrum Clocking

Radiated emissions is an important concern in high current switching power supplies. ISO7741T transformer driver addresses this by modulating the internal clock in such a way that the emitting energy is spread over multiple frequency bins. This Spread Spectrum clocking feature greatly improves the emissions performance of the entire power supply block and hence relieves the system designer from one major concern in isolated power supply design.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The device is a high-performance, quad-channel digital isolator with integrated high efficiency transformer driver. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to integrated transformer driver, with external transformer, the isolated supply can be generated to power the isolated side of the device and peripherals on isolated side, thus saving board space without compromising on efficiency. The voltage range is from 2.25V to 5.5V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

The device is designed for applications that have limited board space and desire more integration. The device is also designed for very high voltage applications with power transformer supporting high voltage isolation.

7.2 Typical Application

The following application circuit is shown for a 3.3V input supply commonly taken from the local, regulated microcontroller supply for SPI isolation. For 5V input voltages requiring different turn ratios refer to the transformer manufacturers and the web sites listed in Transformer Manufacturers

Table 7-1. Transformer Manufacturers

| MANUFACTURER	MORE INFORMATION
Coilcraft Inc.	http://www.coilcraft.com
Halo-Electronics Inc.	http://www.haloelectronics.com
Murata Power Solutions	http://www.murata-ps.com
Wurth Electronics Midcom Inc	http://www.midcom-inc.com
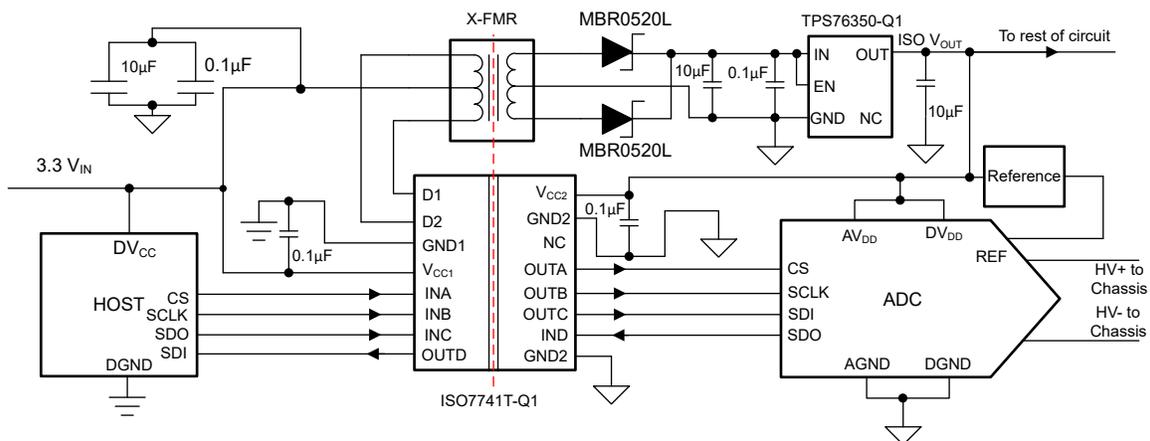
Figure 7-1. Isolated Power and SPI for ADC Sensing Application With ISO7741T-Q1

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

7.2.1 Design Requirements

To design with these devices, use the parameters listed in Design Parameters.

Table 7-2. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1}	2.25V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF +1µF to 10µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF +1µF to 10µF

7.2.2 Detailed Design Procedure

The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Contrary to popular belief, the output voltage of the unregulated converter output drops significantly over a wide range in load current. The characteristic curve in Figure 7-2 and Figure 7-3 for example, shows that the difference between V_{OUT} at minimum load and V_{OUT} at maximum load exceeds a transceiver supply range. Therefore, to provide a stable, load independent supply while maintaining maximum possible efficiency the implementation of a low dropout regulator (LDO) is strongly advised.

7.2.2.1 Drive Capability

The transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 2.25V to 5.5V. While converter designs with higher output voltages are possible, care must be taken that higher turns ratios do not lead to primary currents that exceed the specified current limits of the device.

7.2.2.2 LDO Selection

The minimum requirements for a suitable low dropout regulator are:

- The current drive capability must slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore, for a load current of 550mA, choose a 600mA to 700mA LDO. While regulators with higher drive capabilities are acceptable, these regulators also typically possess higher dropout voltages that reduce the overall converter efficiency.
- The internal dropout voltage, V_{DO}, at the specified load current must be as low as possible to maintain efficiency. For a low-cost 700mA LDO, a V_{DO} of 600mV at 700mA is common. Be aware; however, that this lower value is typically specified at room temperature and can increase by a factor of 2 over temperature, which in turn raises the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max} \tag{1}$$

To determine V_I for worst-case condition, the user must take the maximum values for V_{DO} and V_O specified in the LDO data sheet for rated output current (that is, 600mA) and add these values together. The user must also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than $V_{I\text{-}min}$. If the output voltage is not, the LDO loses line-regulation and any variations at the input passes straight through to the output. Hence, below $V_{I\text{-}min}$ the output voltage follows the input and the regulator behaves like a simple conductor.

- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across $R_{DS\text{-}on}$ negligible and allowing the entire converter input voltage to drop across the primary. At this point, the secondary reaches the maximum voltage of

$$V_{S\text{-}max} = V_{IN\text{-}max} \times n \tag{2}$$

with $V_{IN\text{-}max}$ as the maximum converter input voltage and n as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than $V_{S\text{-}max}$. Table 7-3 lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters.

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Table 7-3. Required Maximum LDO Input Voltages for Various Push-Pull Configurations

	PUSH-PULL CONVERTER			LDO
CONFIGURATION	$V_{IN\text{-}max}$ [V]	TURNS-RATIO	$V_{S\text{-}max}$ [V]	$V_{I\text{-}max}$ [V]
$3.3V_{IN}$ to $3.3V_{OUT}$	3.6	1.5 ± 3%	5.6	6 to 10
$3.3V_{IN}$ to $5V_{OUT}$	3.6	2.2 ± 3%	8.2	10
$5V_{IN}$ to $5V_{OUT}$	5.5	1.5 ± 3%	8.5	10

7.2.2.3 Diode Selection

A rectifier diode must always possess low-forward voltage to provide as much voltage to the converter output as possible. When used in high-frequency switching applications, such as the ISO7741Tx-Q1 however, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs. A good choice for low-volt applications and ambient temperatures of up to 85°C is the low-cost Schottky rectifier MBR0520L with a typical forward voltage of 275mV at 100mA forward current. For higher output voltages such as ±10V and above use the MBR0530 which provides a higher DC blocking voltage of 30V.

Lab measurements have shown that at temperatures higher than 100°C the leakage currents of the above Schottky diodes increase significantly. These conditions can cause thermal runaway leading to the collapse of the rectifier output voltage. Therefore, for ambient temperatures higher than 85°C use low-leakage Schottky diodes, such as RB168MM-40.

ADVANCE INFORMATION
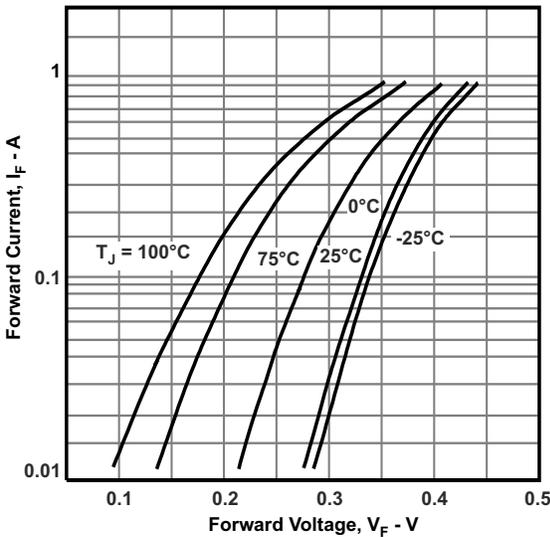
Figure 7-2. Diode Forward Characteristics for MBR0520L
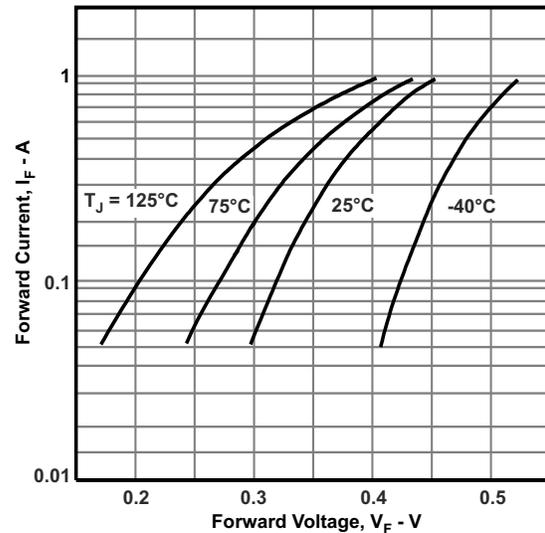
Figure 7-3. Diode Forward Characteristics MBR0530

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

7.2.2.4 Capacitor Selection

As with all high speed CMOS ICs, the device requires a bypass capacitor in the range of 10nF to 100nF.

The input bulk capacitor at the center-tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple make this capacitor 1µF to 10µF. In a 2-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layer board design with low-inductance reference planes for ground and V_{CC}, the capacitor can be placed at the supply entrance of the board. To provide low-inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smooths the output voltage. Make this capacitor 1µF to 10µF.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47nF to 100nF improves the transient response and noise rejection of the regulator.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7µF to 10µF satisfies these requirements.

7.2.2.5 Transformer Selection

7.2.2.5.1 V-t Product Calculation

To prevent a transformer from saturation, the V-t product must be greater than the maximum V-t product applied by the device. The maximum voltage delivered by the device is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the minimum V-t product for the transformer is determined through:

$$Vt_{min} \geq V_{IN-max} \times \frac{T_{max}}{2} = \frac{V_{IN-max}}{2 \times f_{min}} \tag{3}$$

Taking an example of f_{min} as 138kHz for ISO7741TA-Q1 and 363kHZ for ISO7741TB-Q1 with a 5V supply, the following equations yield the minimum V-t products of:

$Vt_{min} \geq \frac{5.5V}{2 \times 138kHz} = 20V\mu s$ for ISO7741TA-Q1 applications, and

$Vt_{min} \geq \frac{5.5V}{2 \times 363kHz} = 7.6V\mu s$ for ISO7741TB-Q1 applications

Common V-t values for low-power center-tapped transformers range from 22Vµs to 150Vµs with typical footprints of 10mm x 12mm. However, transformers specifically designed for PCMCIA applications provide as little as 11Vµs and come with a significantly reduced footprint of 6mm x 6mm only.

While Vt-wise all of these transformers can be driven by the device, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

7.2.2.5.2 Turns Ratio Estimate

Assuming that the rectifier diodes and linear regulator are selected and that the transformer selected must have a V-t product of at least 11Vµs. However, before searching the manufacturer web sites for a suitable transformer, the user still needs to know the minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer typical efficiency of 97% into account:

$$V_{P-min} = V_{IN-min} - V_{DS-max} \tag{4}$$

V_{S-min} must be large enough to allow for a maximum voltage drop, V_{F-max}, across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the *LDO Selection* section, this minimum input voltage is known and by adding V_{F-max} gives the minimum secondary voltage with:

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$$V_{S\text{-min}} = V_{F\text{-max}} + V_{DO\text{-max}} + V_{O\text{-max}} \tag{5}$$
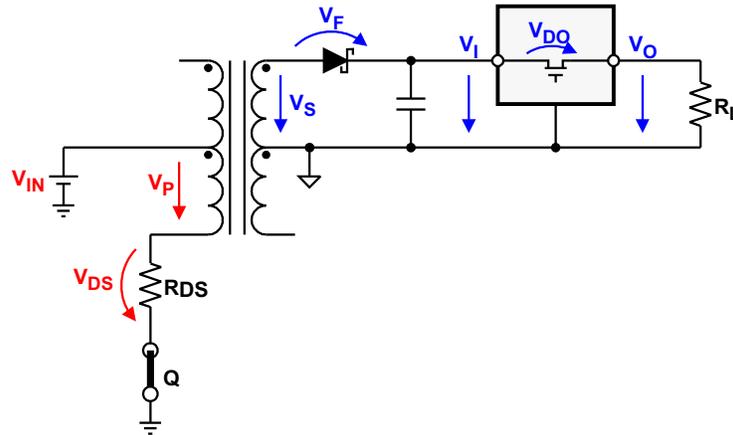
Figure 7-4. Establishing the Required Minimum Turns Ratio Through $N_{min} = 1.031 \times V_{S\text{-min}} / V_{P\text{-min}}$

Then calculating the available minimum primary voltage, $V_{P\text{-min}}$, involves subtracting the maximum possible drain-source voltage of the device, $V_{DS\text{-max}}$, from the minimum converter input voltage $V_{IN\text{-min}}$:

$$V_{P\text{-min}} = V_{IN\text{-min}} - V_{DS\text{-max}} \tag{6}$$

$V_{DS\text{-max}}$ however, is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the data sheet:

$$V_{DS\text{-max}} = R_{DS\text{-max}} \times I_{Dmax} \tag{7}$$

Then inserting Equation 7 into Equation 6 yields:

$$V_{P\text{-min}} = V_{IN\text{-min}} - R_{DS\text{-max}} \times I_{Dmax} \tag{8}$$

and inserting Equation 8 and Equation 5 into Equation 4 provides the minimum turns ration with:

$$n_{min} = 1.031 \times \frac{V_{F\text{-max}} + V_{DO\text{-max}} + V_{O\text{-max}}}{V_{IN\text{-min}} - R_{DS\text{-max}} \times I_{D\text{-max}}} \tag{9}$$

Example:

For a $3.3V_{IN}$ to $5V_{OUT}$ converter using the rectifier diode MBR0520L and the 5V LDO, the data sheet values taken for a load current of 600mA and a maximum temperature of 85°C are $V_{F\text{-max}} = 0.2V$, $V_{DO\text{-max}} = 0.5V$, and $V_{O\text{-max}} = 5.1V$.

Then assuming that the converter input voltage is taken from a 3.3V controller supply with a maximum ±2% accuracy makes $V_{IN\text{-min}} = 3.234V$. Finally the maximum values for drain-source resistance and drain current at 3.3V are taken from the data sheet with $R_{DS\text{-max}} = 0.45\Omega$ and $I_{D\text{-max}} = 700mA$.

Inserting the values above into Equation 10 yields a minimum turns ratio of:

$$n_{min} = 1.031 \times \frac{0.2V + 0.5V + 5.1V}{3.234V - 0.45\Omega \times 700mA} \tag{10}$$

Most commercially available transformers for 3V to 5V push-pull converters offer turns ratios between 2.0 and 2.3 with a common tolerance of ±3%.

7.2.2.5.3 Recommended Transformers

Depending on the application, use the minimum configuration in Figure 7-5 or standard configuration in Figure 7-6.
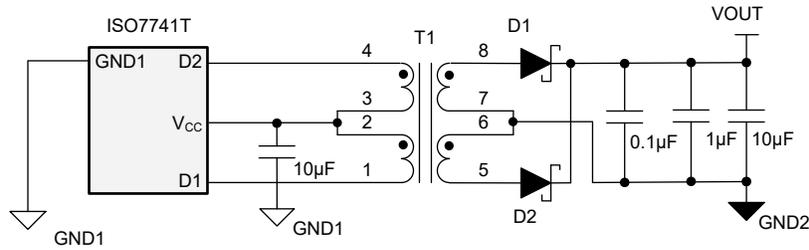
Figure 7-5. Unregulated Output for Low-Current Loads With Wide Supply Range
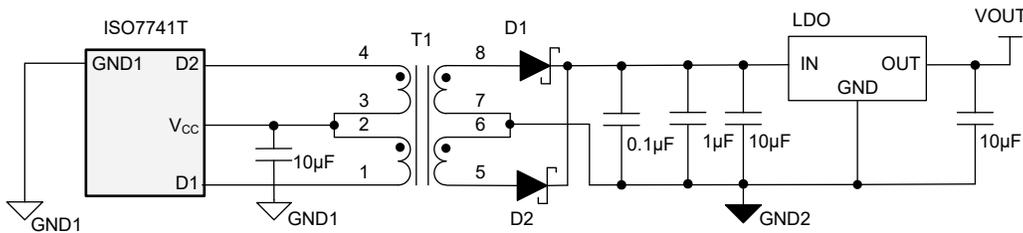
Figure 7-6. Regulated Output for Stable Supplies and High Current Loads

The Wurth Electronics Midcom isolation transformers in Table 7-4 are optimized designs for the device, providing high efficiency and small form factor at low-cost.

The 1:1.1 and 1:1.7 turns-ratios are designed for logic applications with wide supply rails and low load currents. These applications operate without LDO, thus achieving further cost-reduction.

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Table 7-4. Recommended Isolation Transformers Optimized for the Device

TURNS RATIO	V × T (Vµs)	ISOLATION (V_RMS)	DIMENSIONS (mm)	APPLICATION	LDO[1]	ORDER NO.	MANUFACTURER
1:1.1 ±2%	7	2500	6.73 x 10.05 x 4.19	3.3V → 3.3V, 100mA, ISO7741TB-Q1	No	760390011	Wurth Electronics / Midcom
1:1.1 ±2%	11			5V → 5V, 100mA, ISO7741TB-Q1		760390012	
1:1.7 ±2%				3.3V → 5V, 100mA, ISO7741TB-Q1		760390013	
1:1.3 ±2%				3.3V → 3.3V, 100mA, ISO7741TB-Q1	Yes	760390014	
1:1.3 ±2%				5V → 5V, 100mA, ISO7741TB-Q1		760390014	
1:2.1 ±2%				3.3V → 5V, 100mA, ISO7741TB-Q1		760390015	
1.23:1 ±2%				5V → 3.3V, 100mA, ISO7741TB-Q1		750313710	
1:1.7 ±2%	8.9		8.3 x 12.6 x 4.1	3.3V → 3.3V, 1A, ISO7741TB-Q1		750316028	
1:2.1 ±2%				3.3V → 5V, 1A, ISO7741TB-Q1		750316029	
1.3:1 ±2%	10.8			5V → 3.3V, 1A, ISO7741TB-Q1		750316030	
1:1.1 ±2%	8.6			3.3V → 3.3V, 1A, ISO7741TB-Q1 5V → 5V, 1A, ISO7741TB-Q1	No	750315371	
1:1.1 ±2%	11	5000	9.14 x 12.7 x 7.37	3.3V → 3.3V, 100mA, ISO7741TB-Q1		750313734	
1:1.1 ±2%				5V → 5V, 100mA, ISO7741TB-Q1		750313734	
1:1.7 ±2%				3.3V → 5V, 100mA, ISO7741TB-Q1		750313769	
1:1.3 ±2%				3.3V → 3.3V, 100mA, ISO7741TB-Q1 5V → 5V, 100mA, ISO7741TB-Q1	Yes	750313638	
1:2.1 ±2%				3.3V → 5V, 100mA, ISO7741TB-Q1		750313626	
1.3:1 ±2%				5V → 3.3V, 100mA, ISO7741TB-Q1	No	750313638	
1:1.75 ±2%	41		12.32 x 15.41 x 11.05	3.3V → 3.3V, 1A, ISO7741TA-Q1	Yes	750316031	
1:2 ±2%				3.3V → 5V, 1A, ISO7741TA-Q1		750316032	
1.3:1 ±2%	42			5.0V → 3.3V, 1A, ISO7741TA-Q1		750316033	
1:1.1 ±2%	23		12.32 x 15.41 x 11.89	3.3V → 3.3V, 1A, ISO7741TA-Q1 5V → 5V, 1A, ISO7741TA-Q1		750315240	
1:3.5 ±2%	9		9.14 x 12.95 x 7.62	5V → 17.5V, 100mA, ISO7741TB-Q1	No	750342879	
1:3.9 ±2%			9.17 x 12.7 x 7.62	5V → 19.5V, 100mA, ISO7741TB-Q1		750343725	
1:3.75 ±2%	9.5	2500	8.3 x 12.6 x 4.1	5V → 18.75V, 100mA, ISO7741TB-Q1		78931812518	
1:4.75 ±2%				5V → 23.75V, 100mA, ISO7741TB-Q1		78931812523	
1:2.5 ±2%				5V → 12.5V, 200mA, ISO7741TB-Q1		78931812512	
1:3.13 ±2%				5V → 15.65V, 200mA, ISO7741TB-Q1		78931812515	
1:3.5 ±2%	16	6000	9.14 x 12.7 x 7.62	5V → 17.5V, 100mA, ISO7741TB-Q1		750320340	
1:1.3 ±3%	11	5000	10.4 x 12.2 x 6.1	3.3V → 3.3V, 300mA, ISO7741TB-Q1 5V → 5V, 300mA, ISO7741TB-Q1	No	HCT-SM-1.3-8-2	Bourns
1:1.5 ±3%	34.4	2500	10 x 12.07 x 5.97	3.3V → 3.3V, 1A, ISO7741TB-Q1 5V → 5V, 1A, ISO7741TA/B-Q1	Yes	DA2303-AL	Coilcraft
1:2.2 ±3%	21.5	2500	10 x 12.07 x 5.97	3.3V → 5V, 1A, ISO7741TA/B-Q1		DA2304-AL	

(1) For configurations with LDO, a higher voltage than the required output voltage is generated, to allow for LDO drop-out. Figures show the voltage and efficiency at the LDO input.

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7.2.3 Application Curve

The following typical eye diagrams of the device indicates low jitter and wide open eye at the maximum data rate of 100bps.
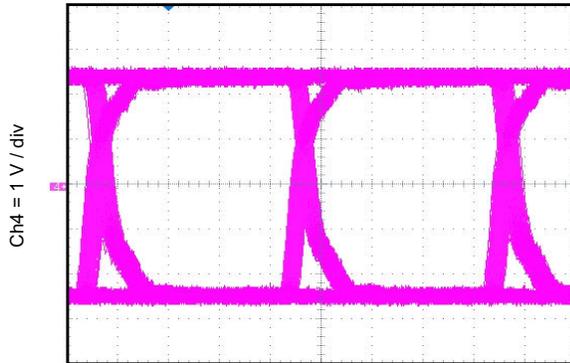

Time = 2.5 ns / div

Figure 7-7. Eye Diagram at 100Mbps PRBS $2^{16} – 1$, 5V and 25°C
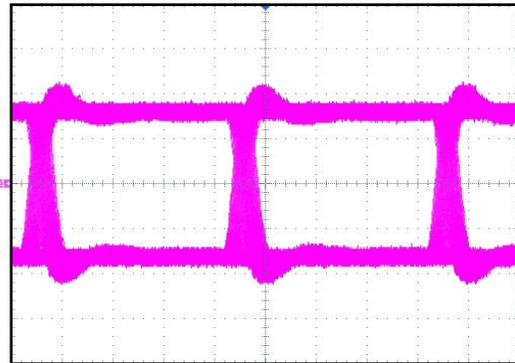
Time = 2.5 ns / div

Figure 7-8. Eye Diagram at 100Mbps PRBS $2^{16} – 1$, 3.3V and 25°C
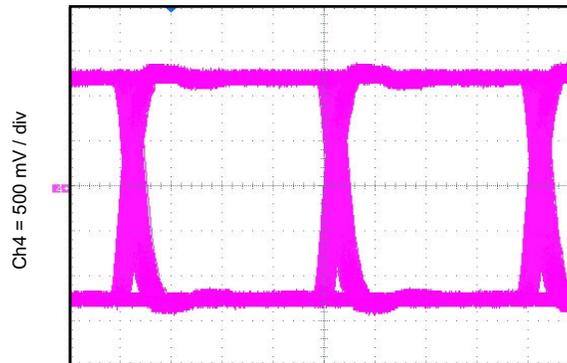
Time = 2.5 ns / div

Figure 7-9. Eye Diagram at 100Mbps PRBS $2^{16} – 1$, 2.5V and 25°C

7.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 7-10 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 7-11 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500V$_{RMS}$ with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, and more can further limit the working voltage of the component. The working voltage of DW-16 package is specified up to 1500V$_{RMS}$. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years. DBQ-16 package at 400 V$_{RMS}$ working voltage has a much longer lifetime than

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ADVANCE INFORMATION
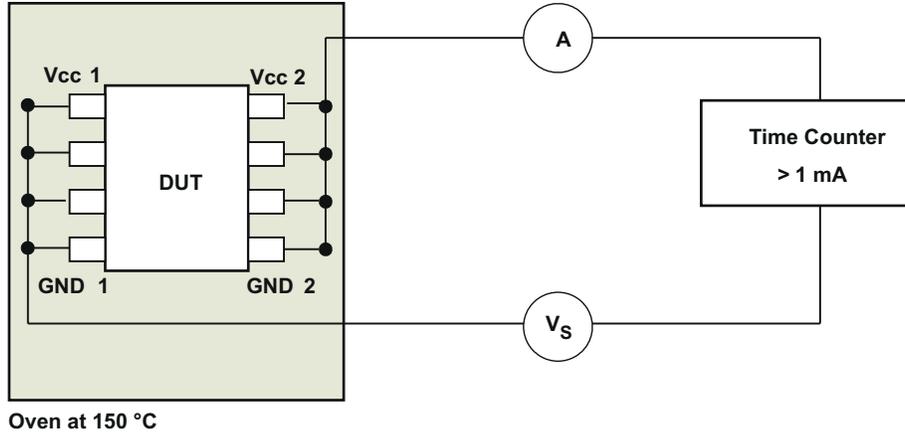
Figure 7-10. Test Setup for Insulation Lifetime Measurement
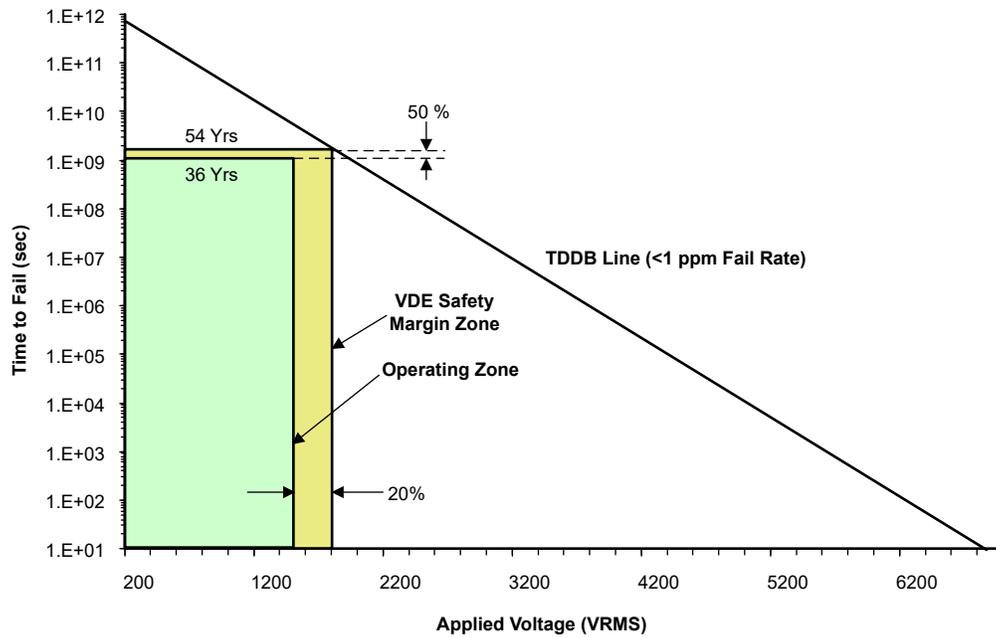
Working Isolation Volatage = 1500 V$_{RMS}$
up to 150°C

Protected Insulation Lifetime = 36 Years
Applied Voltage Frequency = 60 Hz

Figure 7-11. Insulation Lifetime Projection Data

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

7.2.4 System Examples

7.2.4.1 Higher Output Voltage Designs

The device can drive push-pull converters that provide high output voltages of up to 30V, or bipolar outputs of up to ±15V. Using commercially available center-tapped transformers, with relatively low turns ratios of 0.8 to 5, requires different rectifier topologies to achieve high output voltages. Figure 7-12 to Figure 7-14 show some of these topologies together with the respective open-circuit output voltages.
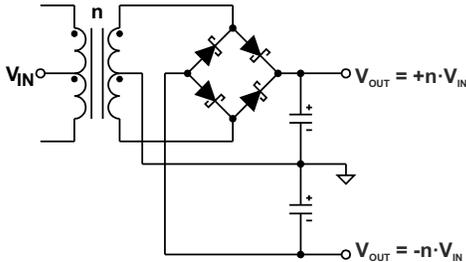
Figure 7-12. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs
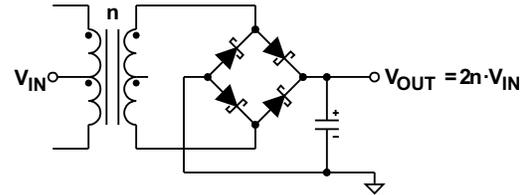
Figure 7-13. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Doubling
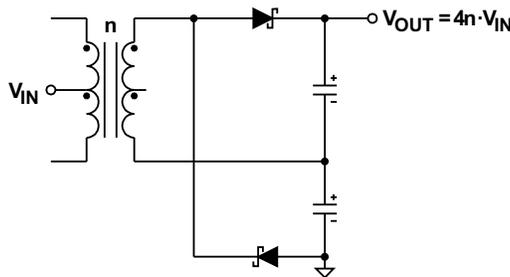
Figure 7-14. Half-Wave Rectifier Without Centered Ground and Center-Tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling V_{IN}

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Submit Document Feedback   35

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:
- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*, application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC

4221009/B   07/2016

ADVANCE INFORMATION
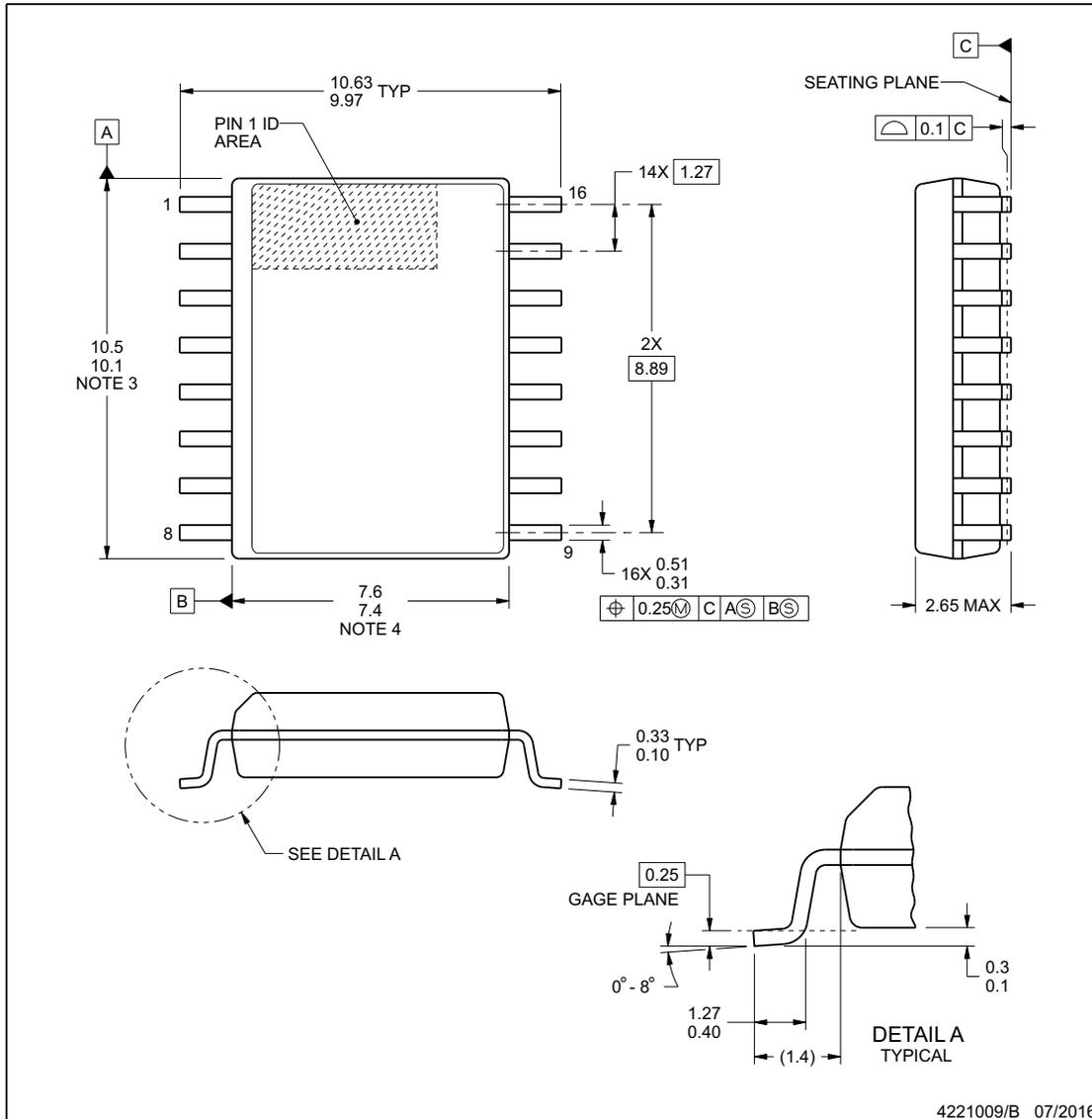
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B
SOIC - 2.65 mm max height

SOIC

ADVANCE INFORMATION

16X (2)

SYMM

SEE
DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

R0.05 TYP

(9.3)

IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

16X (1.65)

SYMM

SEE
DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

R0.05 TYP

(9.75)

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X

METAL

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221009/B   07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

EXAMPLE STENCIL DESIGN

DW0016B
SOIC - 2.65 mm max height

SOIC

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016
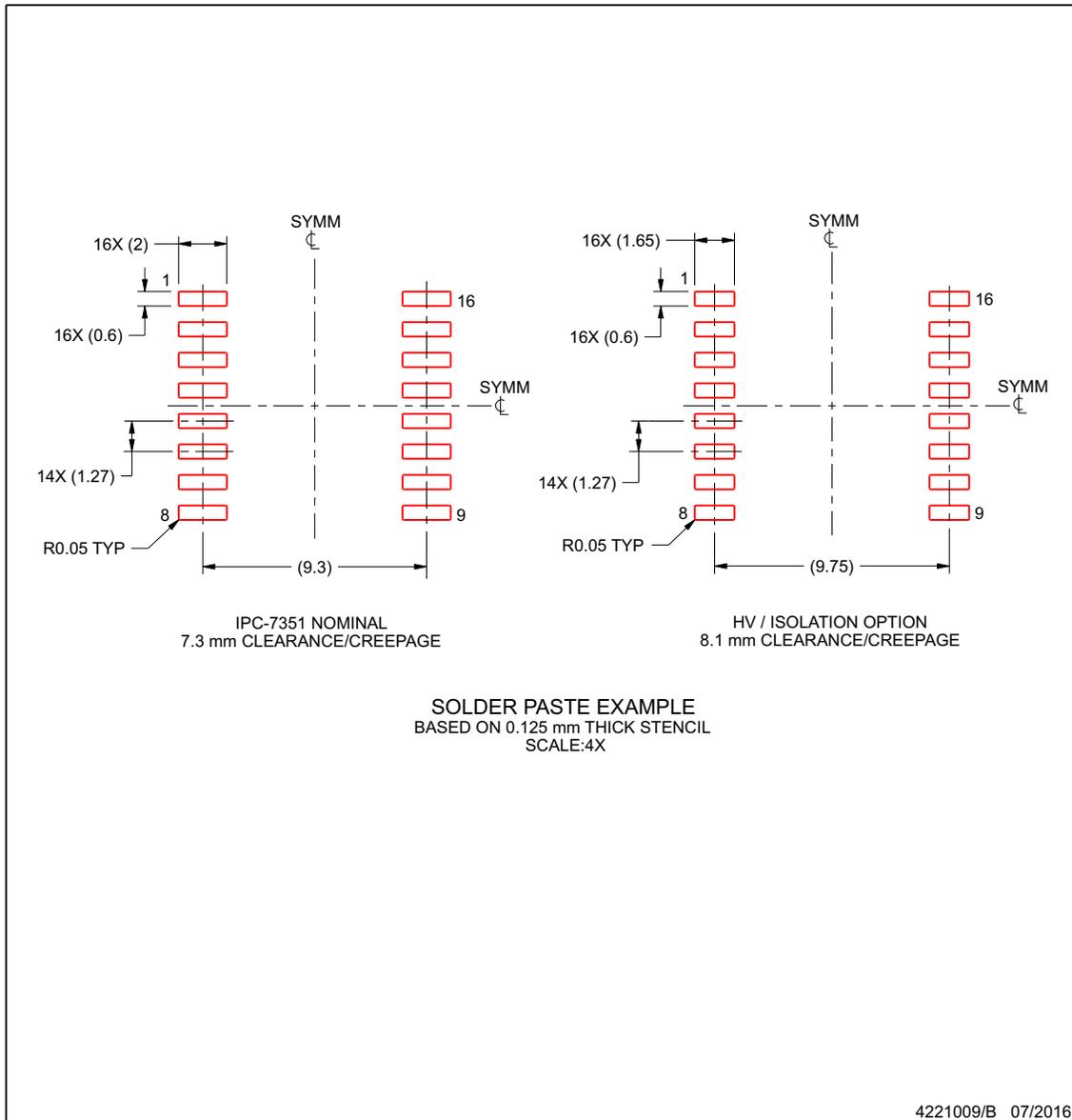
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

www.ti.com

Product Folder Links: *ISO7741TA-Q1 ISO7741TB-Q1*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XISO7741TADWRQ1	ACTIVE	SOIC	DW	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
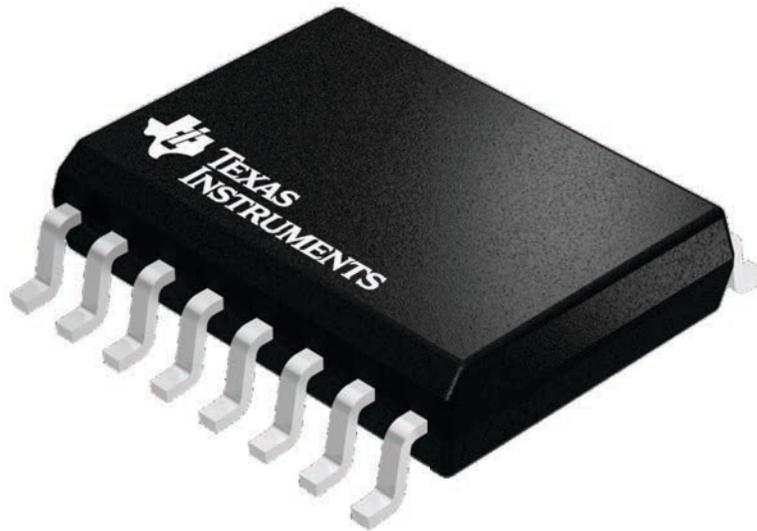
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