DS90LV028A 3-V LVDS Dual CMOS Differential Line Receiver

1 Features

- >400-Mbps (200 MHz) Switching Rates
- 50-ps Differential Skew (Typical)
- 0.1-ns Channel-to-Channel Skew (Typical)
- 2.5-ns Maximum Propagation Delay
- 3.3-V Power Supply Design
- Flow-Through Pinout
- Power Down High Impedance on LVDS Inputs
- Low Power Design (18 mW at 3.3-V static)
- Interoperable with Existing 5-V LVDS Networks
- Accepts Small Swing (350 mV Typical) Differential Signal Levels
- Supports Open, Short and Terminated Input Fail-Safe
- Conforms to ANSI/TIA/EIA-644 Standard
- Industrial Temperature Operating Range: −40°C to 85°C
- Available in SOIC and Space Saving WSON Package

2 Applications

- Multi-Function Printers
- LVDS-to-LVCMOS Translation
- Building and Factory Automation
- Grid Infrastructure

3 Description

The DS90LV028A is a dual CMOS differential line receiver designed for applications requiring ultra low power dissipation, low noise and high data rates. The device is designed to support data rates in excess of 400-Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV028A accepts low voltage (350 mV typical) differential input signals and translates them to 3-V CMOS output levels. The receiver also supports open, shorted and terminated (100 Ω) input fail-safe. The receiver output is HIGH for all fail-safe conditions. The DS90LV028A has a flow-through design for easy PCB layout.

The DS90LV028A and companion LVDS line driver provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90LV028A	SOIC (8)	4.90 mm × 3.91 mm
	WSON (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagram

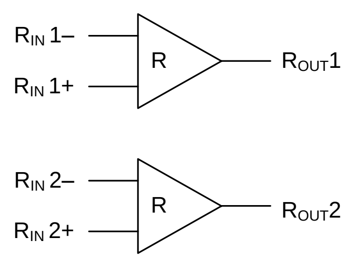


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F — **Page**

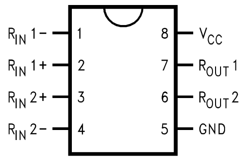
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Added Thermal Information values 4

Changes from Revision D (April 2013) to Revision E — **Page**

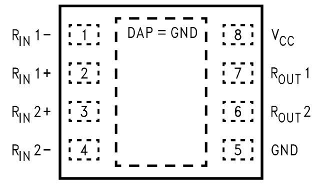
- Changed layout of National Semiconductor Data Sheet to TI format 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



NGN Package
8-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	5	—	Ground pin
$R_{IN}+$	2, 3	I	Noninverting receiver input pin
$R_{IN}-$	1, 4	I	Inverting receiver input pin
R_{OUT}	6, 7	O	Receiver output pin
V_{CC}	8	—	Power supply pin, 3.3 V ±0.3 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.3	4	V
Input voltage, $R_{IN}+$, $R_{IN}-$		–0.3	3.9	V
Output voltage, R_{OUT}		–0.3	V_{CC} + 0.3	V
Maximum package power dissipation at 25°C	D package		1025	mW
	Derate D package		8.2 mW/°C above 25°C	°C
	NGN package		3.3	W
	Derate NGN package		25.6 mW/°C above 25°C	°C
Lead temperature range, soldering (4 s)			260	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±7000	V
		Machine model (MM)(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) EIAJ, 0 Ω, 200 pF

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
	Receiver input voltage	GND		3	V
T_A	Operating free-air temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)			DS90LV028A		UNIT
			D (SOIC)	NGN (WSON)	
			8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance		—	35.9	°C/W
		Low-K thermal resistance	212	—	
		High-K thermal resistance	122	—	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		69.1	24.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		47.7	13.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter		15.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter		47.2	13.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{TH}	Differential input high threshold	V_{CM} = 1.2 V, 0 V, 3 V, R_{IN}+, R_{IN}− pins[3]				100	mV
V_{TL}	Differential input low threshold	V_{CM} = 1.2 V, 0 V, 3 V, R_{IN}+, R_{IN}− pins[3]		–100			mV
I_{IN}	Input current	V_{CC} = 3.6 V or 0 V, R_{IN}+, R_{IN}− pins	V_{IN} = 2.8 V	–10	±1	10	μA
			V_{IN} = 0 V	–10	±1	10	
		V_{CC} = 0 V, V_{IN} = 3.6 V, R_{IN}+, R_{IN}− pins		–20		20	
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{ID} = 200 mV, R_{OUT} pin		2.7	3.1		V
		I_{OH} = –0.4 mA, inputs terminated, R_{OUT} pin		2.7	3.1		
		I_{OH} = –0.4 mA, inputs shorted, R_{OUT} pin		2.7	3.1		
V_{OL}	Output low voltage	I_{OL} = 2 mA, V_{ID} = –200 mV, R_{OUT} pin			0.3	0.5	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V, R_{OUT} pin[4]		–15	–50	–100	mA
V_{CL}	Input clamp voltage	I_{CL} = –18 mA, R_{OUT} pin		–1.5	–0.8		V
I_{CC}	No load supply current	V_{CC} pin, inputs open			5.4	9	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).
(2) All typicals are given for: V_{CC} = 3.3 V and T_A = 25°C.
(3) V_{CC} is always higher than R_{IN}+ and R_{IN}− voltage. R_{IN}+ and R_{IN}− are allowed to have voltage range –0.05 V to 3.05 V. V_{ID} is not allowed to be greater than 100 mV when V_{CM} = 0 V or 3 V.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output must be shorted at a time, do not exceed maximum junction temperature specification.

6.6 Switching Characteristics

V_{CC} = 3.3 V ±10%, and T_A = −40°C to 85°C (unless otherwise noted)[1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHLD}	Differential propagation delay high to low	C_L = 15 pF	1	1.6	2.5	ns
t_{PLHD}	Differential propagation delay low to high	V_{ID} = 200 mV	1	1.7	2.5	ns
t_{SKD1}	Differential pulse skew $\|t_{PHLD} − t_{PLHD}\|$[3]	See Figure 18 and Figure 19	0	50	400	ps
t_{SKD2}	Differential channel-to-channel skew-same device[4]		0	0.1	0.5	ns
t_{SKD3}	Differential part to part skew[5]		0		1	ns
t_{SKD4}	Differential part to part skew[6]		0		1.5	ns
t_{TLH}	Rise Time			325	800	ps
t_{THL}	Fall Time			225	800	ps
f_{MAX}	Maximum operating frequency[7]		200	250		MHz

(1) C_L includes probe and jig capacitance.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
(3) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(4) t_{SKD2} is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(5) t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(6) t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Maximum − Minimum| differential propagation delay.
(7) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), load = 15 pF (stray plus probes).

6.7 Typical Characteristics

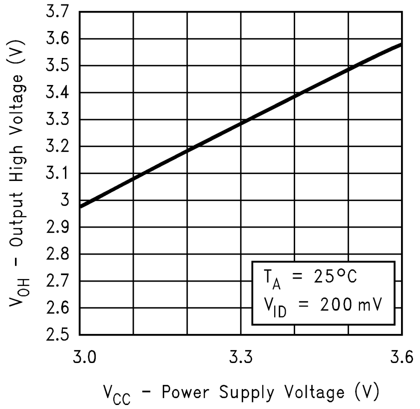


Figure 1. Output High Voltage vs Power Supply Voltage

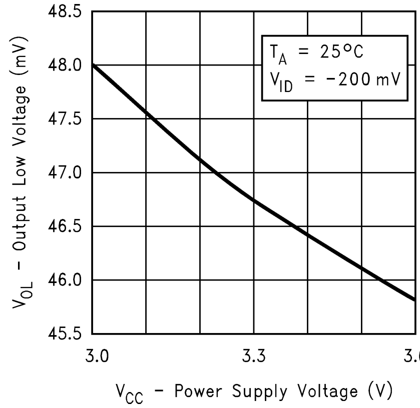


Figure 2. Output Low Voltage vs Power Supply Voltage

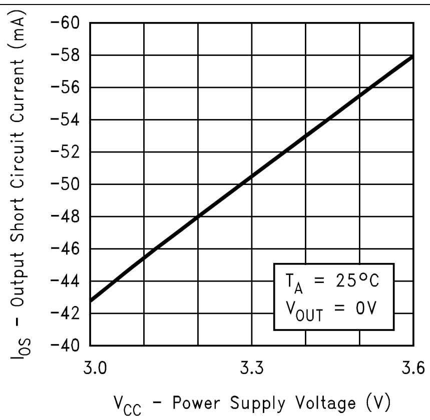


Figure 3. Output Short Circuit Current vs Power Supply Voltage

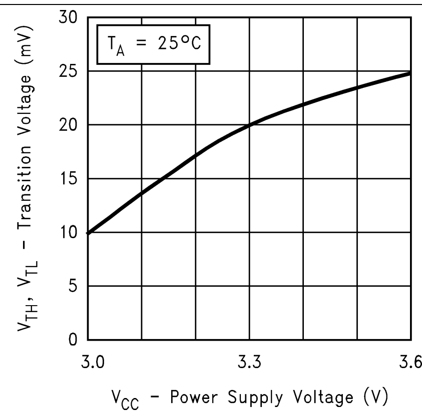


Figure 4. Differential Transition Voltage vs Power Supply Voltage

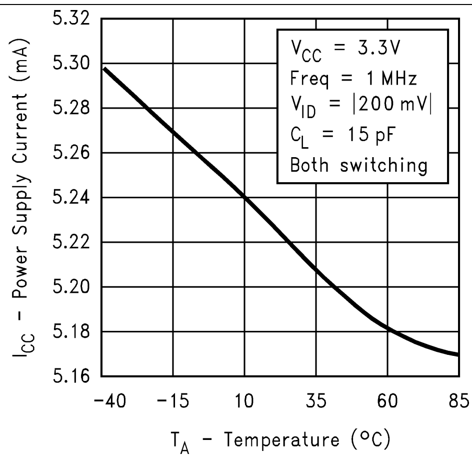


Figure 5. Power Supply Current vs Ambient Temperature

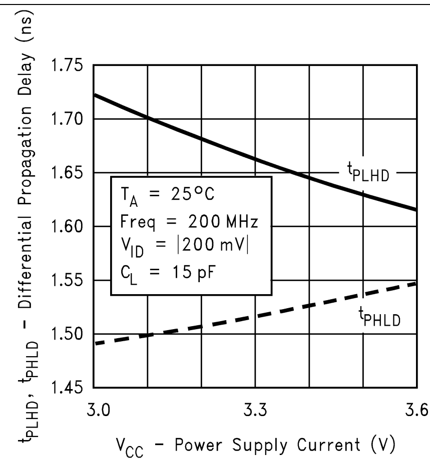


Figure 6. Differential Propagation Delay vs Power Supply Voltage

Typical Characteristics (continued)

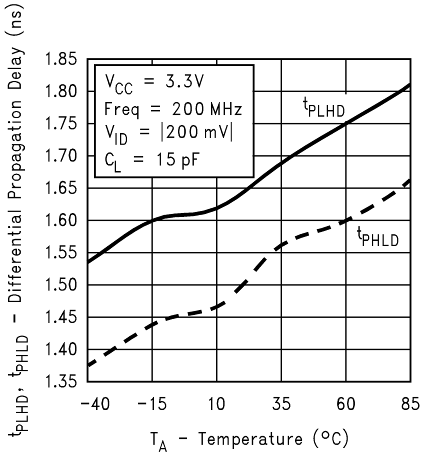


Figure 7. Differential Propagation Delay vs Ambient Temperature

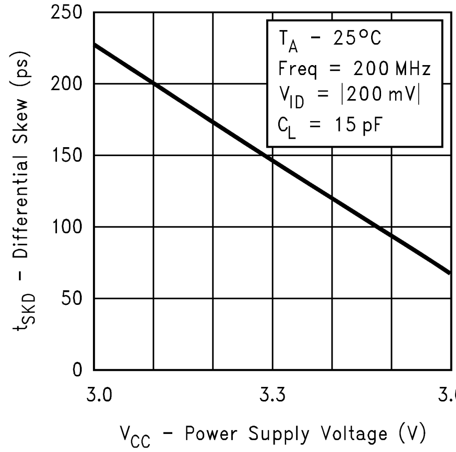


Figure 8. Differential Skew vs Power Supply Voltage

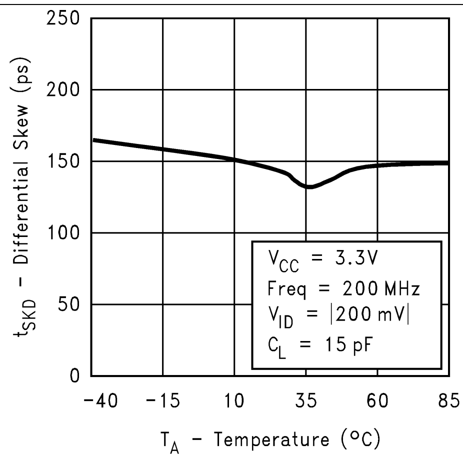


Figure 9. Differential Skew vs Ambient Temperature

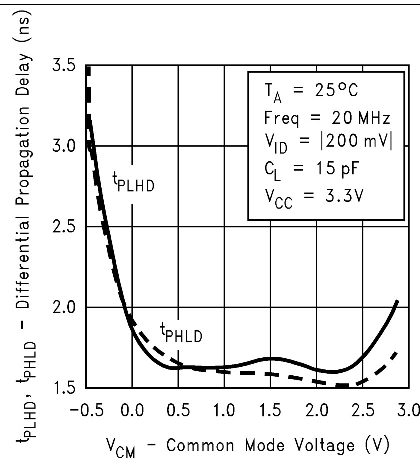


Figure 10. Differential Propagation Delay vs Common Mode Voltage

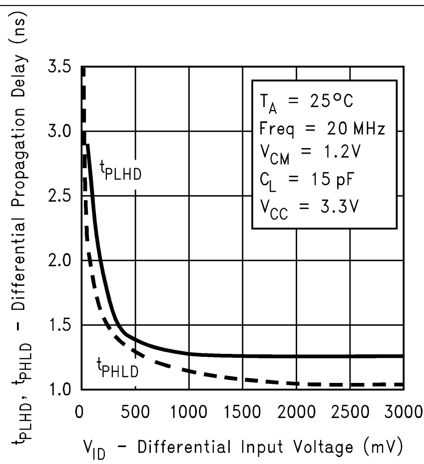


Figure 11. Differential Propagation Delay vs Differential Input Voltage

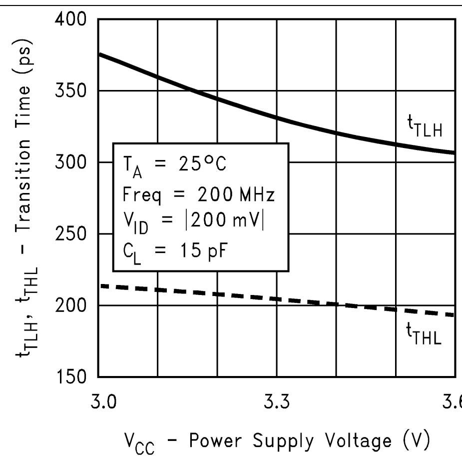


Figure 12. Transition Time vs Power Supply Voltage

Typical Characteristics (continued)

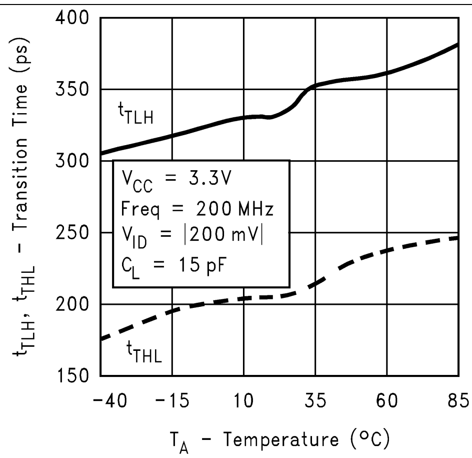


Figure 13. Transition Time vs Ambient Temperature

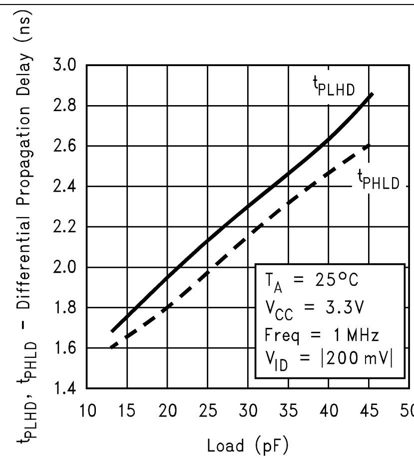


Figure 14. Differential Propagation Delay vs Load

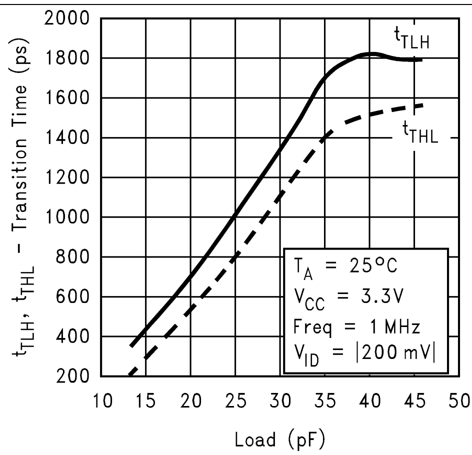


Figure 15. Transition Time vs Load

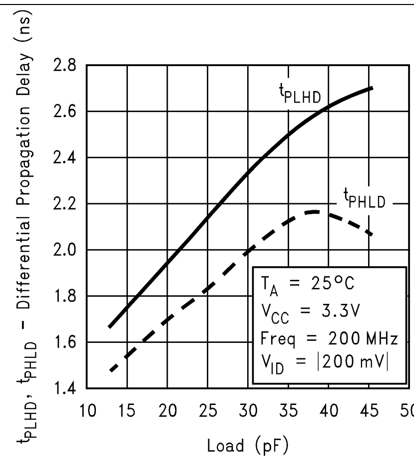


Figure 16. Differential Propagation Delay vs Load

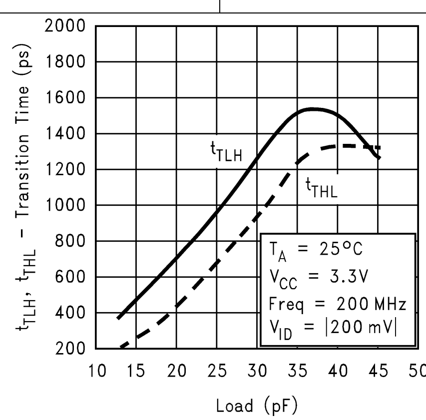


Figure 17. Transition Time vs Load

7 Parameter Measurement Information

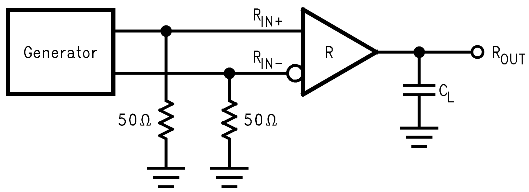


Figure 18. Receiver Propagation Delay and Transition Time Test Circuit

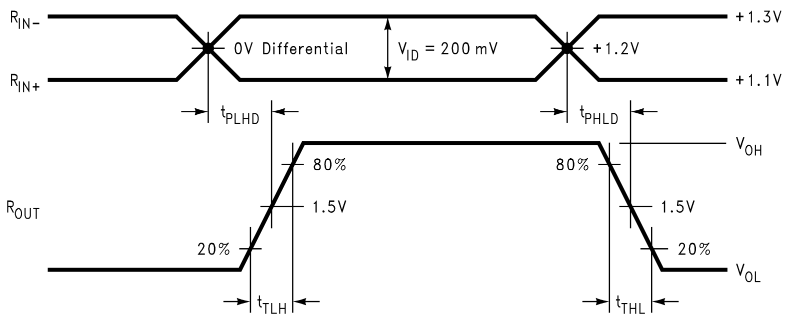


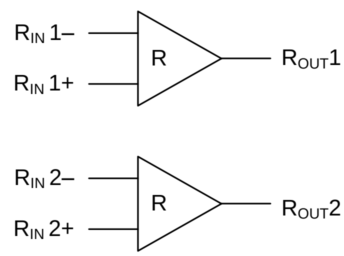
Figure 19. Receiver Propagation Delay and Transition Time Waveforms

8 Detailed Description

8.1 Overview

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 20. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω (selected to match the media), and is placed as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be considered.

8.2 Functional Block Diagram



8.3 Feature Description

The DS90LV028A differential line receiver is capable of detecting signals as low as 100 mV, over a ±1-V common mode range centered around 1.2 V. This is related to the driver offset voltage which is typically 1.2 V. The driven signal is centered around this voltage and may shift ±1 V around this center point. The ±1-V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0 V to 2.4 V (measured from each pin to ground). The device operates for receiver input voltages up to V_{CC}, but exceeding V_{CC} turns on the ESD protection circuitry which clamps the bus voltages.

Feature Description (continued)

8.3.1 Fail-Safe Feature

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20 mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, take care to prevent noise from appearing as a valid signal.

The internal fail-safe circuitry of the receiver is designed to source or sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. Open Input Pins: The DS90LV028A is a dual receiver device, and if an application requires only 1 receiver, the unused channel inputs must be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry ensures a HIGH, stable output state for open inputs.
2. Terminated Input: If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the receiver output is again in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10 mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common mode and not differential, a balanced interconnect must be used. Twisted pair cable offers better balance than flat ribbon cable.
3. Shorted Inputs: If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0 V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common mode range of the device (GND to 2.4 V). It is only supported with inputs shorted and no external common mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors must be in the 5-kΩ to 15-kΩ range to minimize loading and waveform distortion to the driver. The common mode bias point must be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry. Refer to *AN-1194 Failsafe Biasing of LVDS Interfaces* (SNLA051) for more information.

8.3.2 Cables and Connectors

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities.

Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5 M, most cables can be made to work effectively. For distances 0.5 M ≤ d ≤ 10 M, CAT 3 (category 3) twisted pair cable works well, is readily available, and relatively inexpensive.

8.4 Device Functional Modes

Table 1 lists the functional modes of the DS90LV028A.

Table 1. Truth Table

INPUTS	OUTPUT
$[R_{IN}+] - [R_{IN}-]$	**R_{OUT}**
$V_{ID} \geq 0.1$ V	H
$V_{ID} \leq -0.1$ V	L
Full fail-safe OPEN/SHORT or Terminated	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90LV028A has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

9.2 Typical Application

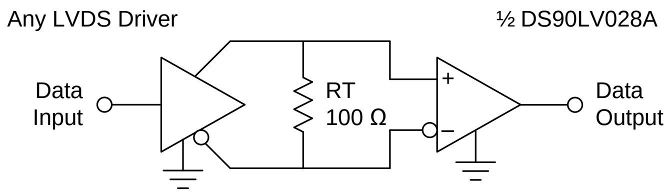


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Figure 20. Point-to-Point Application

9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces, cable assemblies, and connectors. All components of the transmission media must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities.

Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common mode (not differential mode) noise which is rejected by the LVDS receiver.

For cable distances < 0.5 M, most cables can be made to work effectively. For distances 0.5 M ≤ d ≤ 10 M, CAT5 (Category 5) twisted pair cable works well, is readily available, and relatively inexpensive.

9.2.2 Detailed Design Procedure

9.2.2.1 Probing LVDS Transmission Lines

Always use high impedance (>100 kΩ), low capacitance (<2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

9.2.2.2 Threshold

The LVDS Standard (ANSI/TIA/EIA-644) specifies a maximum threshold of ±100 mV for the LVDS receiver. The DS90LV028A supports an enhanced threshold region of −100 mV to 0 V. This is useful for fail-safe biasing. The threshold region is shown in the Voltage Transfer Curve (VTC) in Figure 21. The typical DS90LV028A LVDS receiver switches at about −35 mV.

NOTE

With V_{ID} = 0 V, the output is in a HIGH state. With an external fail-safe bias of 25 mV applied, the typical differential noise margin is now the difference from the switch point to the bias point.

Typical Application (continued)

In the following example, this would be 60 mV of Differential Noise Margin (25 mV − (−35 mV)). With the enhanced threshold region of −100 mV to 0 V, this small external fail-safe biasing of 25 mV (with respect to 0 V) gives a DNM of a comfortable 60 mV. With the standard threshold region of ±100 mV, the external fail-safe biasing would require 25 mV with respect to 100 mV or 125 mV, giving a DNM of 160 mV which is stronger fail-safe biasing than is necessary for the DS90LV028A. If more differential noise margin (DNM) is required, then a stronger fail-safe bias point can be set by changing resistor values.

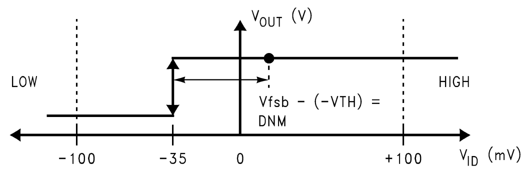

Figure 21. VTC of the DS90LV028A

9.2.3 Application Curve

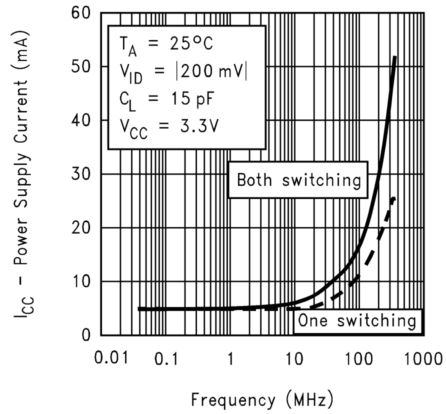

Figure 22. Power Supply Current vs Frequency

10 Power Supply Recommendations

Bypass capacitors must be used on power pins. TI recommends using high-frequency, ceramic, 0.1-µF and 0.01-µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-µF, 35-V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.

11 Layout

11.1 Layout Guidelines

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, and TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. Best practice places TTL and LVDS on different layers which are isolated by a power or ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

For PC board considerations for the WSON package, please refer to *AN-1187, Leadless Leadframe Package* (SNOA401). It is important to note that to optimize signal integrity (minimize jitter and noise coupling), the WSON thermal land pad, which is a metal (normally copper) rectangular region placed under the package as seen in Figure 23, must be attached to ground and match the dimensions of the exposed pad on the PCB (1:1 ratio).

11.1.1 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (that is, cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs must be <10 mm long). This helps eliminate reflections and ensure noise is coupled as common mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3 mm apart because magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and the EMI result. The velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps. Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces must be minimized to maintain common mode rejection of the receivers. On the printed-circuit board, this distance must remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

11.1.2 Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor must be between 90 Ω and 130 Ω. Remember that the current mode outputs require the termination resistor to generate the differential voltage. LVDS does not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% to 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs must be minimized. The distance between the termination resistor and the receiver must be <10 mm (12 mm maximum).

11.2 Layout Examples

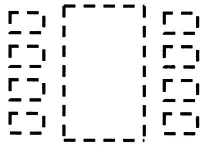

Figure 23. WSON Thermal Land Pad and Pin Pads

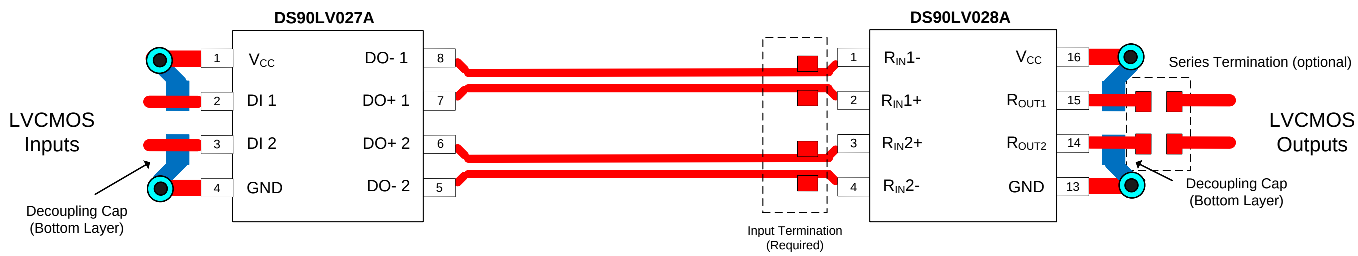

Figure 24. Simplified DS90LV027A and DS90LV028A Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *LVDS Owner's Manual* (SNLA187)
- *AN-808, Long Transmission Lines and Data Signal Quality* (SNLA028)
- *AN-977, LVDS Signal Quality: Jitter Measurements Using Eye Patterns Test Report* (SNLA166)
- *AN-971, An Overview of LVDS Technology* (SNLA165)
- *AN-916, A Practical Guide To Cable Selection* (SNLA219)
- *AN-805, Calculating Power Dissipation for Differential Line Drivers* (SNOA233)
- *AN-903, A Comparison of Differential Termination Techniques* (SNLA034)
- *AN-1194, Failsafe Biasing of LVDS Interfaces* (SNLA051)
- *AN-1187, Leadless Leadframe Package* (SNOA401)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV028ATLD/NOPB	ACTIVE	WSON	NGN	8	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	LV028AT	Samples
DS90LV028ATM	LIFEBUY	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	90LV0 28ATM	
DS90LV028ATM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	90LV0 28ATM	Samples
DS90LV028ATMX	LIFEBUY	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	90LV0 28ATM	
DS90LV028ATMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	90LV0 28ATM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DS90LV028A :

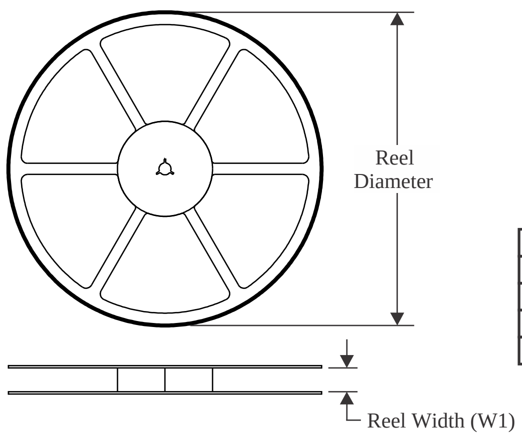
- Automotive : DS90LV028A-Q1

NOTE: Qualified Version Definitions:

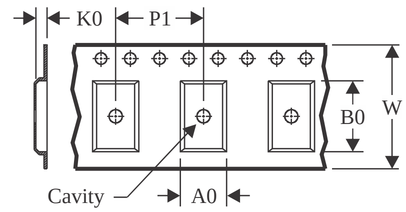
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

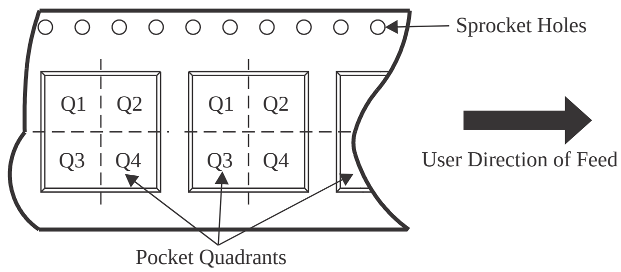


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

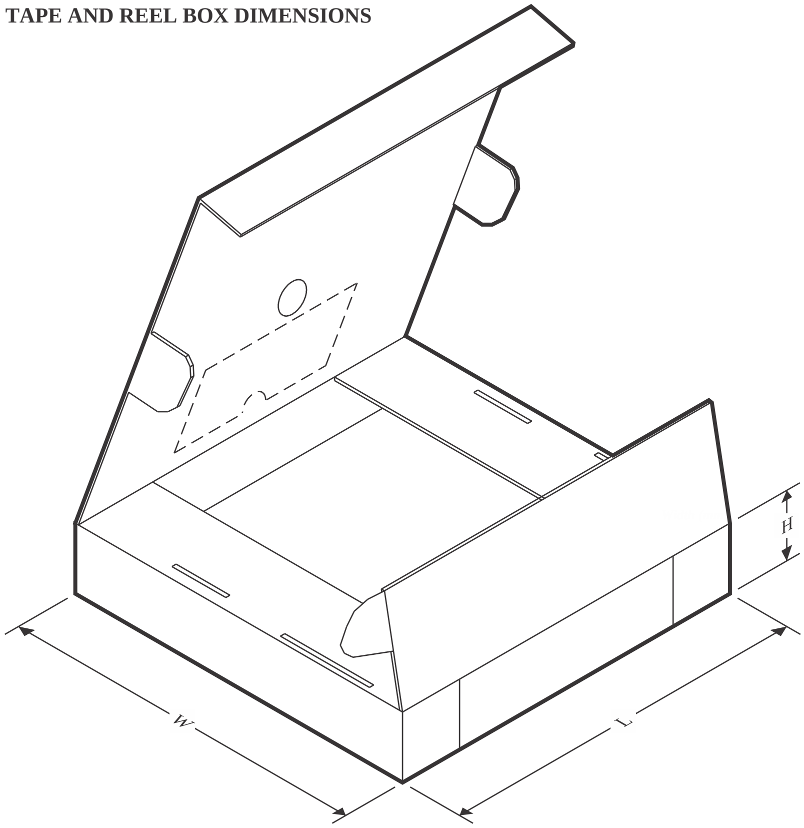
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV028ATLD/NOPB	WSON	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS90LV028ATMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS90LV028ATMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

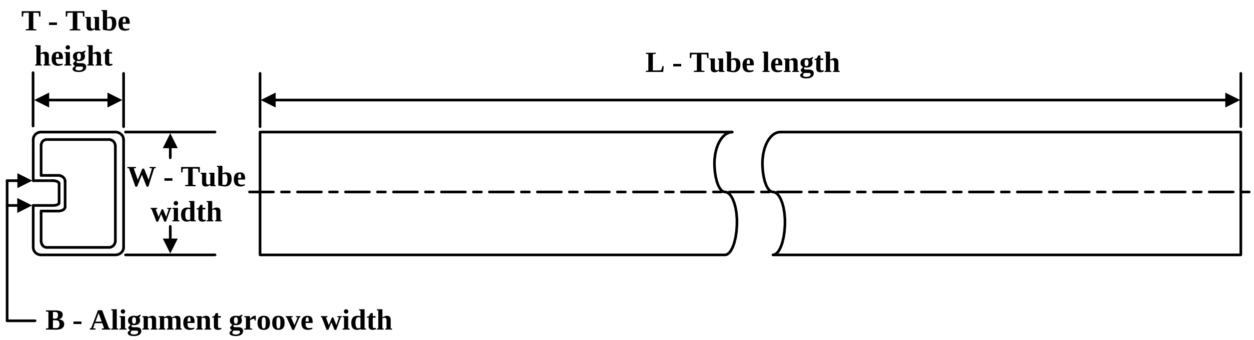
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

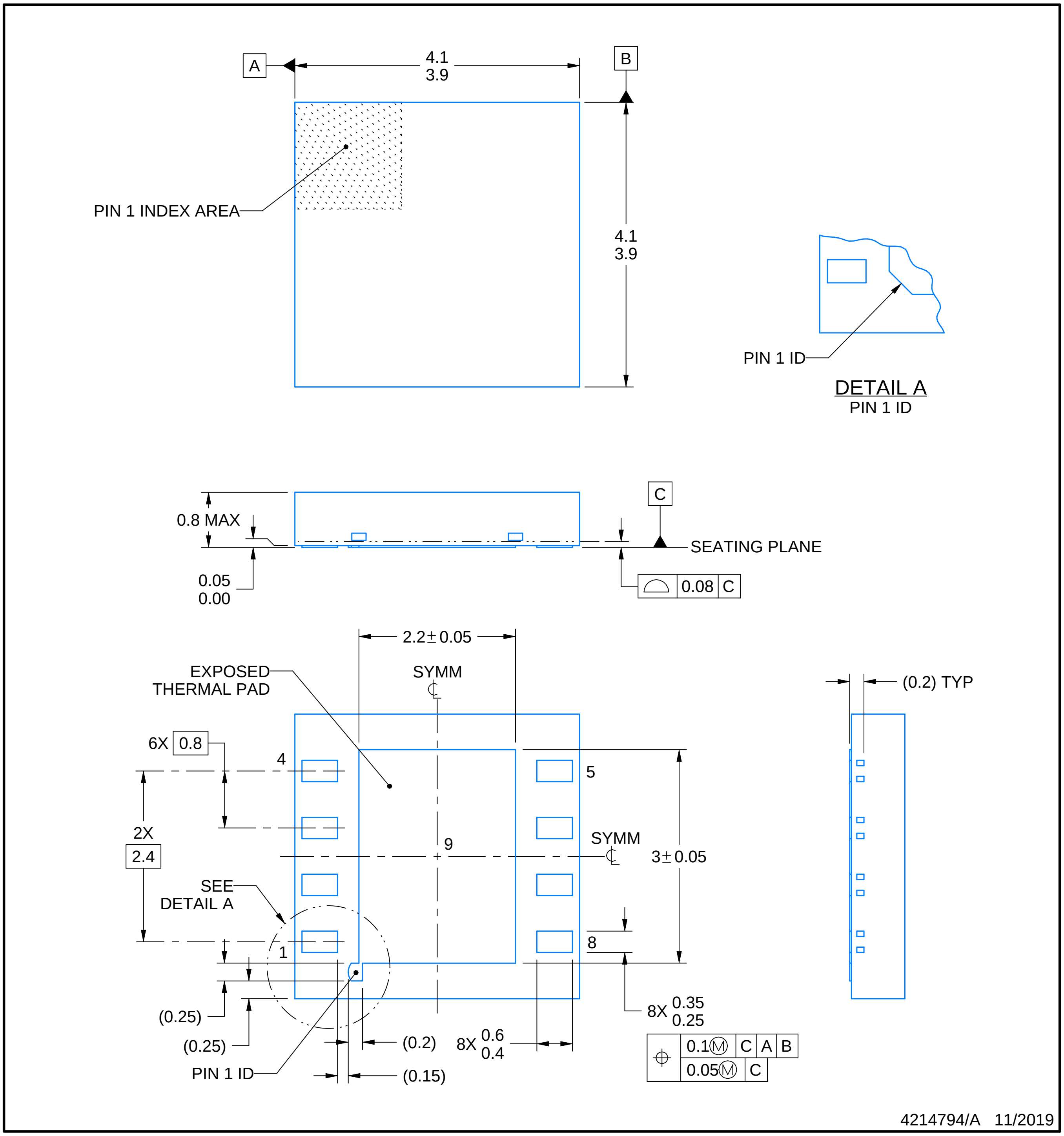
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV028ATLD/NOPB	WSON	NGN	8	1000	208.0	191.0	35.0
DS90LV028ATMX	SOIC	D	8	2500	367.0	367.0	35.0
DS90LV028ATMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



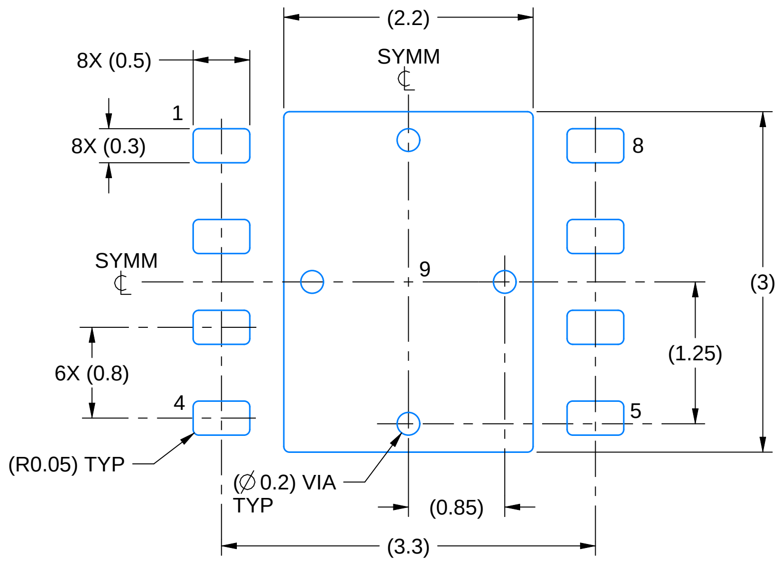
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90LV028ATM	D	SOIC	8	95	495	8	4064	3.05
DS90LV028ATM	D	SOIC	8	95	495	8	4064	3.05
DS90LV028ATM/NOPB	D	SOIC	8	95	495	8	4064	3.05

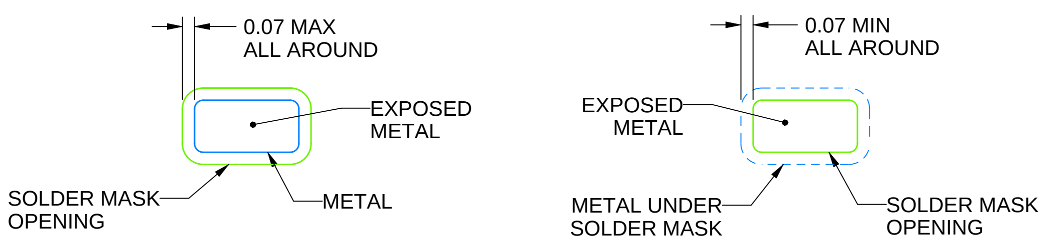


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

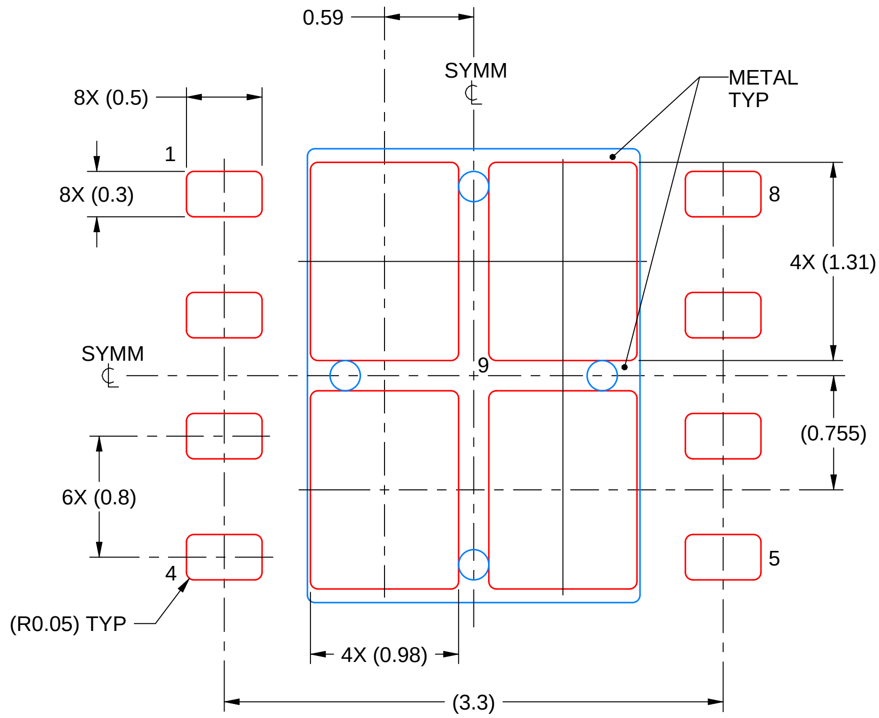
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214794/A 11/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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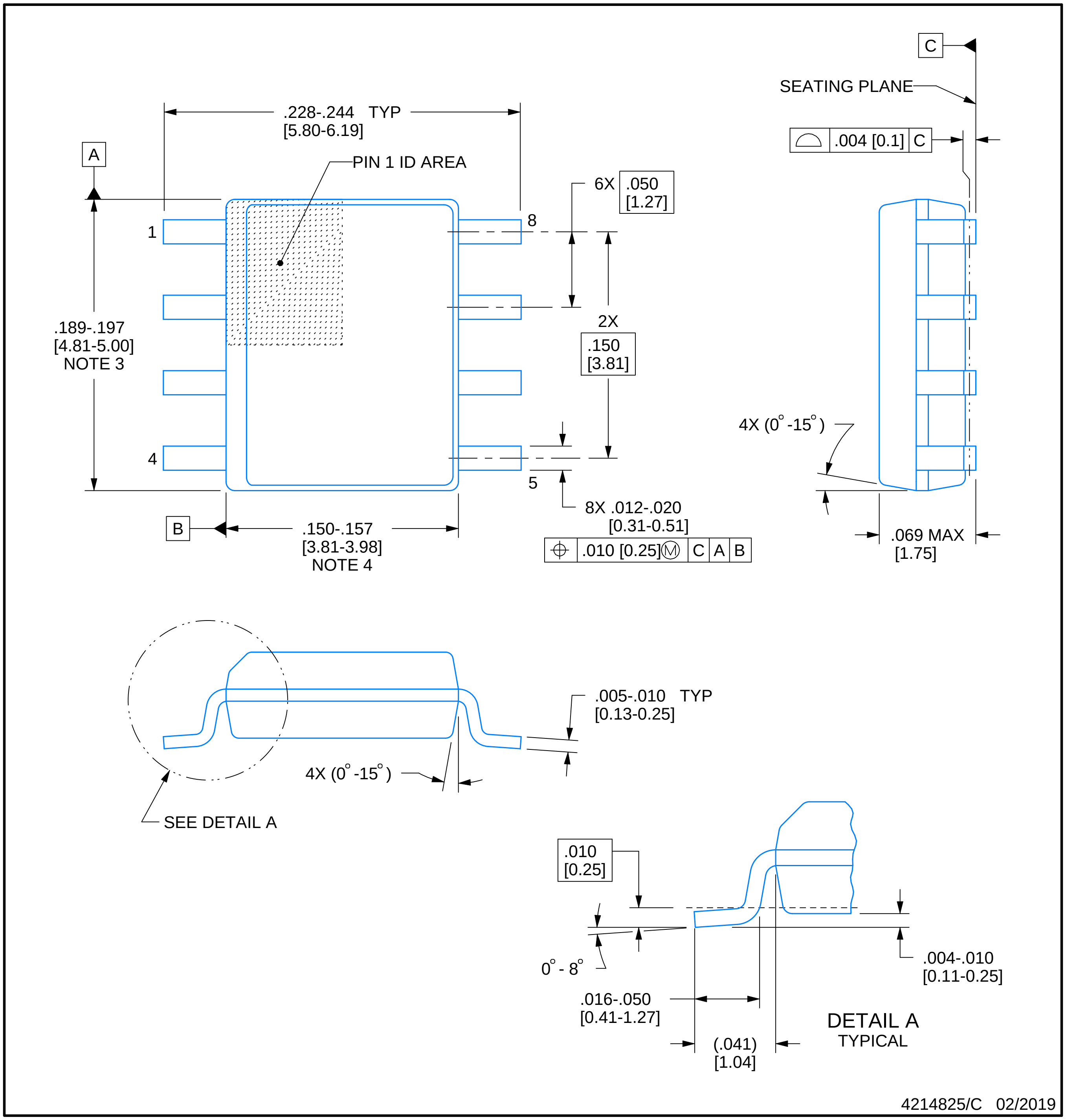
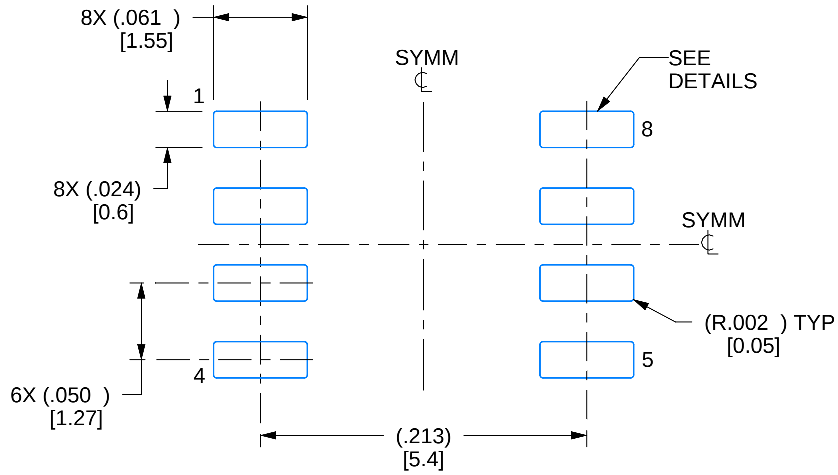
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

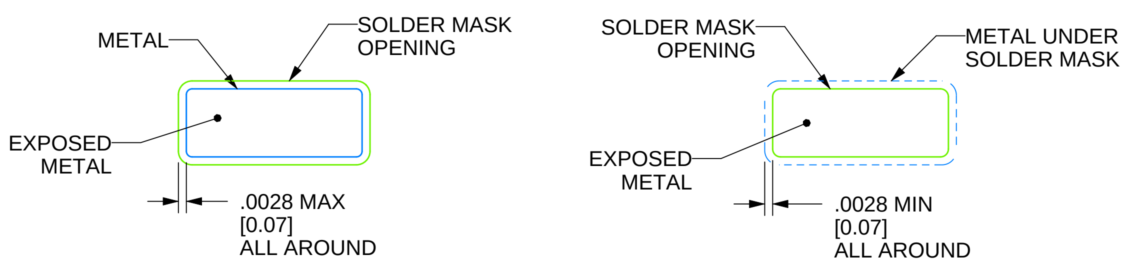


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

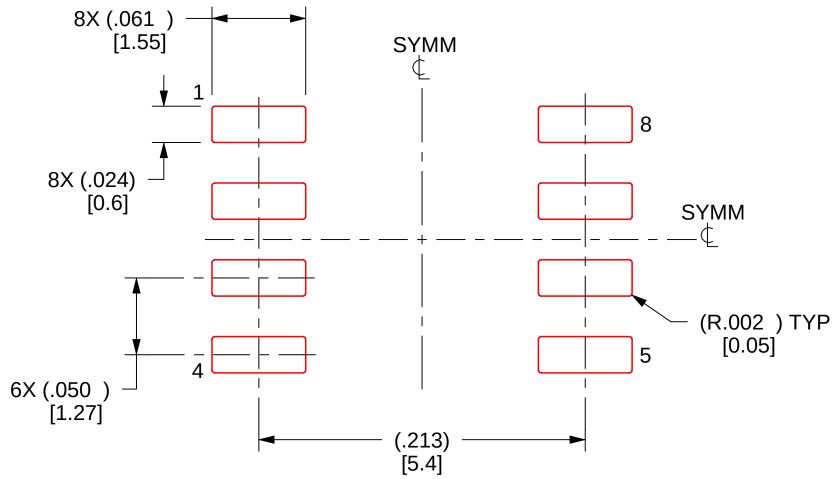
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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