DACx3508 采用微型 3 × 3 WQFN 封装的八路 10 位或 8 位 SPI 接口缓冲电压输出 DAC

1 特性

- ±1LSB INL 和 DNL
- 宽工作范围
  - 电源：1.8V 至 5.5V
  - 温度范围：–40°C 至 +125°C
- 3 线 SPI 接口
  - 2.7V ≤ V_{DD} ≤ 5.5V 时，VIH = 2.4V
  - 1.8V ≤ V_{DD} ≤ 2.7V 时，VIH = (V_{DD} – 0.3V)
- 通过 $\overline{\text{LDAC}}$ 引脚实现同步输出更新
- 功耗极低：0.1mA/通道 (1.8V)
- 低功耗启动模式：输出断电，并通过 10kΩ 连接至 A_{GND}。
- 微型封装
  - 16 引脚 WQFN (3mm × 3mm)

2 应用

- 多功能打印机
- 电视显示面板
- OLED 电视
- 虚拟现实耳麦
- 点钞机
- 自动取款机 (ATM)

3 说明

10 位 DAC53508 和 8 位 DAC43508 (DACx3508) 是低功耗、八通道、电压输出数模转换器 (DAC)。DACx3508 根据设计在 1.8V 至 5.5V 的宽电源电压范围内具有单调性。DACx3508 使用外部基准，可提供 1.8V 至 5.5V 的满标度输出电压范围，同时每通道消耗的静态电流为 0.1mA。DACx3508 还包括基于每通道且用户可编程的断电寄存器。这些寄存器有助于 DAC 输出缓冲器以 10kΩ-AGND 断电状态启动，并保持该状态，直到向这些输出缓冲器发出加电命令。

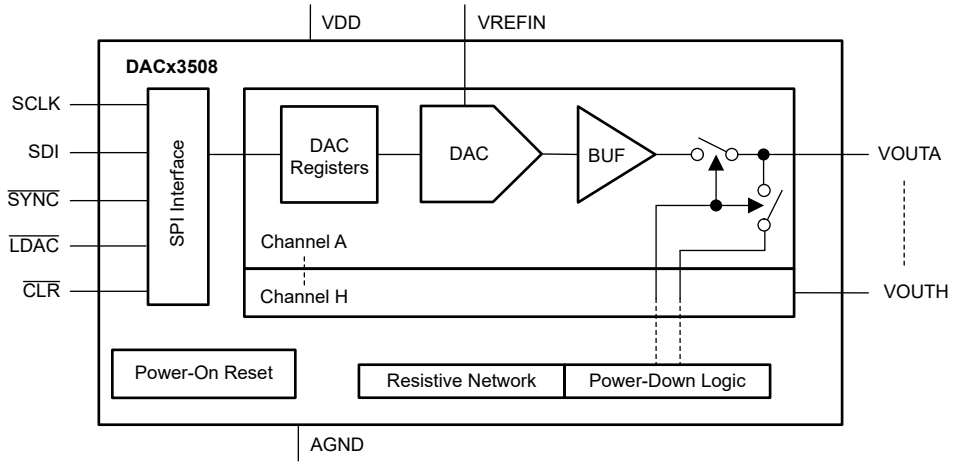
DACx3508 具有低静态电流、宽电源电压范围、八通道和每通道断电选项，因此非常适合高密度、低功耗的电池供电系统。

这些器件通过 3 线（只写）SPI 接口进行通信。这些器件还具有负载 DAC ($\overline{\text{LDAC}}$) 和清零 $\overline{\text{CLR}}$ 输入。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
DAC53508	WQFN (16)	3.00mm × 3.00mm
DAC43508		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



方框图

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4 Revision History

DATE	REVISION	NOTES
December 2021	*	Initial Release

5 Device Comparison Table

DEVICE	RESOLUTION
DAC53508	10-Bit
DAC43508	8-Bit

6 Pin Configurations and Functions

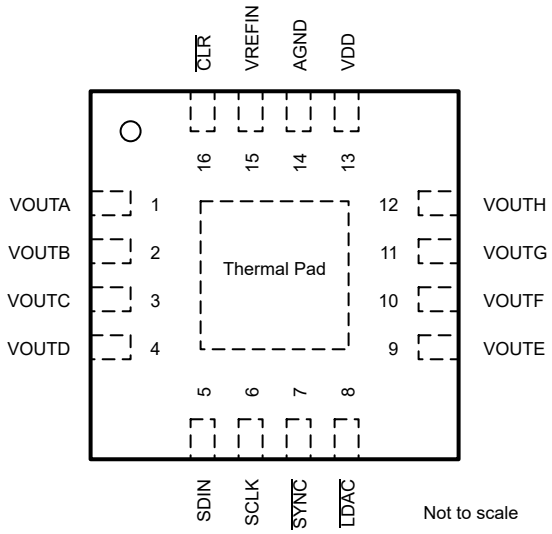


图 6-1. RTE (16-Pin WQFN) Package, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VOUTA	Output	Analog voltage output from DAC channel A.
2	VOUTB	Output	Analog voltage output from DAC channel B.
3	VOUTC	Output	Analog voltage output from DAC channel C.
4	VOUTD	Output	Analog voltage output from DAC channel D.
5	SDIN	Input	SPI data input.
6	SCLK	Input	SPI clock input.
7	$\overline{\text{SYNC}}$	Input	SPI chip select input (active low).
8	$\overline{\text{LDAC}}$	Input	Load DAC (active low) input for synchronous output update, simultaneous output update, or both.
9	VOUTE	Output	Analog voltage output from DAC channel E.
10	VOUTF	Output	Analog voltage output from DAC channel F.
11	VOUTG	Output	Analog voltage output from DAC channel G.
12	VOUTH	Output	Analog voltage output from DAC channel H.
13	VDD	Power	Power supply input (1.8 V to 5.5 V).
14	AGND	Ground	Ground reference for all circuitry on the device.
15	VREFIN	Power	External reference input. To use VDD as the reference, connect this pin to VDD.
16	$\overline{\text{CLR}}$	Input	Asynchronous output clear input (active low).
—	Thermal Pad	Ground	Connect thermal pad to AGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Power-supply voltage to A_{GND}	– 0.3	6	V
V_{REFIN}	External reference voltage to A_{GND}	– 0.3	V_{DD} + 0.3	V
	Digital input(s) to A_{GND}	– 0.3	V_{DD} + 0.3	V
V_{OUT}	Voltage output to A_{GND}	– 0.3	V_{DD} + 0.3	V
	Current into any pin	– 10	10	mA
T_J	Junction temperature,T_J	– 40	150	°C
T_{stg}	Storage temperature, T_{stg}	– 65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to A_{GND}	Positive supply voltage to ground	1.8		5.5	V
V_{REFIN} to A_{GND}	Reference input supply voltage to ground	1.8		V_{DD}	V
VIH	Digital input high voltage, 1.8 V ⩽ V_{DD} ⩽ 2.7 V	V_{DD} – 0.3			V
	Digital input high voltage, 2.7 V < V_{DD} ⩽ 5.5 V	2.4			
VIL	Digital input low voltage			0.5	V
T_A	Ambient temperature	– 40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DACx3508 RTE (WQFN) 16 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report.*

7.5 Electrical Characteristics

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specification at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{REFIN} = 2.5 V for V_{DD} ≥ 2.7 V, V_{REFIN} = 1.8 V for V_{DD} ≤ 2.7 V, R_L= 5 kΩ to A_{GND}, C_L = 200 pF to A_{GND}, and digital inputs at V_{DD} or A_{GND} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC53508	10			Bits
		DAC43508	8			
INL	Integral nonlinearity(1)		–1		1	LSB
DNL	Differential nonlinearity(1)		–1		1	LSB
	Zero-code error	Code 0d into DAC		6	12	mV
	Zero-code-error temperature coefficient	Code 0d into DAC		±5		µV/°C
	Offset error(1)		–0.5	0.25	0.5	%FSR
	Offset-error temperature coefficient(1)			±0.0003		%FSR/°C
	Gain error(1)		–0.5	0.25	0.5	%FSR
	Gain-error temperature coefficient(1)			±0.0004		%FSR/°C
	Full-scale error(4)	2.7 V ≤ V_{DD} ≤ 5.5 V	–0.5	0.25	0.5	%FSR
		1.8 V ≤ V_{DD} ≤ 2.7 V	–1	0.5	1	
	Full-scale-error temperature coefficient(4)			±0.0004		%FSR/°C
OUTPUT						
V_{OUTX}	Output voltage		0		5.5	V
C_L	Capacitive load(2)	R_L = Infinite			1	nF
					2	
	Load regulation	DAC at midscale, –10 mA ≤ I_{OUT} ≤ +10 mA, V_{DD} = 5.5 V		0.1		mV/mA
	Short-circuit current(3)	V_{DD} = 1.8 V		10		mA
		V_{DD} = 2.7 V		25		
		V_{DD} = 5.5 V		50		
	Output voltage headroom	To V_{DD}, DAC output unloaded		0.05		V
	Output voltage headroom(2)	To V_{DD}, load current = 10 mA at V_{DD} = 5.5 V, load current = 3 mA at V_{DD} = 2.7 V, load current = 1 mA at V_{DD} = 1.8 V, DAC code at full-scale	10			%FSR
Z_O	DC output impedance	DAC at midscale		0.25		Ω
		DAC at code 4d		0.25		
		DAC at code 1016d		0.26		
DC PSRR	Power supply rejection ratio (dc)	DAC at midscale, V_{DD} = 5 V ±10%		0.25		mV/V

7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40°C to +125°C and all typical specification at T_A = 25°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{REFIN} = 2.5 V for V_{DD} ≥ 2.7 V, V_{REFIN} = 1.8 V for V_{DD} ≤ 2.7 V, R_L= 5 kΩ to A_{GND}, C_L = 200 pF to A_{GND}, and digital inputs at V_{DD} or A_{GND} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
t_{sett}	Output voltage settling time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, V_{DD} = 5.5 V		10		µs
SR	Slew rate	V_{DD} = 5.5 V		0.6		V/µs
	Power-on glitch magnitude			110		mV
V_n	Output noise	f = 0.1 Hz to 10 Hz, DAC at midscale, V_{DD} = 5.5 V		40		μV_{pp}
V_n	Output noise	f = 0.1 Hz to 100 kHz, DAC at midscale, V_{DD} = 5.5 V		0.05		mV_{rms}
V_n	Output noise density	f = 1 kHz, DAC at midscale, V_{DD} = 5.5 V		0.2		µV/√Hz
		f = 10 kHz, DAC at midscale, V_{DD} = 5.5 V		0.2		
AC PSRR	Power-supply rejection ratio (ac)	200-mV, 50-Hz or 60-Hz sine wave superimposed on power-supply voltage, DAC at midscale		–71		dB
	Channel-to-channel ac crosstalk	Full-scale swing on adjacent channel		1.5		nV-s
	Channel-to-channel dc crosstalk	Full-scale swing on all channels, measured channel at zero-scale or full-scale		0.05		LSB
	Code change glitch impulse	±1-LSB change around midscale (including feedthrough)		10		nV-s
	Code change glitch impulse magnitude	±1-LSB change around midscale (including feedthrough)		25		mV
VOLTAGE REFERENCE INPUT						
	Reference input impedance	All channels powered on		12.5		kΩ
	Reference input capacitance			50		pF
DIGITAL INPUTS						
	Digital feedthrough	SCLK = 1 MHz, DAC output static at midscale		20		nV-s
	Pin capacitance	Per pin		10		pF
POWER						
I_{DD}	Current flowing into V_{DD}	Normal mode, all DACs at full-scale, SPI static		3	5	mA
		All DAC channels powered down		50		µA

(1) End point fit between codes: code 4d to code 1016d for 10 bit, code 1d to code 251d for 8 bit.
(2) Characterized by design. Not production tested.
(3) Full-scale output shorted per channel to A_{GND} or zero-scale output shorted to V_{DD}.
(4) Code 1023d into DAC, no headroom.

7.6 Timing Requirements: SPI

All inputs signals are specified with $t_R = t_F$ = 1 V/ns (10% to 90% of V_{DD}) and timed from a voltage level of $V_{DD}/2$, 1.8 V ≤ V_{DD} ≤ 5.5 V and –40°C ≤ T_A ≤ +125°C

		MIN	NOM	MAX	UNIT
$f_{(SCLK)}$	Serial clock frequency, 1.7 V ≤ V_{DD} < 2.7 V			25	MHz
	Serial clock frequency, 2.7 V ≤ V_{DD} ≤ 5.5 V			50	
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ V_{DD} < 2.7 V	20			ns
	SCLK high time, 2.7 V ≤ V_{DD} ≤ 5.5 V	10			
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ V_{DD} < 2.7 V	20			ns
	SCLK low time, 2.7 V ≤ V_{DD} ≤ 5.5 V	10			
t_{SDIS}	SDI setup time, 1.7 V ≤ V_{DD} < 2.7 V	16			ns
	SDI setup time, 2.7 V ≤ V_{DD} ≤ 5.5 V	8			
t_{SDIH}	SDI hold time, 1.7 V ≤ V_{DD} < 2.7 V	10			ns
	SDI hold time, 2.7 V ≤ V_{DD} ≤ 5.5 V	5			
t_{CSS}	$\overline{SYNC}$ to SCLK falling edge setup time, 1.7 V ≤ V_{DD} < 2.7 V	36			ns
	$\overline{SYNC}$ to SCLK falling edge setup time, 2.7 V ≤ V_{DD} ≤ 5.5 V	18			
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge, 1.7 V ≤ V_{DD} < 2.7 V	10			ns
	SCLK falling edge to $\overline{SYNC}$ rising edge, 2.7 V ≤ V_{DD} ≤ 5.5 V	5			
t_{CSHIGH}	$\overline{SYNC}$ high time, 1.7 V ≤ V_{DD} < 2.7 V	50			ns
	$\overline{SYNC}$ high time, 2.7 V ≤ V_{DD} ≤ 5.5 V	25			

7.7 Timing Requirements: Logic

all input signals are timed from VIL to 70% of V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V, 1.8 V ≤ V_{REFIN} ≤ V_{DD}, –40°C ≤ T_A ≤ +125°C, V_{pullup} = V_{DD} for 1.8 V ≤ V_{DD} ≤ 2.7 V, V_{pullup} = 2.7 V or V_{DD} for 2.7 V ≤ V_{DD} ≤ 5.5 V

		MIN	NOM	MAX	UNIT
$t_{CS2LDAC}$	$\overline{SYNC}$ rise edge to $\overline{LDAC}$ fall edge, 1.7 V ≤ V_{DD} < 2.7 V	100			ns
	$\overline{SYNC}$ rise edge to $\overline{LDAC}$ fall edge, 2.7 V ≤ V_{DD} ≤ 5.5 V	50			
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ V_{DD} < 2.7 V	60			ns
	$\overline{LDAC}$ low time, 2.7 V ≤ V_{DD} ≤ 5.5 V	30			
t_{CLRW}	$\overline{CLR}$ low time, 1.7 V ≤ V_{DD} < 2.7 V	60			ns
	$\overline{CLR}$ low time, 2.7 V ≤ V_{DD} ≤ 5.5 V	30			

7.8 Timing Diagrams

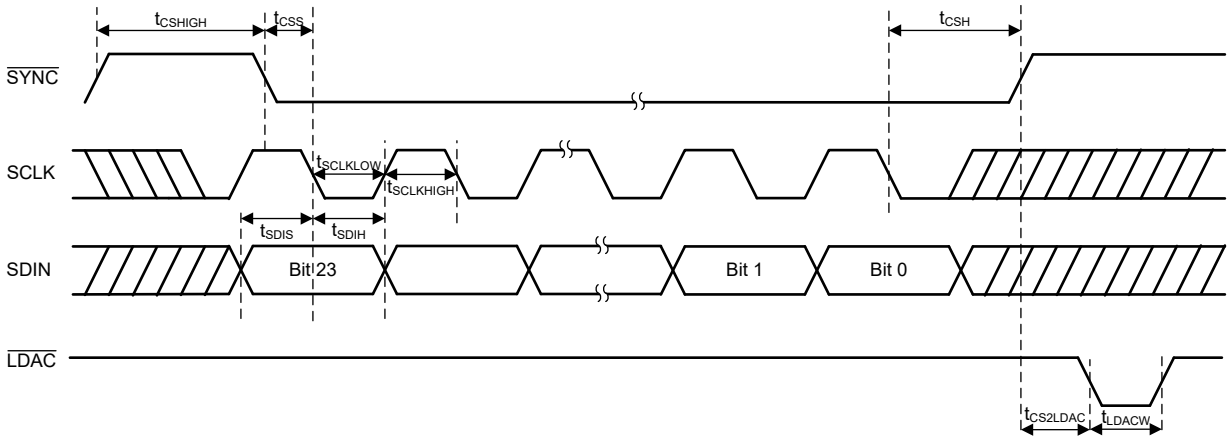
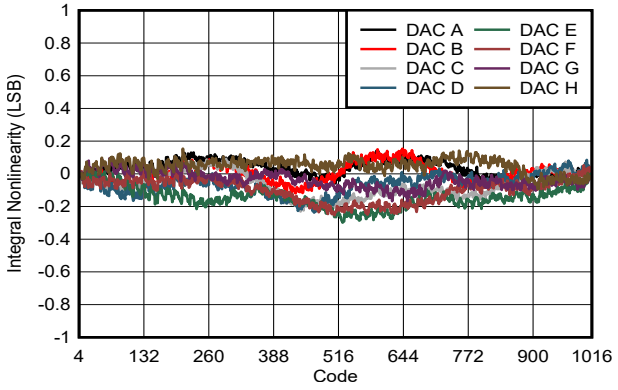


图 7-1. Serial Interface Timing Diagram

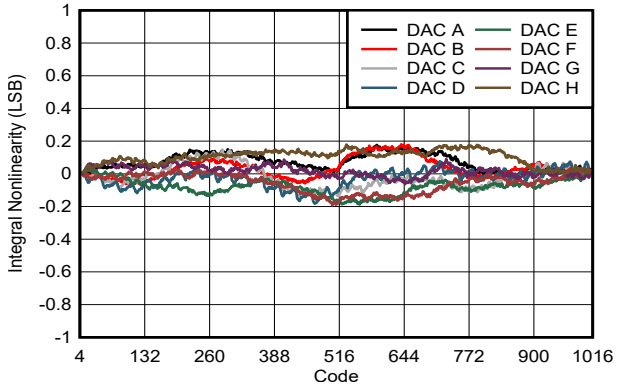
7.9 Typical Characteristics: Static Performance

at T_A = 25°C, reference = 1.8 V, and DAC outputs unloaded (unless otherwise noted)



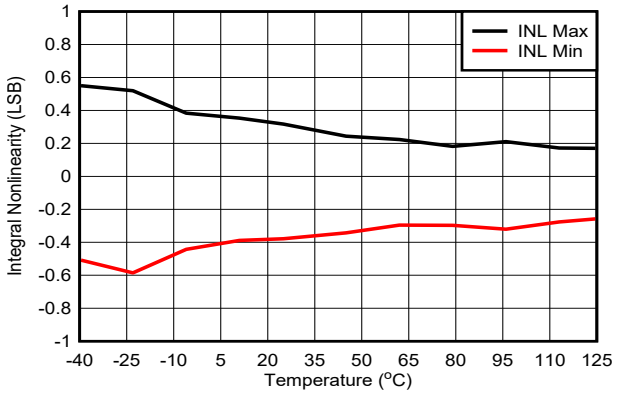
V_{DD} = 1.8 V

图 7-2. Integral Nonlinearity vs Digital Input Code



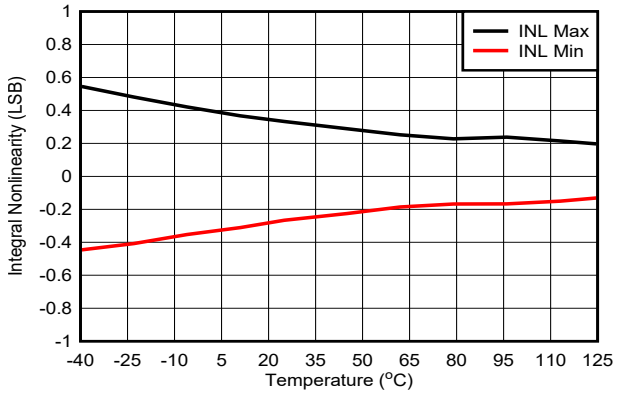
V_{DD} = 5.5 V

图 7-3. Integral Nonlinearity vs Digital Input Code



V_{DD} = 1.8 V

图 7-4. Integral Nonlinearity vs Temperature



V_{DD} = 5.5 V

图 7-5. Integral Nonlinearity vs Temperature

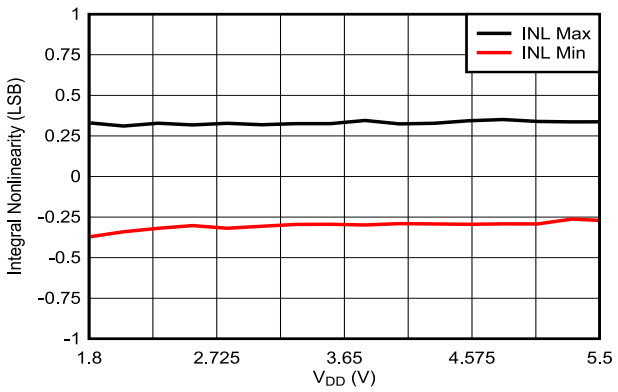
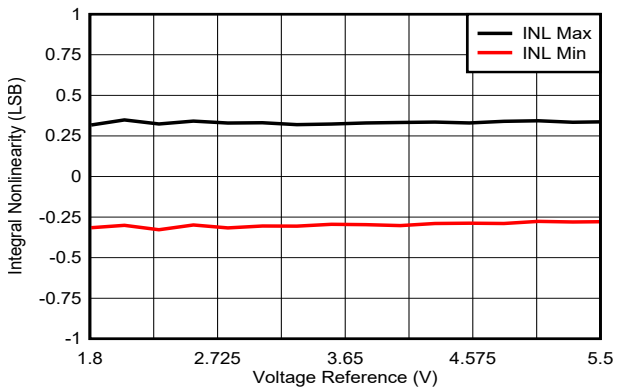


图 7-6. Integral Nonlinearity vs Supply Voltage

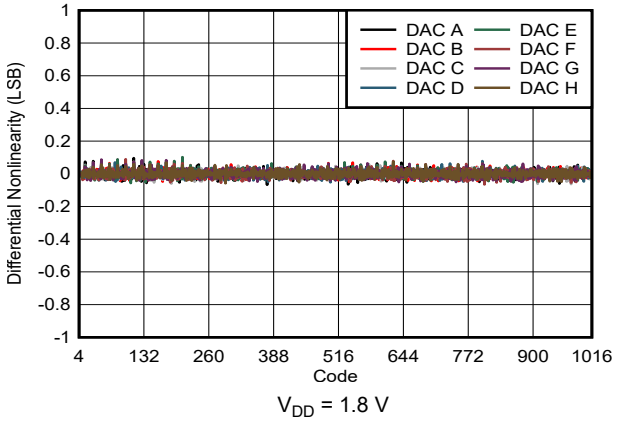


V_{DD} = 5.5 V

图 7-7. Integral Nonlinearity vs Voltage Reference

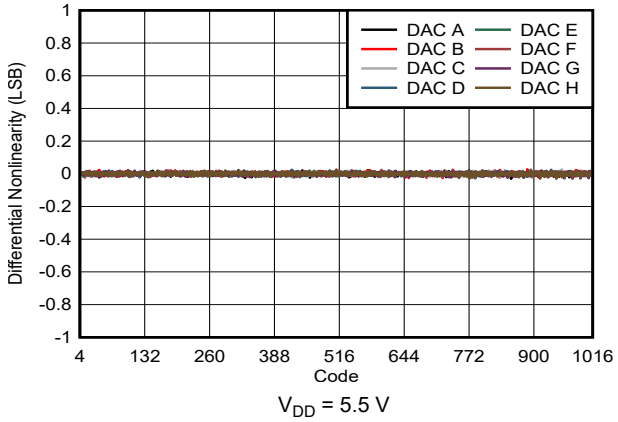
7.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, and DAC outputs unloaded (unless otherwise noted)



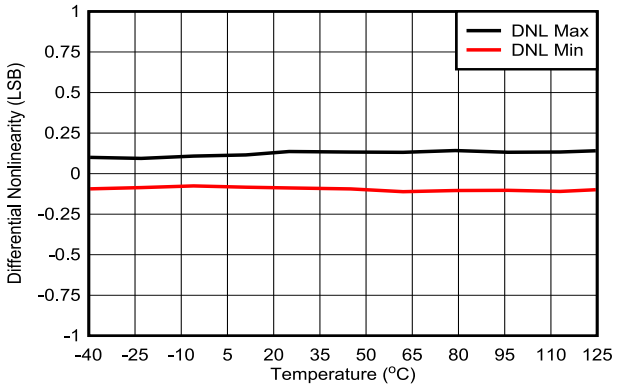
V_{DD} = 1.8 V

图 7-8. Differential Nonlinearity vs Digital Input Code



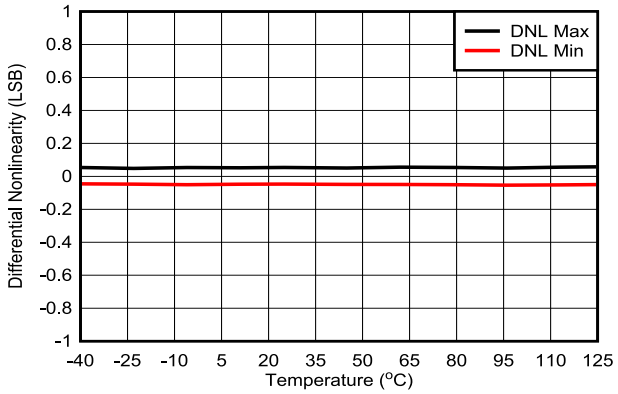
V_{DD} = 5.5 V

图 7-9. Differential Nonlinearity vs Digital Input Code



V_{DD} = 1.8 V

图 7-10. Differential Nonlinearity vs Temperature



V_{DD} = 5.5 V

图 7-11. Differential Nonlinearity vs Temperature

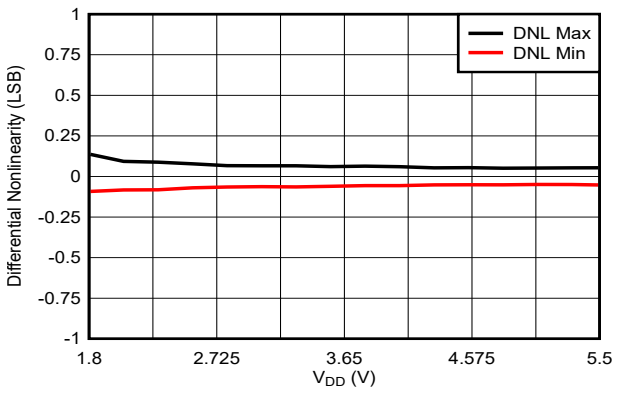


图 7-12. Differential Nonlinearity vs Supply Voltage

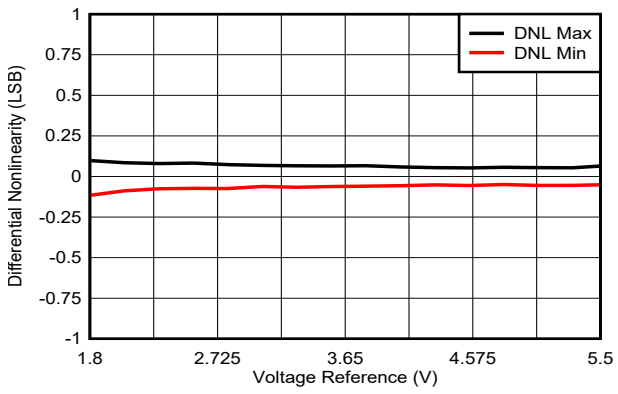
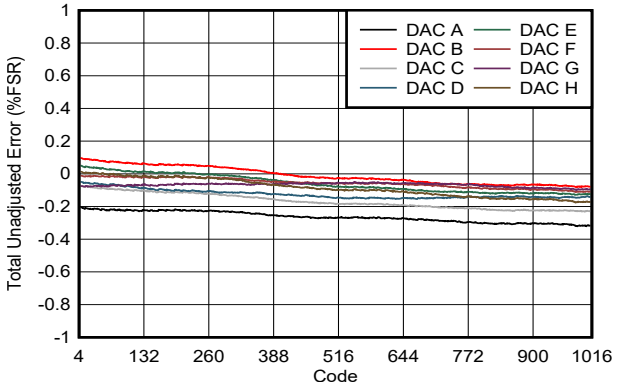


图 7-13. Differential Nonlinearity vs Voltage Reference

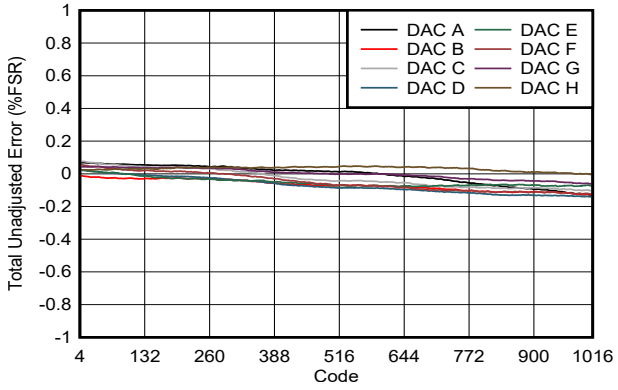
7.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, and DAC outputs unloaded (unless otherwise noted)



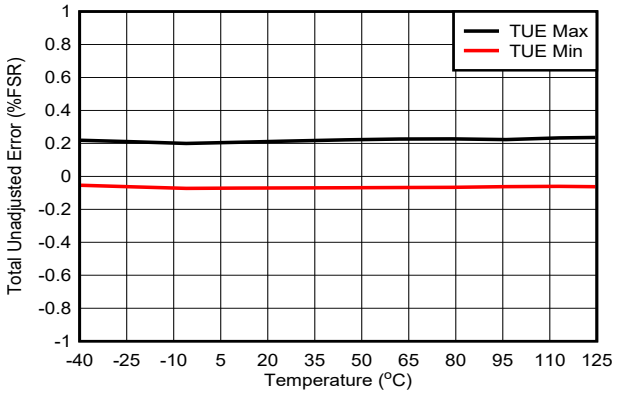
V_{DD} = 1.8 V

图 7-14. Total Unadjusted Error vs Digital Input Code



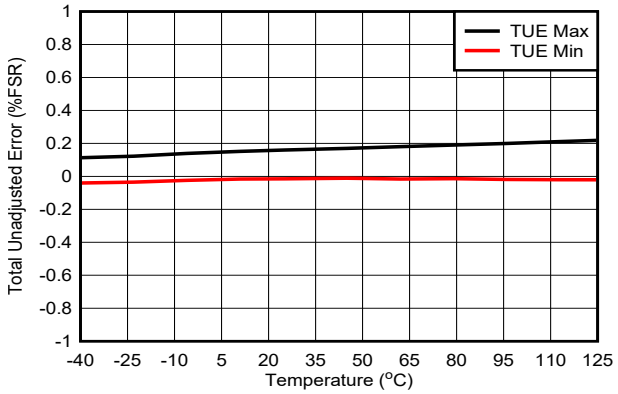
V_{DD} = 5.5 V

图 7-15. Total Unadjusted Error vs Digital Input Code



V_{DD} = 1.8 V

图 7-16. Total Unadjusted Error vs Temperature



V_{DD} = 5.5 V

图 7-17. Total Unadjusted Error vs Temperature

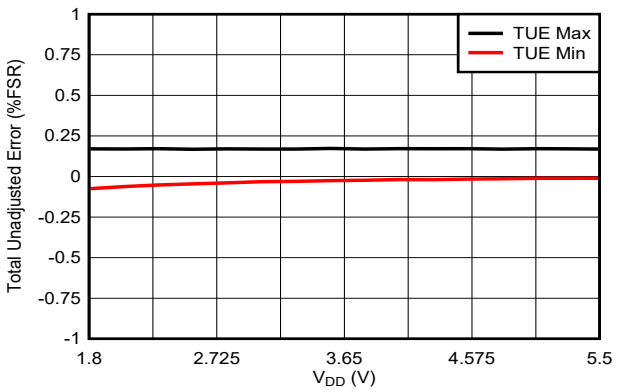
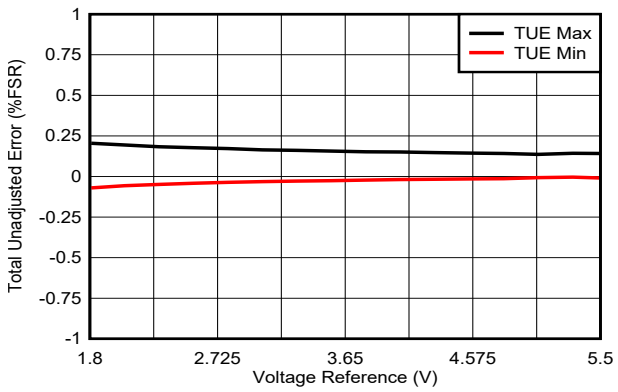


图 7-18. Total Unadjusted Error vs Supply Voltage



V_{DD} = 5.5 V

图 7-19. Total Unadjusted Error vs Voltage Reference

7.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, and DAC outputs unloaded (unless otherwise noted)

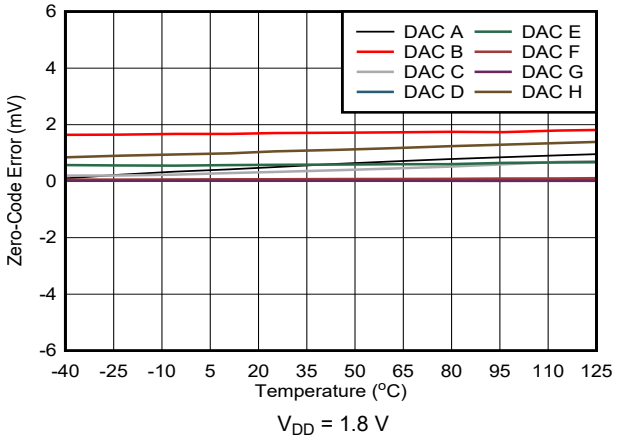


图 7-20. Zero-Code Error vs Temperature

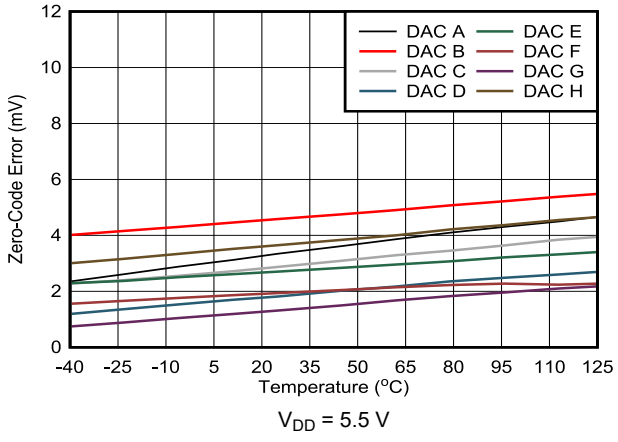


图 7-21. Zero-Code Error vs Temperature

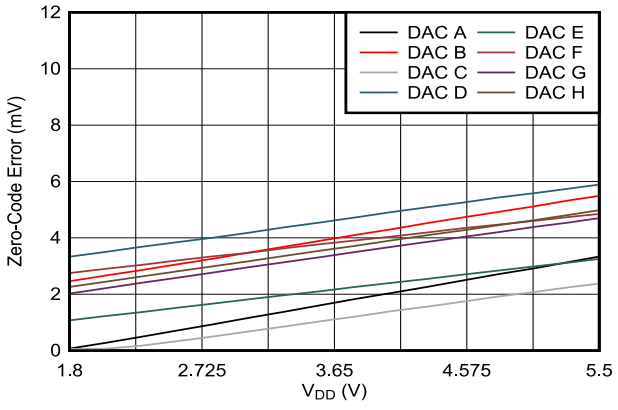


图 7-22. Zero-Code Error vs Supply Voltage

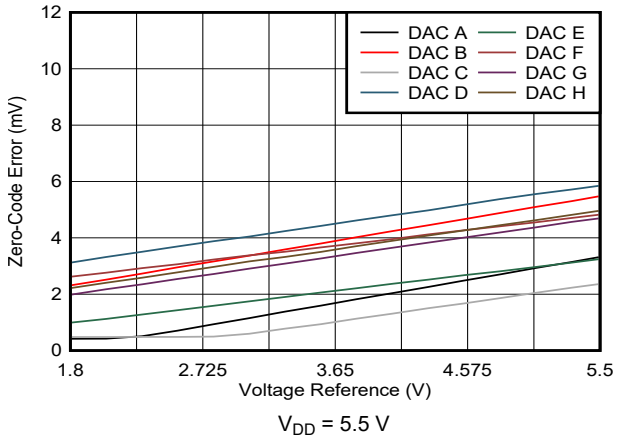


图 7-23. Zero-Code Error vs Voltage Reference

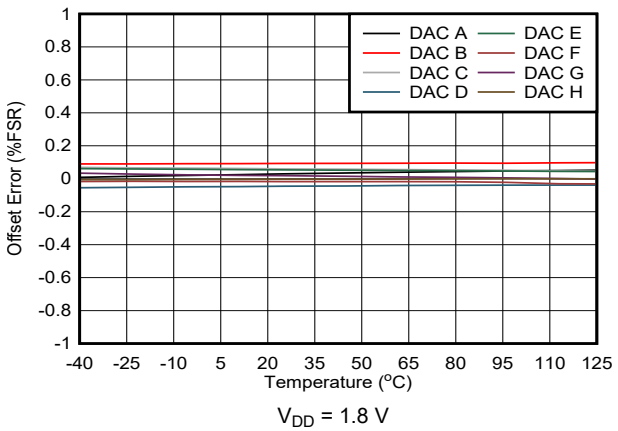


图 7-24. Offset Error vs Temperature

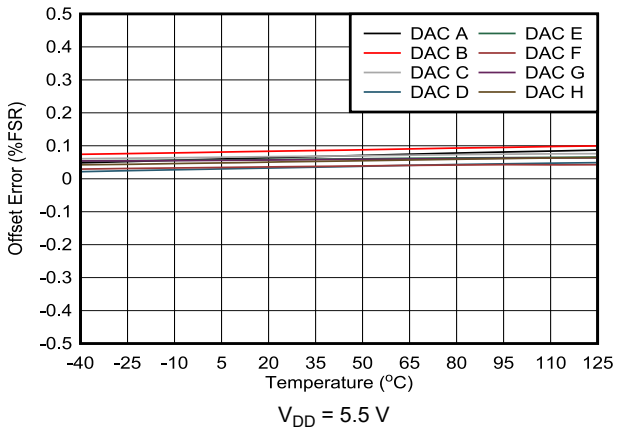


图 7-25. Offset Error vs Temperature

7.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, and DAC outputs unloaded (unless otherwise noted)

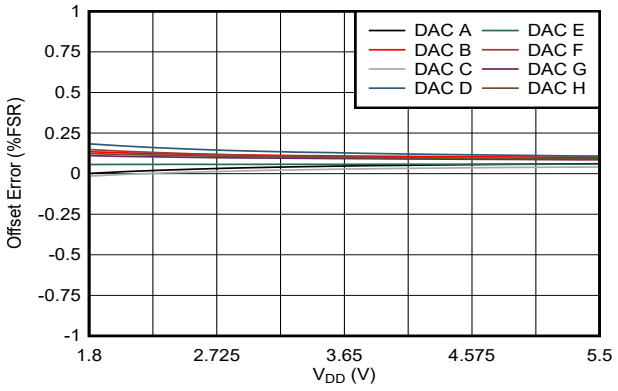


图 7-26. Offset Error vs Supply Voltage

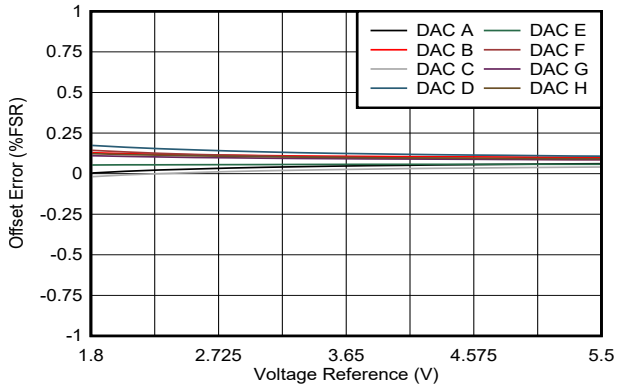


图 7-27. Offset Error vs Voltage Reference

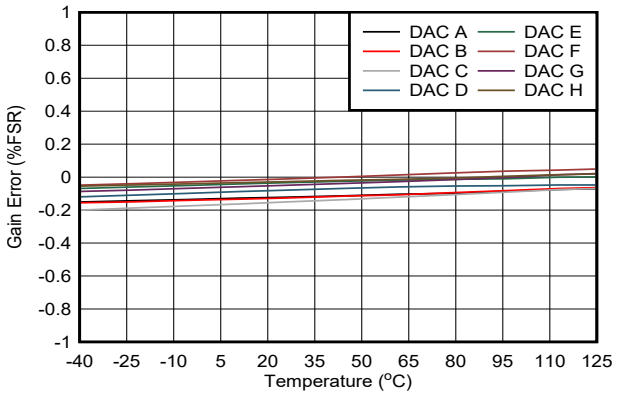


图 7-28. Gain Error vs Temperature

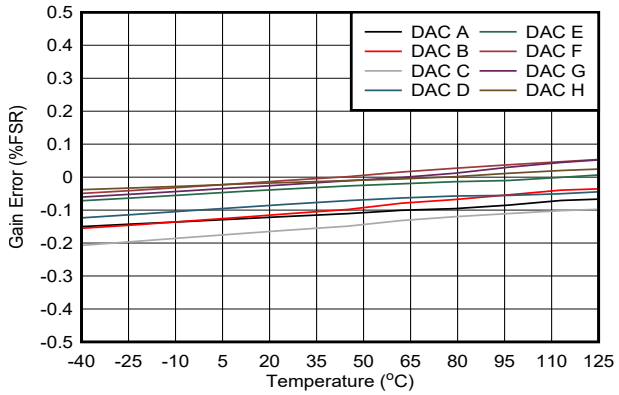


图 7-29. Gain Error vs Temperature

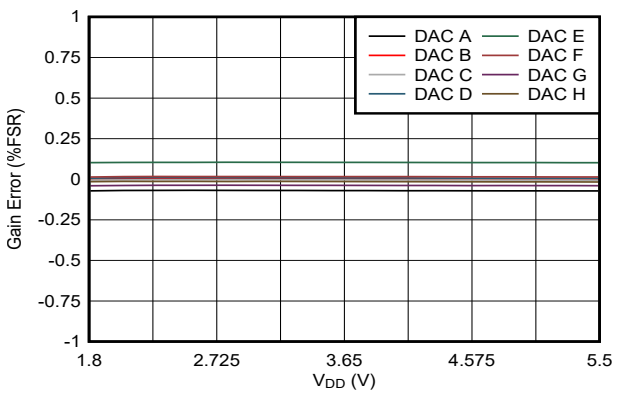


图 7-30. Gain Error vs Supply Voltage

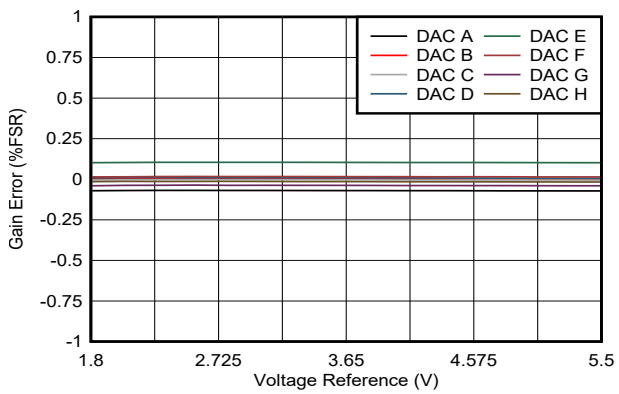
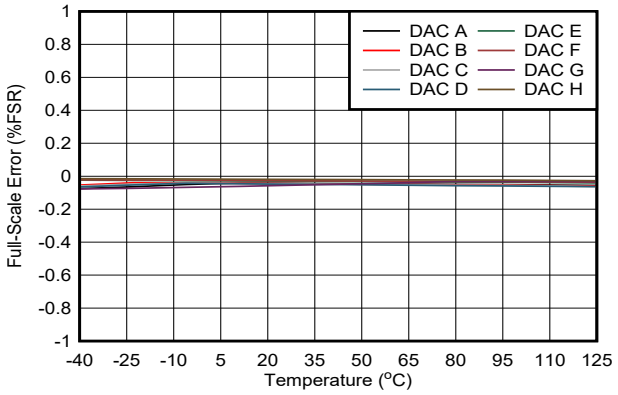


图 7-31. Gain Error vs Voltage Reference

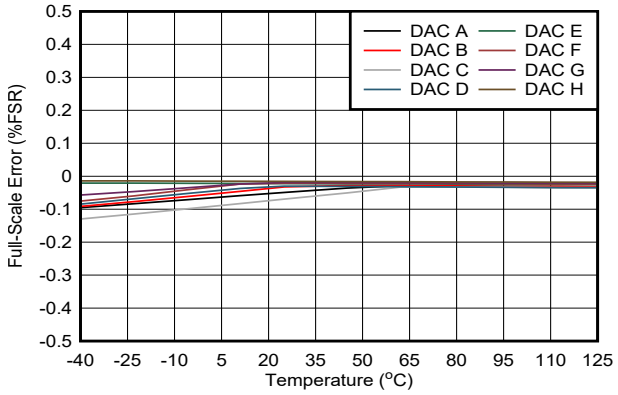
7.9 Typical Characteristics: Static Performance (continued)

at T_A = 25°C, reference = 1.8 V, and DAC outputs unloaded (unless otherwise noted)



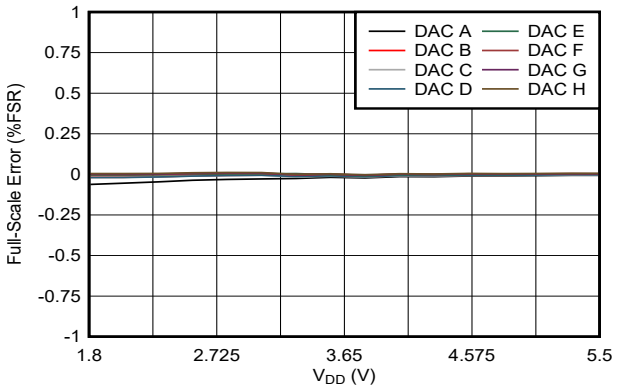
V_{DD} = 1.8 V

图 7-32. Full-Scale Error vs Temperature



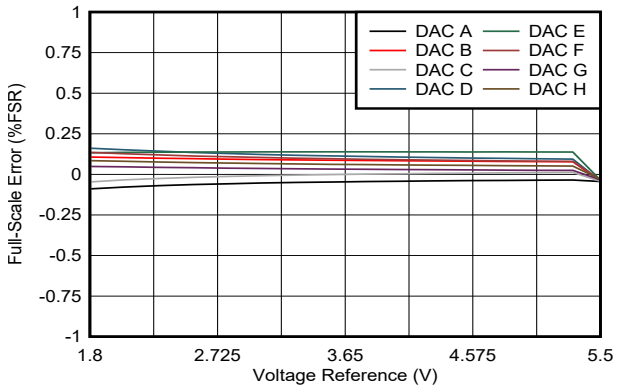
V_{DD} = 5.5 V

图 7-33. Full-Scale Error vs Temperature



V_{DD} = 5.5 V

图 7-34. Full-Scale Error vs Supply Voltage

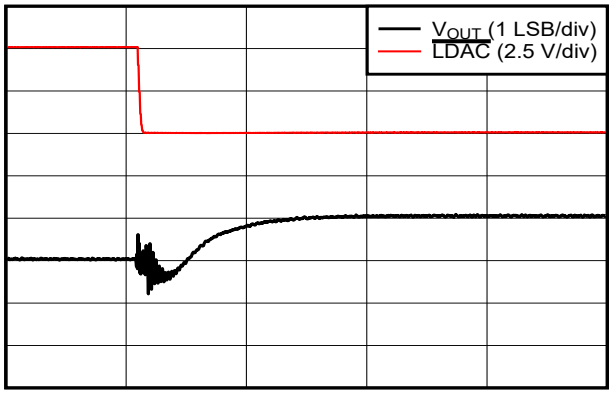


V_{DD} = 5.5 V

图 7-35. Full-Scale Error vs Voltage Reference

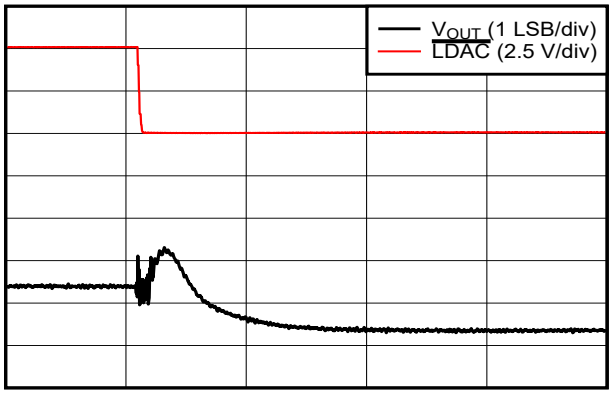
7.10 Typical Characteristics: Dynamic Performance

at T_A = 25°C, V_{DD} = 5.5 V, reference = 5.5 V, and DAC outputs unloaded (unless otherwise noted)



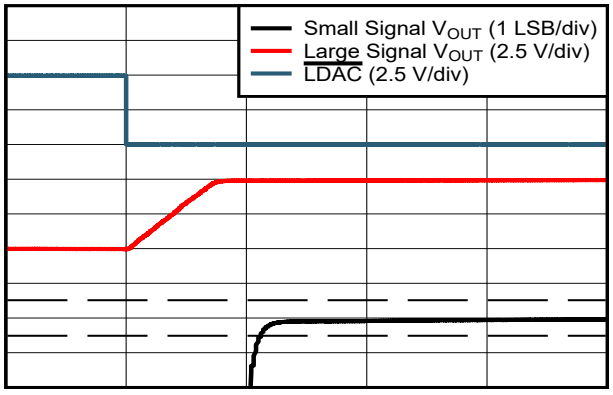
DAC code transition from midscale – 1 to midscale, output load: 5 kΩ || 200 pF

图 7-36. Glitch Impulse, Rising Edge, 1-LSB Step



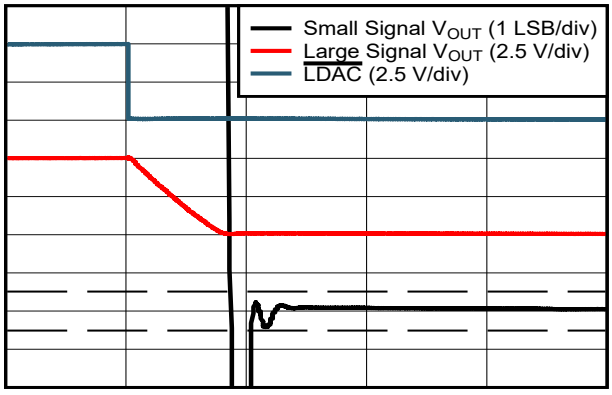
DAC code transition from midscale to midscale – 1 LSB, output load: 5 kΩ || 200 pF

图 7-37. Glitch Impulse, Falling Edge, 1 LSB Step



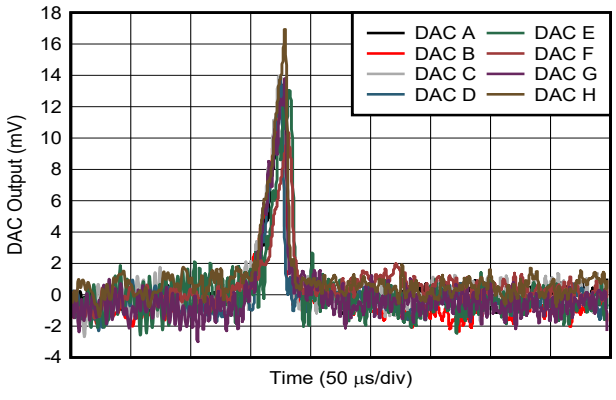
DAC code transition from 102d to 922d, typical channel shown, output load: 5 kΩ || 200 pF

图 7-38. Full-Scale Settling Time, Rising Edge



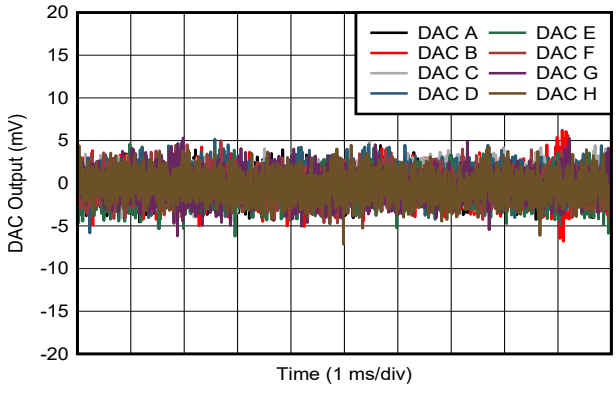
DAC code transition from 922d to 102d, typical channel shown, output load: 5 kΩ || 200 pF

图 7-39. Full-Scale Settling Time, Falling Edge



Output load: 5 kΩ || 200 pF

图 7-40. Power-on Glitch

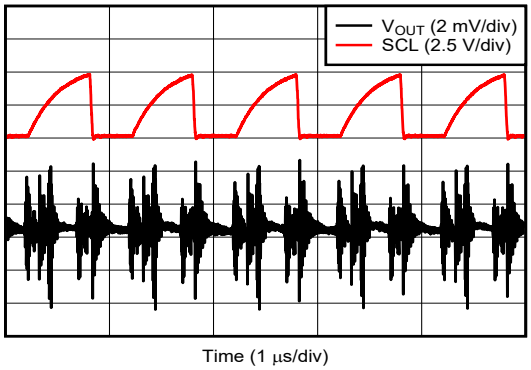


Output load: 5 kΩ || 200 pF

图 7-41. Power-off Glitch

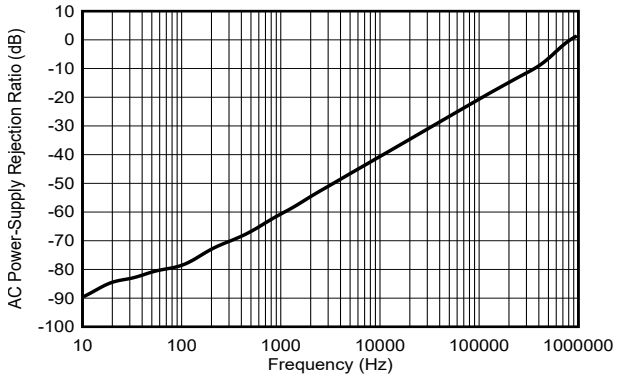
7.10 Typical Characteristics: Dynamic Performance (continued)

at T_A = 25°C, V_{DD} = 5.5 V, reference = 5.5 V, and DAC outputs unloaded (unless otherwise noted)



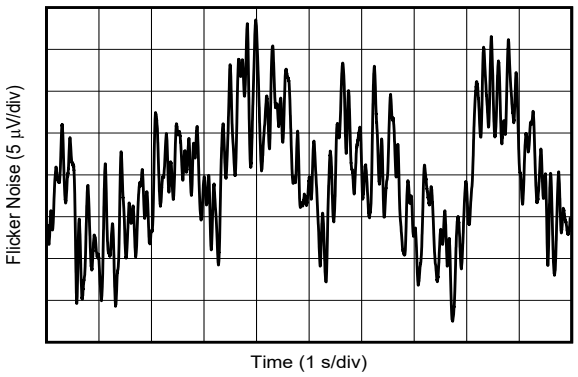
DAC at midscale, reference tied to V_{DD},
output load: 5 kΩ || 200 pF, SCLK = 1 MHz

图 7-42. Clock Feedthrough



DAC at full-scale, output load: 5 kΩ || 200 pF,
V_{DD} = 5.25 V + 0.2 V_{PP}, V_{REFIN} = 4.5 V

图 7-43. AC Power-Supply Rejection Ratio vs Frequency



DAC at midscale, f = 0.1 Hz to 10 Hz

图 7-44. Flicker Noise

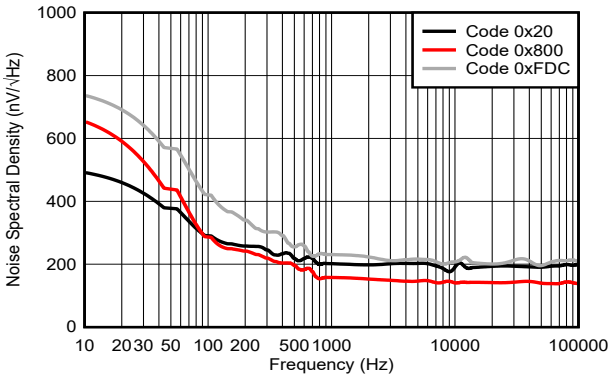
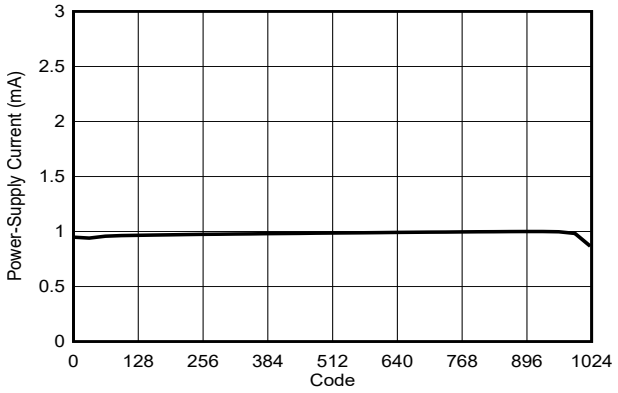


图 7-45. Noise Spectral Density

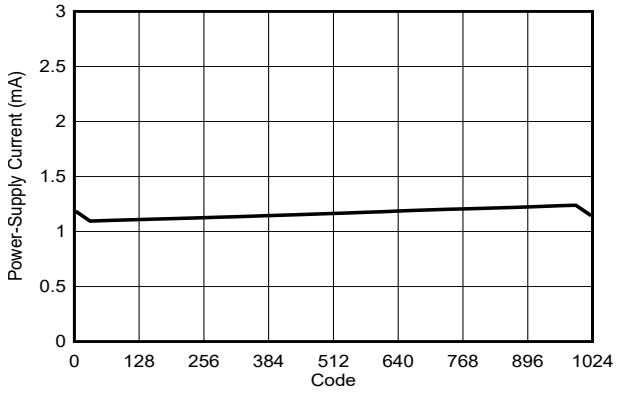
7.11 Typical Characteristics: General

at T_A = 25°C, and DAC outputs unloaded (unless otherwise noted)



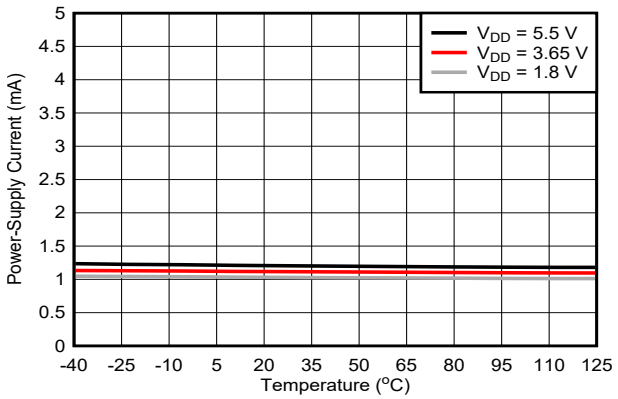
V_{DD} = 1.8 V, reference = 1.8 V

图 7-46. Power-Supply Current vs Digital Input Code



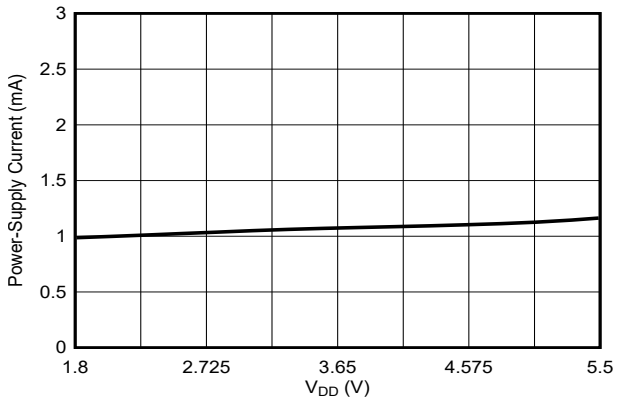
V_{DD} = 5.5 V, reference = 5.5 V

图 7-47. Power-Supply Current vs Digital Input Code



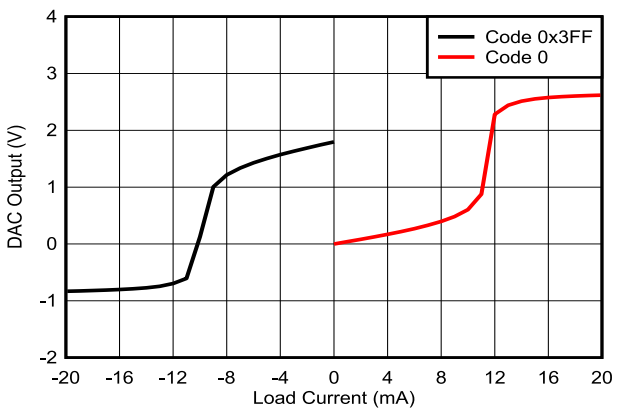
DAC at midscale

图 7-48. Power-Supply Current vs Temperature



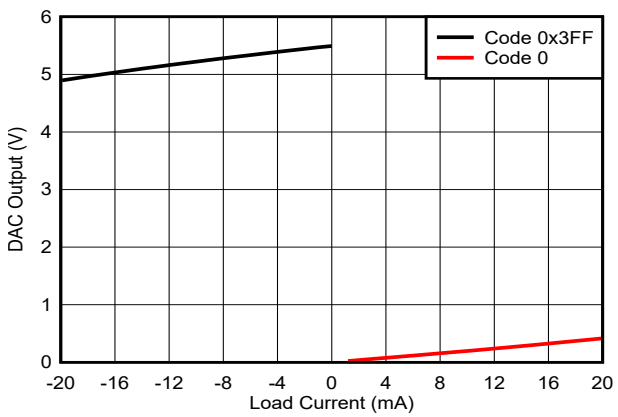
DAC at midscale, reference tied to V_{DD}

图 7-49. Power-Supply Current vs Supply Voltage



V_{DD} = 1.8 V, reference = 1.8 V

图 7-50. Output Source and Sink Capability

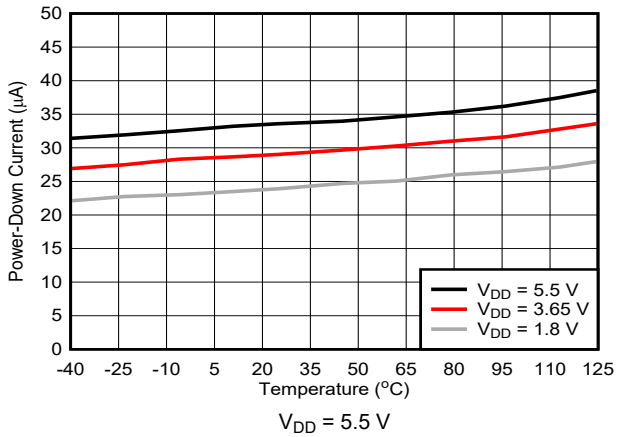


V_{DD} = 5.5 V, reference = 5.5 V

图 7-51. Output Source and Sink Capability

7.11 Typical Characteristics: General (continued)

at T_A = 25°C, and DAC outputs unloaded (unless otherwise noted)



V_{DD} = 5.5 V

图 7-52. Power-Down Current vs Temperature

8 Detailed Description

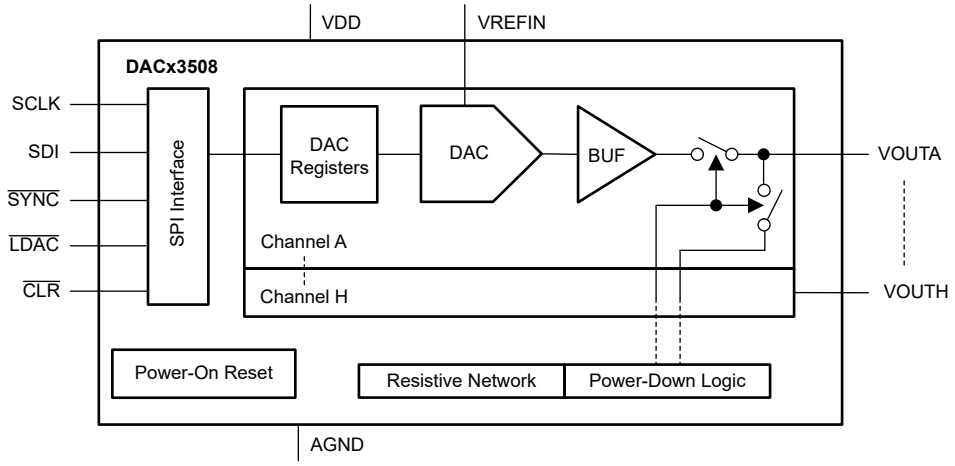
8.1 Overview

The 10-bit DAC53508 and 8-bit DAC43508 (DACx3508) are a pin-compatible family of eight-channel, buffered voltage-output digital-to-analog converters (DACs). With an external reference ranging from 1.8 V to 5.5 V, a full-scale output voltage of 1.8 V to 5.5 V is achievable. These devices are specified monotonic across the power-supply range.

Communication to the devices is established through a three-wire SPI-compatible interface. These devices do not support readback operation. These devices include a load DAC ($\overline{\text{LDAC}}$) pin for simultaneous DAC updates and a clear ($\overline{\text{CLR}}$) pin for setting the outputs to zero scale.

The DACx3508 devices are characterized for operation over the temperature range of –40°C to +125°C and are available in tiny QFN packages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital-to-Analog Converter (DAC) Architecture

Each output channel in the DACx3508 family of devices consists of string architecture with an output buffer amplifier. 图 8-1 shows a block diagram of the DAC architecture.

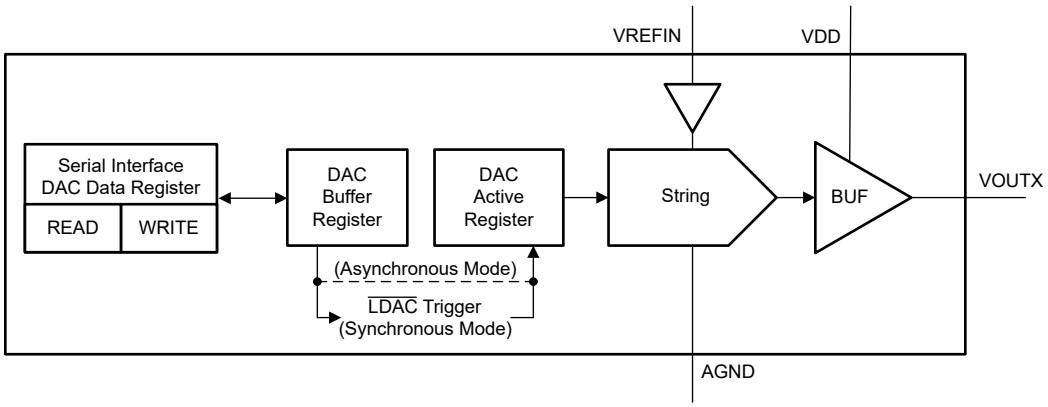


图 8-1. DACx3508 DAC Architecture

8.3.1.1 DAC Transfer Function

The device writes the input data to the individual DAC Data registers in straight binary format. After a power-on or a reset event, the device sets all DAC registers to zero-code. 方程式 1 shows DAC transfer function.

$$V_{OUTX} = \frac{DACn\_DATA}{2^N} \times V_{REFIN} \quad (1)$$

where:

- N = resolution in bits: 10 (DAC53508) or 8 (DAC43508)
- DACn_DATA is the decimal equivalent of the binary code that is loaded to the DAC register
- DACn_DATA ranges from 0 to 2^N – 1
- V_{REFIN} is the DAC reference voltage

8.3.1.2 DAC Register Update and $\overline{LDAC}$ Functionality

The device stores the data written to the DAC Data registers in the DAC buffer registers. Transfer of data from the DAC buffer registers to the DAC active registers can be set to happen immediately (asynchronous mode) or initiated by an $\overline{LDAC}$ trigger (synchronous mode). After the DAC active registers are updated, the DAC outputs change to the new values.

The update mode for each DAC channel is determined by the status of $\overline{LDAC}$ pin.

In asynchronous mode ($\overline{LDAC}$ = low before the DAC write command), a write to the DAC data register results in an immediate update of the DAC active register and DAC output at the end of SPI frame.

In synchronous mode ($\overline{LDAC}$ = high before the DAC write command), writing to the DAC data register does not automatically update the DAC output. Instead, the update occurs only after $\overline{LDAC}$ is pulled low. The synchronous update mode enables simultaneous update of all DAC outputs.

8.3.1.3 $\overline{CLR}$ Functionality

The $\overline{CLR}$ pin is an asynchronous input pin to the DAC. When this pin is pulled low, the DAC buffers and the DAC active registers are set to zero code.

8.3.1.4 Output Amplifier

The output buffer amplifier generates rail-to-rail voltages on the output, giving a maximum output range of 0 V to V_{DD}. 方程式 1 shows that the full-scale output range of the DAC output is determined by the voltage on the VREFIN pin

8.3.2 Reference

The DACx3508 require an external reference to operate. However, the reference pin, VREFIN, and the supply pin, VDD, can be tied together. The reference input pin voltage ranges from 1.8 V to V_{DD}. The typical input impedance of this pin when all the channels are powered on is 12.5 kΩ.

8.3.3 Power-On Reset (POR)

The DACx3508 family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the V_{DD} supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a 5-ms delay, when V_{DD} reaches DAC operating range. The default value for the DAC data registers is zero-code. The DAC output remains at the power-up voltage until a valid command is written to a channel.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific V_{DD} levels, as indicated in 图 8-2, to make sure that the internal capacitors discharge and reset the device on power up. To make sure that a POR occurs, V_{DD} must be less than 0.7 V for at least 1 ms. When V_{DD} drops to less than 1.7 V but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When V_{DD} remains greater than 1.7 V, a POR does not occur.

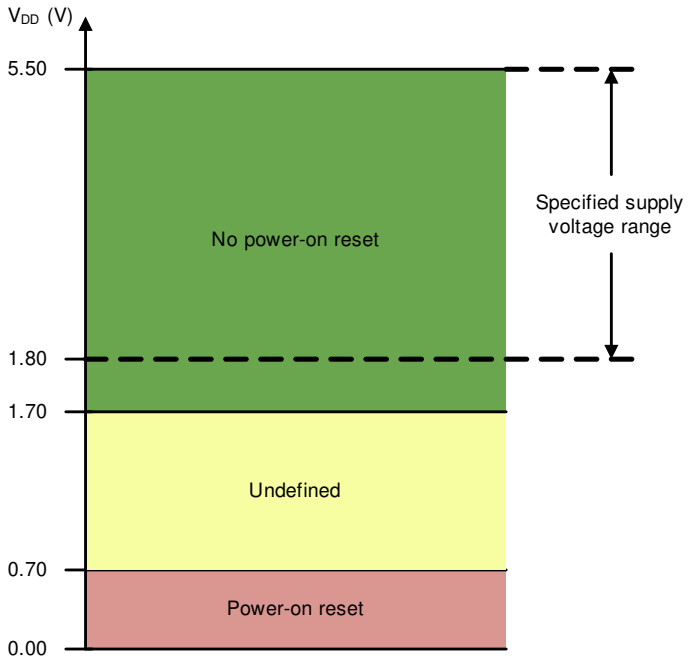


图 8-2. Threshold Levels for V_{DD} POR Circuit

8.3.4 Software Reset

A device software reset event is initiated by writing the reserved code 0x1010 to the SW_RST bit in the STATUS_TRIGGER register.

8.4 Device Functional Modes

The DACx3508 has two modes of operation: normal and power-down.

8.4.1 Power-Down Mode

The DACx3508 DAC output amplifiers can be independently or globally powered down (10 kΩ to A_{GND}) through the DEVICE_CONFIG register. In this state, the device consumes 50 µA (V_{DD} = 1.8 V). At power-up, all output channels buffer amplifiers start in power down (10 kΩ-AGND) mode until a power up command is issued by writing 0 to the per-channel power-down register bits.

8.5 Programming

8.5.1 Serial Peripheral Interface (SPI)

The DACx3508 supports a three-wire SPI interface with write-only functionality. An SPI write cycle for DACx3508 is initiated by asserting the $\overline{SYNC}$ pin low. The serial clock, SCLK, can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for DACx3508 is 24 bits long; therefore, the $\overline{SYNC}$ pin must stay low for at least 24 SCLK falling edges. The write cycle ends when the $\overline{SYNC}$ pin is deasserted high. If the write cycle contains less than the minimum clock edges, the communication is ignored. If the write cycle contains more than the minimum clock edges, only the first 24 bits are used by the device.

表 8-1 describes the format for the 24-bit SPI write access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as the 8-bit address to be written. The last 16 bits in the cycle form the data cycle.

表 8-1. SPI Write Access Cycle

BIT	FIELD	DESCRIPTION
23-16	A[7:0]	Register address: specifies the register to be accessed during the write operation.
15-0	DI[15:0]	Data cycle bits: The data cycle bits are the values written to the register with address A[7:0].

8.6 Register Map

表 8-2. Register Map

REGISTER NAME	COMMAND BITS	DATA BITS												
		MSDB				LSDB								
	B23-B16	B15-B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DEVICE_CONFIG (节 8.6.1)	01h	X	RESERVED			PDN-All	PDNH	PDNG	PDNF	PDNE	PDND	PDNC	PDNB	PDNA
STATUS_TRIGGER (节 8.6.2)	02h	X	X								SW_RST			
BRDCAST (节 8.6.3)	03h	X	BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0]										X	
DACA_DATA (节 8.6.4)	08h	X	DACA_DATA[9:0] / DACA_DATA[7:0]										X	
DACB_DATA (节 8.6.4)	09h	X	DACB_DATA[9:0] / DACB_DATA[7:0]										X	
DACC_DATA (节 8.6.4)	0Ah	X	DACC_DATA[9:0] / DACC_DATA[7:0]										X	
DACD_DATA (节 8.6.4)	0Bh	X	DACD_DATA[9:0] / DACD_DATA[7:0]										X	
DACE_DATA (节 8.6.4)	0Ch	X	DACE_DATA[9:0] / DACE_DATA[7:0]										X	
DACF_DATA (节 8.6.4)	0Dh	X	DACF_DATA[9:0] / DACF_DATA[7:0]										X	
DACG_DATA (节 8.6.4)	0Eh	X	DACG_DATA[9:0] / DACG_DATA[7:0]										X	
DACH_DATA (节 8.6.4)	0Fh	X	DACH_DATA[9:0] / DACAH_DATA[7:0]										X	

表 8-3. Register Section/Block Access Type Codes

Access Type	Code	Description
W	$\overline{W}$	Write only
W	X	Don't care
-n		Value after reset or the default value

8.6.1 DEVICE_CONFIG Register (address = 01h) [reset = 00FFh]

图 8-3. DEVICE_CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				RESERVED			PDN-All	PDNH	PDNG	PDNF	PDNE	PDND	PDNC	PDNB	PDNA
W-0h				W-0h			W-0b	W-FFh							

表 8-4. DEVICE_CONFIG Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	X	W	0h	Don't care
11-9	RESERVED	W	00	Reserved
8	PDN-All	W	0	Global power down bit: 0: Normal operation 1: All DAC channels and internal biasing blocks are powered down.
7-0	PDNx	W	FFh	Channel-specific power down bits: 0: DACx powered up 1: DACx powered down with 10 kΩ pulldown resistor to A_{GND}.

8.6.2 STATUS_TRIGGER Register (address = 02h) [reset = 0000h]

图 8-4. STATUS_TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X												SW_RST			
W-000h												W-0h			

表 8-5. STATUS_TRIGGER Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4	X	W	000h	Don't care
3-0	SW_RST	W	0h	Device resets to default value when this bit field is set to 1010. Other values do not have any impact.

8.6.3 BRDCAST Register (address = 03h) [reset = 0000h]

图 8-5. BRDCAST Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0]										X	
W-0h				W-000h										W-00b	

表 8-6. BRDCAST Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	X	W	0h	Don't care
11-2	BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0]	W	000h	Writing to the BRDCAST register forces the DAC channel to update the active register data to BRDCAST_DATA. Data are MSB-aligned in straight-binary format and follow the format below: DAC53508: { DATA[9:0] } DAC43508: { DATA[7:0], x, x } x – Don’t care bits
1-0	X	W	00	Don't care

8.6.4 DACn_DATA Register (address = 08h to 0Fh) [reset = 0000h]

图 8-6. DACn_DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X				DACn_DATA[9:0] / DACn_DATA[7:0]										X	
W-0h				W-000h										W-00b	

表 8-7. DACn_DATA Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	X	W	0h	Don't care
11-2	DACn_DATA[9:0] / DACn_DATA[7:0]	W	000h	Writing to the DACn_DATA register forces the respective DAC channel to update the active register data to the DACn_DATA. Data are MSB-aligned in straight-binary format and follow the format below: DAC53508: { DATA[9:0] } DAC43508: { DATA[7:0], x, x } x – Don’t care bits
1-0	X	W	00	Don't care

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DACx3508 is a buffered output, eight-channel, low-power DAC available in a tiny 3-mm x 3-mm package. The multichannel, low power, and small package makes this DAC an excellent choice for general-purpose applications in wide range of end equipment. Some of the most-common applications for these devices are LED biasing-in multifunction printers, power-supply supervision with programmable comparators, offset and gain trimming in precision circuits, and power-supply margining.

9.2 Typical Applications

9.2.1 Programmable LED Biasing

End equipments such as multifunction printers, projectors and electronic point-of-sale (EPOS) require a steady luminous intensity from the LED. 图 9-1 shows a simplified circuit diagram for biasing an LED using the DAC53508.

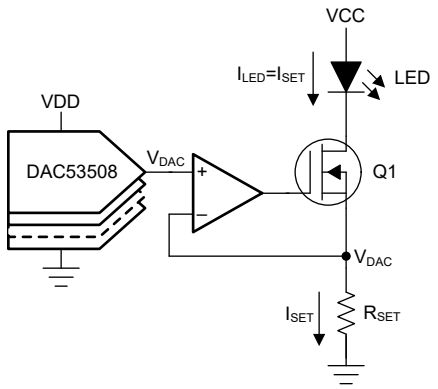


图 9-1. Programmable LED Biasing

9.2.1.1 Design Requirements

- Programmable constant current through an LED tied to a power supply on one end
- DAC output range: 0 V to 5 V
- LED current range: 0 mA to 20 mA

9.2.1.2 Detailed Design Procedure

The DAC is used to set the source current of a MOSFET using a unity-gain buffer, as shown in 图 9-1. Connect the LED between the power supply and the drain of the MOSFET. This configuration allows the DAC to control or set the amount of current through the LED. The buffer following the DAC controls the gate-source voltage of the MOSFET inside the feedback loop, thus compensating this drop and corresponding drift due to temperature, current, and ageing of the MOSFET. The current set by the DAC that flows through the LED is calculated with 方程式 2. To generate 0 mA to 20 mA from a 0 V to 5 V DAC output range, a 250-Ω R_{SET} is required.

$$I_{SET} = \frac{V_{DAC}}{R_{SET}} \quad (2)$$

The following pseudocode is provided to help get started with the LED biasing application:

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <DATA>
//Power-up the device and channels
WRITE DEVICE_CONFIG(0x01), 0x0000
//Program mid code (or the desired voltage) on all channels
WRITE DACA_DATA(0x08), 0x07FC //10-bit MSB aligned
WRITE DACB_DATA(0x09), 0x07FC //10-bit MSB aligned
WRITE DACC_DATA(0x0A), 0x07FC //10-bit MSB aligned
WRITE DACD_DATA(0x0B), 0x07FC //10-bit MSB aligned
WRITE DACE_DATA(0x0C), 0x07FC //10-bit MSB aligned
WRITE DACF_DATA(0x0D), 0x07FC //10-bit MSB aligned
WRITE DACG_DATA(0x0E), 0x07FC //10-bit MSB aligned
WRITE DACH_DATA(0x0F), 0x07FC //10-bit MSB aligned
```

9.2.1.3 Application Curve

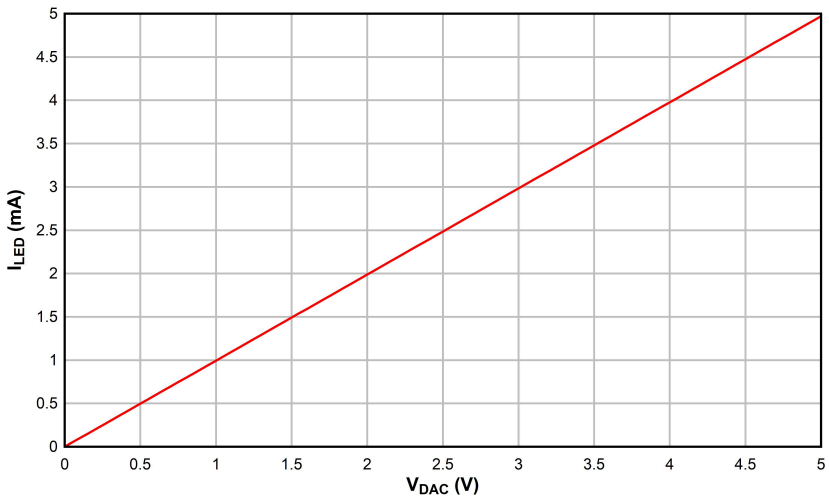


图 9-2. DC Transfer Characteristics of LED Biasing Circuit

9.2.2 Programmable Window Comparator

End equipment that use a centralized power supply (such as network servers, optical modules, and others) require the monitoring of power buses to protect the components. This monitoring or supervision is accomplished using a window comparator. A window comparator monitors a signal input for upper- and lower-threshold violations. A trigger signal is generated when the threshold violations occur. Multichannel monitoring is required to supervise all power supplies available in a module. The DACx3508 provides an easy-to-use, low-footprint method to address this requirement. 图 9-3 shows how the DAC53508 is used to create a programmable window comparator.

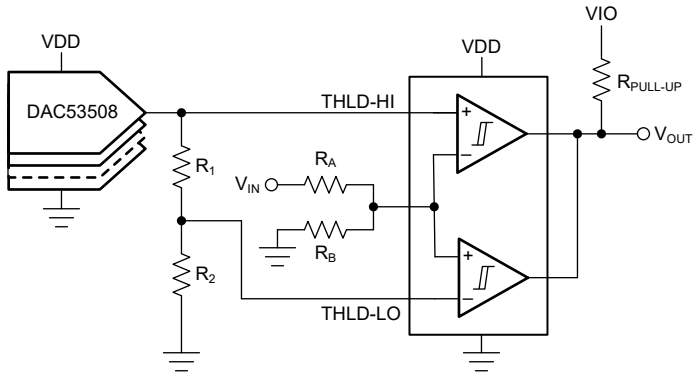


图 9-3. Programmable Window Comparator

9.2.2.1 Design Requirements

- Voltage to be monitored: 5 V
- High threshold: 5 V + 10%
- Low threshold: 5 V – 10%
- Trigger output: 3.3-V open-drain single output

9.2.2.2 Detailed Design Procedure

图 9-3 provides an example in which single DAC channel is used to compare both high and low thresholds. A dual comparator is used per DAC channel, as shown. A voltage divider formed by resistors R_A and R_B are used in order to bring the signal level within the DAC range. Another pair of resistors, R_1 and R_2, are used to settle the low threshold as a factor of the high threshold. This configuration allows the use of a single DAC channel to monitor both the high- and low-threshold levels. Use open-drain comparators to provide the following advantages.

- Generate a logic output level appropriate for the monitoring processor
- Allow shorting of the two outputs to generate a single trigger

In the circuit depicted in 图 9-3, the output of the circuit remains high as long as the signal input remains within the high- and low-threshold levels. Upon violation of any one threshold, the output goes low. 方程式 3 provides the derivation of the low threshold voltage from the high threshold set by the DAC.

$$V_{THLD-LO} = V_{DAC} \times \left(\frac{R_2}{R_1 + R_2}\right) \quad (3)$$

To monitor a power supply of 5 V within ±10%, place the nominal value at the DAC midcode. The output range of the DACx3508 is 0 V to 5 V, thus the midcode voltage output is 2.5 V. Therefore, R_A and R_B are chosen so that the voltage to be compared is 2.5 V. For this example, R_A equals R_B; use 10-kΩ resistors for both. One channel of the DACx3508 must be programmed to $V_{THLD-HI}$ (for example, 2.5 V + 5% = 2.625 V). This result corresponds to a 10-bit DAC code of (2^{10} / 5 V) × 2.625 V = 537.6 (0x21Ah). To generate $V_{THLD-LO}$ (for example, 2.5 V – 5% = 2.405 V) from 2.625 V, the values of R_1 and R_2 are calculated as 7.5 kΩ and 82 kΩ, respectively, using 方程式 3.

The following pseudocode is provided to help get started with the programmable window comparator application at the desired DAC value.

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <DATA>
//Power-up the device and channels
WRITE DEVICE_CONFIG(0x01), 0x0000
//Program 2.625V on channel A
WRITE DACA_DATA(0x08), 0x0868 //10-bit MSB aligned
```

9.2.2.3 Application Curve

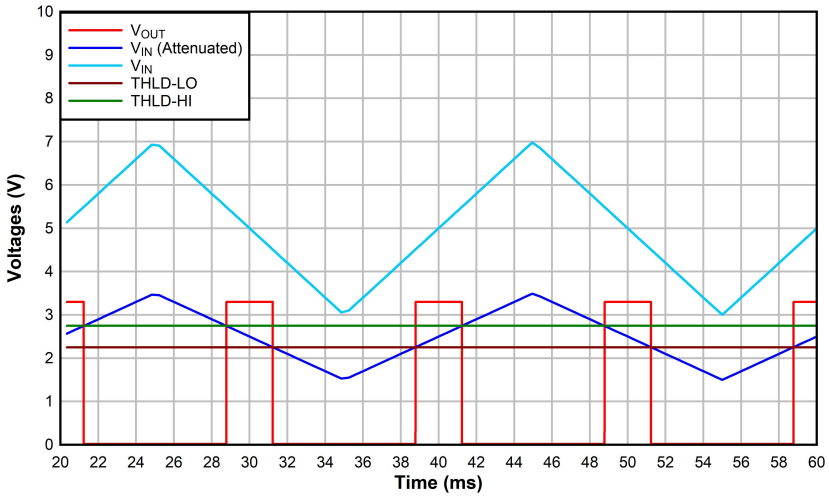


图 9-4. Programmable Comparator Output Waveform

10 Power Supply Recommendations

The DACx3508 family of devices does not require specific supply sequencing. These devices require a single power supply, V_{DD}. A 0.1-µF decoupling capacitor is recommended for the V_{DD} pin.

11 Layout

11.1 Layout Guidelines

The DACx3508 pinout separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate digital and analog traces and place decoupling capacitors close to the device pins.

11.2 Layout Example

图 11-1 shows an example layout drawing with decoupling capacitors and pullup resistors.

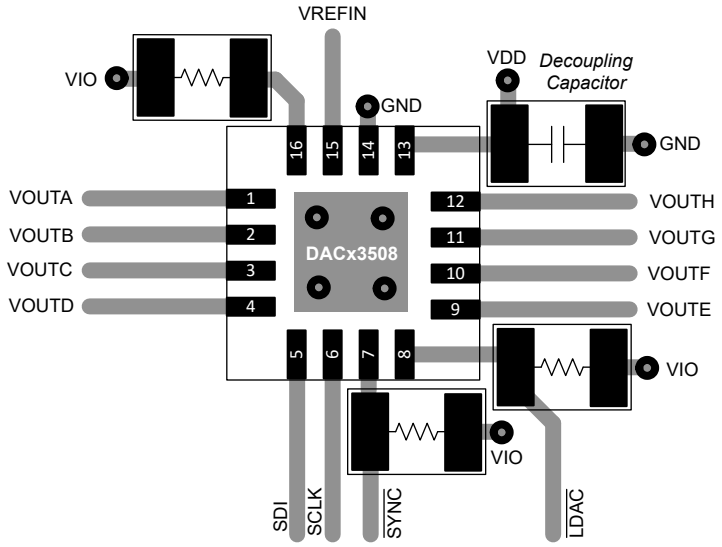


图 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following: Texas Instruments, *DAC53608EVM* user's guide

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC43508RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D43508	Samples
DAC53508RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53508	Samples
DAC53508RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D53508	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

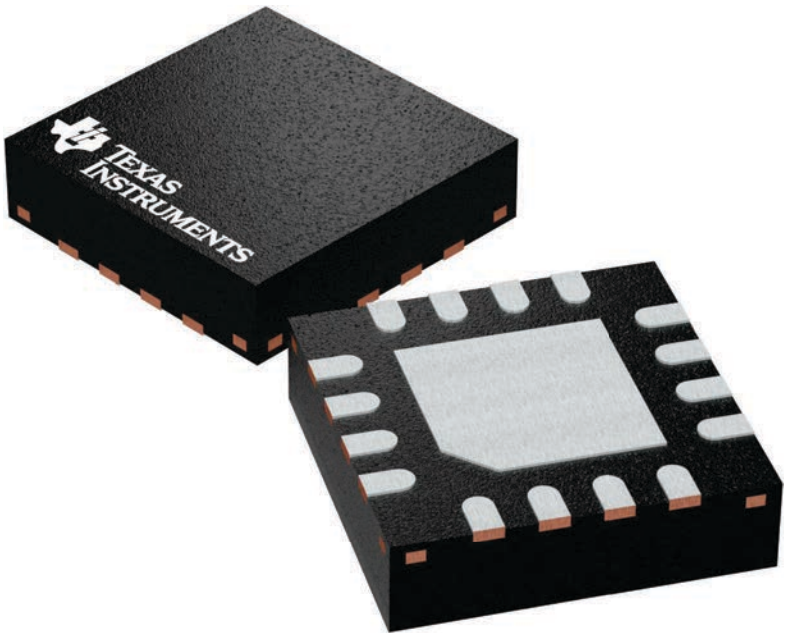
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

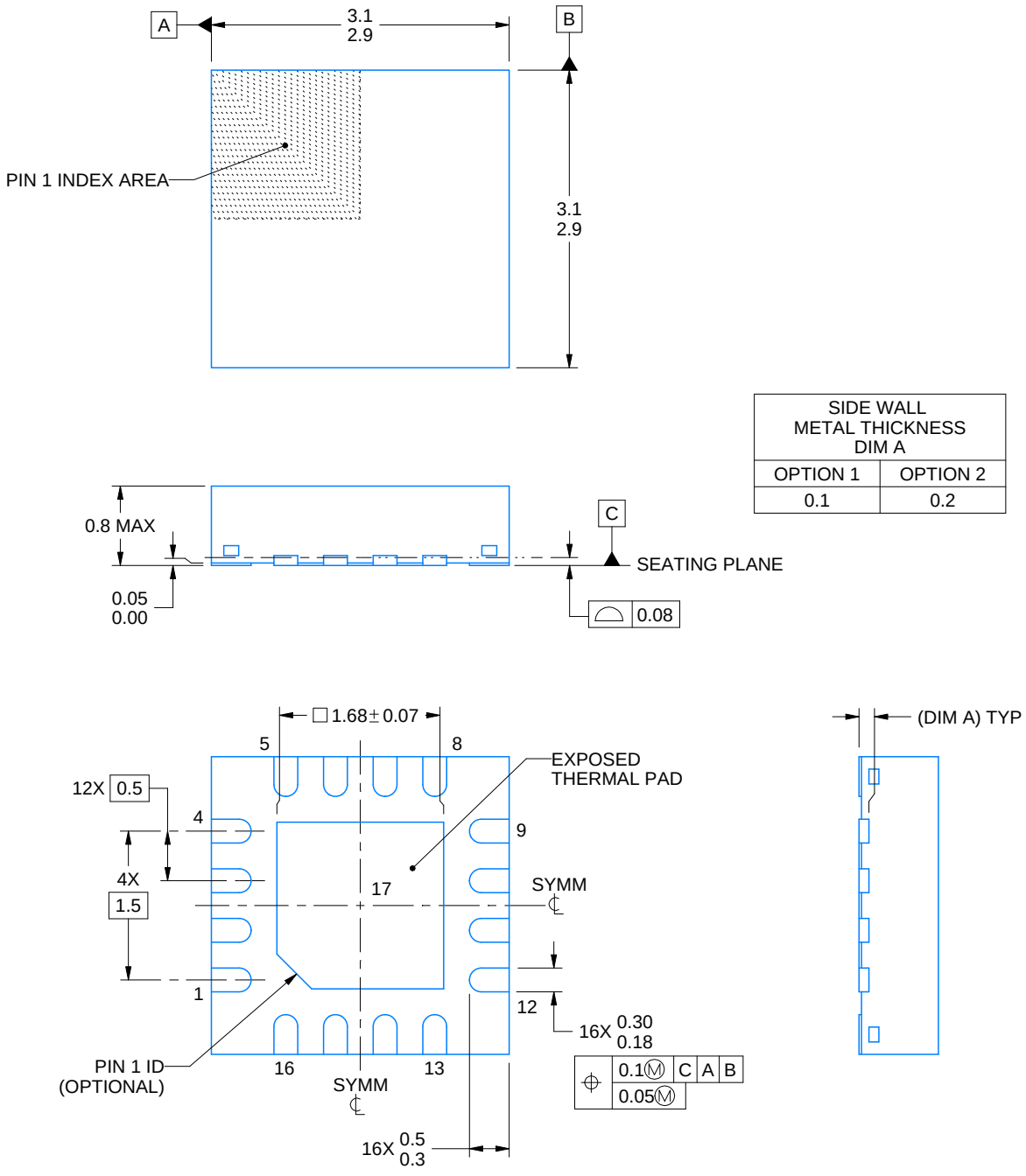


RTE0016C

PACKAGE OUTLINE

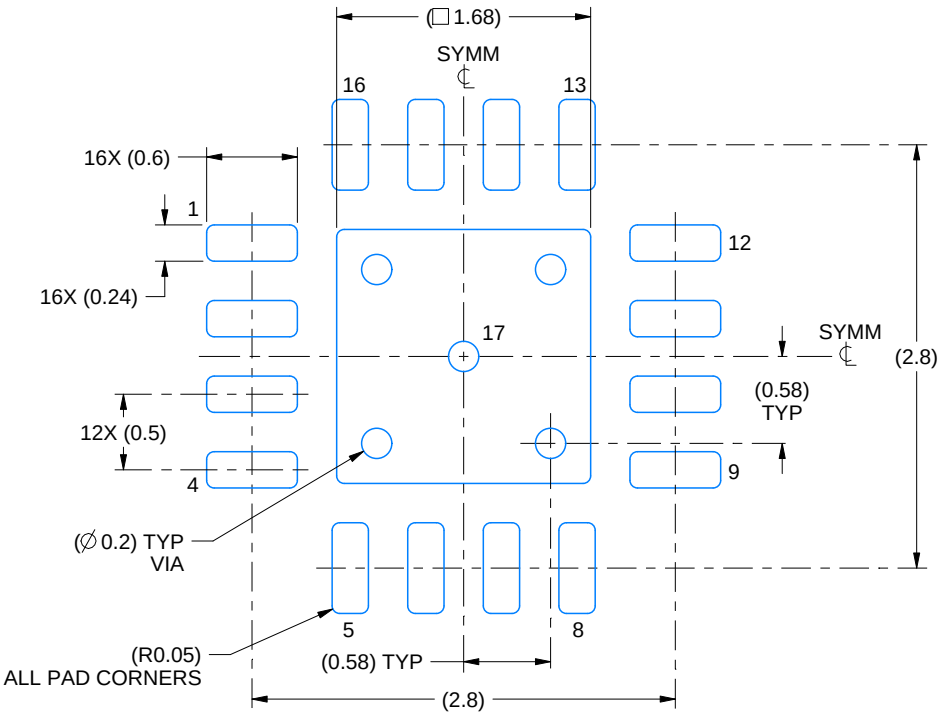
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

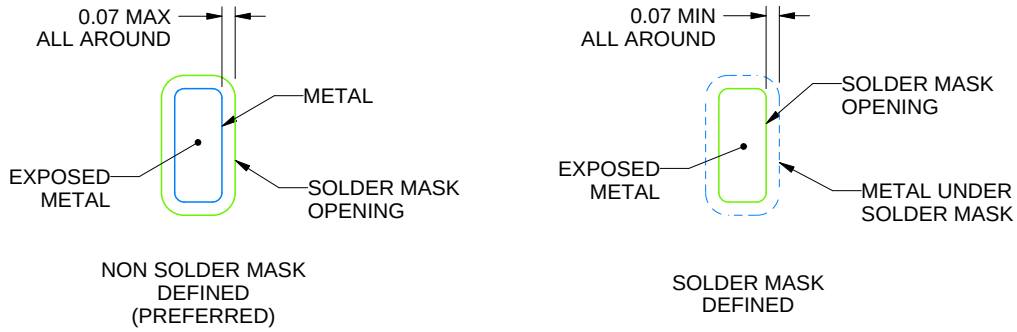


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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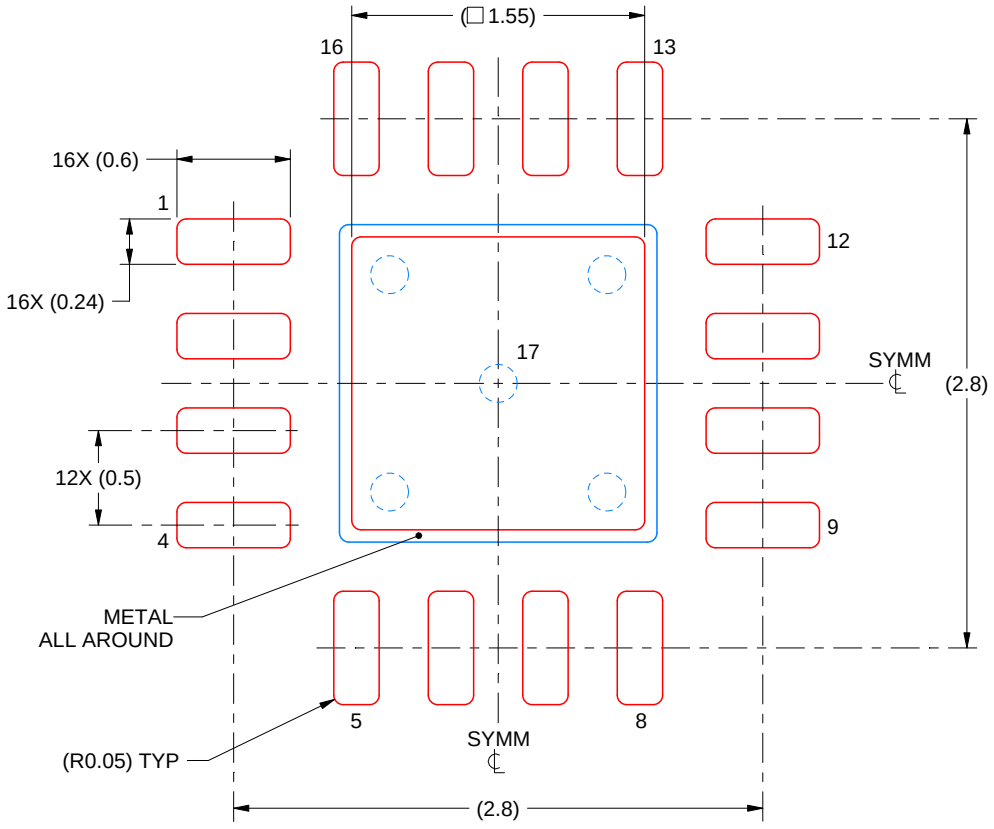
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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