

CC1314R10SimpleLink™ 高性能 Sub-1GHz 无线 MCU

1 特性

无线微控制器

- 采用 TrustZone® 技术的强大的 48MHz Arm® Cortex®-M33 处理器
- FPU 和 DSP 扩展
- 1024 kB 闪存程序存储器
- 8 kB 高速缓存 SRAM
- 具有奇偶校验功能的 256 kB 超低泄漏 SRAM，可实现高度可靠运行
 - 如果禁用奇偶校验，有额外的 32kB SRAM 可用
- 动态多协议管理器 (DMM) 驱动程序
- 支持无线升级 (OTA)

超低功耗传感器控制器

- 具有 4 kB SRAM 的自主 MCU
- 采样、存储和处理传感器数据
- 快速唤醒进入低功耗运行
- 软件定义外设；电容式触控、流量计、LCD

低功耗

- MCU 功耗：
 - 3.4 mA 有源模式，CoreMark®
 - 71 μ A/MHz (运行 CoreMark 时)
 - 0.98 μ A 待机模式，RTC，256kB RAM
 - 0.17 μ A 关断模式，引脚唤醒
- 超低功耗传感器控制器功耗：
 - 2 MHz 模式下为 30 μ A
 - 24MHz 模式下为 809 μ A
- 无线电功耗：
 - TX：25.8 mA (在 +14dBm 和 868 MHz 条件下)

无线协议支持

- Wi-SUN®
- mioty®
- Amazon Sidewalk
- 无线 M-Bus
- SimpleLink™ TI 15.4-Stack (Sub-1GHz)
- 专有系统

高性能无线电

- 相干调制解调器，802.15.4 O-QPSK
- -121dBm (在 2.5kbps 远距离模式下)
- -110dBm (在 50kbps、802.15.4、868MHz 下)

法规遵从性

- 适用于符合以下标准的系统：
 - ¹ RSK 封装 (8.00mm x 8.00mm) 信息只是预发布版，可能会更改。

- ETSI EN 300 220 接收器类别 1.5 和 2、EN 303 131、EN 303 204
- FCC CFR47 第 15 部分
- ARIB STD-T108 和 STD-T67

MCU 外设

- 数字外设大多可连接至任何 GPIO
- 四个 32 位或八个 16 位通用计时器
- 12 位 SAR ADC，200ksps，8 通道
- 8 位 DAC
- 两个比较器
- 可编程电流源
- 四个 UART、四个 SPI、两个 I²C、I²S
- 实时时钟 (RTC)
- 集成温度和电池监控器

安全驱动工具

- 支持安全启动
- 支持安全密钥存储和器件 ID
- Arm TrustZone 打造可信执行环境
- AES 128 位和 256 位加密加速计
- 公钥加速器
- SHA2 加速器 (包括至 SHA-512 的全套装)
- 真随机数发生器 (TRNG)
- 安全调试锁
- 软件防回滚保护

开发工具和软件

- [LP-EM-CC1314R10](#)
- [LP-XDS110](#)、[LP-XDS110ET](#) 或 [TMDSEMU110-U](#) (含 [TMDSEMU110-ETH](#) 附加模块) 调试探针
- [SimpleLink™ LOWPOWER F2 软件开发套件 \(SDK\)](#)
- 用于简单无线电配置的 [SmartRF™ Studio](#)
- 用于构建低功耗检测应用的 [Sensor Controller Studio](#)
- SysConfig 系统配置工具

工作温度范围

- 片上降压直流/直流转换器
- 1.8V 至 3.8V 单电源电压
- -40°C 至 +105°C

封装

- 7mm x 7mm RGZ VQFN48 (30 个 GPIO)
- 8mm x 8mm RSK VQFN64 (46 个 GPIO) ¹
- 符合 RoHS 标准的封装



2 应用

- 315MHz、433MHz、470MHz 至 510MHz、868MHz、902MHz 至 928MHz ISM 和 SRD 系统² 接收带宽低至 4kHz
- 楼宇自动化
 - 楼宇安防系统 - 运动检测器、电子智能锁、门窗传感器、车库门系统、网关
 - HVAC - 恒温器、无线环境传感器、HVAC 系统控制器、网关
 - 防火安全系统 - 烟雾和热量探测器、火警控制面板 (FACP)
 - 视频监控 - IP 网络摄像头
 - 升降机和自动扶梯 - 升降机和自动扶梯的电梯主控板

- 电网基础设施
 - 智能仪表 - 水表、燃气表、电表和热量分配表
 - 电网通信 - 无线通信 - 远距离传感器应用
 - 其他替代能源 - 能量收集、光伏逆变器
- 工业运输 - 资产跟踪
- 工厂自动化和控制
- 医疗
- 电子销售终端 (EPOS) - 电子货架标签 (ESL)
- 个人电子产品
 - 联网外设 - 消费类无线模块
 - 家庭影院和娱乐 - 智能扬声器、机顶盒
 - 游戏
 - 可穿戴设备 (非医用)

3 说明

SimpleLink™ CC1314R10 器件是一款低功耗 Sub-1GHz 无线微控制器 (MCU)，适用于需要增强安全性、片上无线更新功能以及支持高级应用或大型无线协议的应用。它支持 IEEE 802.15.4、支持 IPv6 的智能对象 (6LoWPAN)、无线 M-Bus、Wi-SUN、Amazon Sidewalk、mioty 和专有系统 (包括 Sub-1GHz 的 TI 15.4-Stack)。该器件经过优化，可在楼宇安防系统、HVAC、智能仪表、医疗、有线网络、网关和电网通信、家庭影院和娱乐以及联网外设市场中实现低功耗无线通信和高级检测。该器件的突出特性包括：

- 支持基于 Arm TrustZone 的安全密钥存储、器件 ID 和可信功能。
- 灵活的 Sub-1GHz 无线电，支持业界通用频带 (315MHz、433MHz、868MHz、915MHz 等)，可满足工业需求。
- SimpleLink LOWPOWER F2 软件开发套件 (SDK) 中提供非常灵活的协议栈支持，包括 Wi-SUN、Amazon Sidewalk 和 SimpleLink 15.4-Stack (Sub-1GHz)。
- 对于 Sub-1GHz，最大发送功率为 +14dBm (电流消耗为 25.8 mA)。
- 具有 0.98μA 的低待机电流 (完全 RAM 保持)，从而延长无线应用的电池寿命。
- 支持工业温度，在 105 °C 下最低待机电流大概为 13μA (完全保持 RAM)。
- 通过具有快速唤醒功能的可编程、自主式超低功耗传感器控制器 CPU 实现高级检测。例如，传感器控制器能够在系统电流为 1.2μA 时进行 1Hz ADC 采样。
- 低 SER (软错误率) FIT (时基故障)，可延长运行寿命，不会对工业市场造成干扰，SRAM 奇偶校验功能始终开启，可防止潜在辐射事件导致的损坏。
- 软件控制的专用无线电控制器 (Arm Cortex-M0) 提供灵活的低功耗射频收发器功能，支持多个物理层和射频标准。
- 出色的无线电敏感度 (-121dBm) 和稳健性 (选择性与阻断) 性能，适用于 SimpleLink 远距离模式。

CC1314R10 器件是 SimpleLink™ MCU 平台的一部分，该平台包括 Wi-Fi®、低功耗蓝牙、Thread、Zigbee、Sub-1GHz MCU 和主机 MCU，它们共用一个通用、易于使用的开发环境，其中包含单核软件开发套件 (SDK) 和丰富的工具集。借助一次性集成的 SimpleLink 平台，用户可以将产品组合中器件的任何组合添加至自有设计中，从而在设计要求变更时实现代码的完全重复使用。如需更多信息，请访问 SimpleLink MCU 平台。

除了软件兼容之外，在 Sub-1GHz 无线 MCU 中，7mm × 7mm QFN 封装的 32kB 闪存到最高 1MB 闪存都是引脚对引脚兼容的，以更大限度提高设计的可扩展性。有关 TI 的 Sub-1GHz 解决方案的详细信息，请访问 www.ti.com/sub1ghz。

器件信息

器件型号 ⁽¹⁾	封装	封装尺寸 (标称值)
CC1314R106T0RGZ	VQFN (48)	7.00mm × 7.00mm

² 请参阅 [射频内核](#)，了解有关支持的协议标准、调制格式和数据速率的其他详细信息。

器件信息 (continued)

器件型号 ⁽¹⁾	封装	封装尺寸 (标称值)
CC1314R106T0RSK	VQFN (64)	8.00mm x 8.00mm

(1) 如需所有可用器件的最新器件、封装和订购信息，请参阅节 12 中的“封装选项附录”或访问 TI 网站。

4 Functional Block Diagram

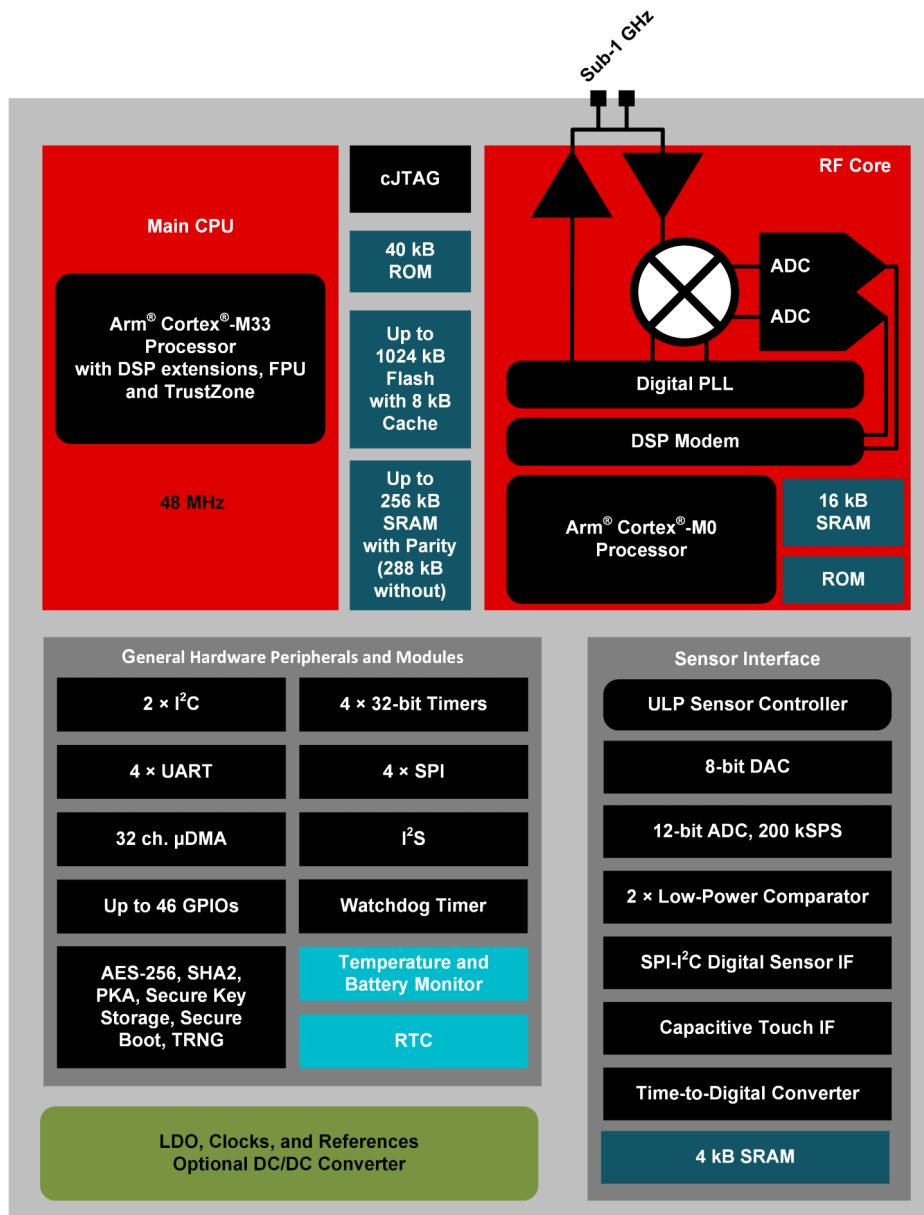


图 4-1. CC1314R10 Block Diagram

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5 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from December 8, 2022 to June 14, 2023 (from Revision * (December 2022) to Revision A (June 2023))

	Page
• Added devices to the Device Comparison table.....	5
• Deleted device revision limitation for LQI in 表 9-1	51
• Updated links in the Reference Designs.....	61

6 Device Comparison

Device	RADIO SUPPORT										FLASH (kB)	RAM + Cache (kB)	GPIO	PACKAGE SIZE						
	Sub-1 GHz Prop.	2.4GHz Prop.	Wireless M-Bus	mioty	Wi-SUN®	Sidewalk	Bluetooth® LE	ZigBee	Thread	Multiprotocol				+20 dBm PA	4 × 4 mm VQFN (24)	4 × 4 mm VQFN (32)	5 × 5 mm VQFN (32)	5 × 5 mm VQFN (40)	7 × 7 mm VQFN (48)	8 × 8 mm VQFN (64)
CC1310	✓		✓	✓								32-128	16-20 + 8	10-30		✓	✓		✓	
CC1311R3	✓		✓	✓								352	32 + 8	22-30				✓	✓	
CC1311P3	✓		✓	✓							✓	352	32 + 8	26					✓	
CC1312R	✓		✓	✓	✓							352	80 + 8	30					✓	
CC1312R7	✓		✓	✓	✓	✓				✓		704	144 + 8	30					✓	
CC1314R10	✓		✓	✓	✓	✓				✓		1024	256 + 8	30-46					✓	✓
CC1352R	✓	✓	✓	✓	✓		✓	✓	✓	✓		352	80 + 8	28					✓	
CC1354R10	✓	✓	✓	✓	✓		✓	✓	✓	✓		1024	256 + 8	28-42					✓	✓
CC1352P	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	352	80 + 8	26					✓	
CC1352P7	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	704	144 + 8	26					✓	
CC1354P10	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	1024	256 + 8	26-42					✓	✓
CC2340R2		✓					✓	✓				256	28	12	✓					
CC2340R5		✓					✓	✓	✓			512	36	12-26	✓			✓		
CC2340R5-Q1							✓					512	36	19			✓			
CC2640R2F							✓					128	20 + 8	10-31		✓	✓		✓	
CC2642R							✓					352	80 + 8	31					✓	
CC2642R-Q1							✓					352	80 + 8	31					✓	
CC2651R3		✓					✓	✓				352	32 + 8	23-31				✓	✓	
CC2651P3		✓					✓	✓			✓	352	32 + 8	22-26				✓	✓	
CC2652R		✓					✓	✓	✓	✓		352	80 + 8	31					✓	
CC2652RB		✓					✓	✓	✓	✓		352	80 + 8	31					✓	
CC2652R7		✓					✓	✓	✓	✓		704	144 + 8	31					✓	
CC2652P		✓					✓	✓	✓	✓	✓	352	80 + 8	26					✓	
CC2652P7		✓					✓	✓	✓	✓	✓	704	144 + 8	26					✓	
CC2674R10		✓					✓	✓	✓	✓		1024	256 + 8	31-45					✓	✓
CC2674P10		✓					✓	✓	✓	✓	✓	1024	256 + 8	26-45					✓	✓

ADVANCE INFORMATION

7 Terminal Configuration and Functions

7.1 Pin Diagram - RGZ Package (Top View)

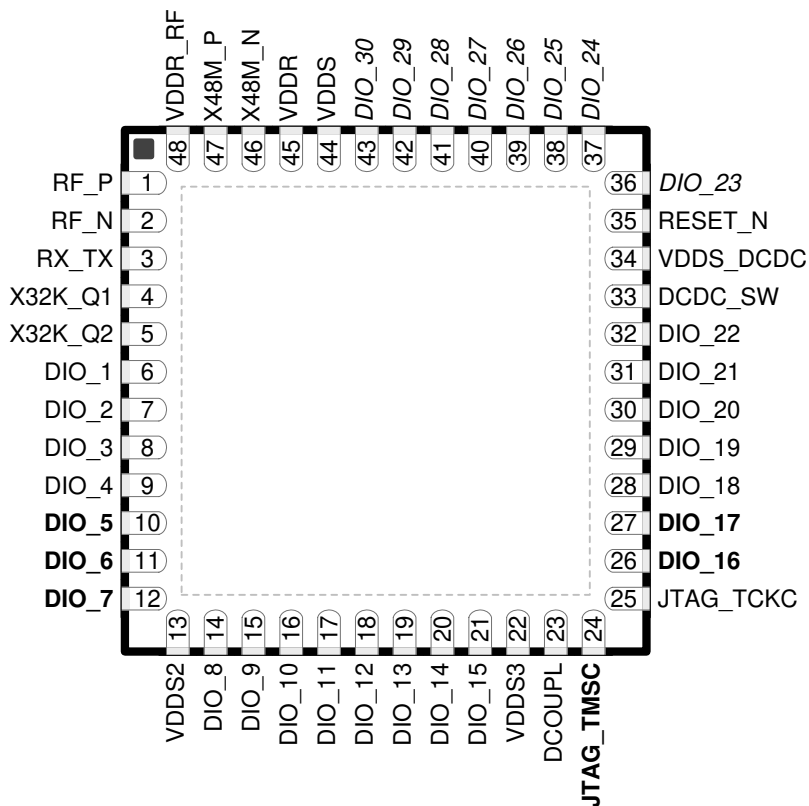


图 7-1. RGZ (7 mm × 7 mm) Pinout, 0.5 mm Pitch (Top View)

The following I/O pins marked in 图 7-1 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

The following I/O pins marked in 图 7-1 in *italics* have analog capabilities:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

7.2 Signal Descriptions - RGZ Package

表 7-1. Signal Descriptions - RGZ Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	33	—	Power	Output from internal DC/DC converter ⁽¹⁾
DCOUPPL	23	—	Power	For decoupling of internal 1.27 V regulated digital-supply ⁽²⁾
DIO_1	6	I/O	Digital	GPIO
DIO_2	7	I/O	Digital	GPIO
DIO_3	8	I/O	Digital	GPIO
DIO_4	9	I/O	Digital	GPIO
DIO_5	10	I/O	Digital	GPIO, high-drive capability
DIO_6	11	I/O	Digital	GPIO, high-drive capability
DIO_7	12	I/O	Digital	GPIO, high-drive capability
DIO_8	14	I/O	Digital	GPIO
DIO_9	15	I/O	Digital	GPIO
DIO_10	16	I/O	Digital	GPIO
DIO_11	17	I/O	Digital	GPIO
DIO_12	18	I/O	Digital	GPIO
DIO_13	19	I/O	Digital	GPIO
DIO_14	20	I/O	Digital	GPIO
DIO_15	21	I/O	Digital	GPIO
DIO_16	26	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	I/O	Digital	GPIO
DIO_19	29	I/O	Digital	GPIO
DIO_20	30	I/O	Digital	GPIO
DIO_21	31	I/O	Digital	GPIO
DIO_22	32	I/O	Digital	GPIO
DIO_23	36	I/O	Digital or Analog	GPIO, analog capability
DIO_24	37	I/O	Digital or Analog	GPIO, analog capability
DIO_25	38	I/O	Digital or Analog	GPIO, analog capability
DIO_26	39	I/O	Digital or Analog	GPIO, analog capability
DIO_27	40	I/O	Digital or Analog	GPIO, analog capability
DIO_28	41	I/O	Digital or Analog	GPIO, analog capability
DIO_29	42	I/O	Digital or Analog	GPIO, analog capability
DIO_30	43	I/O	Digital or Analog	GPIO, analog capability
EGP	—	—	GND	Ground - exposed ground pad ⁽³⁾
JTAG_TMSC	24	I/O	Digital	JTAG TMS, high-drive capability
JTAG_TCKC	25	I	Digital	JTAG TCK
RESET_N	35	I	Digital	Reset, active low. No internal pullup resistor
RF_P	1	—	RF	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RF_N	2	—	RF	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RX_TX	3	—	RF	Optional bias pin for the RF LNA
VDDR	45	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO ^{(2) (4) (6)}

表 7-1. Signal Descriptions - RGZ Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDR_RF	48	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO ⁽²⁾ ⁽⁵⁾ ⁽⁶⁾
VDDS	44	—	Power	1.8 V to 3.8 V main chip supply ⁽¹⁾
VDDS2	13	—	Power	1.8 V to 3.8 V DIO supply ⁽¹⁾
VDDS3	22	—	Power	1.8 V to 3.8 V DIO supply ⁽¹⁾
VDDS_DCDC	34	—	Power	1.8 V to 3.8 V DC/DC converter supply
X48M_N	46	—	Analog	48 MHz crystal oscillator pin N
X48M_P	47	—	Analog	48 MHz crystal oscillator pin P
X32K_Q1	4	—	Analog	32 kHz crystal oscillator pin 1
X32K_Q2	5	—	Analog	32 kHz crystal oscillator pin 2

- (1) For more details, see technical reference manual listed in 节 11.2.
- (2) Do not supply external circuitry from this pin.
- (3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
- (4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
- (5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.
- (6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

7.3 Connections for Unused Pins and Modules - RGZ Package

表 7-2. Connections for Unused Pins - RGZ Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE ⁽¹⁾	PREFERRED PRACTICE ⁽¹⁾
GPIO	DIO_n	6 - 12	NC or GND	NC
		14 - 21		
		26 - 32		
		36 - 43		
32.768 kHz crystal	X32K_Q1	4	NC or GND	NC
	X32K_Q2	5		
DC/DC converter ⁽²⁾	DCDC_SW	33	NC	NC
	VDDS_DCDC	34	VDDS	VDDS

- (1) NC = No connect
- (2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the 22 μ F DCDC capacitor must be kept on the VDDR net.

7.4 Pin Diagram - RSK Package (Top View)

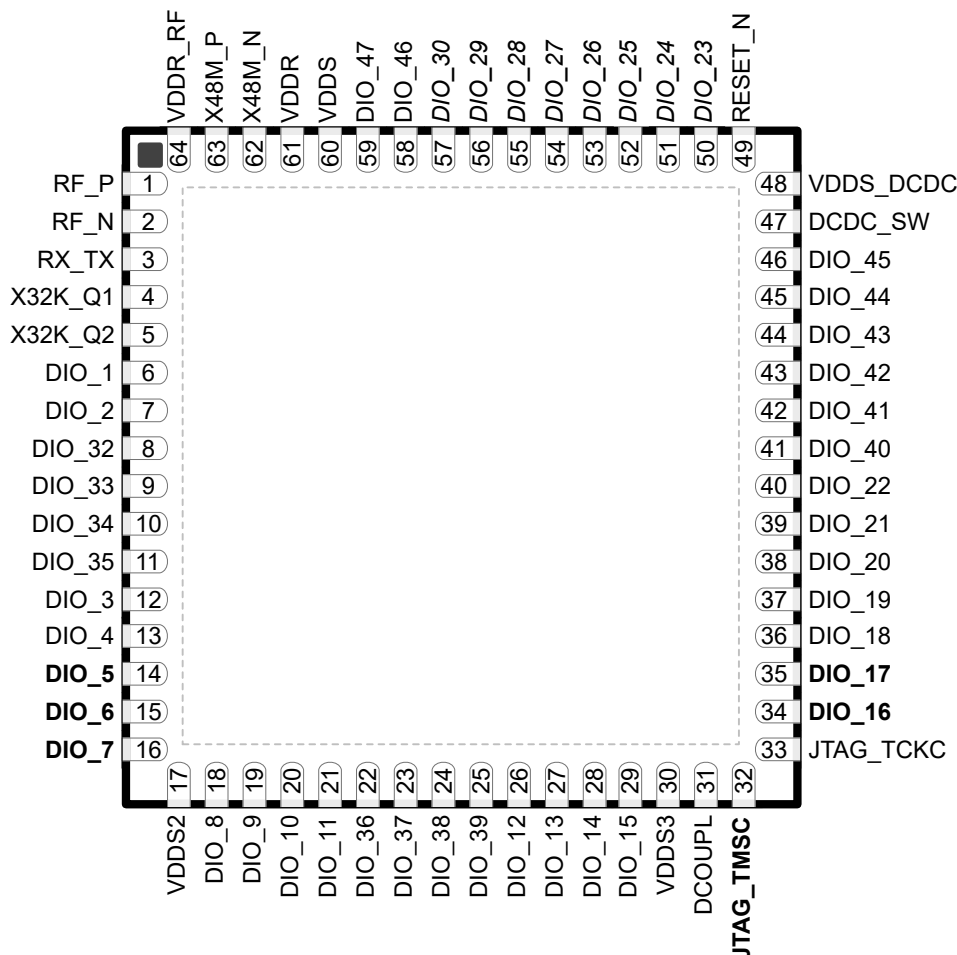


图 7-2. RSK (8 mm × 8 mm) Pinout, 0.4 mm Pitch (Top View)

The following I/O pins marked in 图 7-2 in **bold** have high-drive capabilities:

- Pin 14, **DIO_5**
- Pin 15, **DIO_6**
- Pin 16, **DIO_7**
- Pin 32, **JTAG_TMSC**
- Pin 34, **DIO_16**
- Pin 35, **DIO_17**

The following I/O pins marked in 图 7-2 in *italics* have analog capabilities:

- Pin 50, *DIO_23*
- Pin 51, *DIO_24*
- Pin 52, *DIO_25*
- Pin 53, *DIO_26*
- Pin 54, *DIO_27*
- Pin 55, *DIO_28*
- Pin 56, *DIO_29*
- Pin 57, *DIO_30*

7.5 Signal Descriptions - RSK Package

表 7-3. Signal Descriptions - RSK Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	47	—	Power	Output from internal DC/DC converter ⁽¹⁾
DCOUP_L	31	—	Power	For decoupling of internal 1.27 V regulated digital-supply ⁽²⁾
DIO_1	6	I/O	Digital	GPIO
DIO_2	7	I/O	Digital	GPIO
DIO_3	12	I/O	Digital	GPIO
DIO_4	13	I/O	Digital	GPIO
DIO_5	14	I/O	Digital	GPIO, high-drive capability
DIO_6	15	I/O	Digital	GPIO, high-drive capability
DIO_7	16	I/O	Digital	GPIO, high-drive capability
DIO_8	18	I/O	Digital	GPIO
DIO_9	19	I/O	Digital	GPIO
DIO_10	20	I/O	Digital	GPIO
DIO_11	21	I/O	Digital	GPIO
DIO_12	26	I/O	Digital	GPIO
DIO_13	27	I/O	Digital	GPIO
DIO_14	28	I/O	Digital	GPIO
DIO_15	29	I/O	Digital	GPIO
DIO_16	34	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_17	35	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_18	36	I/O	Digital	GPIO
DIO_19	37	I/O	Digital	GPIO
DIO_20	38	I/O	Digital	GPIO
DIO_21	39	I/O	Digital	GPIO
DIO_22	40	I/O	Digital	GPIO
DIO_23	50	I/O	Digital or Analog	GPIO, analog capability
DIO_24	51	I/O	Digital or Analog	GPIO, analog capability
DIO_25	52	I/O	Digital or Analog	GPIO, analog capability
DIO_26	53	I/O	Digital or Analog	GPIO, analog capability
DIO_27	54	I/O	Digital or Analog	GPIO, analog capability
DIO_28	55	I/O	Digital or Analog	GPIO, analog capability
DIO_29	56	I/O	Digital or Analog	GPIO, analog capability
DIO_30	57	I/O	Digital	GPIO, analog capability
DIO_32	8	I/O	Digital	GPIO
DIO_33	9	I/O	Digital	GPIO
DIO_34	10	I/O	Digital	GPIO
DIO_35	11	I/O	Digital	GPIO
DIO_36	22	I/O	Digital	GPIO
DIO_37	23	I/O	Digital	GPIO
DIO_38	24	I/O	Digital	GPIO
DIO_39	25	I/O	Digital	GPIO
DIO_40	41	I/O	Digital	GPIO
DIO_41	42	I/O	Digital	GPIO

表 7-3. Signal Descriptions - RSK Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DIO_42	43	I/O	Digital	GPIO
DIO_43	44	I/O	Digital	GPIO
DIO_44	45	I/O	Digital	GPIO
DIO_45	46	I/O	Digital	GPIO
DIO_46	58	I/O	Digital	GPIO
DIO_47	59	I/O	Digital	GPIO
EGP	—	—	GND	Ground - exposed ground pad ⁽³⁾
JTAG_TMSC	32	I/O	Digital	JTAG TMS, high-drive capability
JTAG_TCKC	33	I	Digital	JTAG TCKC
RESET_N	49	I	Digital	Reset, active low. No internal pullup resistor
RF_P_SUB_1GHZ	1	—	RF	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RF_N_SUB_1GHZ	2	—	RF	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RX_TX	3	—	RF	Optional bias pin for the RF LNA
VDDR	61	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO ^{(2) (4) (6)}
VDDR_RF	64	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO ^{(2) (5) (6)}
VDDS	60	—	Power	1.8 V to 3.8 V main chip supply ⁽¹⁾
VDDS2	17	—	Power	1.8 V to 3.8 V DIO supply ⁽¹⁾
VDDS3	30	—	Power	1.8 V to 3.8 V DIO supply ⁽¹⁾
VDDS_DCDC	48	—	Power	1.8 V to 3.8 V DC/DC converter supply
X48M_N	62	—	Analog	48 MHz crystal oscillator pin N
X48M_P	63	—	Analog	48 MHz crystal oscillator pin P
X32K_Q1	4	—	Analog	32 kHz crystal oscillator pin 1
X32K_Q2	5	—	Analog	32 kHz crystal oscillator pin 2

(1) For more details, see technical reference manual listed in 节 11.2.

(2) Do not supply external circuitry from this pin.

(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.

(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.

(5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.

(6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

7.6 Connection of Unused Pins and Module - RSK Package

表 7-4. Connections for Unused Pins - RSK Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE ⁽¹⁾	PREFERRED PRACTICE ⁽¹⁾
GPIO	DIO_n	6 - 16, 18 - 29 34 - 46, 50 - 59	NC or GND	NC
32.768 kHz crystal	X32K_Q1	4	NC or GND	NC
	X32K_Q2	5		
DC/DC converter ⁽²⁾	DCDC_SW	47	NC	NC
	VDDS_DCDC	48	VDDS	VDDS

(1) NC = No connect

- (2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the 22 μ F DCDC capacitor must be kept on the VDDR net.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

			MIN	MAX	UNIT
V _{DDS} ⁽³⁾	Supply voltage		- 0.3	4.1	V
	Voltage on any digital pin ^{(4) (5)}		- 0.3	V _{DDS} + 0.3, max 4.1	V
	Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P		- 0.3	V _{DDR} + 0.3, max 2.25	V
V _{in}	Voltage on ADC input	Voltage scaling enabled	- 0.3	V _{DDS}	V
		Voltage scaling disabled, internal reference	- 0.3	1.49	
		Voltage scaling disabled, V _{DDS} as reference	- 0.3	V _{DDS} / 2.9	
	Input level, RF pins			10	dBm
T _{stg}	Storage temperature		- 40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ground, unless otherwise noted.
- (3) V_{DDS_DCDC}, V_{DDS2} and V_{DDS3} must be at the same potential as V_{DDS}.
- (4) Including analog capable DIOs.
- (5) Injection current is not supported on any GPIO pin

8.2 ESD Ratings

				VALUE	UNIT
V _{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	All pins	±500	V

- (1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process
- (2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Operating ambient temperature ^{(1) (3)}			- 40	105	°C
Operating supply voltage (V _{DDS})			1.8	3.8	V
Operating supply voltage (V _{DDS}), boost mode		V _{DDR} = 1.95 V +14 dBm RF output power	2.1	3.8	V
Rising supply voltage slew rate			0	100	mV/μs
Falling supply voltage slew rate ⁽²⁾			0	20	mV/μs

- (1) Operation at or near maximum operating temperature for extended durations will result in lifetime reduction.
- (2) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22 μF V_{DDS} input capacitor must be used to ensure compliance with this slew rate.
- (3) For thermal resistance characteristics refer to [Thermal Resistance Characteristics](#). For application considerations, refer to [SPRA953](#)

8.4 Power Supply and Modules

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V _{DDS} Power-on-Reset (POR) threshold		1.1 - 1.55			V
V _{DDS} Brown-out Detector (BOD) ⁽¹⁾	Rising threshold	1.77			V
V _{DDS} Brown-out Detector (BOD), before initial boot ⁽²⁾	Rising threshold	1.70			V
V _{DDS} Brown-out Detector (BOD) ⁽¹⁾	Falling threshold	1.75			V

- (1) For boost mode (V_{DDR} = 1.95 V), TI drivers software initialization will trim V_{DDS} BOD limits to maximum (approximately 2.0 V)

- (2) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET_N pin

ADVANCE INFORMATION

8.5 Power Consumption - Power Modes

When measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.6\text{ V}$ with DC/DC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
Core Current Consumption				
I _{core}	Reset and Shutdown	Reset. RESET_N pin asserted or VDD5 below power-on-reset threshold	150	nA
		Shutdown. No clocks running, no retention	171	
	Standby without cache retention	RTC running, CPU, 256 kB RAM and (partial) register retention. RCOSC_LF	0.98	μA
		RTC running, CPU, 128 kB RAM and (partial) register retention. RCOSC_LF	0.88	μA
		RTC running, CPU, 256 kB RAM and (partial) register retention XOSC_LF	1.08	μA
		RTC running, CPU, 128 kB RAM and (partial) register retention XOSC_LF	0.99	μA
		RTC running, CPU, 256 kB RAM and (partial) register retention. RCOSC_LF	2.24	μA
	Standby with cache retention	RTC running, CPU, 128 kB RAM and (partial) register retention. RCOSC_LF	2.16	μA
		RTC running, CPU, 256 kB RAM and (partial) register retention. XOSC_LF	2.34	μA
		RTC running, CPU, 128 kB RAM and (partial) register retention. XOSC_LF	2.25	μA
		Idle	Supply Systems and RAM powered RCOSC_HF	635
	Active	MCU running CoreMark at 48 MHz with parity enabled RCOSC_HF	3.5	mA
		MCU running CoreMark at 48 MHz with parity disabled RCOSC_HF	3.4	mA
	Peripheral Current Consumption			
I _{peri}	Peripheral power domain	Delta current with domain enabled	62.4	μA
	Serial power domain	Delta current with domain enabled	5.83	
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle	102.0	
	μDMA	Delta current with clock enabled, module is idle	58.0	
	Timers	Delta current with clock enabled, module is idle ⁽³⁾	97.2	
	I2C	Delta current with clock enabled, module is idle	9.8	
	I2S	Delta current with clock enabled, module is idle	22.2	
	SPI	Delta current with clock enabled, module is idle ⁽²⁾	55.8	
	UART	Delta current with clock enabled, module is idle ⁽¹⁾	114.2	
	CRYPTO (AES)	Delta current with clock enabled, module is idle	15.5	
	PKA	Delta current with clock enabled, module is idle	66.6	
	TRNG	Delta current with clock enabled, module is idle	21.0	
	Sensor Controller Engine Consumption			
I _{SCE}	Active mode	24 MHz, infinite loop, V _{DD5} = 3.0 V	820	μA
	Low-power mode	2 MHz, infinite loop, V _{DD5} = 3.0 V	32	

- (1) Only one UART running
(2) Only one SPI running
(3) Only one GPTimer running

8.6 Power Consumption - Radio Modes

When measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.6\text{ V}$ with DC/DC enabled unless otherwise noted.

Using boost mode (increasing VDDR up to 1.95 V), will increase system current by 15% (does not apply to TX +14 dBm setting where this current is already included).

Relevant I_{core} and I_{peri} currents are included in below numbers.

PARAMETER	TEST CONDITIONS	TYP	UNIT
Radio receive current, 868 MHz		5.8	mA
Radio transmit current	0 dBm output power setting 868 MHz	7.5	mA
	+10 dBm output power setting 868 MHz	16.1	mA
Radio transmit current Boost mode	+14 dBm output power setting 868 MHz	25.8	mA

8.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and $V_{DD5} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			2		kB
Supported flash erase cycles before failure, full bank ^{(1) (5)}		30			k Cycles
Supported flash erase cycles before failure, single sector ⁽²⁾		60			k Cycles
Maximum number of write operations per row before sector erase ⁽³⁾				83	Write Operations
Flash retention	105 °C	11.4			Years
Flash sector erase current	Average delta current		0.3		mA
Flash sector erase time ⁽⁴⁾	Zero cycles		2.1		ms
	30k cycles			4000	ms
Flash write current	Average delta current, 16 bytes at a time		3.0		mA
Flash write time ⁽⁴⁾	16 bytes at a time		21.4		µs

(1) A full bank erase is counted as a single erase cycle on each sector

(2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles

(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.

(4) This number is dependent on Flash aging and increases over time and erase cycles

(5) Aborting flash during erase or program modes is not a safe operation.

8.8 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		PACKAGE		UNIT
		RGZ (VQFN)	RSK(VQFN)	
		48 PINS	64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.4	TBD	°C/W ⁽²⁾
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	TBD	°C/W ⁽²⁾
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	TBD	°C/W ⁽²⁾
ψ_{JT}	Junction-to-top characterization parameter	0.1	TBD	°C/W ⁽²⁾
ψ_{JB}	Junction-to-board characterization parameter	7.9	TBD	°C/W ⁽²⁾
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	TBD	°C/W ⁽²⁾

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) °C/W = degrees Celsius per watt.

8.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	1076		1315	MHz
	861		1054	
	431		527	
	359		439	
	287		351	

8.10 861 MHz to 1054 MHz - Receive (RX)

When Measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Digital channel filter programmable receive bandwidth		4		4000	kHz
Data rate step size			1.5		bps
Spurious emissions 25 MHz to 1 GHz	868 MHz		< -57		dBm
Spurious emissions 1 GHz to 13 GHz	Conducted emissions measured according to ETSI EN 300 220		< -47		dBm
Wi-SUN, 50 kbps, ± 12.5 kHz deviation, 2-GFSK, 78 kHz RX BW, #1a					
Sensitivity	MRFSK, 866.6 MHz, 10% PER, 250 byte payload		-106		dBm
Saturation limit	10% PER, 250 byte payload, 866.6 MHz		10		dBm
Selectivity, +100 kHz	10% PER, 250 byte payload, 866.6 MHz. Wanted signal 3 dB above sensitivity level.		33		dB
Selectivity, -100 kHz			31		dB
Selectivity, +200 kHz			38		dB
Selectivity, -200 kHz			37		dB
RSSI dynamic range	Starting from the sensitivity limit		93		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Wi-SUN, 50 kbps, ± 25 kHz deviation, 2-GFSK, 100 kHz RX BW, #1b					
Sensitivity	MRFSK, 918.2 MHz, 10% PER, 250 byte payload		-106		dBm
Saturation limit	10% PER, 250 byte payload, 918.2 MHz		10		dBm
Selectivity, +200 kHz	10% PER, 250 byte payload, 918.2 MHz. Wanted signal 3 dB above sensitivity level.		37		dB
Selectivity, -200 kHz			35		dB
Selectivity, +400 kHz			42		dB
Selectivity, -400 kHz			41		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Wi-SUN, 100 kbps, ± 25 kHz deviation, 2-GFSK, 135 kHz RX BW, #2a					
Sensitivity	MRFSK, 866.6 MHz, 10% PER, 250 byte payload		-103		dBm
Saturation limit	10% PER, 250 byte payload, 866.6 MHz		10		dBm
Selectivity, +200 kHz	10% PER, 250 byte payload, 866.6 MHz. Wanted signal 3 dB above sensitivity level.		40		dB
Selectivity, -200 kHz			38		dB
Selectivity, +400 kHz			46		dB
Selectivity, -400 kHz			44		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Wi-SUN, 100 kbps, ± 50 kHz deviation, 2-GFSK, 208 kHz RX BW, #2b					
Sensitivity	MRFSK, 920.9 MHz, 10% PER, 250 byte payload		-102		dBm
Saturation limit	10% PER, 250 byte payload, 920.9 MHz		10		dBm
Selectivity, +400 kHz	10% PER, 250 byte payload, 920.9 MHz. Wanted signal 3 dB above sensitivity level, modulated blocker.		42		dB
Selectivity, -400 kHz			39		dB
Selectivity, +800 kHz			52		dB
Selectivity, -800 kHz			46		dB
RSSI dynamic range	Starting from the sensitivity limit		91		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Wi-SUN, 150 kbps, ± 37.5 kHz deviation, 2-GFSK, 273 kHz RX BW, #3					
Sensitivity	MRFSK, 918.4 MHz, 10% PER, 250 byte payload		-99		dBm
Saturation limit	10% PER, 250 byte payload, 918.4 MHz		10		dBm

8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When Measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, +400 kHz	10% PER, 250 byte payload, 918.4 MHz. Wanted signal 3 dB above sensitivity level.	41			dB
Selectivity, -400 kHz		39			dB
Selectivity, +800 kHz		50			dB
Selectivity, -800 kHz		46			dB
RSSI dynamic range	Starting from the sensitivity limit	86			dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range	±3			dB
Wi-SUN, 200 kbps, ±50 kHz deviation, 2-GFSK, 335 kHz RX BW, #4a					
Sensitivity	MRFSK, 918.4 MHz, 10% PER, 250 byte payload	-99			dBm
Saturation limit	10% PER, 250 byte payload, 918.4 MHz	10			dBm
Selectivity, +400 kHz	10% PER, 250 byte payload, 918.4 MHz. Wanted signal 3 dB above sensitivity level.	42			dB
Selectivity, -400 kHz		40			dB
Selectivity, +800 kHz		51			dB
Selectivity, -800 kHz		47			dB
RSSI dynamic range	Starting from the sensitivity limit	91			dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range	±3			dB
Wi-SUN, 200 kbps, ±100 kHz deviation, 2-GFSK, 416 kHz RX BW, #4b					
Sensitivity	MRFSK, 920.8 MHz, 10% PER, 250 byte payload	-98			dBm
Saturation limit	10% PER, 250 byte payload, 920.8 MHz	10			dBm
Selectivity, +600 kHz	10% PER, 250 byte payload, 920.8 MHz. Wanted signal 3 dB above sensitivity level, modulated blocker.	46			dB
Selectivity, -600 kHz		43			dB
Selectivity, +1200 kHz		54			dB
Selectivity, -1200 kHz		51			dB
RSSI dynamic range	Starting from the sensitivity limit	86			dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range	±3			dB
Wi-SUN, 300 kbps, ±75 kHz deviation, 2-GFSK, 496 kHz RX BW, #5					
Sensitivity	MRFSK, 917.6 MHz, 10% PER, 250 byte payload	-97			dBm
Saturation limit	10% PER, 250 byte payload, 917.6 MHz	10			dBm
Selectivity, +600 kHz	10% PER, 250 byte payload, 917.6 MHz. Wanted signal 3 dB above sensitivity level.	42			dB
Selectivity, -600 kHz		37			dB
Selectivity, +1200 kHz		51			dB
Selectivity, -1200 kHz		40			dB
RSSI dynamic range	Starting from the sensitivity limit	86			dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range	±3			dB
802.15.4-2020, 10 kbps, 2-FSK, 26 kHz RX BW, Mode #1a					
Sensitivity	FSK, 915.0 MHz, 20 byte PSDU < 10% PER	-113			dBm
Sensitivity	FSK, 868.3 MHz, 20 byte PSDU < 10% PER	-113			dBm
Saturation limit	PSDU length 20 octets; PER < 10%, 868.3 MHz	10			dBm

8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When Measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, +50 kHz	PSDU length 20 octets; PER < 10%, 868.3 MHz		36		dB
Selectivity, -50 kHz			36		dB
Selectivity, +100 kHz			40		dB
Selectivity, -100 kHz			39		dB
Selectivity, +200 kHz			44		dB
Selectivity, -200 kHz			37		dB
Blocking, +1 MHz			60		dB
Blocking, -1 MHz			59		dB
Blocking, +2 MHz			64		dB
Blocking, -2 MHz			64		dB
Blocking, +5 MHz			75		dB
Blocking, -5 MHz			74		dB
Blocking, +10 MHz			79		dB
Blocking, -10 MHz			79		dB
Selectivity, +50 kHz	PSDU length 20 octets; PER < 10%, 868.3 MHz. Wanted signal 3 dB above sensitivity level.		35		dB
Selectivity, -50 kHz			35		dB
Selectivity, +100 kHz			39		dB
Selectivity, -100 kHz			38		dB
Selectivity, +200 kHz			44		dB
Selectivity, -200 kHz			44		dB
Blocking, +1 MHz			58		dB
Blocking, -1 MHz			58		dB
Blocking, +2 MHz			62		dB
Blocking, -2 MHz			63		dB
Blocking, +5 MHz			74		dB
Blocking, -5 MHz			74		dB
Blocking, +10 MHz			73		dB
Blocking, -10 MHz			78		dB
Blocking + 5% Fc. (45.75 MHz)	10% PER, 20 byte payload, 866.6 MHz 802.15.4g mandatory mode, wanted signal -94 dBm. 3 dB above usable sensitivity limit according to ETSI EN 300 220 V3.1.1 (usable sensitivity -97 dBm). Limit is Cat 1.5 requirement.		-15		dBm
Blocking - 5% Fc. (-45.75 MHz)			-15		dBm
Image rejection (image compensation enabled)			39		dB
Image rejection (image compensation enabled)	PSDU length 20 octets; PER < 10%, 868.3 MHz		39		dB
Image rejection (image compensation enabled)	-40 to 125°C, 10% PER, 250 byte payload, 866.6 MHz		39		dB
RSSI dynamic range	Starting from the sensitivity limit		100		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
Frequency error tolerance (ppm)	10% PER, 20 byte payload, measured at 10 dB above sensitivity level. Negative offset		-12		ppm
Frequency error tolerance (ppm)	10% PER, 20 byte payload, measured at 10 dB above sensitivity level. Positive offset		12		ppm
Symbol rate error tolerance (ppm)	10% PER, 20 byte payload, measured at 10 dB above sensitivity level. Negative offset		-1000		ppm
Symbol rate error tolerance (ppm)	1% BER, measured at 10 dB above sensitivity level. Positive offset		1000		ppm

802.15.4-2020, 20 kbps, 2-FSK, 52 kHz RX BW, Mode #1b

8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When Measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sensitivity	FSK, 20 kbps, $\pm 10\text{ kHz}$ deviation, 2-GFSK, 915.0 MHz, 52 kHz RX BW, 20 byte PSDU < 10% PER		-110		dBm
Sensitivity	FSK, 20 kbps, $\pm 10\text{ kHz}$ deviation, 2-GFSK, 868.3 MHz, 52 kHz RX BW, 20 byte PSDU < 10% PER		-110		dBm
Saturation limit	20 byte PSDU < 10% PER, 868.3 MHz		10		dBm
Selectivity, +100 kHz	20 byte PSDU < 10% PER, 868.3 MHz		38		dB
Selectivity, -100 kHz			36		dB
Selectivity, +200 kHz			44		dB
Selectivity, -200 kHz			42		dB
Selectivity, +400 kHz			49		dB
Selectivity, -400 kHz			44		dB
Blocking, +1 MHz			58		dB
Blocking, -1 MHz			54		dB
Blocking, -2 MHz			61		dB
Blocking, +2 MHz			61		dB
Blocking, -5 MHz			70		dB
Blocking, +5 MHz			70		dB
Blocking, -10 MHz			75		dB
Blocking, +10 MHz			76		dB
Selectivity, +100 kHz	20 byte PSDU < 10% PER, 868.3 MHz. Wanted signal 3 dB above sensitivity level.		36		dB
Selectivity, -100 kHz			34		dB
Selectivity, +200 kHz			42		dB
Selectivity, -200 kHz			41		dB
Selectivity, +400 kHz			47		dB
Selectivity, -400 kHz			46		dB
Blocking, +1 MHz			56		dB
Blocking, -1 MHz			55		dB
Blocking, +2 MHz			61		dB
Blocking, -2 MHz			61		dB
Blocking, +5 MHz			71		dB
Blocking, -5 MHz			70		dB
Blocking, +10 MHz			75		dB
Blocking, -10 MHz			75		dB
Blocking + 5% Fc. (45.75 MHz)	20 byte PSDU < 10% PER, 866.6 MHz, wanted signal -94 dBm. 3 dB above usable sensitivity limit according to ETSI EN 300 220 V3.1.1 (usable sensitivity -97 dBm). Limit is Cat 1.5 requirement.		-13		dBm
Blocking - 5% Fc. (-45.75 MHz)			-13		dBm
Image rejection (image compensation enabled)	20 byte PSDU < 10% PER, 866.6 MHz. Wanted signal 3 dB above sensitivity limit.		39		dB
Image rejection (image compensation enabled)	20 byte PSDU < 10% PER, 866.6 MHz ⁽¹⁾		39		dB
Image rejection (image compensation enabled)	-40 to 125°C, 10% PER, 250 byte payload, 866.6 MHz		39		dB
RSSI dynamic range	Starting from the sensitivity limit		100		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Frequency error tolerance (ppm)	20 byte PSDU < 10% PER, measured at 10 dB above sensitivity level. Negative offset		-24		ppm
Frequency error tolerance (ppm)	20 byte PSDU < 10% PER, measured at 10 dB above sensitivity level. Positive offset		24		ppm

8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When Measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Symbol rate error tolerance (ppm)	20 byte PSDU < 10% PER, measured at 10 dB above sensitivity level. Negative offset		-1000		ppm
Symbol rate error tolerance (ppm)	20 byte PSDU < 10% PER, measured at 10 dB above sensitivity level. Negative offset		1000		ppm
802.15.4, 200 kbps, $\pm 50\text{ kHz}$ deviation, 2-GFSK, 311 kHz RX BW					
Sensitivity	BER = 10^{-2} , 868 MHz		-103		dBm
Sensitivity	BER = 10^{-2} , 915 MHz		-103		dBm
Selectivity, +400 kHz	BER = 10^{-2} , 915 MHz. Wanted signal 3 dB above sensitivity limit.		45		dB
Selectivity, -400 kHz	BER = 10^{-2} , 915 MHz. Wanted signal 3 dB above sensitivity limit.		45		dB
Selectivity, +800 kHz	BER = 10^{-2} , 915 MHz. Wanted signal 3 dB above sensitivity limit.		52		dB
Selectivity, -800 kHz	BER = 10^{-2} , 915 MHz. Wanted signal 3 dB above sensitivity limit.		47		dB
Blocking, +2 MHz	BER = 10^{-2} , 915 MHz. Wanted signal 3 dB above sensitivity limit.		59		dB
Blocking, -2 MHz	BER = 10^{-2} , 915 MHz. Wanted signal 3 dB above sensitivity limit.		56		dB
Blocking, +10 MHz	BER = 10^{-2} , 915 MHz. Wanted signal 3 dB above sensitivity limit.		71		dB
Blocking, -10 MHz	BER = 10^{-2} , 915 MHz. Wanted signal 3 dB above sensitivity limit.		70		dB
802.15.4, 500 kbps, $\pm 190\text{ kHz}$ deviation, 2-GFSK, 622 kHz RX BW					
Sensitivity 500 kbps	915 MHz, 1% PER, 127 byte payload		-95		dBm
Selectivity, $\pm 1\text{ MHz}$	915 MHz, 1% PER, 127 byte payload. Wanted signal at -88 dBm		34		dB
Selectivity, $\pm 2\text{ MHz}$	915 MHz, 1% PER, 127 byte payload. Wanted signal at -88 dBm		46		dB
Co-channel rejection	915 MHz, 1% PER, 127 byte payload. Wanted signal at -71 dBm		-8		dB
SimpleLink™ Long Range 2.5/5 kbps (20 ksps), $\pm 5\text{ kHz}$ Deviation, 2-GFSK, 34 kHz RX Bandwidth, FEC = 1:2, DSSS = 1:4/1:2					
Sensitivity	2.5 kbps, BER = 10^{-2} , 868 MHz		-121		dBm
Sensitivity	2.5 kbps, BER = 10^{-2} , 915 MHz		-121		dBm
Sensitivity	5 kbps, BER = 10^{-2} , 868 MHz		-119		dBm
Sensitivity	5 kbps, BER = 10^{-2} , 915 MHz		-119		dBm
Saturation limit	2.5 kbps, BER = 10^{-2} , 868 MHz		10		dBm
Selectivity, +100 kHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		49		dB
Selectivity, -100 kHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		49		dB
Selectivity, +200 kHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		52		dB
Selectivity, -200 kHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		48		dB
Selectivity, +300 kHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		54		dB
Selectivity, -300 kHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		48		dB
Blocking, +1 MHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		65		dB
Blocking, -1 MHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		60		dB
Blocking, +2 MHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		70		dB
Blocking, -2 MHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		68		dB
Blocking, +5 MHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		78		dB
Blocking, -5 MHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		77		dB
Blocking, +10 MHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		87		dB
Blocking, -10 MHz	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		92		dB

8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When Measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Image rejection (image compensation enabled)	2.5 kbps, BER = 10^{-2} , 868 MHz ⁽¹⁾		47		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		± 3		dB
Frequency error tolerance (ppm)	2.5 kbps, 20 kbaud, DSSS=4, $\frac{1}{2}$ K=7 FEC. measured at -110 dBm.		-24/26		ppm
Symbolrate error tolerance (ppm)	2.5 kbps, 20 kbaud, DSSS=4, $\frac{1}{2}$ K=7 FEC. measured at -110 dBm. Referred to 20 kbaud chip rate.		-90/70		ppm
Narrowband, 9.6 kbps ± 2.4 kHz deviation, 2-GFSK, 868 MHz, 17.1 kHz RX BW					
Sensitivity	1% BER		-117		dBm
Adjacent Channel Rejection	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6 dBm). Interferer ± 20 kHz		42		dB
Alternate Channel Rejection	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6 dBm). Interferer ± 40 kHz		42		dB
Blocking, ± 1 MHz	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6 dBm).		66		dB
Blocking, ± 2 MHz	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6 dBm).		71		dB
Blocking, ± 10 MHz	1% BER. Wanted signal 3 dB above usable sensitivity limit (usable sensitivity -104.6 dBm).		85		dB
802.15.4, 50 kbps, ± 25 kHz Deviation, 2-GFSK, 100 kHz RX BW (Legacy)					
Sensitivity	BER = 10^{-2} , 868 MHz		- 110		dBm
Sensitivity	BER = 10^{-2} , 915 MHz		- 110		dBm
Saturation limit	BER = 10^{-2} , 868 MHz		10		dBm
Selectivity, +200 kHz	BER = 10^{-2} , 868 MHz ⁽¹⁾		44		dB
Selectivity, -200 kHz			44		dB
Selectivity, +400 kHz			54		dB
Selectivity, -400 kHz			44		dB
Blocking, +1 MHz			57		dB
Blocking, -1 MHz			57		dB
Blocking, +2 MHz			61		dB
Blocking, -2 MHz			61		dB
Blocking, +5 MHz			67		dB
Blocking, -5 MHz			67		dB
Blocking, +10 MHz			76		dB
Blocking, -10 MHz			76		dB
Selectivity, +200 kHz	BER = 10^{-2} , 868 MHz. Wanted signal 3 dB above sensitivity limit.		45		dB
Selectivity, -200 kHz			45		dB
Selectivity, +400 kHz			51		dB
Selectivity, -400 kHz			45		dB
Blocking, +1 MHz			61		dB
Blocking, -1 MHz			61		dB
Blocking, +2 MHz			63		dB
Blocking, -2 MHz			63		dB
Blocking, +5 MHz			67		dB
Blocking, -5 MHz			67		dB
Blocking, +10 MHz			73		dB
Blocking, -10 MHz			73		dB

8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When Measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Blocking + 5% Fc. (43.42 MHz)	BER = 10^{-2} , 868 MHz		-15		dBm
Blocking - 5% Fc. (-43.42 MHz)	802.15.4g mandatory mode, wanted signal -94 dBm. 3 dB above usable sensitivity limit according to ETSI EN 300 220 V3.1.1 (usable sensitivity -97 dBm). Limit is Cat 1.5 requirement.		-15		dBm
Image rejection (image compensation enabled)	BER = 10^{-2} , 868 MHz. Wanted signal 3 dB above sensitivity limit.		39		dB
Image rejection (image compensation enabled)	BER = 10^{-2} , 868 MHz ⁽¹⁾		39		dB
Image rejection (image compensation enabled)	-40 to 125°C. BER = 10^{-2} , 868 MHz		41		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
Frequency error tolerance (ppm)	1% BER, measured at -100 dBm (10 dB above sensitivity level). Negative offset		-30		ppm
Frequency error tolerance (ppm)	1% BER, measured at -100 dBm (10 dB above sensitivity level). Positive offset		25		ppm
Symbol rate error tolerance (ppm)	1% BER, measured at -100 dBm (10 dB above sensitivity level). Negative offset		-2000		ppm
Symbol rate error tolerance (ppm)	1% BER, measured at -100 dBm (10 dB above sensitivity level) Positive offset		2000		ppm
802.15.4, 100 kbps, ±25 kHz deviation, 2-GFSK, 137 kHz RX BW					
Sensitivity 100 kbps	868 MHz, 1% PER, 127 byte payload		-103		dBm
Selectivity, ±200 kHz	868 MHz, 1% PER, 127 byte payload. Wanted signal at -96 dBm		38		dB
Selectivity, ±400 kHz			44		dB
Co-channel rejection	868 MHz, 1% PER, 127 byte payload. Wanted signal at -79 dBm		-9		dB
Generic OOK (16.384 kbps, OOK w / Manchester encoding, 100 kHz RX BW)					
Sensitivity	OOK, 915.0 MHz, 1% BER		-114		dBm
Sensitivity	OOK, 868.8 MHz, 1% BER		-113		dBm
Saturation limit	868.3 MHz		0		dBm
Selectivity, +200 kHz	868.3 MHz ⁽¹⁾		52		dB
Selectivity, -200 kHz			48		dB
Selectivity, +400 kHz			68		dB
Selectivity, -400 kHz			64		dB
Blocking, +1 MHz			64		dB
Blocking, -1 MHz			59		dB
Blocking, +2 MHz			64		dB
Blocking, -2 MHz			59		dB
Blocking, +5 MHz			72		dB
Blocking, -5 MHz			73		dB
Blocking, +10 MHz			64		dB
Blocking, -10 MHz			58		dB

8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When Measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, +200 kHz	868.3 MHz. Wanted signal 3 dB above sensitivity level.		52		dB
Selectivity, -200 kHz			47		dB
Selectivity, +400 kHz			42		dB
Selectivity, -400 kHz			42		dB
Blocking, +1 MHz			68		dB
Blocking, -1 MHz			64		dB
Blocking, +2 MHz			68		dB
Blocking, -2 MHz			64		dB
Blocking, +5 MHz			74		dB
Blocking, -5 MHz			73		dB
Blocking, +10 MHz			68		dB
Blocking, -10 MHz			64		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
Frequency error tolerance (ppm)	Measured at 10 dB above sensitivity level. Negative offset		-40		ppm
Frequency error tolerance (ppm)	Measured at 10 dB above sensitivity level. Positive offset		40		ppm
Symbol rate error tolerance (ppm)	Measured at 10 dB above sensitivity level. Negative offset		-2000		ppm
Symbol rate error tolerance (ppm)	Measured at 10 dB above sensitivity level. Positive offset		2000		ppm

(1) Wanted signal 3 dB above usable sensitivity limit according to ETSI EN 300 220 v. 3.1.1.

8.11 861 MHz to 1054 MHz - Transmit (TX)

When measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted. ⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General parameters						
Max output power, boost mode		VDDR = 1.95 V Minimum supply voltage (VDDS) for boost mode is 2.1 V 868 MHz and 915 MHz		14		dBm
Max output power		868 MHz and 915 MHz		12		dBm
Output power programmable range		868 MHz and 915 MHz, 1dB step size.		34		dB
Output power variation over temperature		+10 dBm setting Over recommended temperature operating range		± 2		dB
Output power variation over temperature Boost mode		+14 dBm setting Over recommended temperature operating range		± 1.5		dB
Spurious emissions and harmonics						
Spurious emissions (excluding harmonics) ⁽³⁾	30 MHz to 1 GHz	+14 dBm setting ETSI restricted bands		< -54		dBm
		+14 dBm setting ETSI outside restricted bands		< -36		dBm
	1 GHz to 12.75 GHz (outside ETSI restricted bands)	+14 dBm setting measured in 1 MHz bandwidth (ETSI)		< -30		dBm
Spurious emissions out-of-band, 915 MHz ⁽³⁾	30 MHz to 88 MHz (within FCC restricted bands)	+14 dBm setting		< -56		dBm
	88 MHz to 216 MHz (within FCC restricted bands)	+14 dBm setting		< -52		dBm
	216 MHz to 960 MHz (within FCC restricted bands)	+14 dBm setting		< -50		dBm
	960 MHz to 2390 MHz and above 2483.5 MHz (within FCC restricted band)	+14 dBm setting		< -42		dBm
	1 GHz to 12.75 GHz (outside FCC restricted bands)	+14 dBm setting		< -40		dBm
Spurious emissions out-of-band, 920.6/928 MHz ⁽³⁾	Below 710 MHz (ARIB T-108)	+14 dBm setting		< -36		dBm
	710 MHz to 900 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	900 MHz to 915 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	930 MHz to 1000 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	1000 MHz to 1215 MHz (ARIB T-108)	+14 dBm setting		< -45		dBm
	Above 1215 MHz (ARIB T-108)	+14 dBm setting		< -30		dBm
Harmonics	Second harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -30		
	Third harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -42		
	Fourth harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -30		
	Fifth harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -42		

- (1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.

- (2) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

8.12 861 MHz to 1054 MHz - PLL Phase Noise Wideband Mode

When measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868- and 915-MHz bands 20 kHz PLL loop bandwidth	±10 kHz offset		- 74		dBc/Hz
	±100 kHz offset		- 97		dBc/Hz
	±200 kHz offset		- 107		dBc/Hz
	±400 kHz offset		- 113		dBc/Hz
	±1000 kHz offset		- 120		dBc/Hz
	±2000 kHz offset		- 127		dBc/Hz
	±10000 kHz offset		- 141		dBc/Hz

8.13 861 MHz to 1054 MHz - PLL Phase Noise Narrowband Mode

When measured on the LP-EM-CC1314R10 reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868- and 915-MHz bands 150 kHz PLL loop bandwidth	±10 kHz offset		- 96		dBc/Hz
	±100 kHz offset		- 95		dBc/Hz
	±200 kHz offset		- 94		dBc/Hz
	±400 kHz offset		- 104		dBc/Hz
	±1000 kHz offset		- 121		dBc/Hz
	±2000 kHz offset		- 130		dBc/Hz
	±10000 kHz offset		- 140		dBc/Hz

8.14 Timing and Switching Characteristics

8.14.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

8.14.2 Wakeup Timing

Measured over operating free-air temperature with $V_{\text{DDS}} = 3.0\text{ V}$ (unless otherwise noted). The times listed here do not include software overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset to Active ⁽¹⁾		850 - 4000			µs
MCU, Shutdown to Active ⁽¹⁾		850 - 4000			µs
MCU, Standby to Active		160			µs
MCU, Active to Standby		39			µs
MCU, Idle to Active		15			µs

- (1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again. The wake up time increases with a higher capacitor value.

8.14.3 Clock Specifications

8.14.3.1 48 MHz Clock Input (TCXO)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.⁽¹⁾

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Clock frequency			48		MHz
	TCXO clipped sine output, peak-to-peak	TCXO clipped sine output connected to pin X48M_P through series capacitor	0.8		1.7	V
	TCXO with CMOS output, High input voltage	TCXO with CMOS output	1.3		VDDR	V
	TCXO with CMOS output, Low input voltage	directly coupled to pin X48M_P	0		0.3	V

(1) Probing or otherwise stopping the TCXO while the DC/DC converter is enabled may cause permanent damage to the device.

8.14.3.2 48 MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.⁽¹⁾

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance $6\text{ pF} < C_L \leq 9\text{ pF}$		20	60	Ω
ESR	Equivalent series resistance $5\text{ pF} < C_L \leq 6\text{ pF}$			80	Ω
L_M	Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads) ⁽⁵⁾	$< 3 \times 10^{-25} / C_L^2$			H
C_L	Crystal load capacitance ⁽⁴⁾	5	7 ⁽³⁾	9	pF
	Start-up time ⁽²⁾		200		μs

- (1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
- (2) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
- (3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
- (4) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations. See the device errata for further details.
- (5) The crystal manufacturer's specification must satisfy this requirement for proper operation.

8.14.3.3 48 MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		± 1		%
Calibrated frequency accuracy ⁽¹⁾		± 0.25		%
Start-up time		5		μs

(1) Accuracy relative to the calibration source (XOSC_HF)

8.14.3.4 2 MHz RC Oscillator (RCOSC_MF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		2		MHz
Start-up time		5		μs

8.14.3.5 32.768 kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Crystal frequency		32.768		kHz

8.14.3.5 32.768 kHz Crystal Oscillator (XOSC_LF) (continued)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

		MIN	TYP	MAX	UNIT
ESR	Equivalent series resistance		30	100	k Ω
C _L	Crystal load capacitance	6	7 ⁽¹⁾	12	pF

- (1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

8.14.3.6 32 kHz RC Oscillator (RCOSC_LF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

		MIN	TYP	MAX	UNIT
	Calibrated frequency		32.8 ⁽¹⁾		kHz
	Temperature coefficient		50		ppm/ $^\circ\text{C}$

- (1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

8.14.4 Serial Peripheral Interface (SPI) Characteristics

8.14.4.1 SPI Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK} 1/ t_{sclk}	SPI clock frequency	Master Mode $1.8 < V_{\text{DDS}} < 3.8$			12	MHz
		Slave Mode $2.7 < V_{\text{DDS}} < 3.8$			8	
		Slave Mode $V_{\text{DDS}} < 2.7$			7	
DC _{SCK}	SCK Duty Cycle		45	50	55	%

8.14.4.2 SPI Master Mode

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{SCLK}_H/L}$	SCLK High or Low time		$(t_{\text{SPI}}/2) - 1$	$t_{\text{SPI}} / 2$	$(t_{\text{SPI}}/2) + 1$	ns
$t_{\text{CS.LEAD}}$	CS lead-time, CS active to clock		1			SCLK
$t_{\text{CS.LAG}}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{\text{CS.ACC}}$	CS access time, CS active to MOSI data out				1	SCLK
$t_{\text{CS.DIS}}$	CS disable time, CS inactive to MOSI high impedance				1	SCLK
$t_{\text{SU.MI}}$	MISO input data setup time ⁽¹⁾	$V_{\text{DDS}} = 3.3\text{ V}$	12.5			ns
$t_{\text{SU.MI}}$	MISO input data setup time	$V_{\text{DDS}} = 1.8\text{ V}$	23.5			ns
$t_{\text{HD.MI}}$	MISO input data hold time		0			ns
$t_{\text{VALID.MO}}$	MOSI output data valid time ⁽²⁾	SCLK edge to MOSI valid, CL = 20 pF (4)			13	ns
$t_{\text{HD.MO}}$	MOSI output data hold time ⁽³⁾	CL = 20 pF	0			ns

- (1) The MISO input data setup time can be fully compensated when delayed sampling feature is enabled.
 (2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
 (3)

Specifies how long data on the output is valid after the output changing SCLK clock edge

8.14.4.3 SPI Master Mode Timing Diagrams

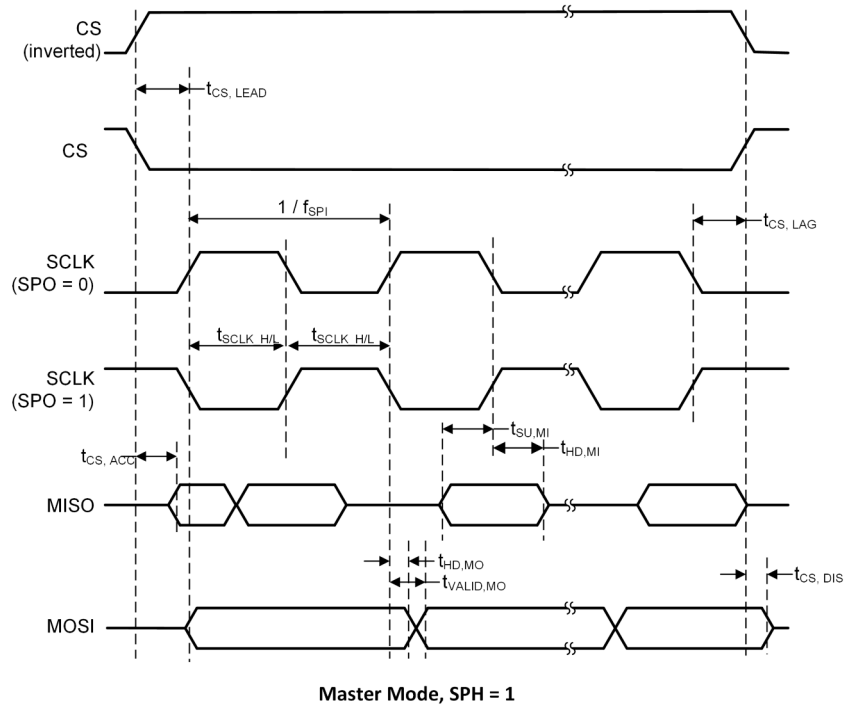
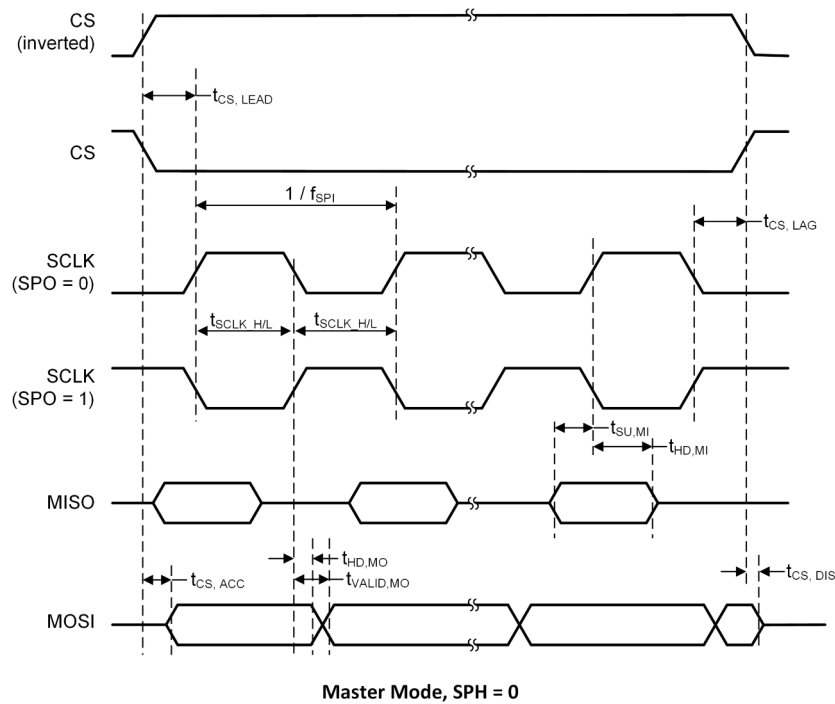


图 8-1. SPI Master Mode Timing

8.14.4.4 SPI Slave Mode

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to MISO data out	VDDS = 3.3V			56	ns
$t_{CS.ACC}$	CS access time, CS active to MISO data out	VDDS = 1.8V			70	ns
$t_{CS.DIS}$	CS disable time, CS inactive to MISO high impedance	VDDS = 3.3V			56	ns
$t_{CS.DIS}$	CS disable time, CS inactive to MISO high impedance	VDDS = 1.8V			70	ns
$t_{SU.SI}$	MOSI input data setup time		30			ns
$t_{HD.SI}$	MOSI input data hold time		0			ns
$t_{VALID.SO}$	MISO output data valid time ⁽¹⁾	SCLK edge to MISO valid, $C_L = 20$ pF, 3.3V (4)			50	ns
$t_{VALID.SO}$	MISO output data valid time ⁽¹⁾	SCLK edge to MISO valid, $C_L = 20$ pF, 1.8V (4)			65	ns
$t_{HD.SO}$	MISO output data hold time ⁽²⁾	$C_L = 20$ pF	0			ns

- (1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
 (2) Specifies how long data on the output is valid after the output changing SCLK clock edge

8.14.4.5 SPI Slave Mode Timing Diagrams

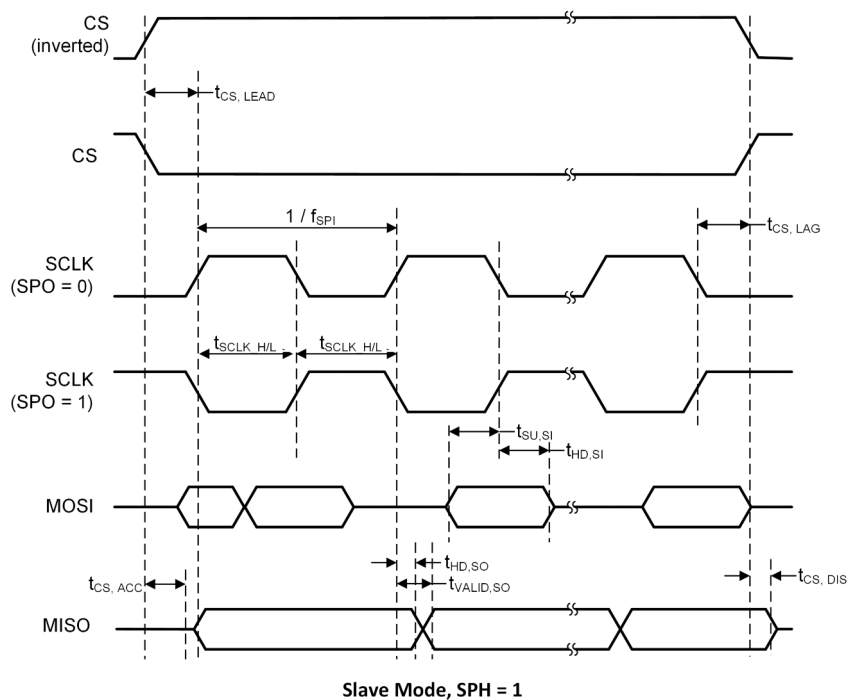
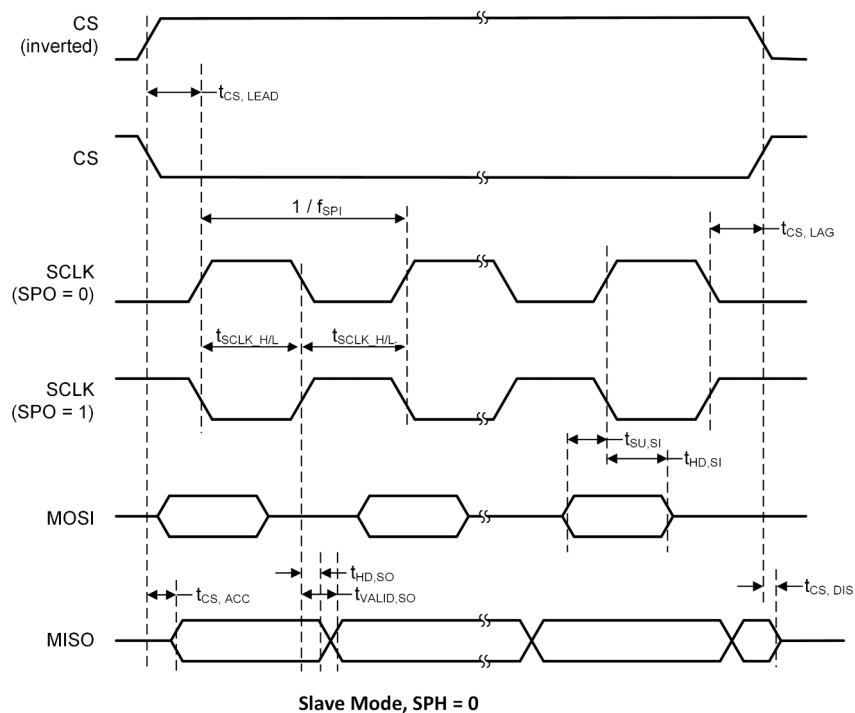


图 8-2. SPI Slave Mode Timing

8.14.5 UART

8.14.5.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

8.15 Peripheral Characteristics

8.15.1 ADC

8.15.1.1 Analog-to-Digital Converter (ADC) Characteristics

$T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$ and voltage scaling enabled, unless otherwise noted.⁽¹⁾

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V _{DDS}	V
Resolution			12		Bits
Sample Rate				200	ksps
Offset	Internal 4.3 V equivalent reference ⁽²⁾		- 0.24		LSB
Gain error	Internal 4.3 V equivalent reference ⁽²⁾		7.14		LSB
DNL ⁽⁴⁾	Differential nonlinearity		> - 1		LSB
INL	Integral nonlinearity		±4		LSB
ENOB	Effective number of bits	Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone		9.8	Bits
		Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled		9.8	
		V _{DDS} as reference, 200 kSamples/s, 9.6 kHz input tone		10.1	
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		11.1	
		Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 300 Hz input tone ⁽⁵⁾		11.3	
		Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 300 Hz input tone ⁽⁵⁾		11.6	
THD	Total harmonic distortion	Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone		- 65	dB
		V _{DDS} as reference, 200 kSamples/s, 9.6 kHz input tone		- 70	
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		- 72	
SINAD, SNDR	Signal-to-noise and distortion ratio	Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone		60	dB
		V _{DDS} as reference, 200 kSamples/s, 9.6 kHz input tone		63	
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		68	
SFDR	Spurious-free dynamic range	Internal 4.3 V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6 kHz input tone		70	dB
		V _{DDS} as reference, 200 kSamples/s, 9.6 kHz input tone		73	
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		75	
	Conversion time	Serial conversion, time-to-output, 24 MHz clock		50	Clock Cycles
	Current consumption	Internal 4.3 V equivalent reference ⁽²⁾		0.42	mA
	Current consumption	V _{DDS} as reference		0.6	mA
	Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1		4.3 ⁽²⁾ ⁽³⁾	V

8.15.1.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

$T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$ and voltage scaling enabled, unless otherwise noted.⁽¹⁾

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: $V_{\text{ref}} = 4.3\text{ V} \times 1408 / 4095$		1.48		V
	Reference voltage	VDDS as reference, input voltage scaling enabled		VDDS		V
	Reference voltage	VDDS as reference, input voltage scaling disabled		VDDS / 2.82 ⁽³⁾		V
	Input impedance	200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		M Ω

- (1) Using IEEE Std 1241-2010 for terminology and test methods
- (2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
- (3) Applied voltage must be within [Absolute Maximum Ratings](#) at all times
- (4) No missing codes
- (5) $\text{ADC_output} = \Sigma (4^n \text{ samples}) \gg n$, n = desired extra bits

8.15.2 DAC

8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics

$T_c = 25\text{ }^{\circ}\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters						
	Resolution		8			Bits
V _{DD5}	Supply voltage	Any load, any V _{REF} , pre-charge OFF, DAC charge-pump ON	1.8		3.8	V
		External Load ⁽⁴⁾ , any V _{REF} , pre-charge OFF, DAC charge-pump OFF	2.0		3.8	
		Any load, V _{REF} = DCOUPL, pre-charge ON	2.6		3.8	
F _{DAC}	Clock frequency	Buffer ON (recommended for external load)	16		250	kHz
		Buffer OFF (internal load)	16		1000	
	Voltage output settling time	V _{REF} = VDD5, buffer OFF, internal load		13		1 / F _{DAC}
		V _{REF} = VDD5, buffer ON, external capacitive load = 20 pF ⁽³⁾		13.8		
	External capacitive load			20	200	pF
	External resistive load		10			M Ω
	Short circuit current				400	μA
Z _{MAX}	Max output impedance Vref = VDD5, buffer ON, CLK 250 kHz	VDD5 = 3.8 V, DAC charge-pump OFF		50.8		k Ω
		VDD5 = 3.0 V, DAC charge-pump ON		51.7		
		VDD5 = 3.0 V, DAC charge-pump OFF		53.2		
		VDD5 = 2.0 V, DAC charge-pump ON		48.7		
		VDD5 = 2.0 V, DAC charge-pump OFF		70.2		
		VDD5 = 1.8 V, DAC charge-pump ON		46.3		
		VDD5 = 1.8 V, DAC charge-pump OFF		88.9		
Internal Load - Continuous Time Comparator / Low Power Clocked Comparator						
DNL	Differential nonlinearity	V _{REF} = VDD5, load = Continuous Time Comparator or Low Power Clocked Comparator F _{DAC} = 250 kHz		±1		LSB ⁽¹⁾
	Differential nonlinearity	V _{REF} = VDD5, load = Continuous Time Comparator or Low Power Clocked Comparator F _{DAC} = 16 kHz		±1.2		
	Offset error ⁽²⁾ Load = Continuous Time Comparator	V _{REF} = VDD5 = 3.8 V		±0.64		LSB ⁽¹⁾
		V _{REF} = VDD5= 3.0 V		±0.81		
		V _{REF} = VDD5 = 1.8 V		±1.27		
		V _{REF} = DCOUPL, pre-charge ON		±3.43		
		V _{REF} = DCOUPL, pre-charge OFF		±2.88		
		V _{REF} = ADCREF		±2.37		
	Offset error ⁽²⁾ Load = Low Power Clocked Comparator	V _{REF} = VDD5= 3.8 V		±0.78		LSB ⁽¹⁾
		V _{REF} = VDD5 = 3.0 V		±0.77		
		V _{REF} = VDD5= 1.8 V		±3.46		
		V _{REF} = DCOUPL, pre-charge ON		±3.44		
		V _{REF} = DCOUPL, pre-charge OFF		±4.70		
		V _{REF} = ADCREF		±4.11		
	Max code output voltage variation ⁽²⁾ Load = Continuous Time Comparator	V _{REF} = VDD5 = 3.8 V		±1.53		LSB ⁽¹⁾
		V _{REF} = VDD5 = 3.0 V		±1.71		
		V _{REF} = VDD5= 1.8 V		±2.10		
		V _{REF} = DCOUPL, pre-charge ON		±6.00		
		V _{REF} = DCOUPL, pre-charge OFF		±3.85		
		V _{REF} = ADCREF		±5.84		

8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

$T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Max code output voltage variation ⁽²⁾ Load = Low Power Clocked Comparator	V _{REF} = V _{DDS} = 3.8 V		±2.92		LSB ⁽¹⁾
		V _{REF} =V _{DDS} = 3.0 V		±3.06		
		V _{REF} = V _{DDS} = 1.8 V		±3.91		
		V _{REF} = DCOUPL, pre-charge ON		±7.84		
		V _{REF} = DCOUPL, pre-charge OFF		±4.06		
		V _{REF} = ADCREF		±6.94		
	Output voltage range ⁽²⁾ Load = Continuous Time Comparator	V _{REF} = V _{DDS} = 3.8 V, code 1		0.03		V
		V _{REF} = V _{DDS} = 3.8 V, code 255		3.62		
		V _{REF} = V _{DDS} = 3.0 V, code 1		0.02		
		V _{REF} = V _{DDS} = 3.0 V, code 255		2.86		
		V _{REF} = V _{DDS} = 1.8 V, code 1		0.01		
		V _{REF} = V _{DDS} = 1.8 V, code 255		1.71		
		V _{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V _{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V _{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V _{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V _{REF} = ADCREF, code 1		0.01		
		V _{REF} = ADCREF, code 255		1.41		
	Output voltage range ⁽²⁾ Load = Low Power Clocked Comparator	V _{REF} = V _{DDS} = 3.8 V, code 1		0.03		V
		V _{REF} = V _{DDS} = 3.8 V, code 255		3.61		
		V _{REF} = V _{DDS} = 3.0 V, code 1		0.02		
		V _{REF} = V _{DDS} = 3.0 V, code 255		2.85		
		V _{REF} = V _{DDS} = 1.8 V, code 1		0.01		
		V _{REF} = V _{DDS} = 1.8 V, code 255		1.71		
		V _{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V _{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V _{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V _{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V _{REF} = ADCREF, code 1		0.01		
		V _{REF} = ADCREF, code 255		1.41		
External Load (Keysight 34401A Multimeter)						
INL	Integral nonlinearity	V _{REF} = V _{DDS} , F _{DAC} = 250 kHz		±1		LSB ⁽¹⁾
		V _{REF} = DCOUPL, F _{DAC} = 250 kHz		±1		
		V _{REF} = ADCREF, F _{DAC} = 250 kHz		±1		
DNL	Differential nonlinearity	V _{REF} = V _{DDS} , F _{DAC} = 250 kHz		±1		LSB ⁽¹⁾
	Offset error	V _{REF} = V _{DDS} = 3.8 V		±0.20		LSB ⁽¹⁾
		V _{REF} = V _{DDS} = 3.0 V		±0.25		
		V _{REF} = V _{DDS} = 1.8 V		±0.45		
		V _{REF} = DCOUPL, pre-charge ON		±1.55		
		V _{REF} = DCOUPL, pre-charge OFF		±1.30		
		V _{REF} = ADCREF		±1.10		
	Max code output voltage variation	V _{REF} = V _{DDS} = 3.8 V		±0.60		LSB ⁽¹⁾
		V _{REF} = V _{DDS} = 3.0 V		±0.55		
		V _{REF} = V _{DDS} = 1.8 V		±0.60		
		V _{REF} = DCOUPL, pre-charge ON		±3.45		
		V _{REF} = DCOUPL, pre-charge OFF		±2.10		
		V _{REF} = ADCREF		±1.90		

8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

$T_c = 25\text{ }^{\circ}\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage range Load = Low Power Clocked Comparator	$V_{REF} = V_{DD5} = 3.8\text{ V}$, code 1		0.03		V
	$V_{REF} = V_{DD5} = 3.8\text{ V}$, code 255		3.61		
	$V_{REF} = V_{DD5} = 3.0\text{ V}$, code 1		0.02		
	$V_{REF} = V_{DD5} = 3.0\text{ V}$, code 255		2.85		
	$V_{REF} = V_{DD5} = 1.8\text{ V}$, code 1		0.02		
	$V_{REF} = V_{DD5} = 1.8\text{ V}$, code 255		1.71		
	$V_{REF} = \text{DCOUPPL}$, pre-charge OFF, code 1		0.02		
	$V_{REF} = \text{DCOUPPL}$, pre-charge OFF, code 255		1.20		
	$V_{REF} = \text{DCOUPPL}$, pre-charge ON, code 1		1.27		
	$V_{REF} = \text{DCOUPPL}$, pre-charge ON, code 255		2.46		
	$V_{REF} = \text{ADCREFL}$, code 1		0.02		
	$V_{REF} = \text{ADCREFL}$, code 255		1.42		

- (1) 1 LSB ($V_{REF} = 3.8\text{ V}/3.0\text{ V}/1.8\text{ V}/\text{DCOUPPL}/\text{ADCREFL}$) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV
- (2) Includes comparator offset
- (3) A load > 20 pF will increase the settling time
- (4) Keysight 34401A Multimeter

8.15.3 Temperature and Battery Monitor

8.15.3.1 Temperature Sensor

Measured on a Texas Instruments reference design with $T_c = 25\text{ }^{\circ}\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			2		$^{\circ}\text{C}$
Accuracy	$-40\text{ }^{\circ}\text{C}$ to $0\text{ }^{\circ}\text{C}$		± 4.0		$^{\circ}\text{C}$
Accuracy	$0\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		± 2.5		$^{\circ}\text{C}$
Supply voltage coefficient ⁽¹⁾			3.6		$^{\circ}\text{C/V}$

(1) The temperature sensor is automatically compensated for V_{DD5} variation when using the TI-provided driver.

8.15.3.2 Battery Monitor

Measured on a Texas Instruments reference design with $T_c = 25\text{ }^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			25		mV
Range		1.8		3.8	V
Integral nonlinearity (max)			23		mV
Accuracy	$V_{DD5} = 3.0\text{ V}$		22.5		mV
Offset error			-32		mV
Gain error			-1		%

8.15.4 Comparators

8.15.4.1 Low-Power Clocked Comparator

$T_c = 25^\circ\text{C}$, $V_{DDS} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			SCLK_LF		
Internal reference voltage ⁽¹⁾	Using internal DAC with V_{DDS} as reference voltage, DAC code = 0 - 255		0.024 - 2.865		V
Offset	Measured at $V_{DDS} / 2$, includes error from internal DAC		± 5		mV
Decision time	Step from - 50 mV to 50 mV		1		Clock Cycle

- (1) The comparator can use an internal 8 bits DAC as its reference. The DAC output voltage range depends on the reference voltage selected. See [DAC Characteristics](#)

8.15.4.2 Continuous Time Comparator

$T_c = 25^\circ\text{C}$, $V_{DDS} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ⁽¹⁾		0		V_{DDS}	V
Offset	Measured at $V_{DDS} / 2$		± 5		mV
Decision time	Step from - 10 mV to 10 mV		0.78		μs
Current consumption	Internal reference		8.6		μA

- (1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

8.15.5 Current Source

8.15.5.1 Programmable Current Source

$T_c = 25^\circ\text{C}$, $V_{DDS} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range (logarithmic range)			0.25 - 20		μA
Resolution			0.25		μA

8.15.6 GPIO

8.15.6.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDs} = 1.8 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		1.56		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.24		V
GPIO VOH at 4 mA load	IOCURR = 1		1.59		V
GPIO VOL at 4 mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		73		μA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDs		19		μA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.73		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.35		V
T_A = 25 °C, V_{DDs} = 3.0 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		2.59		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.42		V
GPIO VOH at 4 mA load	IOCURR = 1		2.63		V
GPIO VOL at 4 mA load	IOCURR = 1		0.40		V
T_A = 25 °C, V_{DDs} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		282		μA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDs		110		μA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.55		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.42		V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a <i>High</i>	0.8*V _{DDs}			V
VIL	Highest GPIO input voltage reliably interpreted as a <i>Low</i>		0.2*V _{DDs}		V

8.16 Typical Characteristics

All measurements in this section are done with $T_c = 25^\circ\text{C}$ and $V_{\text{DD5}} = 3.0\text{ V}$, unless otherwise noted. See *Recommended Operating Conditions*, 节 8.3, for device limits. Values exceeding these limits are for reference only.

8.16.1 MCU Current

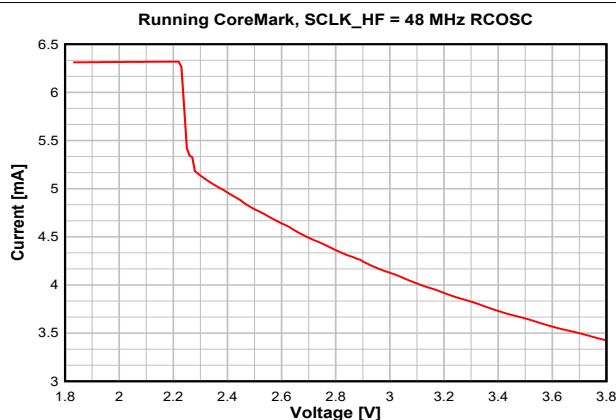


图 8-3. Active Mode (MCU) Current vs. Supply Voltage (V_{DD5})

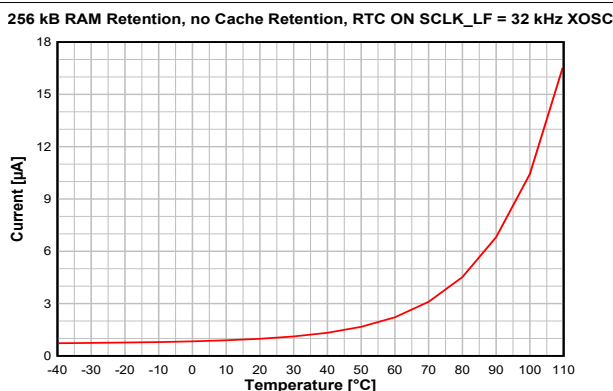


图 8-4. Standby Mode (MCU) Current vs. Temperature

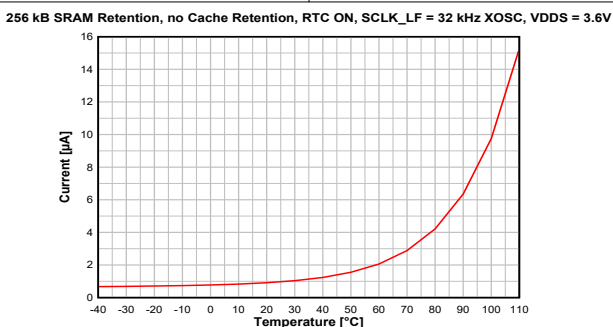


图 8-5. Standby Mode (MCU) Current vs. Temperature ($V_{\text{DD5}} = 3.6\text{ V}$)

8.16.2 RX Current

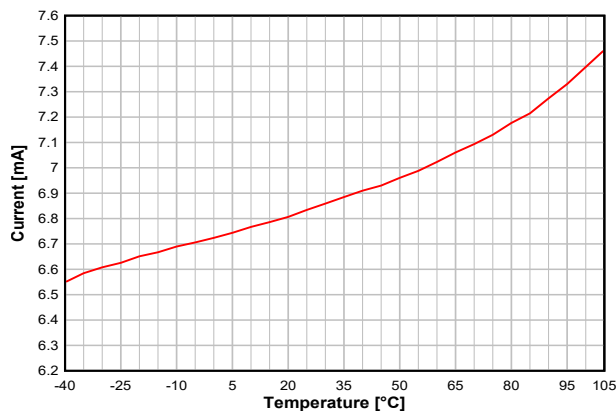


图 8-6. RX Current vs. Temperature (50 kbps, 868.3 MHz)

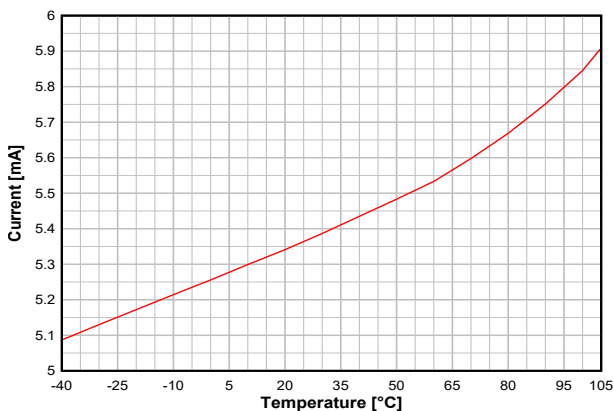


图 8-7. RX Current vs. Temperature (50 kbps, 868.3 MHz, $V_{\text{DD5}} = 3.6\text{ V}$)

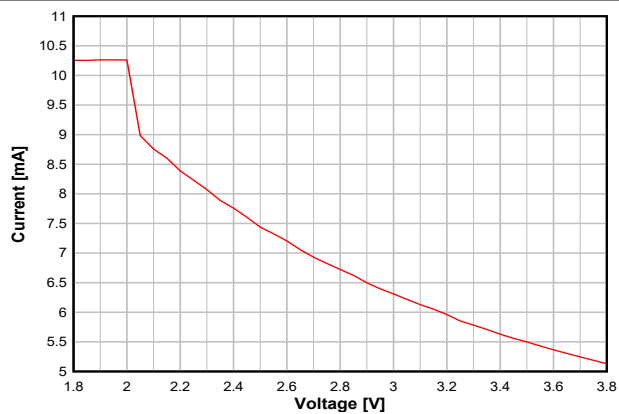


图 8-8. RX Current vs.
Supply Voltage (VDD) (50 kbps, 868.3 MHz)

8.16.3 TX Current

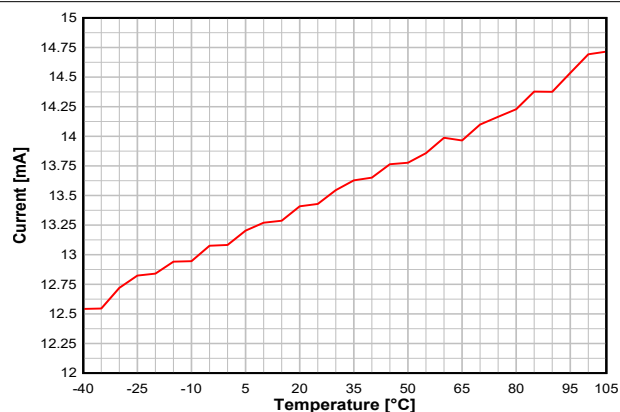


图 8-9. TX Current vs.
Temperature (50 kbps, 868.3 MHz, VDD = 3.6 V)

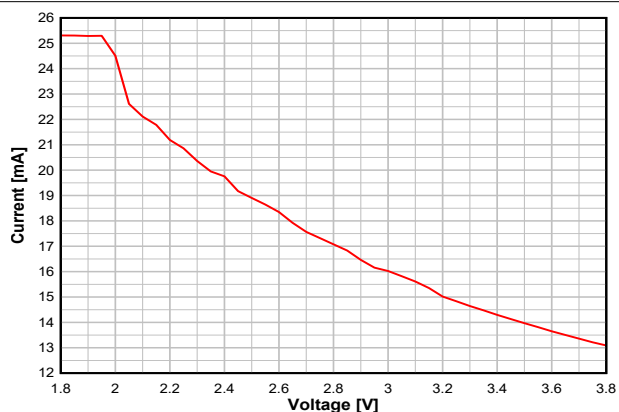


图 8-10. TX Current vs.
Supply Voltage (VDD) (50 kbps, 868.3 MHz)

CC1314R10

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表 8-1 shows typical TX current and output power for different output power settings.

表 8-1. Typical TX Current and Output Power

CC1314R10 at 868 MHz, VDD5 = 3.6 V (Measured on CC1312-R7EM-XD7793)			
txPower	TX Power Setting (SmartRF Studio)	Typical Output Power [dBm]	Typical Current Consumption [mA]
0x013F	14	14.6	25
0xB224	12.5	13.0	18.3
0x895E	12	12.6	17.4
0x669A	11	11.6	15.8
0x3E92	10	10.7	14.2
0x3EDC	9	9.7	13.3
0x2CD8	8	9.1	12.4
0x26D4	7	8.2	11.5
0x20D1	6	7.2	10.6
0x1CCE	5	5.9	9.8
0x16CD	4	5.4	9.4
0x14CB	3	4.1	8.8
0x12CA	2	3.3	8.4
0x12C9	1	2.5	8.0
0x10C8	0	1.5	7.7
0x0AC4	-5	-4.6	6.1
0x0AC2	-10	-10.3	5.4
0x06C1	-15	-14.8	5.0
0x04C0	-20	-19.8	4.7

8.16.4 RX Performance

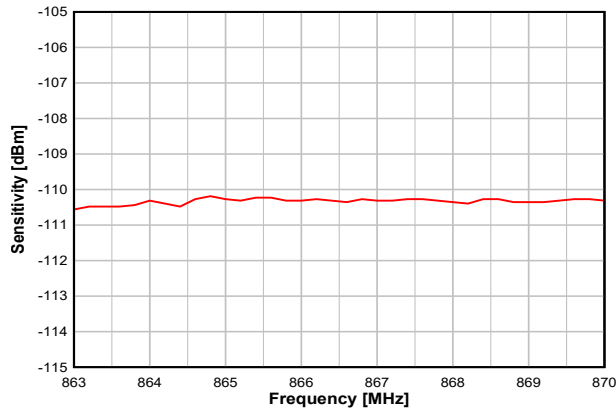


图 8-11. Sensitivity vs.
Frequency (50 kbps, 868 MHz)

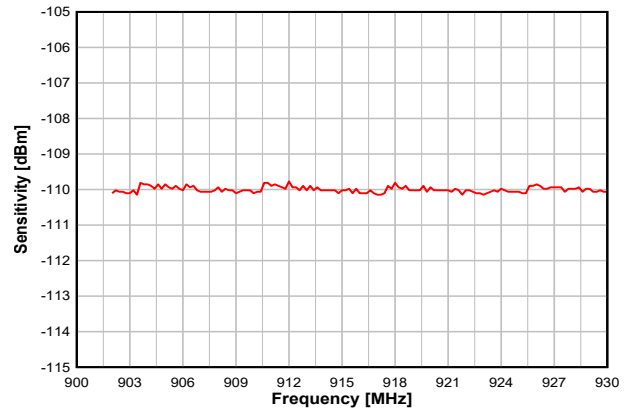


图 8-12. Sensitivity vs.
Frequency (50 kbps, 915 MHz)

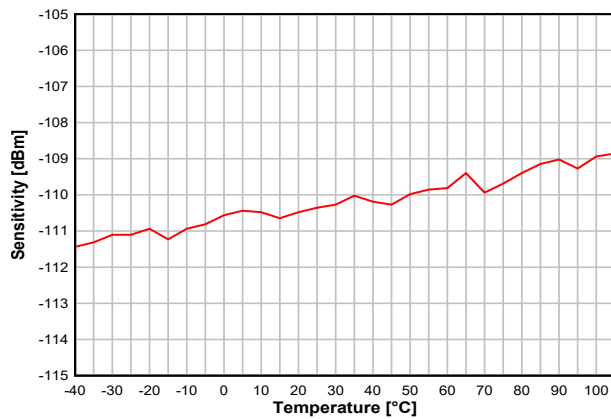


图 8-13. Sensitivity vs.
Temperature (50 kbps, 868.3 MHz)

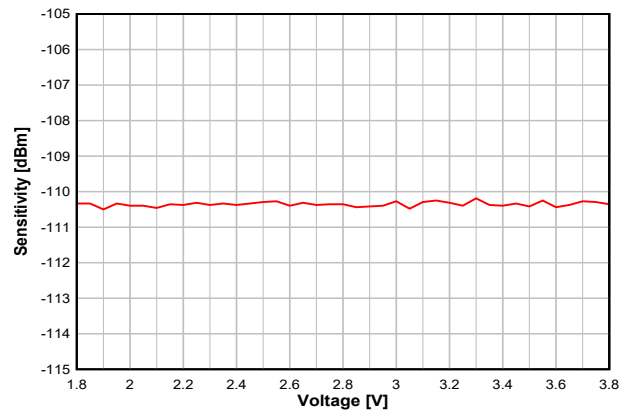


图 8-14. Sensitivity vs.
Supply Voltage (VDD5) (50 kbps, 868.3 MHz)

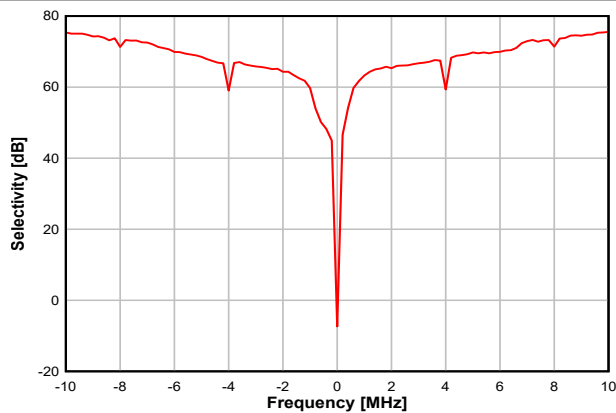


图 8-15. Selectivity vs.
Frequency Offset (50 kbps, 868.3 MHz)

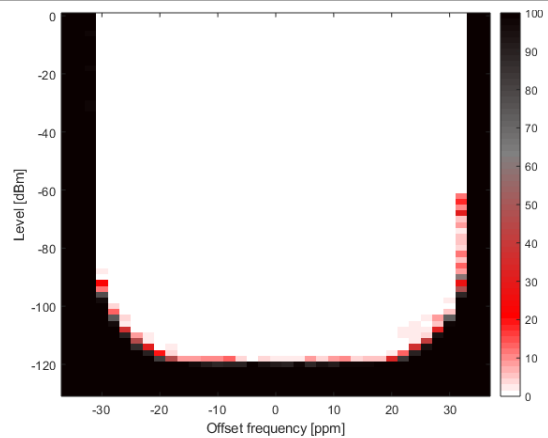


图 8-16. PER vs. Level vs.
Frequency (SimpleLink™ Long Range 5 kbps, 868
MHz)

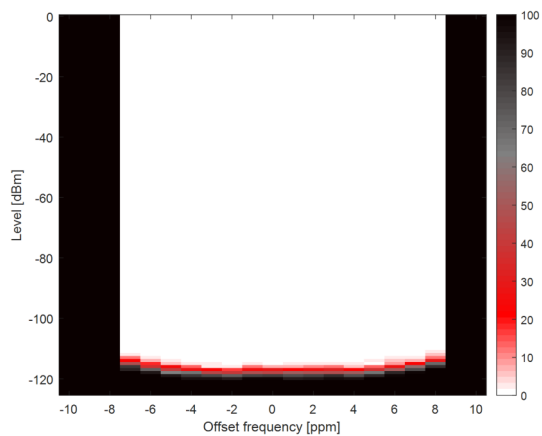


图 8-17. PER vs. Level vs.
Frequency (Narrowband, 9.6 kbps, ± 2.4 kHz deviation, 2-GFSK, 868 MHz, 17.1 kHz RX bandwidth)

8.16.5 TX Performance

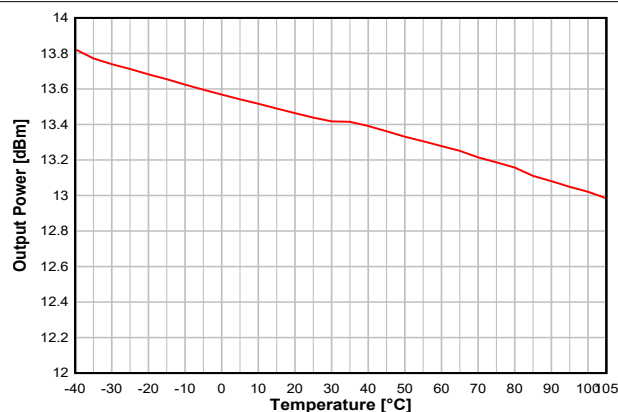


图 8-18. Output Power vs. Temperature (50 kbps, 868.3 MHz)

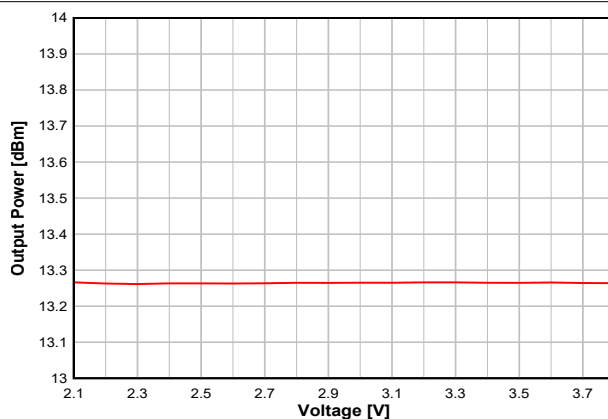


图 8-19. Output Power vs. Supply Voltage (VDD5) (50 kbps, 868.3 MHz)

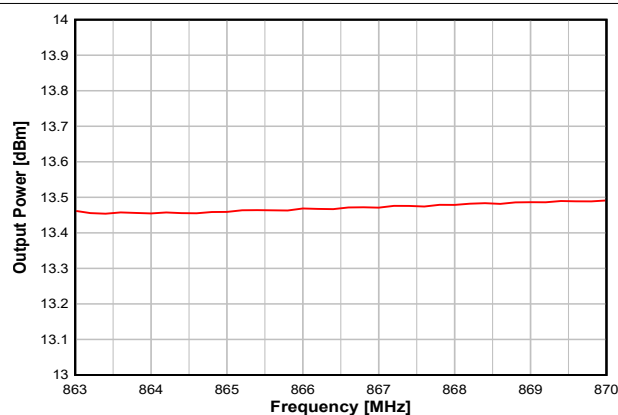


图 8-20. Output Power vs. Frequency (50 kbps, 868 MHz)

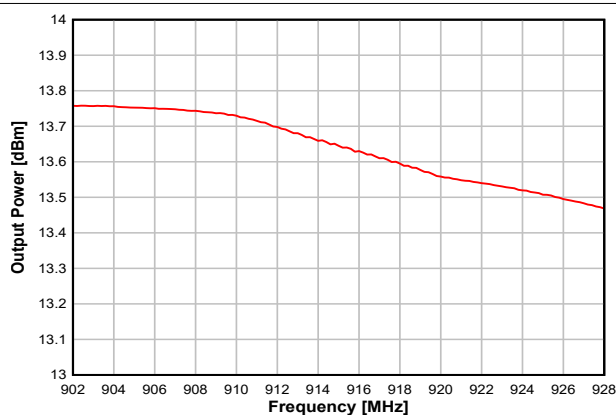


图 8-21. Output Power vs. Frequency (50 kbps, 915 MHz)

8.16.6 ADC Performance

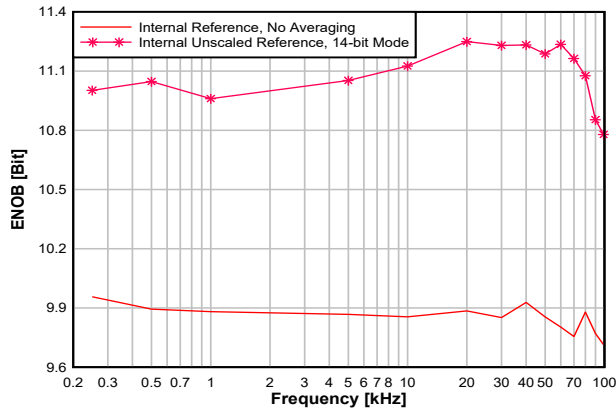


图 8-22. ENOB vs.
Input Frequency

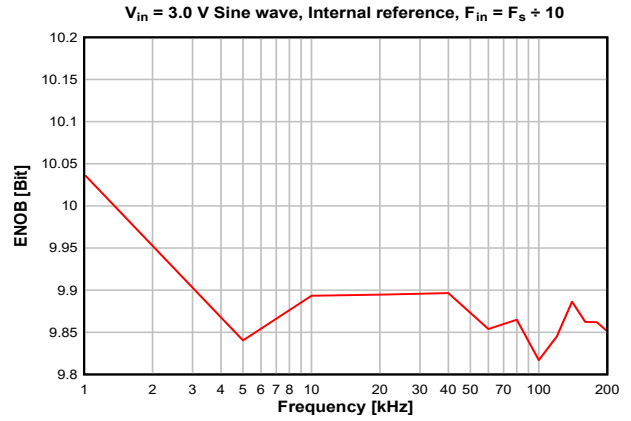


图 8-23. ENOB vs.
Sampling Frequency

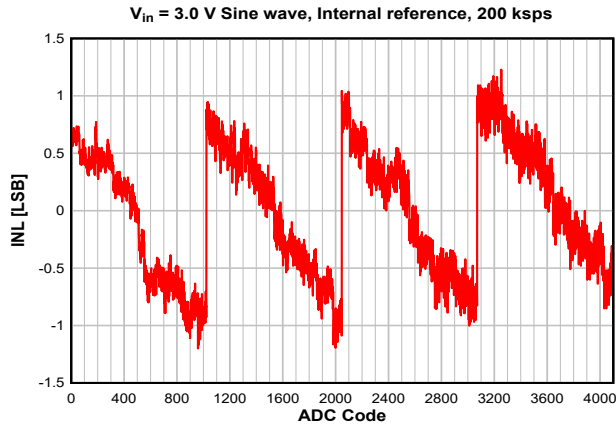


图 8-24. INL vs.
ADC Code

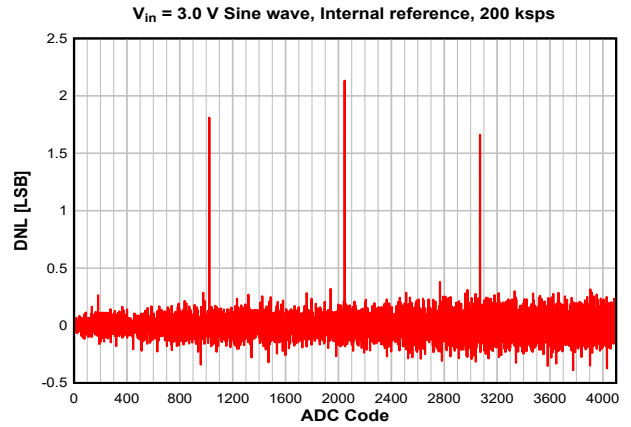


图 8-25. DNL vs.
ADC Code

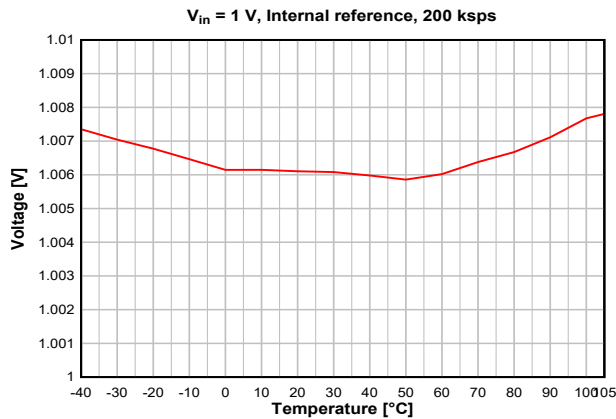


图 8-26. ADC Accuracy vs.
Temperature

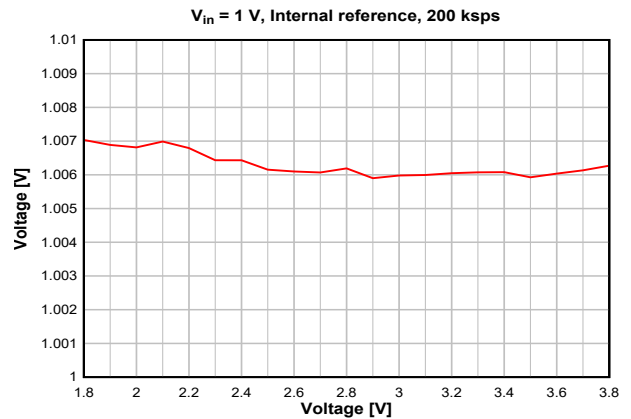


图 8-27. ADC Accuracy vs.
Supply Voltage (VDD)

9 Detailed Description

9.1 Overview

节 4 shows the core modules of the CC1314R10 device.

Throughout this section, see the Technical Reference Manual listed in [Section 11.2](#) for more details.

9.2 System CPU

The CC1314R10 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M33 system CPU with TrustZone®, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv8-M architecture with TrustZone® security extension optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- 8 regions of non-secure memory protected regions
- 8 regions of secure memory protected regions
- 4 regions of Security Attribute Unit (SAU)
- Single-cycle multiply instruction and hardware divide
- Digital-signal-processing (DSP) extension
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Full debug with data matching for watchpoint generation
 - Data Watchpoint and Trace Unit (DWT)
 - JTAG Debug Access Port (DAP)
 - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
 - Instrumentation Trace Macrocell Unit (ITM)
 - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8 kB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation

9.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

备注

Not all combinations of features, frequencies, data rates, and modulation formats described in this chapter are supported. Over time, TI can enable new physical radio formats (PHYs) for the device and provides performance numbers for selected PHYs in the data sheet. Supported radio formats for a specific device, including optimized settings to use with the TI RF driver, are included in the [SmartRF Studio](#) tool with performance numbers of selected formats found in [节 8](#).

9.3.1 Proprietary Radio Formats

The CC1314R10 radio can support a wide range of physical radio formats through a set of hardware peripherals combined with firmware available in the device ROM, covering various customer needs for optimizing towards parameters such as speed or sensitivity. This allows great flexibility in tuning the radio both to work with legacy protocols as well as customizing the behavior for specific application needs.

表 9-1 gives a simplified overview of features of the various radio formats available in ROM. Other radio formats may be available in the form of radio firmware patches or programs through the Software Development Kit (SDK) and may combine features in a different manner, as well as add other features.

表 9-1. Feature Support

Feature	Main 2-(G)FSK Mode	High Data Rates	Low Data Rates	SimpleLink™ Long Range
Programmable preamble, sync word and CRC	Yes	Yes	Yes	No
Programmable receive bandwidth	Yes	Yes	Yes (down to 4 kHz)	Yes
Data / Symbol rate ⁽³⁾	20 to 1000 kbps	≤ 2 Msps	≤ 100 ksps	≤ 20 ksps
Modulation format	2-(G)FSK	2-(G)FSK 4-(G)FSK	2-(G)FSK 4-(G)FSK SUN-O-QPSK	2-(G)FSK
Dual Sync Word	Yes	Yes	No	No
Carrier Sense ⁽¹⁾ ⁽²⁾	Yes	No	No	No
Preamble Detection ⁽²⁾	Yes	Yes	Yes	No
Data Whitening	Yes	Yes	Yes	Yes
Digital RSSI	Yes	Yes	Yes	Yes
CRC filtering	Yes	Yes	Yes	Yes
Direct-sequence spread spectrum (DSSS)	No	No	No	1:2 1:4 1:8
Forward error correction (FEC)	No	No	No	Yes
Link Quality Indicator (LQI)	Yes	Yes	Yes	Yes

- (1) Carrier Sense can be used to implement HW-controlled listen-before-talk (LBT) and Clear Channel Assessment (CCA) for compliance with such requirements in regulatory standards. This is available through the CMD_PROP_CS radio API.
- (2) Carrier Sense and Preamble Detection can be used to implement sniff modes where the radio is duty cycled to save power.
- (3) Data rates are only indicative. Data rates outside this range may also be supported. For some specific combinations of settings, a smaller range might be supported.

9.4 Memory

The up to 1024 kB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the `ccfg.c` source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to eight 32 kB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. Parity can be disabled for an additional 32 kB which can be allocated for general purpose SRAM. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8 kB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4 kB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

9.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still [ensuring ultra-low power](#)
- 2 MHz low-power mode enables lowest possible handling of digital sensors
- Dynamic reuse of hardware resources
- 40-bit accumulator supporting multiplication, addition and shift
- Observability and debugging options

[Sensor Controller Studio](#) is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or I²C (UART and I²C are bit-banged)
- Capacitive sensing
- Waveform generation
- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.
- The ADC is a 12-bit 200 ksps ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs
- Dedicated SPI master with up to 6 MHz clock speed

The peripherals in the Sensor Controller can also be controlled from the main application processor.

9.6 Cryptography

The CC1314R10 device comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit
- **Secure Hash Algorithm 2 (SHA-2)** with support for SHA224, SHA256, SHA384, and SHA512
- **Advanced Encryption Standard (AES)** with 128, 192 and 256 bit key lengths
- **Public Key Accelerator** - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for an application or stack:

- **Key Agreement Schemes**
 - Elliptic Curve Diffie - Hellman with static or ephemeral keys (ECDH and ECDHE)
 - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- **Signature Processing**
 - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
 - Edwards-curve Digital Signature Algorithm (EdDSA)
- **Curve Support**
 - Short Weierstrass form, such as:
 - NIST-P224 (secp224r1), NIST-P256 (secp256r1), NIST-P384 (secp384r1), NIST-P521 (secp521r1)
 - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
 - Montgomery form, such as:
 - Curve25519
 - Twisted Edwards form, such as:
 - Ed25519
- **Message Authentication Codes**
 - AEC CBC-MAC
 - AES CMAC
 - HMAC with SHA224, SHA256, SHA384 and SHA512
- **Block cipher mode of operation**
 - AES CCM and AES CCM-Star
 - AES GCM
 - AES ECB
 - AES CBC
 - AES CTR
- **Hash Algorithm**
 - SHA224
 - SHA256
 - SHA384
 - SHA512
- **True random number generation**

Other capabilities, such as RSA encryption and signatures (using keys as large as 2048 bits) as well as other ECC curves such as Curve1174, can be implemented using the provided public key accelerator but are not part of the TI SimpleLink SDK for the CC1314R10 device.

9.7 Timers

A large selection of timers are available as part of the CC1314R10 device. These timers are:

- **Real-Time Clock (RTC)**

A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF)

This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. The real time clock can also be read by the Sensor Controller Engine to timestamp sensor data and also has dedicated capture channels. By default, the RTC halts when a debugger halts the device.

- **General Purpose Timers (GPTIMER)**

The four flexible GPTIMERS can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERS are available in Active and Idle power modes.

- **Sensor Controller Timers**

The Sensor Controller contains 3 timers:

AUX Timer 0 and 1 are 16-bit timers with a 2^N prescaler. Timers can either increment on a clock or on each edge of a selected tick source. Both one-shot and periodical timer modes are available.

AUX Timer 2 is a 16-bit timer that can operate at 24 MHz, 2 MHz or 32 kHz independent of the Sensor Controller functionality. There are 4 capture or compare channels, which can be operated in one-shot or periodical modes. The timer can be used to generate events for the Sensor Controller Engine or the ADC, as well as for PWM output or waveform generation.

- **Radio Timer**

A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.

- **Watchdog timer**

The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt and reset the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer continues to run in Standby power mode but pauses when a debugger halts the device.

- **Always On Watchdog Timer (AON_WDT)**

The Always On Watchdog Timer is used during standby to regain control when the system has failed due to a software error or failure of an external device to respond in the expected way. It generates a reset when its configured time-out counter reaches zero and cannot be stopped once started, unless by asserting a device reset. The Always-on watchdog timer runs in Standby power mode and may pause when a debugger halts the device.

9.8 Serial Peripherals and I/O

The SPI interface provides a standardized synchronous serial interface to communicate with devices compatible with SPI (3 and 4 wire), MICROWIRE and TI Synchronous Serial Format. The SPIs support master/slave operation up to 12 MHz, programmable clock bit rate with prescaler, as well as configurable phase and polarity.

The UART interface implements universal asynchronous receiver and transmitter functions. The UART supports flexible baud-rate generation up to a maximum of 3 Mbps with FIFO, multiple data sizes, stop and parity bits as well as hardware handshake.

The I²S interface provides a standardized interface to exchange digital audio with devices compatible with this standard, including ADCs, DACs and CODECs. The I²S can also receive pulse-density modulation (PDM) data from devices such as digital microphones and perform conversion to PCM data.

The I²C interface enables low speed serial communications with devices compatible with the I²C standard. The I²C interface can handle both standard (100 kHz) and fast (400 kHz) speeds, as well as four modes of operation: master transmit/receive and slave transmit/receive.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in 节 7. All digital peripherals can be connected to any digital pin on the device.

9.9 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC1314R10 device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

9.10 μ DMA

The device includes a direct memory access (μ DMA) controller. The μ DMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The μ DMA controller can perform a transfer between memory and peripherals. The μ DMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the μ DMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

9.11 Debug

The debug subsystem implements two IEEE standards for debug and test purposes:

IEEE 1149.7 Class 4: Reduced-pin and Enhanced-functionality Test Access Port and Boundary-scan Architecture. This is known by the acronym cJTAG (compact JTAG) and this device uses only two pins to communicate to the target: TMS (JTAG_TMSC) and TCK (JTAG_TCKC). This is the default mode of operation.

IEEE standard 1149.1: Test Access Port and Boundary Scan Architecture Test Access Port (TAP). This standard is known by the acronym JTAG and this device uses four pins to communicate to the target: TMS (JTAG_TMSC), TCK (JTAG_TCKC), TDI (JTAG_TDI) and TDO (JTAG_TDO).

The debug subsystem also implements a user-configurable firewall to control unauthorized access to debug/test ports.

9.12 Power Management

To minimize power consumption, the CC1314R10 supports a number of power modes and power management features (see 表 9-2).

表 9-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
48 MHz high-speed clock (SCLK_HF)	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
2 MHz medium-speed clock (SCLK_MF)	RCOSC_MF	RCOSC_MF	Available	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	Off	Off
Watchdog timer (WDT)	Available	Available	Paused	Off	Off
Always-on Watchdog timer (AON_WDT)	Available	Available	Available	Off	Off

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see 表 9-2).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The [Sensor Controller Studio](#) tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

备注

The power, RF and clock management for the CC1314R10 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC1314R10 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete [SDK](#) with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

9.13 Clock Systems

The CC1314R10 device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or an external 48 MHz crystal (XOSC_HF). Radio operation requires an external 48 MHz crystal.

SCLK_MF is an internal 2 MHz clock that is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK_MF clock is always driven by the internal 2 MHz RC Oscillator (RCOSC_MF).

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

9.14 Network Processor

Depending on the product configuration, the CC1314R10 device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

10 Application, Implementation, and Layout

备注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

For general design guidelines and hardware configuration guidelines, refer to [CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Report](#).

10.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC1314R10 device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

[CC1312-R7EM-XD7793 Design Files](#)

The CC1312-R7EM-XD7793 reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document.

[LP-EM-CC1314R10 Design Files](#)

The CC1314R10 LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC1314R10 device.

[Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag](#)

The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz

The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

10.2 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see [Semiconductor and IC Package Thermal Metrics](#).

There are three recommended ways to derive the junction temperature from other measured temperatures:

1. From package temperature:

$$T_J = \psi_{JT} \times P + T_{\text{case}} \quad (1)$$

2. From board temperature:

$$T_J = \psi_{JB} \times P + T_{\text{board}} \quad (2)$$

3. From ambient temperature:

$$T_J = R_{\theta JA} \times P + T_A \quad (3)$$

P is the power dissipated from the device and can be calculated by multiplying current consumption with supply voltage. Thermal resistance coefficients are found in [节 8.8](#).

For various application use cases current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, etc. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in [Measuring CC13xx and CC26xx current consumption](#).

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

11.1 Tools and Software

The CC1314R10 device is supported by a variety of software and hardware development tools.

Development Kit

CC1314R10 LaunchPad™ Development Kit

The CC1314R10 LaunchPad™ Development Kit enables development of high-performance Sub-1 GHz wireless applications that benefit from low-power operation. The kit features the CC1314R10 Sub-1 GHz SimpleLink Wireless MCU. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more.

LP-XDS110 LaunchPad™ Debug Probe

The LP-XDS110 LaunchPad™ Debug Probe enables development of high-performance wireless applications in the entire family of LP-EM LaunchPad™ development boards. Featuring a seamless connection with the new 20-pin LP-EM Debug connector, it supports not only multiple standards such as JTAG/cJTAG/SWD but also a UART backchannel for maximum debugging flexibility. It also features an Arm® 10-pin Debug connector to perform debugging in any custom board.

LP-XDS110ET LaunchPad™ Debug Probe

The LP-XDS110ET LaunchPad™ Debug Probe enables development of high-performance wireless applications in the entire family of LP-EM LaunchPad™ development boards. Featuring a seamless connection with the new 20-pin LP-EM Debug connector, it supports not only multiple standards such as JTAG/cJTAG/SWD but also a UART backchannel for maximum debugging flexibility. In addition, it also features an Arm® 10-pin Debug connector to perform debugging in any custom board. This Debug Probe also features the XDS110 EnergyTrace™ technology, which is a new method for measuring the current consumption that captures the complete operational profile of the wireless MCU.

TMDSEMU110-U Debug Probe

The TMDSEMU110-U Debug Probe enables development of high-performance wireless applications in the entire family of SimpleLink LaunchPad™ development boards. Featuring a convenient enclosure, which grants the proper mechanical robustness for field and production environments, it supports not only multiple standards such as JTAG/cJTAG/SWD but also a UART backchannel and four GPIOs for maximum debugging flexibility. In addition, the expansion connector allows using the [TMDSEMU110-ETH](#) add-on (sold separately), which adds the full featured XDS110 EnergyTrace™ technology with variable supply voltage from 1.8V to 3.6V and up to 800 mA of supply current. The XDS110 EnergyTrace™ technology is a new method for measuring the current consumption that captures the complete operational profile of the wireless MCU.

Software

SimpleLink™ LOWPOWER F2 SDK

The SimpleLink LOWPOWER F2 Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13XX / CC26XX family of devices. The SDK includes a comprehensive software package for the CC1314R10 device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.3
- Thread (based on OpenThread)
- TI Z-Stack (Zigbee 3.0)

- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz
- EasyLink - a large set of building blocks for building proprietary RF software stacks
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)
- TI Wi-SUN FAN Stack
- Matter

The SimpleLink LOWPOWER F2 SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit ti.com/simplelink.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 kB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

Sensor Controller Studio

Sensor Controller Studio is used to write, test and debug code for the Sensor Controller peripheral. The tool generates a Sensor Controller Interface driver, which is a set of C source files that are compiled into the System CPU application. These source files also contain the Sensor Controller binary image and allow the System CPU application to control and exchange data with the Sensor Controller. Features of the Sensor Controller Studio include:

- Ready-to-use examples for several common use cases
- Full toolchain with built-in compiler and assembler for programming in a C-like programming language
- Provides rapid development by using the integrated sensor controller task testing and debugging functionality, including visualization of sensor data and verification of algorithms

UniFlash

UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. UniFlash is available free of charge.

11.1.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

11.2 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC1314R10. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer

Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC1314R10 Silicon Errata

The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC1314R10 device are found on the device product folder at: ti.com/product/CC1314R10/technicaldocuments.

Technical Reference Manual (TRM)

CC13x4, CC26x4 SimpleLink™ Wireless MCU Technical Reference Manual

The TRM provides a detailed description of all modules and peripherals available in the device family.

11.3 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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J-Link™ is a trademark of SEGGER Microcontroller Systeme GmbH.

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mioty® is a registered trademark of Fraunhofer-Gesellschaft.

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is a registered trademark of Arm Limited.

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IAR Embedded Workbench® is a registered trademark of IAR Systems AB.

Windows® is a registered trademark of Microsoft Corporation.

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11.5 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

12.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

备注

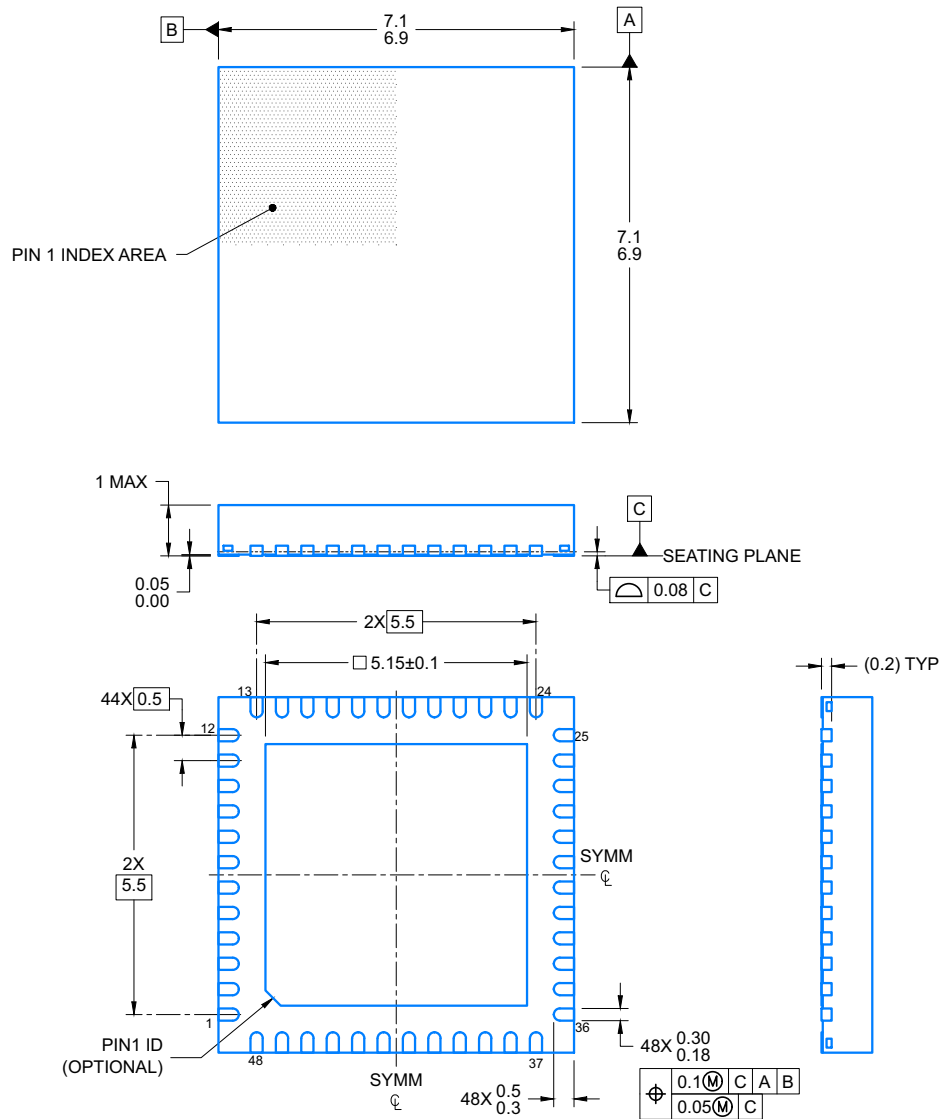
The RSK (S-PQVFN-N64) package drawings in this datasheet are preliminary and will change for the production release of this IC. The change will be related to the exposed thermal pad size of the IC. The current sample has a 3.7 mm x 3.7 mm thermal ground pad. Production devices will have a 4.7 mm x 4.7mm thermal ground pad. It is recommended to design the thermal ground pad to be 4.7 mm x 4.7 mm, with a stencil opening of 3.7 mm x 3.7mm for pre-production devices. For production devices, only the stencil will need to change to 4.7 mm x 4.7 mm. No change to the PCB will be required.

RGZ0048A

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



4219044/A 05/2018

NOTES:

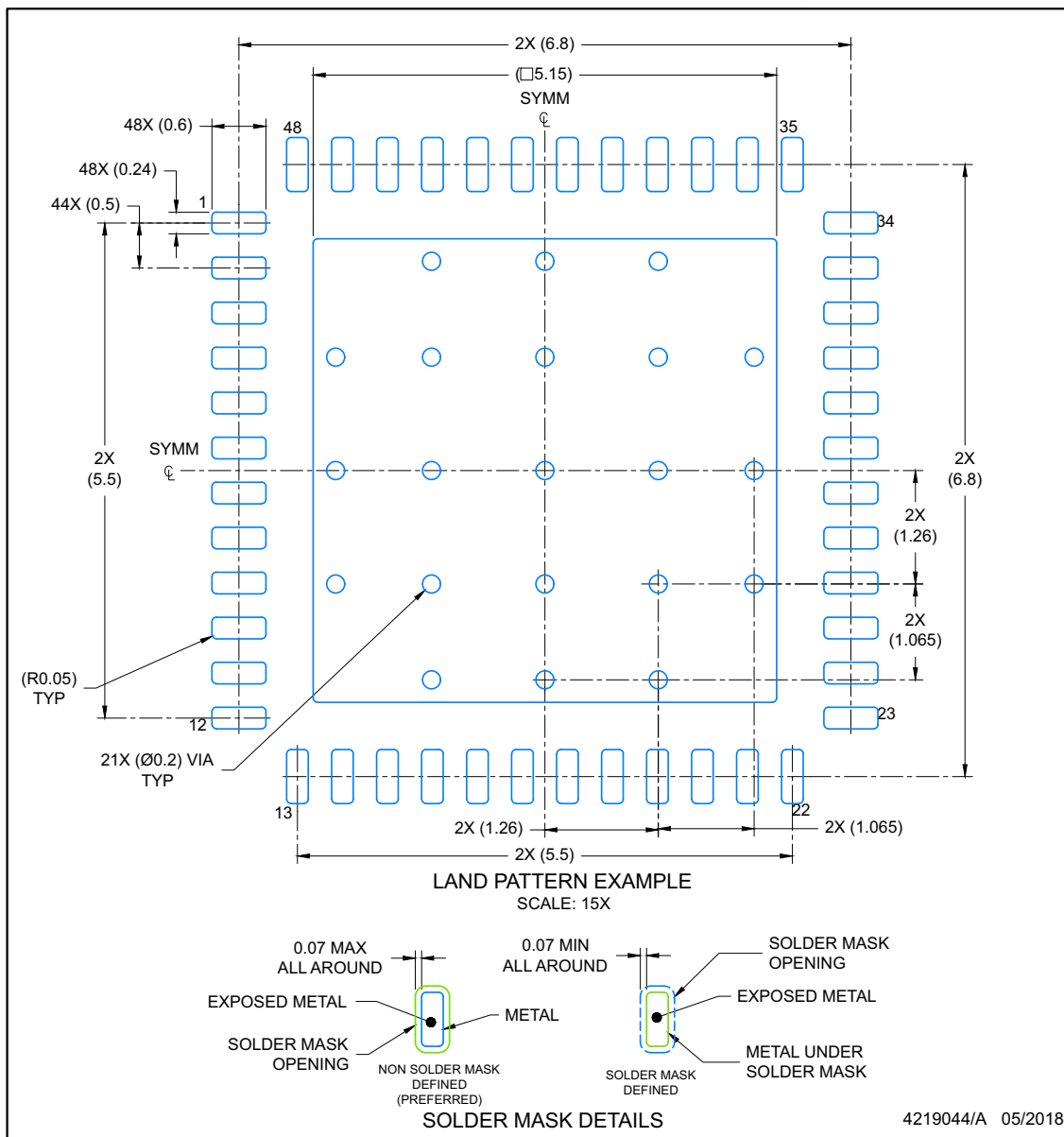
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VQFN - 1 mm max height

RGZ0048A

PLASTIC QUADFLAT PACK- NO LEAD

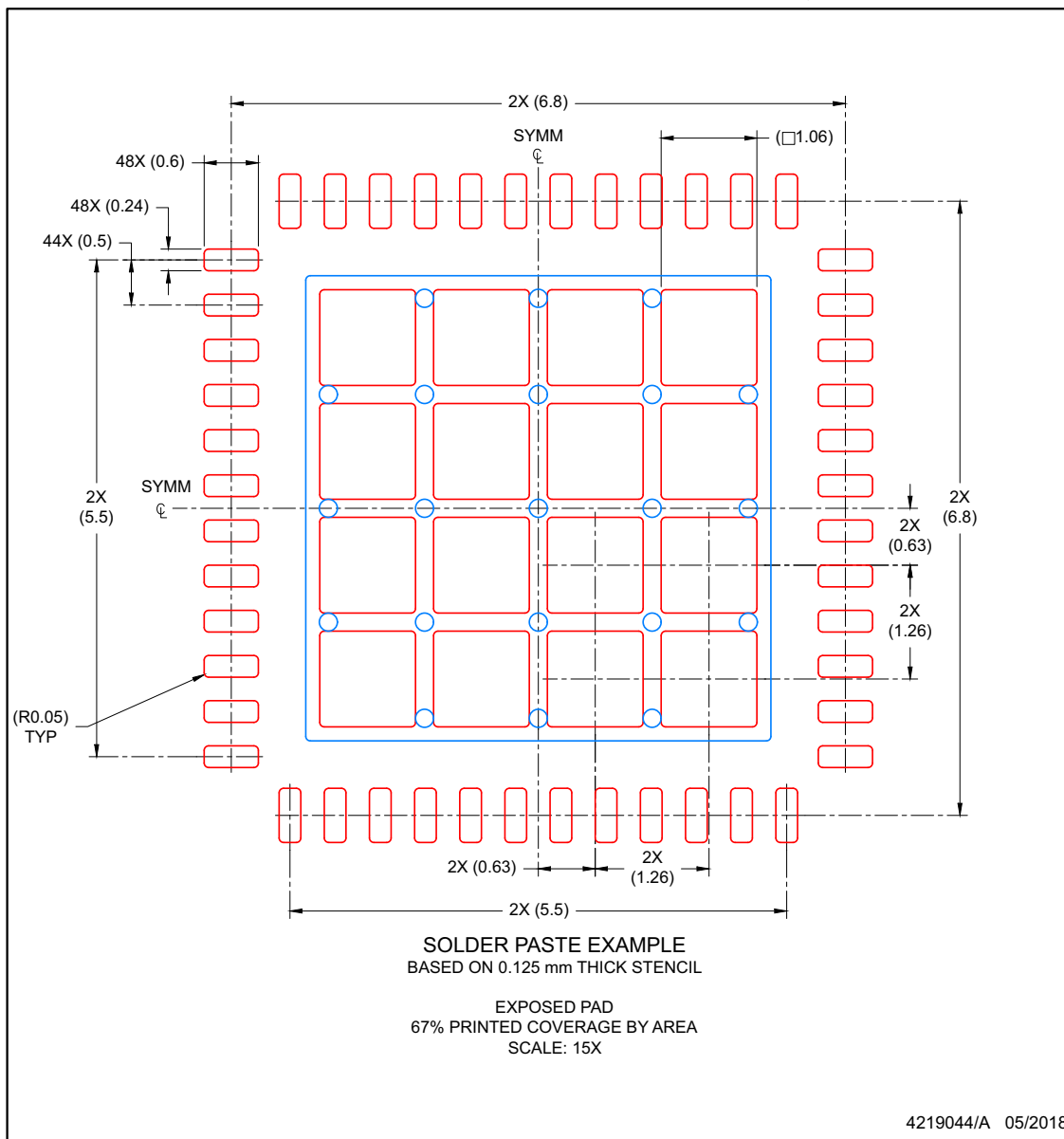


NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN**RGZ0048A****VQFN - 1 mm max height**

PLASTIC QUADFLAT PACK- NO LEAD



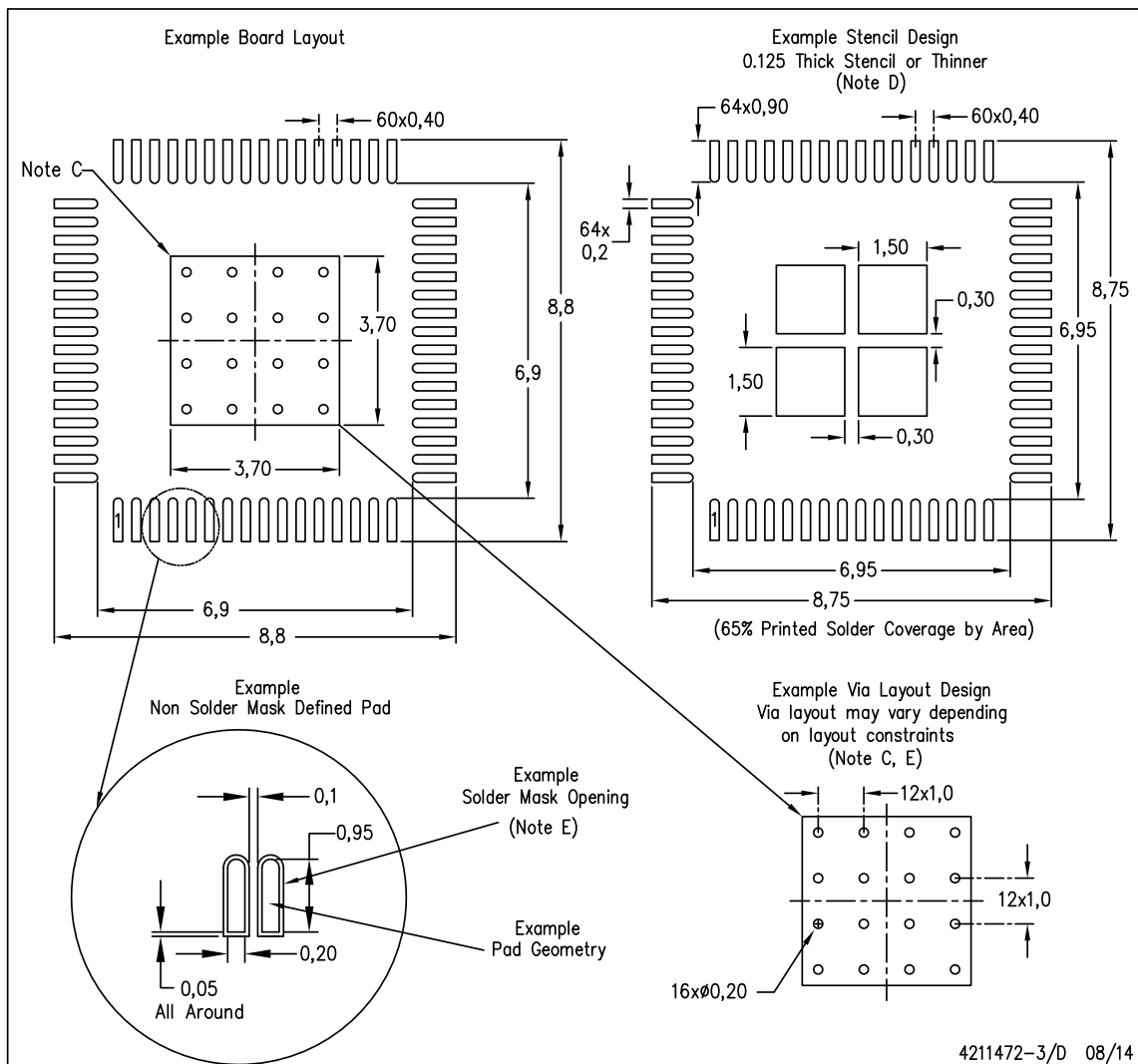
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

LAND PATTERN DATA

RSK (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD

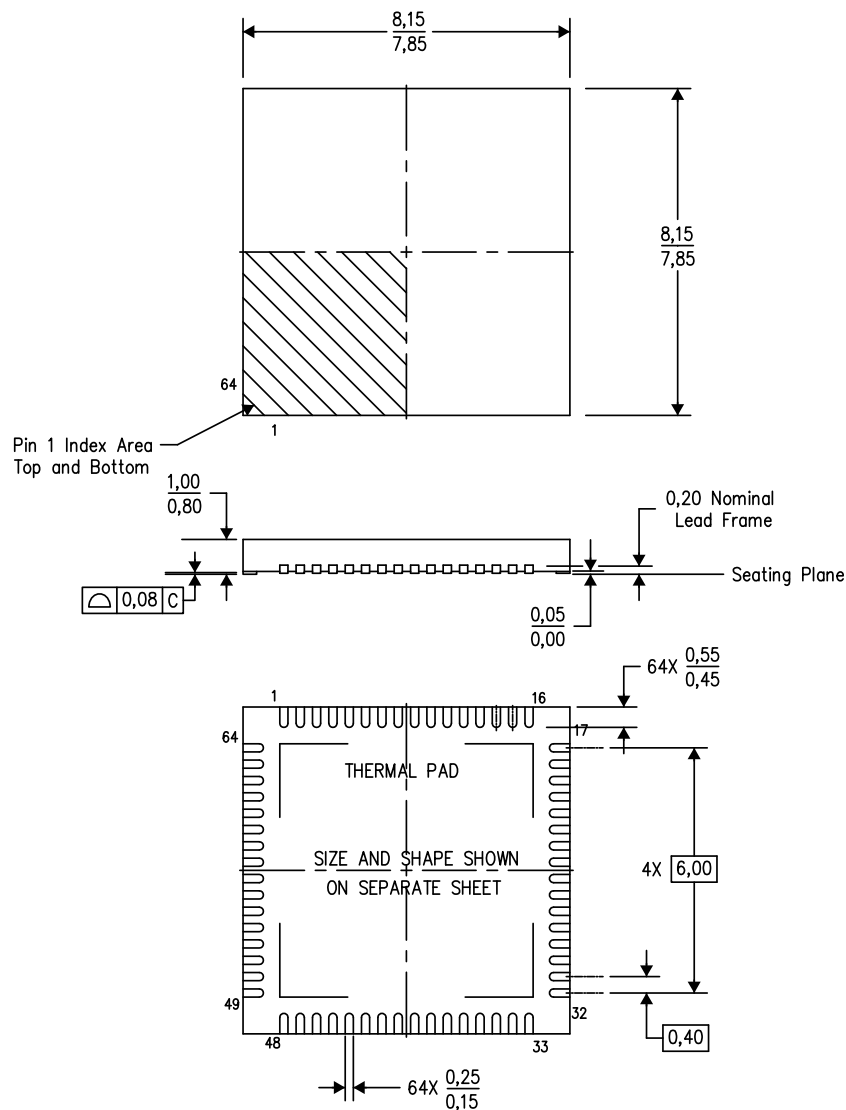


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

MECHANICAL DATA

RSK (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



4207547/C 04/12

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RSK (S-PVQFN-N64)

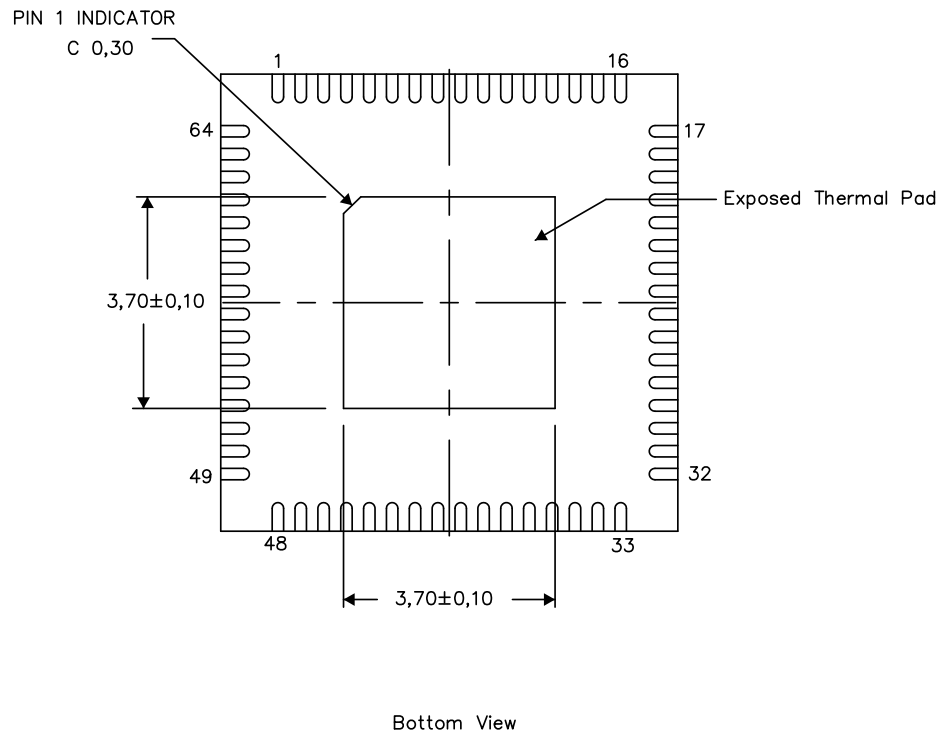
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4208001-3/H 08/14

NOTE: A. All linear dimensions are in millimeters

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XCC1314R106T0RGZ	ACTIVE	VQFN	RGZ	48	260	TBD	Call TI	Call TI	-40 to 105		Samples
XCC1314R106T0RSK	ACTIVE	VQFN	RSK	64	4000	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

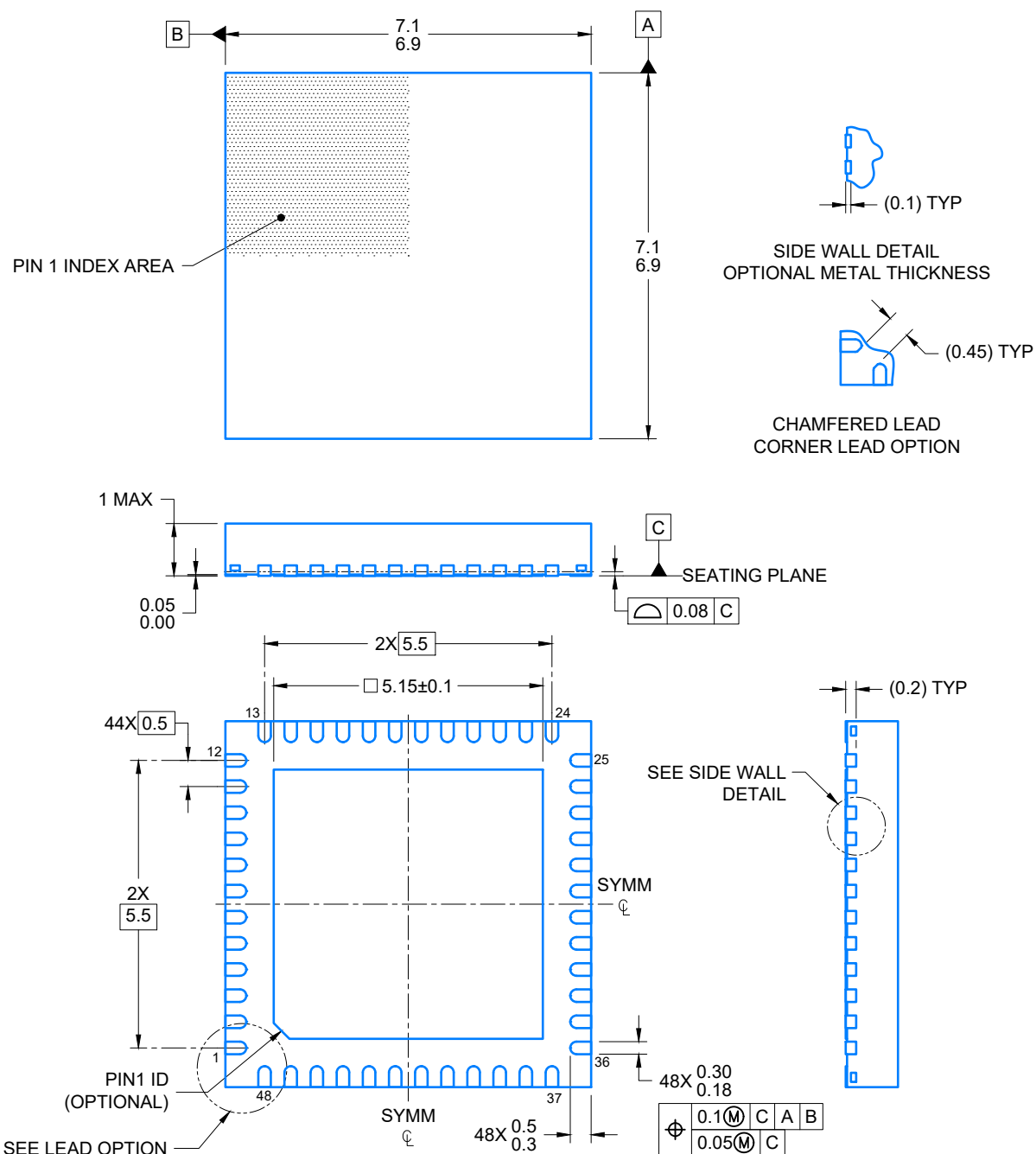
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

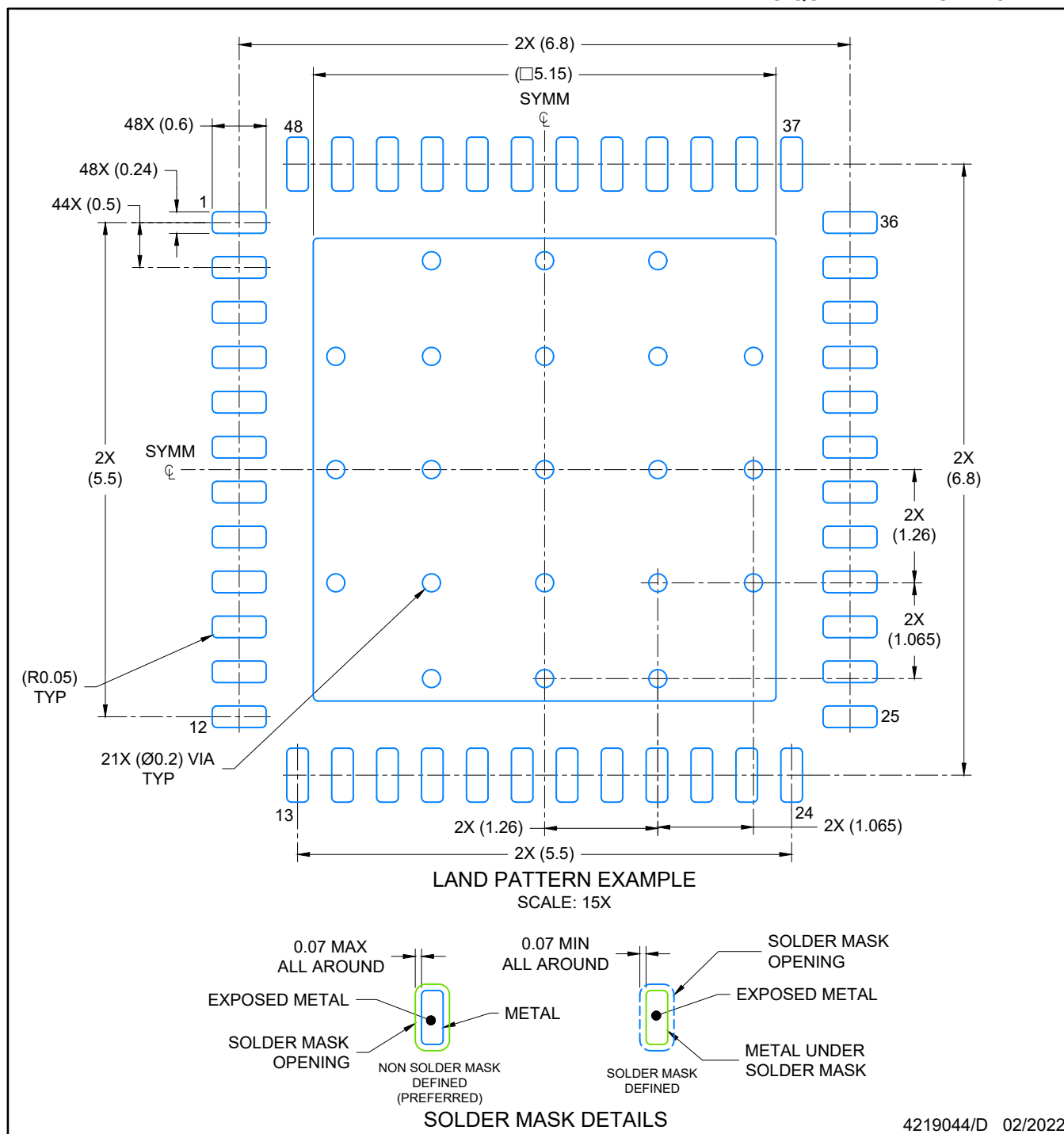
4224671/A



4219044/D 02/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



4219044/D 02/2022

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

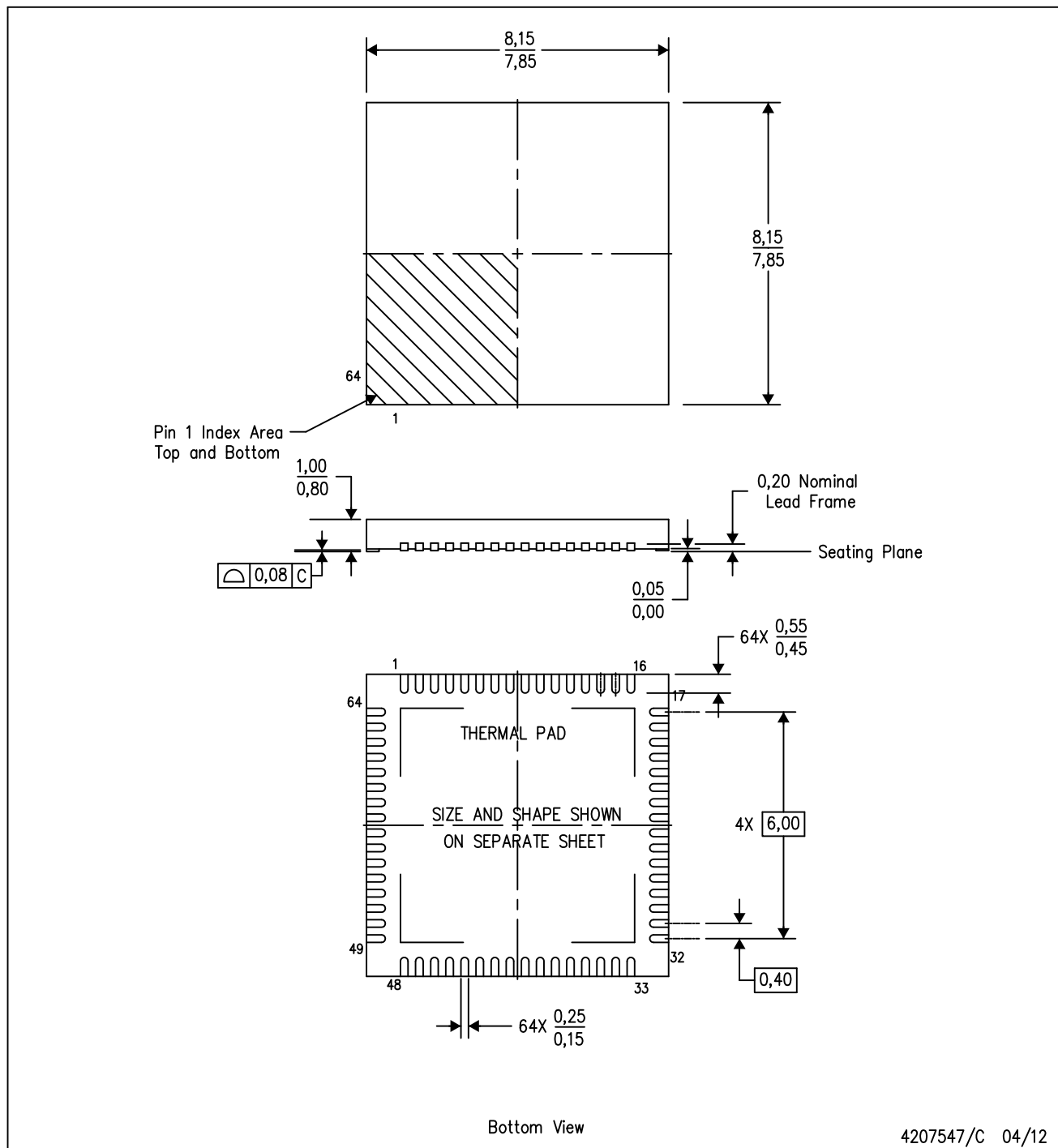


NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RSK (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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