



CC1201 低功率、高性能射频 (RF) 收发器

1 器件概述

1.1 特性

- RF 性能和模拟特性：
 - 高性能、单芯片收发器
 - 出色的接收器灵敏度：
 - 1.2kbps 时为 -120dBm
 - 50kbps 时为 -109dBm
 - 阻断性能：10MHz 时为 85dB
 - 邻道选择性：50kHz 偏移时高达 62dB
 - 极低相位噪声：10kHz 偏移 (169 MHz) 时为 -114dBc/Hz
 - 步长为 0.4dB，高达 +16dBm 的可编程输出功率
 - 自动输出功率斜升
 - 所支持的调制格式：
 - 2 - 频移键控 (FSK)，2 - 高斯频移监控 (GFSK)，4-FSK，4-GFSK，最小频移键控 (MSK)，开关键控 (OOK)
 - 发送和接收时支持高达 1.25Mbps 的数据速率
- 低功耗：
 - 针对自动低功率接收轮询的增强型无线电唤醒 (eWOR) 功能
 - 断电：0.12μA (eWOR 定时器激活时为 0.5μA)
 - RX：在 RX 嗅探模式中为 0.5mA
 - RX：在低功耗模式中，峰值电流为 19mA
 - RX：在高性能模式中，峰值电流为 23mA
 - TX：+14dBm 时为 46mA
- 其他：
 - 数据先入先出 (FIFO)：独立的 128 字节 RX 和 TX
 - 支持与 CC1190 器件无缝集成以实现范围扩展，从而使 RX 灵敏度提升 3dB 并且实现高达 +27dBm 的 TX 输出功率
- 数字特性：
 - 波形监视：针对改进的同步检测性能的高级数字信号处理
 - 自主图像删除
 - 安全性：硬件 AES128 加速器
 - 数据先入先出 (FIFO)：独立的 128 字节 RX 和 TX
 - 包括针对天线多样性支持的功能
 - 支持重传
 - 支持接收到的数据包自动确认
 - 针对载波监听 (LBT) 系统的自动空闲信道评估 (CCA)
 - 增加范围和提高稳定耐用性的内置编码增益支持
 - 数字接收信号强度指示 (RSSI) 测量
 - 用于实现更少占用带宽的经改进 OOK 整形，从而在满足规定要求的同时实现更高的输出功率
 - 针对 802.15.4g 的专用数据包处理：
 - 循环冗余校验 (CRC) 16/32
 - 前向纠错 (FEC)，双同步检测 (FEC 和无 FEC 数据包)
 - 数据白化
 - 总体说明：
 - 符合 RoHS 标准的 5mm × 5mm 无脚四方扁平无引线 (QFN) 32 引脚封装 (RHB)
 - 与 CC1120 器件引脚兼容
 - 法规 - 适用于符合下列标准的系统：
 - 欧洲：ETSI EN 300 220
 - 美国：FCC CFR47 第 15 部分
 - 日本：ARIB STD-T108

1.2 应用

- 数据速率高达 1250kbps 的低功耗高性能无线系统
- ISM/SRD 频带：169、433、868、915 和 920MHz
- 有可能支持额外的频率频带：137 至 158.3MHz，205 至 237.5MHz，以及 274 至 316.6MHz
- 智能仪表计量 (自动计量读取 (AMR) / 自动计量基础设施 (AMI))
- 家庭和楼宇自动化
- 无线警报和安全系统
- 工业用监控和控制
- 无线医疗应用
- 无线传感器网络和有源射频识别 (RFID)
- IEEE 802.15.4g 应用

1.3 说明

CC1201 是一款全集成单芯片射频收发器，此器件设计用于在成本有效无线系统中实现极低功耗和低压运行的高性能。所有滤波器都已集成，因此无需昂贵的外部 SAW 和 IF 滤波器。该器件主要用于 ISM（工业、科学和医疗）以及处于 164 - 190MHz，410 - 475MHz 和 820 - 950MHz 的 SRD（短程设备）频带。



CC1201 器件提供大量硬件，以支持数据包处理、数据缓冲、突发传输、空闲信道评估、链路质量指示和无线唤醒。CC1201 器件的主要运行参数可由 SPI 接口控制。在典型系统中，CC1201 器件将与微控制器和极少的外部无源组件搭配使用。

对于 50kHz 或更高的信道滤波带宽，CC1201 提供与 CC1200 同样的性能，因此为无需窄带支持的应用提供一个更低成本选择。

器件信息⁽¹⁾

部件号	封装	封装尺寸
CC1201RHB	超薄四方扁平无引线 (VQFN) (32)	5.00mm x 5.00mm

(1) 更多信息请参见 节 8，机械封装和可订购产品信息

1.4 功能方框图

图 1-1 显示 CC120x 系列器件的系统方框图。

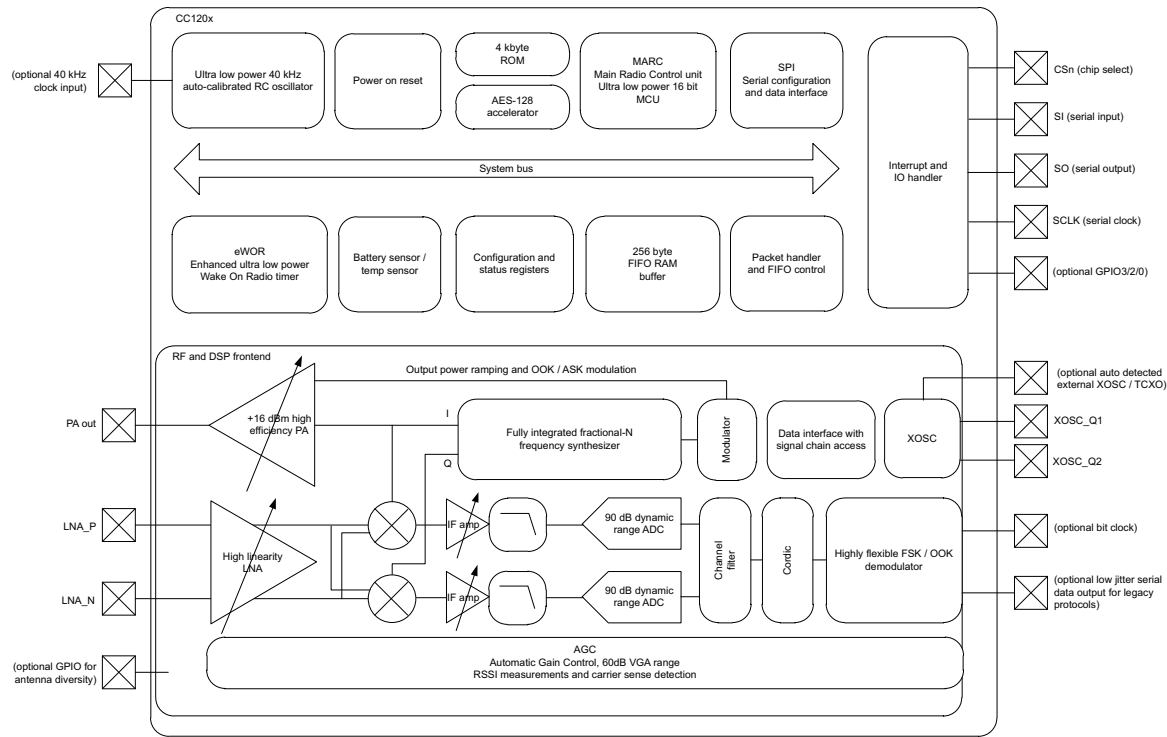


图 1-1. 系统方框图

内容

1	器件概述	1			
1.1	特性	1		4.15	40-MHz Clock Input (TCXO) 16
1.2	应用	1		4.16	32-kHz Clock Input..... 17
1.3	说明	1		4.17	40-kHz RC Oscillator..... 17
1.4	功能方框图.....	2		4.18	I/O and Reset 17
2	修订历史记录.....	4		4.19	Temperature Sensor 17
3	Terminal Configuration and Functions.....	5		4.20	Typical Characteristics 18
3.1	Pin Diagram	5		5	Detailed Description
3.2	Pin Configuration	6		5.1	Block Diagram..... 21
4	Specifications	7		5.2	Frequency Synthesizer..... 21
4.1	Absolute Maximum Ratings	7		5.3	Receiver 22
4.2	Handling Ratings	7		5.4	Transmitter 22
4.3	Recommended Operating Conditions (General Characteristics)	7		5.5	Radio Control and User Interface 22
4.4	Thermal Resistance Characteristics for RHB Package	7		5.6	Enhanced Wake-On-Radio (eWOR) 22
4.5	RF Characteristics.....	8		5.7	RX Sniff Mode..... 23
4.6	Regulatory Standards	8		5.8	Antenna Diversity 23
4.7	Current Consumption, Static Modes	9		5.9	WaveMatch..... 24
4.8	Current Consumption, Transmit Modes	9		6	Typical Application Circuit
4.9	Current Consumption, Receive Modes.....	10		7	器件和文档支持
4.10	Receive Parameters.....	11		7.1	器件支持..... 26
4.11	Transmit Parameters.....	14		7.2	文档支持..... 27
4.12	PLL Parameters	15		7.3	社区资源..... 27
4.13	Wake-up and Timing	16		7.4	商标..... 27
4.14	40-MHz Crystal Oscillator	16		7.5	静电放电警告
				7.6	术语表
				8	机械封装和可订购信息
					28

2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

本数据手册修订历史记录强调了使 SWRS154A 器件专用数据手册变为 SWRS154B 修订版本所做的更改。

Changes from Revision A (June 2014) to Revision B	Page
• Added Ambient to the temperature range condition and removed Tj from Temperature range	7
• Added data to TCXO table	16

3 Terminal Configuration and Functions

3.1 Pin Diagram

Figure 3-1 shows pin names and locations for the CC1201 device.

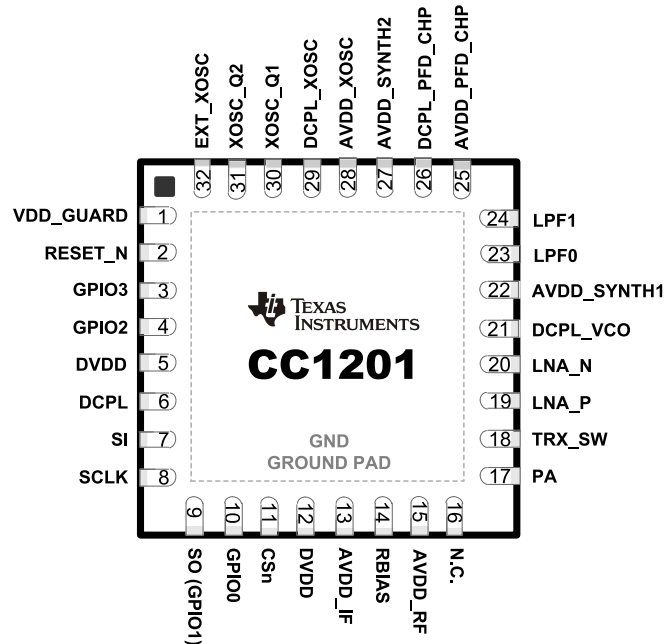


Figure 3-1. Package 5-mm × 5-mm QFN

3.2 Pin Configuration

The following table lists the pin-out configuration for the CC1201 device.

PIN NO.	PIN NAME	TYPE / DIRECTION	DESCRIPTION
1	VDD_GUARD	Power	2.0–3.6 V VDD
2	RESET_N	Digital input	Asynchronous, active-low digital reset
3	GPIO3	Digital I/O	General-purpose I/O
4	GPIO2	Digital I/O	General-purpose I/O
5	DVDD	Power	2.0–3.6 VDD to internal digital regulator
6	DCPL	Power	Digital regulator output to external decoupling capacitor
7	SI	Digital input	Serial data in
8	SCLK	Digital input	Serial data clock
9	SO(GPIO1)	Digital I/O	Serial data out (general-purpose I/O)
10	GPIO0	Digital I/O	General-purpose I/O
11	CSn	Digital input	Active-low chip select
12	DVDD	Power	2.0–3.6 V VDD
13	AVDD_IF	Power	2.0–3.6 V VDD
14	RBIAS	Analog	External high-precision resistor
15	AVDD_RF	Power	2.0–3.6 V VDD
16	N.C.		Not connected
17	PA	Analog	Single-ended TX output (requires DC path to VDD)
18	TRX_SW	Analog	TX and RX switch. Connected internally to GND in TX and floating (high-impedance) in RX.
19	LNA_P	Analog	Differential RX input (requires DC path to ground)
20	LNA_N	Analog	Differential RX input (requires DC path to ground)
21	DCPL_VCO	Power	Pin for external decoupling of VCO supply regulator
22	AVDD_SYNTH1	Power	2.0–3.6 V VDD
23	LPF0	Analog	External loopfilter components
24	LPF1	Analog	External loopfilter components
25	AVDD_PFD_CHP	Power	2.0–3.6 V VDD
26	DCPL_PFD_CHP	Power	Pin for external decoupling of PFD and CHP regulator
27	AVDD_SYNTH2	Power	2.0–3.6 V VDD
28	AVDD_XOSC	Power	2.0–3.6 V VDD
29	DCPL_XOSC	Power	Pin for external decoupling of XOSC supply regulator
30	XOSC_Q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to EXT_XOSC is used)
31	XOSC_Q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to EXT_XOSC is used)
32	EXT_XOSC	Digital input	Pin for external clock input (must be grounded if a regular crystal connected to XOSC_Q1 and XOSC_Q2 is used)
–	GND	Ground pad	The ground pad must be connected to a solid ground plane.

4 Specifications

All measurements performed on CC1200EM_868_930 rev.1.0.0, CC1200EM_420_470 rev.1.0.1, or CC1200EM_169 rev.1.2.

4.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT	CONDITION
Supply voltage (VDD, AVDD_x)	−0.3	3.9	V	All supply pins must have the same voltage
Input RF level		+10	dBm	
Voltage on any digital pin	−0.3	VDD+0.3	V	max 3.9 V
Voltage on any analog Pin (including DCPL pins)	−0.3	2.0	V	

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS}, unless otherwise noted.

4.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	−40	125	°C
V _{ESD}	Electrostatic discharge (ESD) performance:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 ⁽¹⁾		kV
		Charged device model (CDM), per JESD22-C101 ⁽²⁾		V
			All pins	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions (General Characteristics)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Voltage supply range	2.0		3.6	V	All supply pins must have the same voltage
Voltage on digital inputs	0		VDD	V	
Temperature range	−40		85	°C	Ambient

4.4 Thermal Resistance Characteristics for RHB Package

	°C/W ⁽¹⁾	AIR FLOW (m/s) ⁽²⁾
R θ_{JC} Junction-to-case (top)	21.1	0.00
R θ_{JB} Junction-to-board	5.3	0.00
R θ_{JA} Junction-to-free air	31.3	0.00
Ps i_{JT} Junction-to-package top	0.2	0.00
Ps i_{JB} Junction-to-board	5.3	0.00
R θ_{JC} Junction-to-case (bottom)	0.8	0.00

- (1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
 - JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
 - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
Power dissipation of 40 mW and an ambient temperature of 25°C is assumed.
- (2) m/s = meters per second

4.5 RF Characteristics

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Frequency bands	820		950	MHz	Contact TI for more information about the use of these frequency bands.
	410		475	MHz	
	164		190	MHz	
	(274)		(316.6)	MHz	
	(205)		(237.5)	MHz	
	(137)		(158.3)	MHz	
Frequency resolution		30		Hz	In 820–950 MHz band
		15		Hz	In 410–475 MHz band
		6		Hz	In 164–190 MHz band
Data rate	0		1250	kbps	Packet mode
	0		625	kbps	Transparent mode

4.6 Regulatory Standards

PERFORMANCE MODE	FREQUENCY BAND	SUITABLE FOR COMPLIANCE WITH	COMMENTS
High-performance mode	820–950 MHz	ARIB STD-T108 ETSI EN 300 220 receiver categories 2 and 3 FCC PART 15.247 FCC PART 15.249	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender such as the CC1190
	410–475 MHz	ETSI EN 300 220 receiver categories 2 and 3	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
	164–190 MHz	ETSI EN 300 220	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
Low-power mode	820–950 MHz	ETSI EN 300 220 receiver categories 2 and 3 FCC PART 15.247 FCC PART 15.249	
	410–475 MHz	ETSI EN 300 220 receiver categories 2 and 3	
	164–190 MHz	ETSI EN 300 220	

4.7 Current Consumption, Static Modes

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Power down with retention		0.12	1	μA	
		0.5		μA	Low-power RC oscillator running
XOFF mode		180		μA	Crystal oscillator / TCXO disabled
IDLE mode		1.5		mA	Clock running, system waiting with no radio activity

4.8 Current Consumption, Transmit Modes

4.8.1 868-, 915-, and 920-MHz Bands (High-Performance Mode)

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +14 dBm		46		mA	
TX current consumption +10 dBm		36		mA	

4.8.2 433-MHz Band (High-Performance Mode)

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +15 dBm		49		mA	
TX current consumption +14 dBm		46		mA	
TX current consumption +10 dBm		35		mA	

4.8.3 169-MHz Band (High Performance Mode)

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +15 dBm		54		mA	
TX current consumption +14 dBm		50		mA	
TX current consumption +10 dBm		39		mA	

4.8.4 Low-Power Mode

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, $f_c = 869.5\text{ MHz}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX Current Consumption +10 dBm		33.6		mA	

4.9 Current Consumption, Receive Modes

4.9.1 High-Performance Mode

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, $f_c = 869.5\text{ MHz}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
RX wait for sync					
1.2 kbps, 4-byte preamble		0.5		mA	
38.4 kbps, 12-byte preamble		3.5		mA	
50 kbps, 24-byte preamble		2.1		mA	
RX peak current					
1.2 kbps		23.6		mA	Peak current consumption during packet reception
Average current consumption Check for data packet every 1 second using eWOR		8		μA	50 kbps, 5-byte preamble, 40-kHz RC oscillator used as eWOR timer

(1) See the sniff mode design note for more information ([SWRA428](#))

4.9.2 Low-Power Mode

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, $f_c = 869.5\text{ MHz}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
RX Peak current low-power RX mode					
50 kbps		19		mA	Peak current consumption during packet reception at the sensitivity limit

4.10 Receive Parameters

All RX measurements made at the antenna connector, to a bit error rate (BER) limit of 1%. Selectivity and blocking is measured with the desired signal 3 dB above the sensitivity level.

4.10.1 General Receive Parameters (High-Performance Mode)

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, $f_c = 869.5\text{ MHz}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Saturation		+10		dBm	
Digital channel filter programmable bandwidth	50		1600	kHz	
IIP3		–14		dBm	At maximum gain
Data rate offset tolerance		± 14 ± 1600		% ppm	With carrier sense detection enabled With carrier sense detection disabled
Spurious emissions 1–13 GHz (VCO leakage at 3.5 GHz)		< –56		dBm	Radiated emissions measured according to ETSI EN 300 220, $f_c = 869.5\text{ MHz}$
30 MHz to 1 GHz		< –57		dBm	
Optimum source impedance 868-, 915-, and 920-MHz bands	$60 + j60 / 30 + j30$			Ω	(Differential or Single-Ended RX Configurations)
433-MHz band	$100 + j60 / 50 + j30$			Ω	
169-MHz band	$140 + j40 / 70 + j20$			Ω	

4.10.2 RX Performance in 868-, 915-, and 920-MHz Bands (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Sensitivity		–119		dBm	1.2 kbps 2-FSK, DEV=20 kHz CHF=50 kHz ⁽¹⁾
		–113		dBm	4.8 kbps OOK CHF=128 kHz ⁽¹⁾
		–108		dBm	32.768 kbps 2-GFSK, DEV=50 kHz CHF=208 kHz ⁽¹⁾
		–110		dBm	38.4 kbps 2-GFSK, DEV=20 kHz CHF=104 kHz ⁽¹⁾
		–109		dBm	50 kbps 2-GFSK, DEV=25 kHz, CHF=104 kHz ⁽¹⁾
		–97		dBm	500 kbps 2-GMSK, CHF=833 kHz ⁽¹⁾
		–97		dBm	1 Mbps 4-GFSK, DEV=400 kHz, CHF=1.66 MHz ⁽¹⁾
Blocking and selectivity 1.2-kbps 2-FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter		50		dB	± 50 kHz (adjacent channel)
		50		dB	± 100 kHz (alternate channel)
		75		dB	± 2 MHz
		80		dB	± 10 MHz
Blocking and selectivity 32.768-kbps 2-GFSK, 200-kHz channel separation, 50-kHz deviation, 208-kHz channel filter		38		dB	± 200 kHz
		46		dB	± 400 kHz
		66		dB	± 2 MHz
		70		dB	± 10 MHz
Blocking and selectivity 38.4-kbps 2-GFSK, 100-kHz channel separation, 20-kHz deviation, 104-kHz channel filter		44		dB	+ 100 kHz (adjacent channel)
		44		dB	± 200 kHz (alternate channel)
		64		dB	± 2 MHz
		72		dB	± 10 MHz
Blocking and selectivity 50-kbps 2-GFSK, 200-kHz channel separation, 25-kHz deviation, 104-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)		41		dB	± 200 kHz (adjacent channel)
		46		dB	± 400 kHz (alternate channel)
		65		dB	± 2 MHz
		71		dB	± 10 MHz
Blocking and selectivity 100-kbps 2-GFSK, 50-kHz deviation, 208-kHz channel filter		45		dB	± 400 kHz (adjacent channel)
		54		dB	± 800 kHz (alternate channel)
		63		dB	± 2 MHz
		68		dB	± 10 MHz
Blocking and selectivity 500-kbps GMSK, 833-kHz channel filter		42		dB	+ 1 MHz (adjacent channel)
		42		dB	± 2 MHz (alternate channel)
		57		dB	± 10 MHz
Blocking and selectivity 1-Mbps 4-GFSK, 400-kHz deviation, 1.6-MHz channel filter		46		dB	± 2 MHz (adjacent channel)
		52		dB	± 4 MHz (alternate channel)
		59		dB	± 10 MHz

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

4.10.3 RX Performance in 433-MHz Band (High-Performance Mode)

 $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Sensitivity		–120		dBm	1.2 kbps 2-FSK, DEV=20 kHz CHF=50 kHz ⁽¹⁾
		–111		dBm	38.4 kbps 2-GFSK, DEV=20 kHz CHF=104 kHz ⁽¹⁾
Blocking and selectivity 1.2-kbps 2-FSK, 50-kHz channel separation, 20-kHz deviation, 50-kHz channel filter		56		dB	± 50 kHz (adjacent channel)
		56		dB	± 100 kHz (alternate channel)
		79		dB	± 2 MHz
		84		dB	± 10 MHz
Blocking and selectivity 38.4-kbps 2-GFSK, 100-kHz channel separation, 20-kHz deviation, 104-kHz channel filter		49		dB	+ 100 kHz (adjacent channel)
		48		dB	± 200 kHz (alternate channel)
		66		dB	± 2 MHz
		74		dB	± 10 MHz

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

4.10.4 RX Performance in 169-MHz Band (High-Performance Mode)

 $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Sensitivity		–119		dBm	1.2 kbps 2-FSK, DEV=20 kHz CHF=50 kHz ⁽¹⁾
Blocking and Selectivity 1.2 kbps 2-FSK, 50 kHz channel separation, 20 kHz deviation, 50 kHz channel filter		62		dB	± 50 kHz (adjacent channel)
		62		dB	± 100 kHz (alternate channel)
		81		dB	± 2 MHz
		85		dB	± 10 MHz
Image rejection (Image compensation enabled)		67		dB	1.2 kbps, DEV=20 kHz, CHF=50 kHz, image at –417 kHz ⁽¹⁾

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

4.10.5 RX Performance in Low-Power Mode

 $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, $f_c = 869.5\text{ MHz}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Sensitivity		–96		dBm	50 kbps 2-GFSK, DEV=25 kHz, CHF=119 kHz ⁽¹⁾
Blocking and selectivity 50 kbps 2-GFSK, 200-kHz channel separation, 25-kHz deviation, 104-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)		41		dB	+ 200 kHz (adjacent channel)
		45		dB	+ 400 kHz (alternate channel)
		62		dB	± 2 MHz
		60		dB	± 10 MHz
Saturation		10		dBm	

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

4.11 Transmit Parameters

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, $f_c = 869.5\text{ MHz}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Max output power		+14		dBm	At 915/920 MHz
		+15		dBm	At 915/920 MHz with $V_{DD} = 3.6\text{ V}$
		+15		dBm	At 868 MHz
		+16		dBm	At 868 MHz with $V_{DD} = 3.6\text{ V}$
		+15		dBm	At 433 MHz
		+16		dBm	At 433 MHz with $V_{DD} = 3.6\text{ V}$
Min output power		–12		dBm	Within fine step size range
		–38		dBm	Within coarse step size range
Output power step size		0.4		dB	Within fine step size range
Adjacent channel power		–60		dBc	4-GFSK 9.6 kbps in 12.5 kHz channel, measured in 8.75 kHz bandwidth (ETSI 300 220 compliant)
Spurious emissions (Excluding harmonics)					Transmission at +14 dBm Suitable for systems targeting compliance with ETSI EN 300-220, FCC part 15, ARIB STD-T108 Measured in 1 MHz bandwidth
30 MHz–1 GHz		< –57		dBm	
1–12.75 GHz		< –50		dBm	
Harmonics					Transmission at +14 dBm (or maximum allowed in applicable band where this is less than +14 dBm) using TI reference design Suitable for systems targeting compliance with ETSI EN 300-220, FCC part 15, ARIB STD-T108
Second Harm, 169 MHz (ETSI)		–43		dBm	
Third Harm, 169 MHz (ETSI)		–57		dBm	
Fourth Harm, 169 MHz (ETSI)		–63		dBm	
Second Harm, 433 MHz (ETSI)		–59		dBm	
Third Harm, 433 MHz (ETSI)		–51		dBm	
Fourth Harm, 433 MHz (ETSI)		–63		dBm	
Second Harm, 868 MHz (ETSI)		–50		dBm	
Third Harm, 868 MHz (ETSI)		–44		dBm	
Fourth Harm, 868 MHz (ETSI)		–56		dBm	
Second Harm, 915 MHz (FCC)		–58		dBm	
Third Harm, 915 MHz (FCC)		–46		dBm	
Fourth Harm, 915 MHz (FCC)		–62		dBm	
Second Harm, 920 MHz (ARIB)		–65		dBm	
Third Harm, 920 MHz (ARIB)		–60		dBm	
Optimum load impedance					
868-, 915-, and 920-MHz bands		$35 + j35$		Ω	
433-MHz band		$55 + j25$		Ω	
169-MHz band		$80 + j0$		Ω	

4.12 PLL Parameters

4.12.1 High Performance Mode

 $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Phase noise in 868-, 915-, and 920-MHz Bands 200-kHz loop bandwidth setting		–94		dBc/Hz	$\pm 10\text{ kHz offset}$
		–96		dBc/Hz	$\pm 100\text{ kHz offset}$
		–123		dBc/Hz	$\pm 1\text{ MHz offset}$
		–137		dBc/Hz	$\pm 10\text{ MHz offset}$
Phase noise in 868-, 915-, and 920-MHz Bands 300-kHz loop bandwidth setting		–100		dBc/Hz	$\pm 10\text{ kHz offset}$
		–102		dBc/Hz	$\pm 100\text{ kHz offset}$
		–121		dBc/Hz	$\pm 1\text{ MHz offset}$
		–136		dBc/Hz	$\pm 10\text{ MHz offset}$
Phase noise in 868-, 915-, and 920-MHz Bands 400-kHz loop bandwidth setting		–103		dBc/Hz	$\pm 10\text{ kHz offset}$
		–104		dBc/Hz	$\pm 100\text{ kHz offset}$
		–119		dBc/Hz	$\pm 1\text{ MHz offset}$
		–133		dBc/Hz	$\pm 10\text{ MHz offset}$
Phase noise in 868-, 915-, and 920-MHz Bands 500-kHz loop bandwidth setting		–104		dBc/Hz	$\pm 10\text{ kHz offset}$
		–106		dBc/Hz	$\pm 100\text{ kHz offset}$
		–116		dBc/Hz	$\pm 1\text{ MHz offset}$
		–130		dBc/Hz	$\pm 10\text{ MHz offset}$
Phase noise in 433-MHz band 300-kHz loop bandwidth setting		–106		dBc/Hz	$\pm 10\text{ kHz offset}$
		–107		dBc/Hz	$\pm 100\text{ kHz offset}$
		–127		dBc/Hz	$\pm 1\text{ MHz offset}$
		–141		dBc/Hz	$\pm 10\text{ MHz offset}$
Phase noise in 169-MHz band 300-kHz loop bandwidth setting		–114		dBc/Hz	$\pm 10\text{ kHz offset}$
		–114		dBc/Hz	$\pm 100\text{ kHz offset}$
		–132		dBc/Hz	$\pm 1\text{ MHz offset}$
		–142		dBc/Hz	$\pm 10\text{ MHz offset}$

4.12.2 Low-Power Mode

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Phase noise in 868-, 915-, and 920-MHz bands 200-kHz loop bandwidth setting		–99		dBc/Hz	$\pm 10\text{ kHz offset}$
		–101		dBc/Hz	$\pm 100\text{ kHz offset}$
		–121		dBc/Hz	$\pm 1\text{ MHz offset}$
		–135		dBc/Hz	$\pm 10\text{ MHz offset}$

4.13 Wake-up and Timing

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$, $f_c = 869.5\text{ MHz}$ (unless otherwise noted)

The turnaround behavior to and from RX and/or TX is highly configurable, and the time it takes will depend on how the device is set up. See the CC120X user guide ([SWRU346](#)) for more information.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Powerdown to IDLE		0.24		ms	Depends on crystal
IDLE to RX/TX		133		μs	Calibration disabled
		369		μs	Calibration enabled
RX/TX turnaround		43		μs	
RX-to-RX turnaround		369		μs	With PLL calibration
		0		μs	Without PLL calibration
TX-to-TX turnaround		369		μs	With PLL calibration
		0		μs	Without PLL calibration
RX/TX to IDLE time		237		μs	Calibrate when leaving RX/TX enabled
		0		μs	Calibrate when leaving RX/TX disabled
Frequency synthesizer calibration		314		μs	When using SCAL strobe
Minimum required number of preamble bytes		0.5		bytes	Required for RF front end gain settling only. Digital demodulation does not require preamble for settling
Time from start RX until valid RSSI ⁽¹⁾ Including gain settling (function of channel bandwidth. Programmable for trade-off between speed and accuracy)		0.25		ms	120-kHz channels

(1) See the design note on RSSI and response time. It is written for the CC112X devices, but the same principles apply for the CC1201 device.

4.14 40-MHz Crystal Oscillator

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Crystal frequency	38.4		40	MHz	It is expected that there will be degraded sensitivity at multiples of XOSC/2 in RX, and an increase in spurious emissions when the RF channel is close to multiples of XOSC in TX. We recommend that the RF channel is kept RX_BW/2 away from XOSC/2 in RX, and that the level of spurious emissions be evaluated if the RF channel is closer than 1 MHz to multiples of XOSC in TX.
Load capacitance (C_L)		10		pF	
ESR			60	Ω	Simulated over operating conditions
Start-up time		0.24		ms	Depends on crystal

4.15 40-MHz Clock Input (TCXO)

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Clock frequency	38.4		40	MHz	
TCXO with CMOS output					TCXO with CMOS output directly coupled to pin EXT_OSC
High input voltage	1.4		V_{DD}	V	
Low input voltage	0		0.6	V	
Rise / Fall time			2	ns	
Clipped sine output					TCXO clipped sine output connected to pin EXT_OSC through series capacitor
Clock input amplitude (peak-to-peak)	0.8		1.5	V	

4.16 32-kHz Clock Input

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Clock frequency		32		kHz	
32-kHz clock input pin input high voltage	$0.8 \times V_{DD}$			V	
32-kHz clock input pin input low voltage			$0.2 \times V_{DD}$	V	

4.17 40-kHz RC Oscillator

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Frequency		40		kHz	After calibration (frequency calibrated against the 40-MHz crystal or TCXO)
Frequency accuracy after calibration		± 0.1		%	Relative to frequency reference (that is, 40-MHz crystal or TCXO)
Initial calibration time		1.32		ms	

4.18 I/O and Reset

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Logic input high voltage	$0.8 \times V_{DD}$			V	
Logic input low voltage			$0.2 \times V_{DD}$	V	
Logic output high voltage	$0.8 \times V_{DD}$			V	At 4-mA output load or less
Logic output low voltage			$0.2 \times V_{DD}$	V	
Power-on reset threshold		1.3		V	Voltage on DVDD pin

4.19 Temperature Sensor

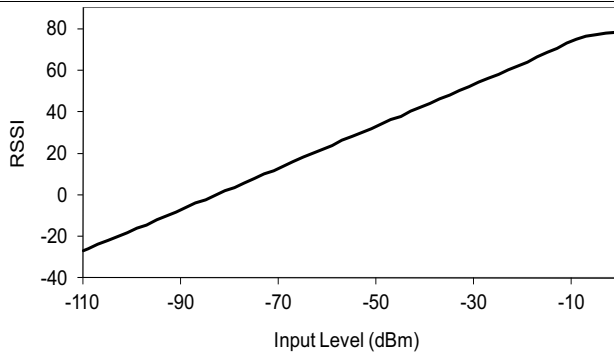
$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$ (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Temperature sensor range	-40		85	$^\circ\text{C}$	
Temperature coefficient		2.66		mV / $^\circ\text{C}$	Change in sensor output voltage versus change in temperature
Typical output voltage		794		mV	Typical sensor output voltage at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{ V}$
VDD coefficient		1.17		mV / V	Change in sensor output voltage versus change in VDD

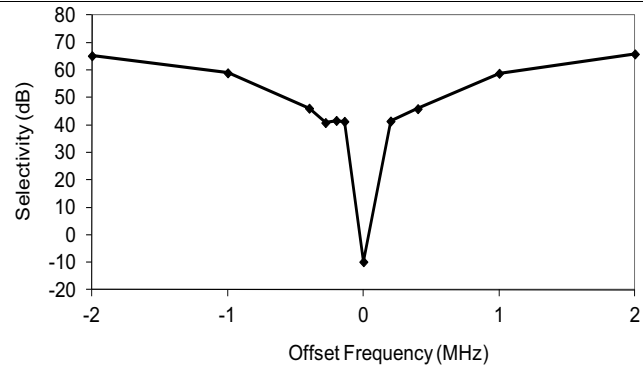
The CC1201 device can be configured to provide a voltage proportional to temperature on GPIO1. The temperature can be estimated by measuring this voltage (see [Section 4.19, Temperature Sensor](#)). For more information, see the temperature sensor design note ([SWRA415](#)).

4.20 Typical Characteristics

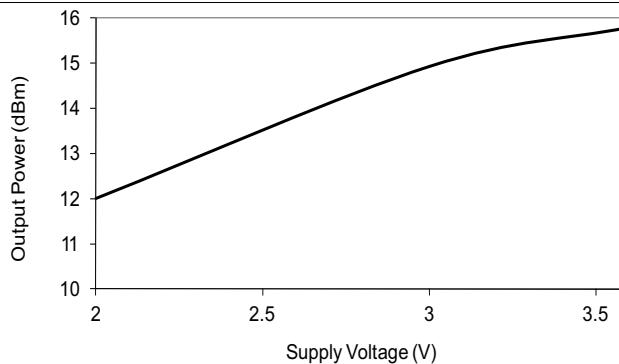
TA = 25°C, VDD = 3.0 V, f_c = 869.5 MHz (unless otherwise noted)



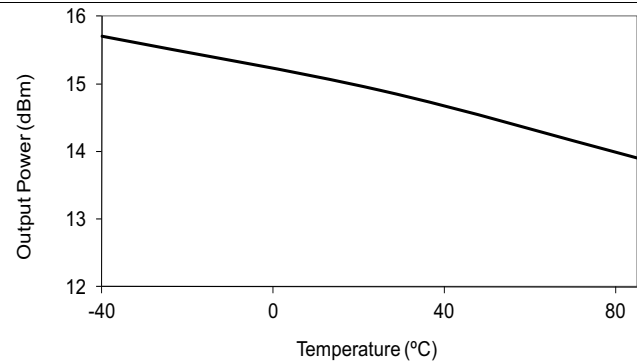
50-kbps GFSK, 25-kHz Deviation, 104-kHz Channel Filter Bandwidth
Figure 4-1. RSSI vs Input Level



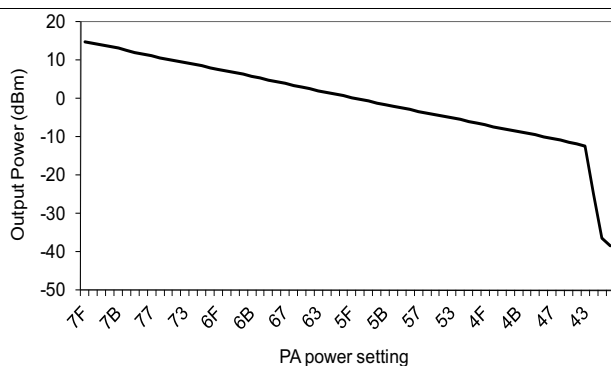
50 kbps, 25-kHz Deviation, 104-kHz Channel Filter Bandwidth Image
Frequency at -0.28-MHz Offset
Figure 4-2. Selectivity vs Offset Frequency (100-kHz Channels)



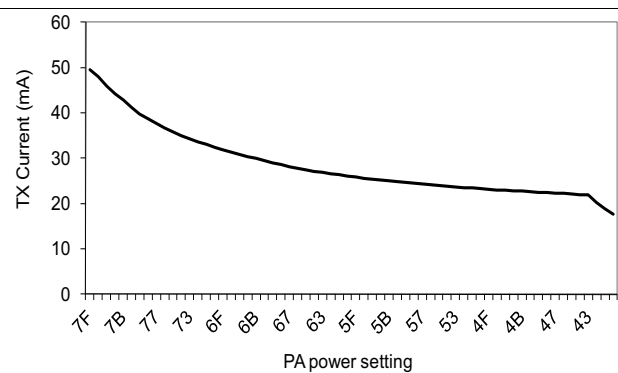
Maximum Output Power Setting (0x7F)
Figure 4-3. Output Power vs Supply Voltage



Maximum Output Power Setting (0x7F)
Figure 4-4. Output Power vs Temperature

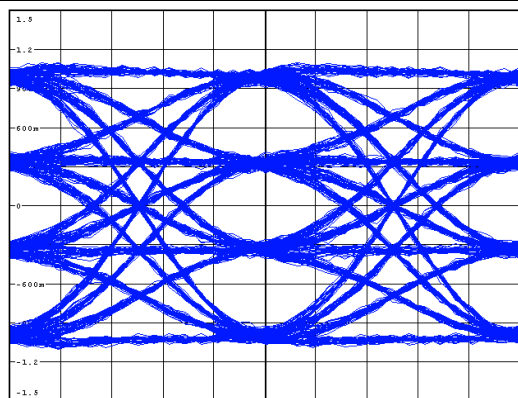


**Figure 4-5. Output Power at 868 MHz
vs PA Power Setting**

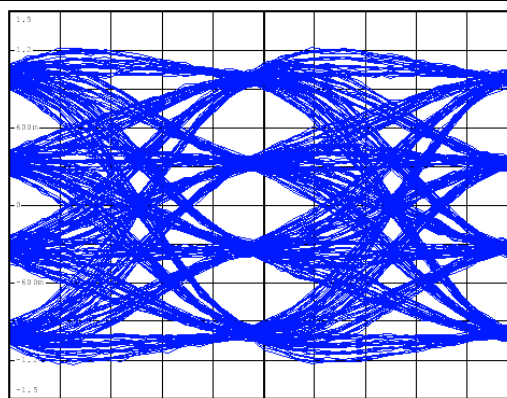


**Figure 4-6. TX Current at 868 MHz
vs PA Power Setting**

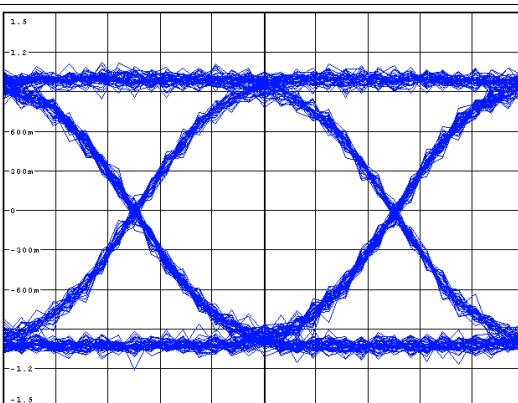
Typical Characteristics (continued)



1 Mbps 4-GFSK, 400-kHz Deviation 500-kHz Loop Bandwidth
Figure 4-7. Eye Diagram



1 Mbps 4-GFSK, 400-kHz Deviation 300-kHz Loop Bandwidth
Figure 4-8. Eye Diagram



1 kbps GFSK, 25-kHz Deviation 200-kHz Loop Bandwidth
Figure 4-9. Eye Diagram

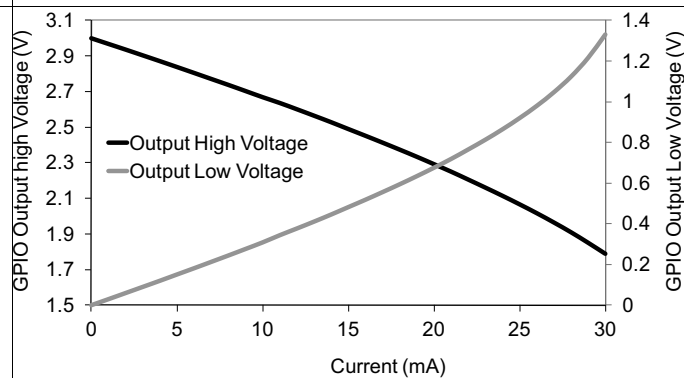
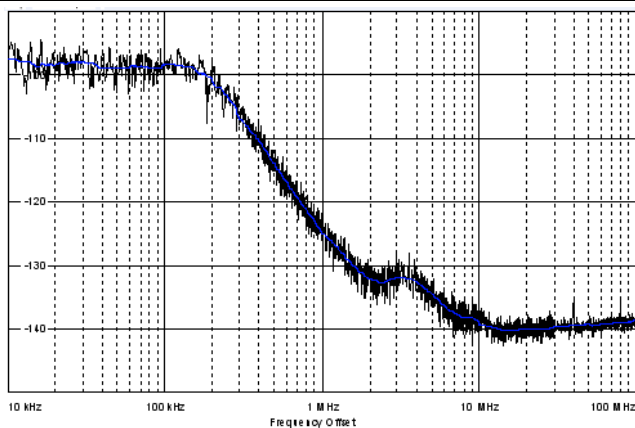
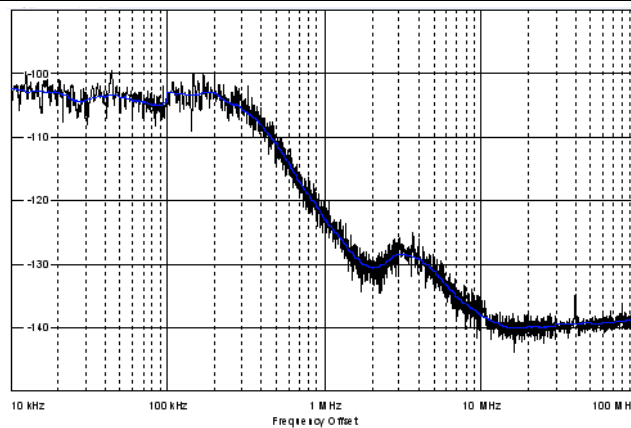


Figure 4-10. GPIO Output High and Low Voltage vs Current Being Sourced and Sunk

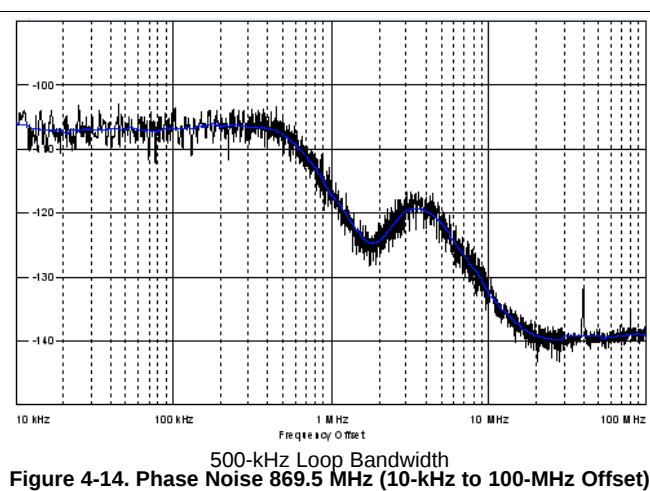
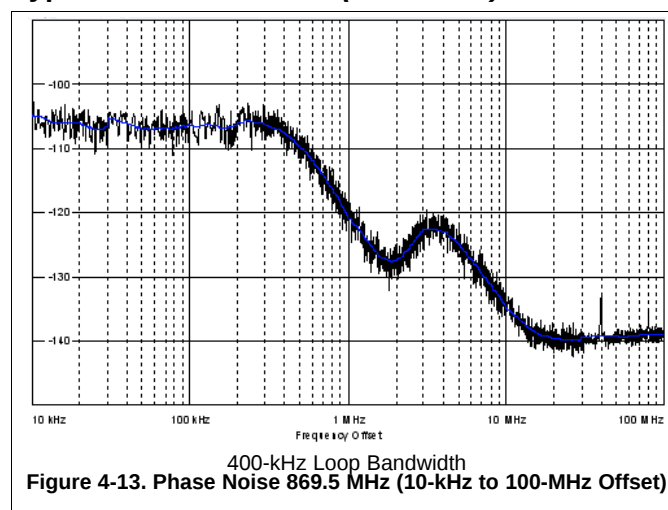


200-kHz Loop Bandwidth
Figure 4-11. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)



300-kHz Loop Bandwidth
Figure 4-12. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)

Typical Characteristics *(continued)*



5 Detailed Description

5.1 Block Diagram

Figure 5-1 shows the system block diagram of the CC120x family of devices.

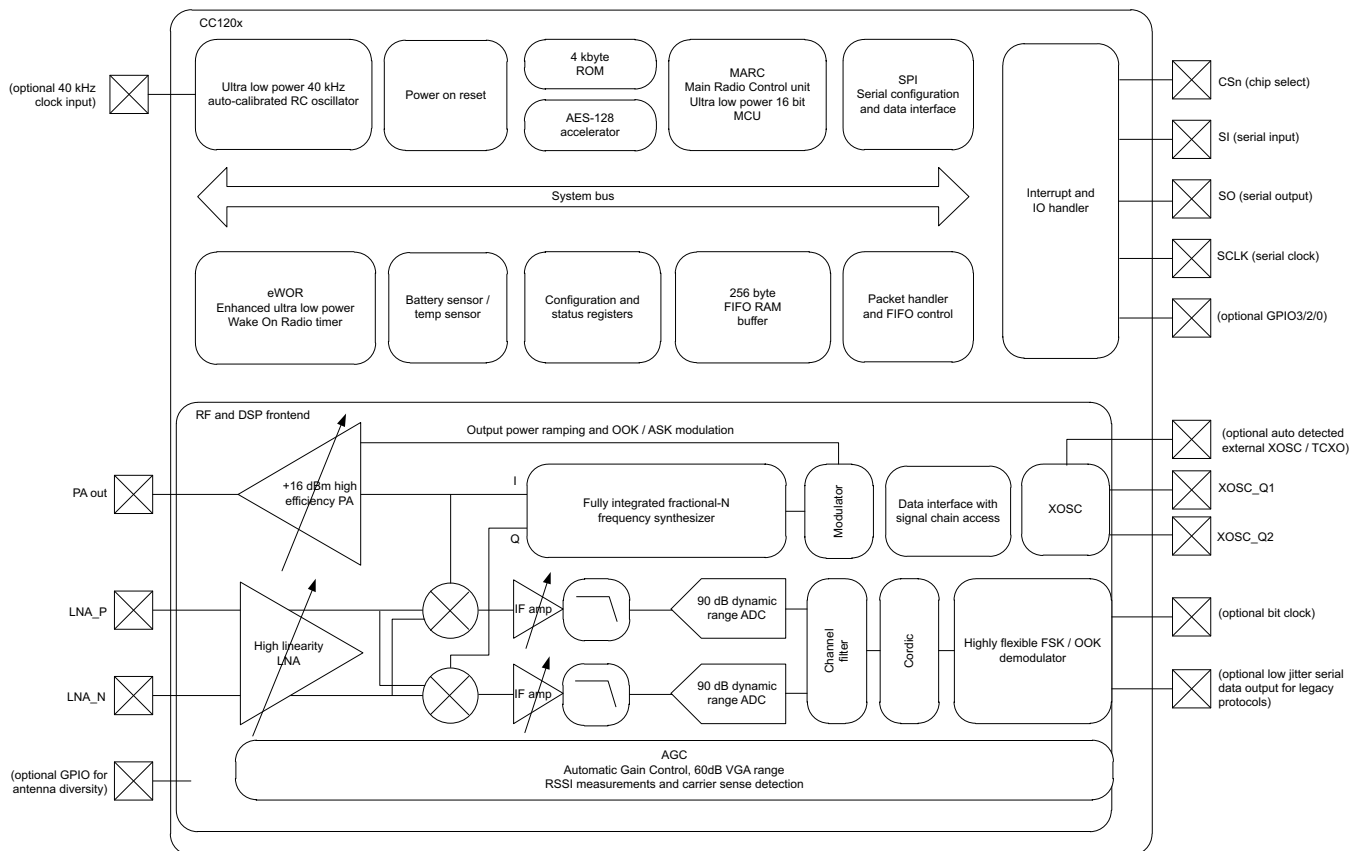


Figure 5-1. System Block Diagram

5.2 Frequency Synthesizer

At the center of the CC1201 device there is a fully integrated, fractional-N, ultra-high-performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance, providing very high selectivity and blocking performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power.

Either a crystal can be connected to XOSC_Q1 and XOSC_Q2, or a TCXO can be connected to the EXT_XOSC input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the analog-to-digital converter (ADC) and the digital part. To reduce system cost, the CC1201 device has high-accuracy frequency estimation and compensation registers to measure and compensate for crystal inaccuracies. This compensation enables the use of lower cost crystals. If a TCXO is used, the CC1201 device automatically turns on and off the TCXO when needed to support low-power modes and Wake-On-Radio operation.

5.3 Receiver

The CC1201 device features a highly flexible receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and is down-converted in quadrature (I/Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitized by the high dynamic-range ADCs.

An advanced automatic gain control (AGC) unit adjusts the front-end gain, and enables the CC1201 device to receive strong and weak signals, even in the presence of strong interferers. High-attenuation channel and data filtering enable reception with strong neighbor channel interferers. The I/Q signal is converted to a phase and magnitude signal to support the FSK and OOK modulation schemes.

NOTE

A unique I/Q compensation algorithm removes any problem of I/Q mismatch, thus avoiding time-consuming and costly I/Q image calibration steps.

5.4 Transmitter

The CC1201 transmitter is based on direct synthesis of the RF frequency (in-loop modulation). To use the spectrum effectively, the CC1201 device has extensive data filtering and shaping in TX mode to support high throughput data communication in narrowband channels. The modulator also controls power ramping to remove issues such as spectral splattering when driving external high-power RF amplifiers.

5.5 Radio Control and User Interface

The CC1201 digital control system is built around the main radio control (MARC), which is implemented using an internal high-performance, 16-bit ultra-low-power processor. MARC handles power modes, radio sequencing, and protocol timing.

A 4-wire SPI serial interface is used for configuration, strobe commands, and FIFO access. The digital baseband includes support for channel configuration, packet handling, and data buffering. The host MCU can stay in sleep mode until a valid RF packet is received. This greatly reduces power consumption. When the host MCU receives a valid RF packet, it burst-reads the data. This reduces the required computing power.

The CC1201 radio control and user interface are based on the widely used CC1101 transceiver. This relationship enables an easy transition between the two platforms. The command strobes and the main radio states are the same for the two platforms.

For legacy formats, the CC1201 device also supports two serial modes.

- Synchronous serial mode: The CC1201 device performs bit synchronization and provides the MCU with a bit clock with associated data.
- Transparent mode: The CC1201 device outputs the digital baseband signal using a digital interpolation filter to eliminate jitter introduced by digital filtering and demodulation.

5.6 Enhanced Wake-On-Radio (eWOR)

eWOR, using a flexible integrated sleep timer, enables automatic receiver polling with no intervention from the MCU. When the CC1201 device enters RX mode, it listens and then returns to sleep if a valid RF packet is not received. The sleep interval and duty cycle can be configured to make a trade-off between network latency and power consumption. Incoming messages are time-stamped to simplify timer re-synchronization.

The eWOR timer runs off an ultra-low-power RC oscillator. To improve timing accuracy, the RC oscillator can be automatically calibrated to the RF crystal in configurable intervals.

5.7 RX Sniff Mode

The CC1201 device supports quick start up times, and requires few preamble bits. RX Sniff Mode uses these conditions to dramatically reduce the current consumption while the receiver is waiting for data.

Because the CC1201 device can wake up and settle much faster than the duration of most preambles, it is not required to be in RX mode continuously while waiting for a packet to arrive. Instead, the Enhanced Wake On Radio feature can be used to put the device into sleep mode periodically. By setting an appropriate sleep time, the CC1201 device can wake up and receive the packet when it arrives with no performance loss. This sequence removes the need for accurate timing synchronization between transmitter and receiver, and lets the user trade off current consumption between the transmitter and receiver.

For more information, see the sniff mode design note ([SWRA428](#)).

5.8 Antenna Diversity

Antenna diversity can increase performance in a multipath environment. An external antenna switch is required. The CC1201 device uses one of the GPIO pins to automatically control the switch. This device also supports differential output control signals typically used in RF switches.

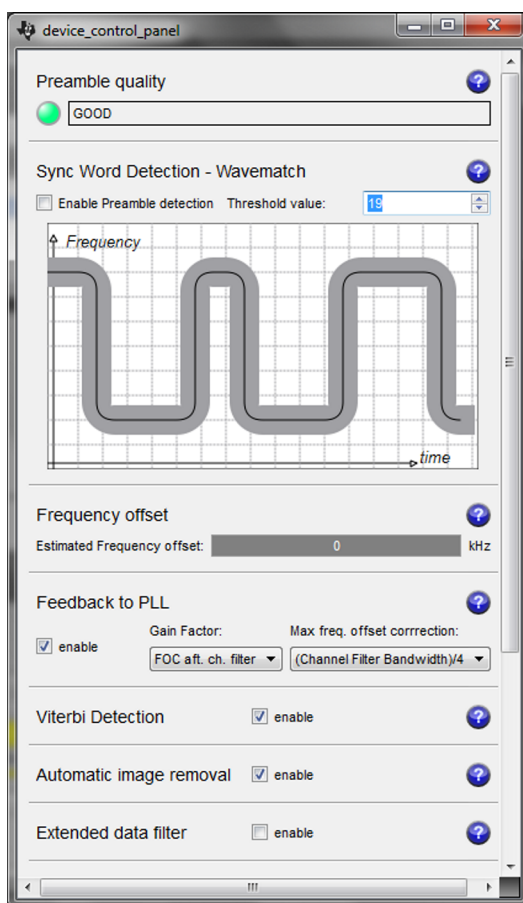
If antenna diversity is enabled, the GPIO alternates between high and low states until a valid RF input signal is detected. An optional acknowledge packet can be transmitted without changing the state of the GPIO.

An incoming RF signal can be validated by received signal strength or by using the automatic preamble detector. Using the automatic preamble detector ensures a more robust system and avoids the need to set a defined signal strength threshold (such a threshold sets the sensitivity limit of the system).

5.9 WaveMatch

Advanced capture logic locks onto the synchronization word and does not require preamble settling bytes. Therefore, receiver settling time is reduced to the settling time of the AGC, typically 4 bits.

The WaveMatch feature also greatly reduces false sync triggering on noise, further reducing the power consumption and improving sensitivity and reliability. The same logic can also be used as a high-performance preamble detector to reliably detect a valid preamble in the channel.



See [swrc046](#) for more information.

Figure 5-2. Receiver Configurator in SmartRF™ Studio

6 Typical Application Circuit

NOTE

This section is intended only as an introduction.

Very few external components are required for the operation of the CC1201 device. [Figure 6-1](#) shows a typical application circuit. The board layout will greatly influence the performance of the CC1201 device. [Figure 6-1](#) does not show decoupling capacitors for power pins.

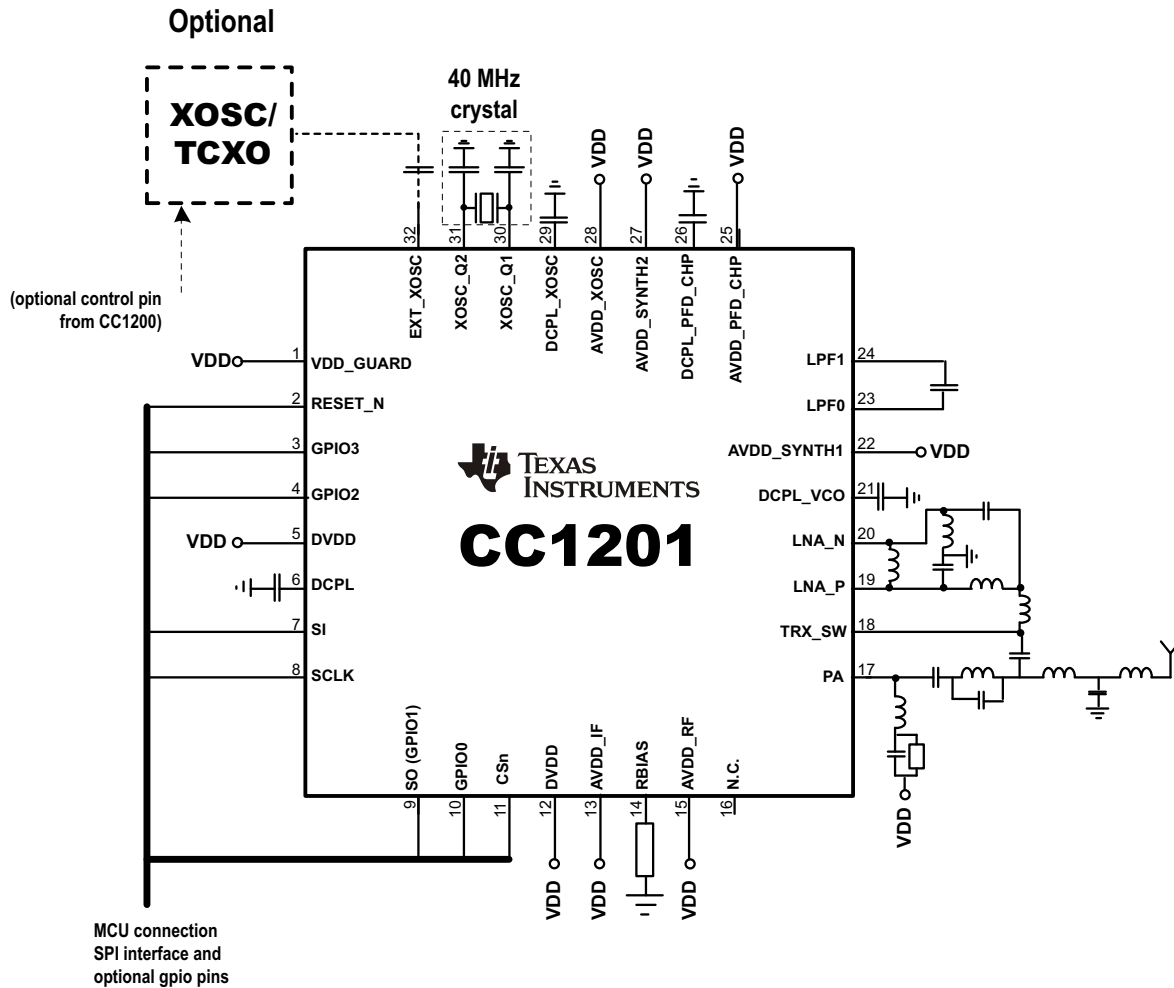


Figure 6-1. Typical Application Circuit

For more information, see the reference designs available for the CC1201 device in [节 7.2, Documentation Support](#).

7 器件和文档支持

7.1 器件支持

7.1.1 开发支持

7.1.1.1 配置软件

CC1201 器件可使用 SmartRF Studio 软件 ([SWRC046](#)) 进行配置。强烈建议使用 SmartRF Studio 软件来获取最优寄存器设置并评估相关性能和功能。

7.1.2 器件和支持开发工具命名规则

为了指出产品开发周期所处的阶段，TI 为所有微处理器 (MPU) 和支持工具的产品型号分配了前缀。每个器件都具有以下三个前缀中的一个：X、P 或无（无前缀）（例如，CC1201）。德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：TMDX 和 TMDS。这些前缀代表了产品的发展阶段，即从工程原型 (TMDX) 直到完全合格的生产器件和工具 (TMDS)。

器件开发进化流程：

- X** 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。
- P** 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。
- 无** 完全合格的芯片模型的生产版本。

支持工具开发发展流程：

- TMDX** 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。
- TMDS** 完全合格的开发支持产品。

X 和 P 器件和 TMDX 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

生产器件和 TMDS 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件 (X 或者 P) 的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如，RHB），温度范围（例如，“空白”是默认的商业级温度范围）以及器件速度范围（以 MHz 为单位），提供了读取任一 CC1201 器件完整器件名称的图例。

要获得 QFN 封装类型的 CC1201 器件订购部件号，请参见本文档的“封装选项附录”（TI 网站 [www.ti.com](#)），或者联系您的 TI 销售代表。

7.2 文档支持

以下文档介绍了 CC1201 处理器。 www.ti.com 网站上提供了这些文档的副本。 提示：请在 www.ti.com 上提供的搜索框中输入文献编号。

- [SWRR106](#) CC112x IPC 868MHz 和 915MHz 2 层参考设计
- [SWRR107](#) CC112x IPC 868MHz 和 915MHz 4 层参考设计
- [SWRR122](#) CC1201EM 420MHz 至 470MHz 参考设计
- [SWRR121](#) CC1201EM 868MHz 至 930MHz 参考设计
- [SWRC046](#) SmartRF Studio 软件
- [SWRA428](#) CC112x/CC120x 嗅探模式应用手册

7.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范 and 标准且不一定反映 TI 的观点；请见 TI 的[使用条款](#)。

[TI E2E™ 在线社区](#) **TI 工程师对工程师 (E2E) 社区**。此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以咨询问题、共享知识、探索思路，在同领域工程师的帮助下解决问题。

[德州仪器 \(TI\) 嵌入式处理器维基网站](#) **德州仪器 (TI) 嵌入式处理器维基网站**。此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.4 商标

SmartRF, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

8 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1201RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1201	Samples
CC1201RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1201	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

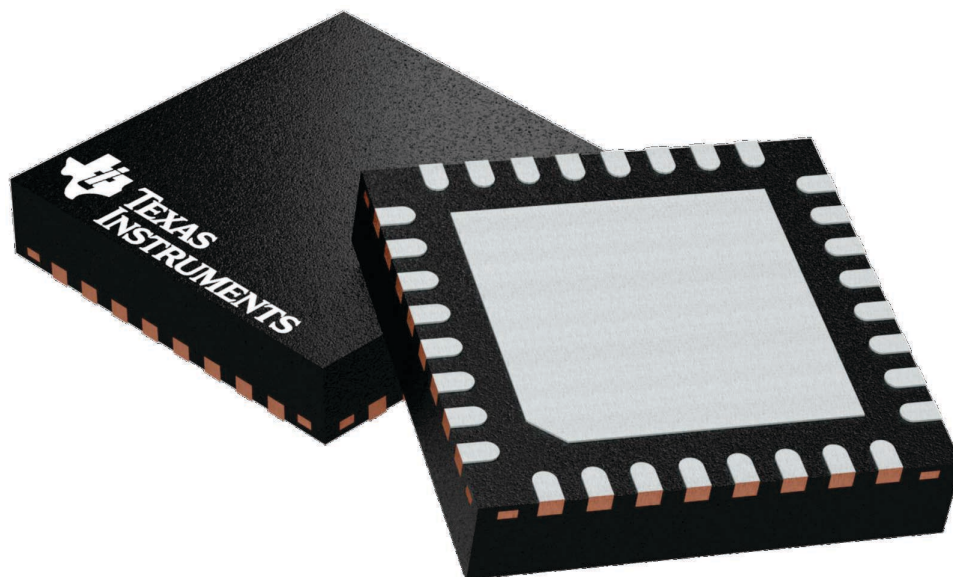
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

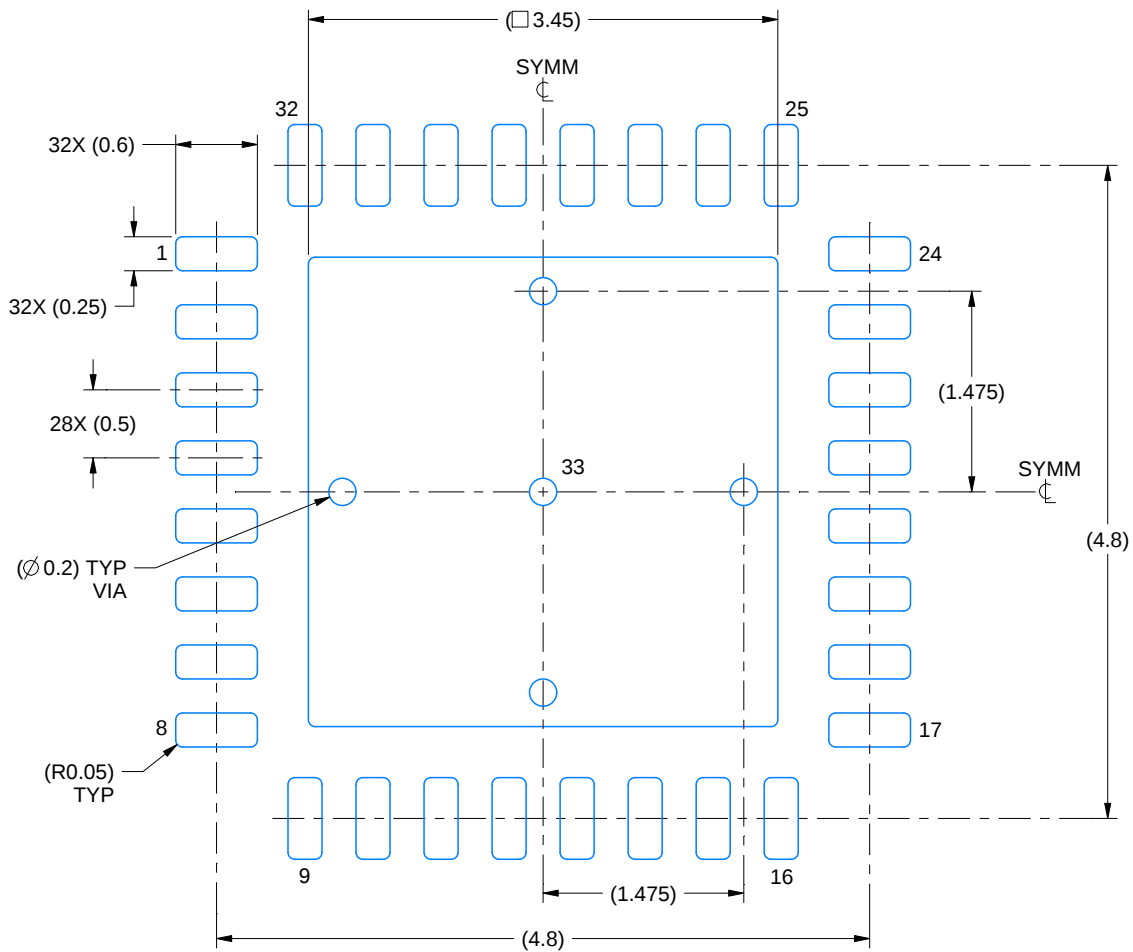
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

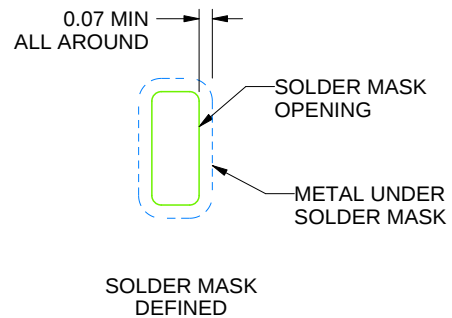
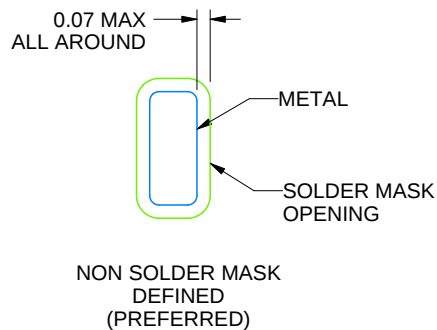
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

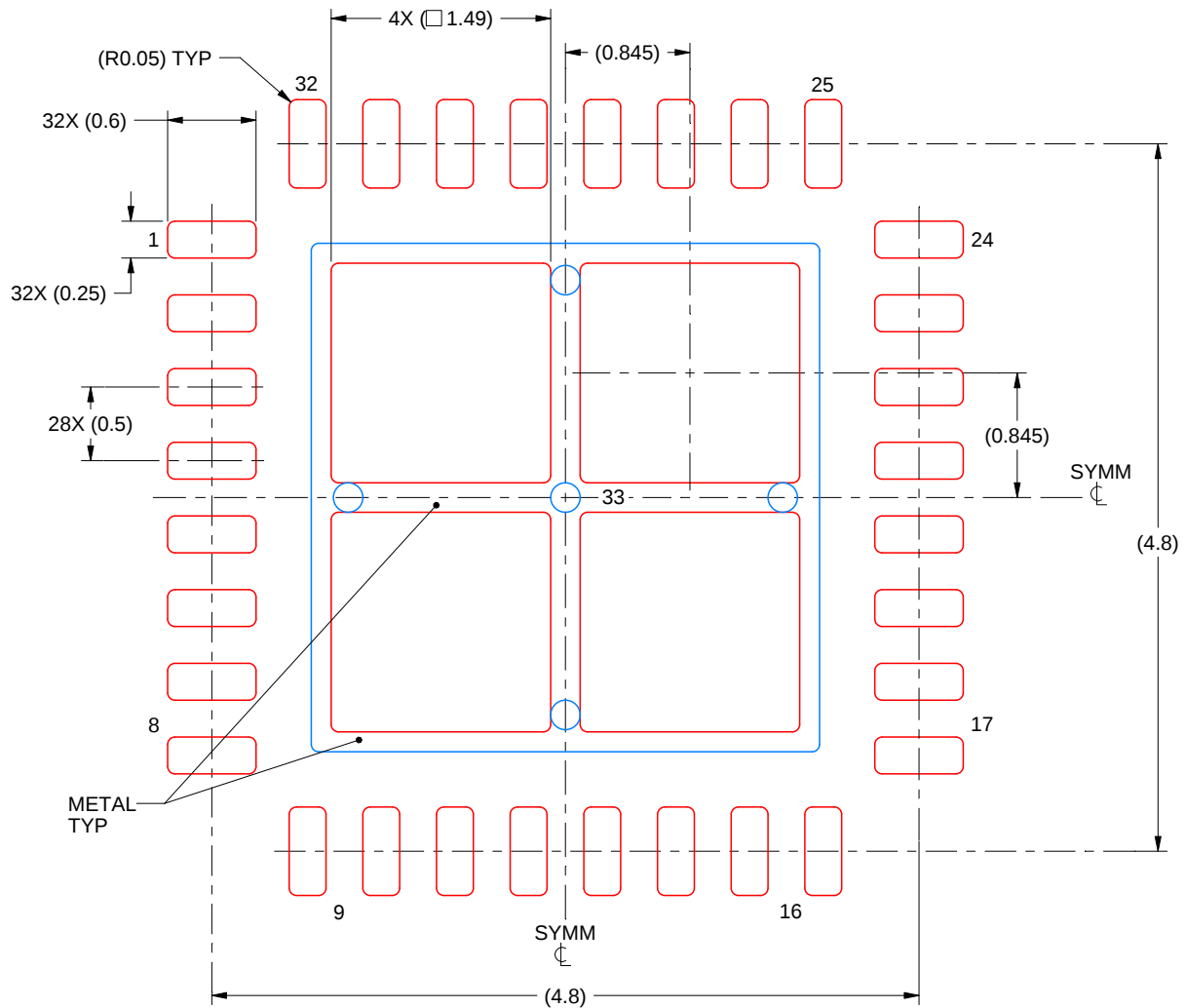
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

4223442/B 08/2019

NOTES: (continued)

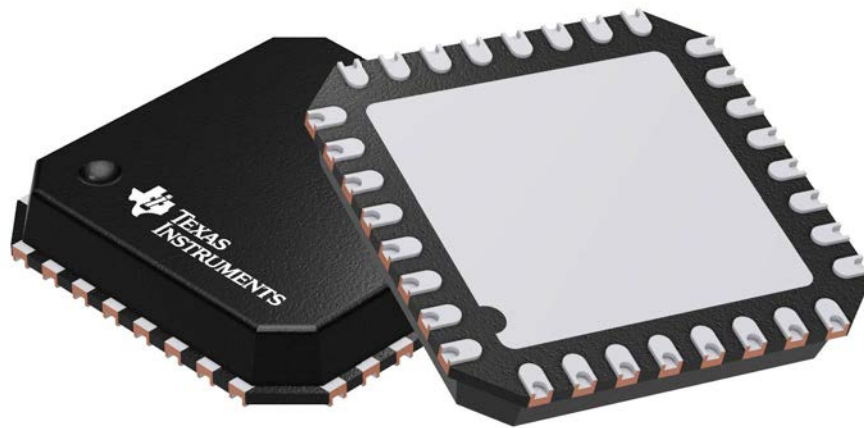
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

RHM 32

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4205347/C

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024，德州仪器 (TI) 公司