TPS6256x 采用 TSOT 和 2mm × 2mm × 0.8mm QFN 封装的 2.25MHz、600mA 降压转换器

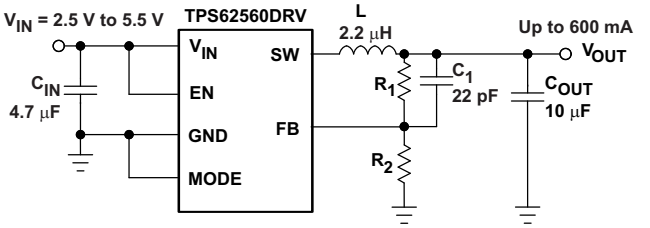
1 特性

- 输出电流最高达 600mA
- 输入电压范围：2.5V 至 5.5V
- PWM 模式下的输出电压精度为 ±2.5%
- 静态电流典型值为 15μA
- 可实现最低压降的 100% 占空比
- 软启动
- 采用小外形尺寸晶体管 (SOT) 和 2mm × 2mm × 0.8mm 小外形尺寸无引线 (SON) 封装
- 有关改进的 特性 集，请参见《TPS62290 器件》（文献编号：SLVS764）

2 应用

- 个人数字助理 (PDA)、掌上电脑和便携式媒体播放器
- 低功耗数字信号处理器 (DSP) 电源
- 负载点 (POL) 应用

典型应用电路原理图



3 说明

TPS62560 器件是一款高效同步降压转换器，针对由电池供电的便携式 应用进行了优化。在诸如单节锂离子电池或由其他常见化学成分组成的 AA 或 AAA 电池供电下，该器件可提供高达 600mA 的输出电流。

凭借 2.5V 至 5.5V 的输入电压范围，该器件适用于为各类便携式手持设备或 POL 应用供电。

TPS62560 系列工作在 2.25MHz 固定开关频率下，并且在轻负载电流条件下会进入节能模式，从而在整个负载电流范围内保持高效率。

该节能模式针对低输出电压纹波进行了优化。对于低噪声 应用，可通过将 MODE 引脚拉为高电平来强制器件进入固定频率 PWM 模式。在关断模式中，电流消耗减小至 1μA 以下。TPS62560 允许使用小型电感和电容，以减小解决方案尺寸。

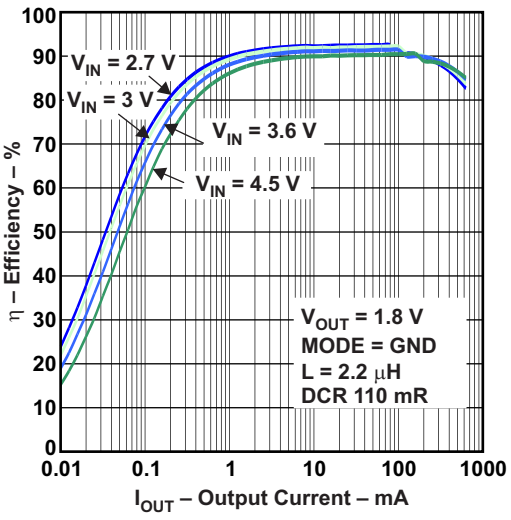
TPS62560 和 TPS62562 采用 2mm x 2mm、6 引脚 SON 封装，而 TPS62561 则采用 5 引脚 SOT 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS62560，TPS62562	SON (6)	2.00mm x 2.00mm
TPS62561	小外形尺寸晶体管 (SOT) (5)	2.90mm x 1.60mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

效率与输出电流间的关系



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Typical Characteristics ... 6
8 Detailed Description ... 7
8.1 Overview ... 7
8.2 Functional Block Diagram ... 7
8.3 Feature Description ... 8
8.4 Device Functional Modes ... 9
9 Application and Implementation ... 10
9.1 Application Information ... 10
9.2 Typical Application ... 10
9.3 System Examples ... 17
10 Power Supply Recommendations ... 17
11 Layout ... 18
11.1 Layout Guidelines ... 18
11.2 Layout Examples ... 18
12 器件和文档支持 ... 20
12.1 器件支持 ... 20
12.2 相关链接 ... 20
12.3 接收文档更新通知 ... 20
12.4 社区资源 ... 20
12.5 商标 ... 20
12.6 静电放电警告 ... 20
12.7 Glossary ... 20
13 机械、封装和可订购信息 ... 20

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (December 2009) to Revision D — **Page**

- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1
- 已删除所有层级下的*订购信息表* ... 1
- 已更改 文本字符串，从“...高达 1000mA 的输出电流...” 更改为“...高达 600mA 的输出电流...”（说明）。 ... 1
- Corrected typographical errors in Figure 32; from "V_{IN}= 2 V to 6 V" to "V_{IN} = 2.5 V to 5.5 V" ... 17

Changes from Revision B (March 2009) to Revision C — **Page**

- 已删除 高效降压转换器 ... 1
- 已删除 特性要点中的 “宽” ... 1
- 已删除 特性中的 “面向具有扩展电压范围的锂离子电池” ... 1
- 已删除 特性中的 “可调和固定两种输出电压选项” ... 1
- 已删除 特性中的 “2.25MHz 固定工作频率” ... 1
- 已删除 特性中的 “轻负载电流下的节能模式” ... 1
- 已删除 特性中的 “可在轻载时进行电压定位” ... 1
- 已删除 特性中的 “允许 < 1mm 的解决方案高度” ... 1
- 已更改 说明 以更好地反映器件功能以及与 TPS62260 的差异 ... 1

Changes from Revision A (July 2008) to Revision B — **Page**

- 已添加 TPS62562 器件编号。 ... 1

Changes from Original (January 2008) to Revision A — **Page**

- 已更改 。版本 A 是本数据表的完全改版。 ... 1

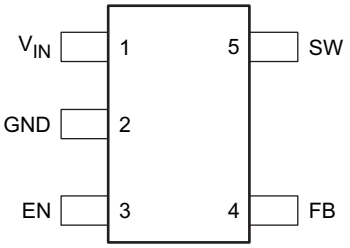
5 Device Comparison Table

Part Number	Package	Mode Pin	Output Voltage(1)	Device Marking(2)
TPS62560	SON (6)	yes	Adjustable	CEY
TPS62561	SOT (5)	forced PWM only	Adjustable	CVO
TPS62562	SON (6)	yes	1.8 V fixed	NXT

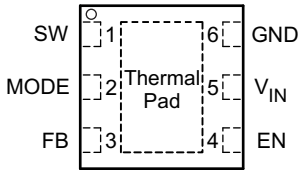
(1) Contact TI for other fixed output voltage options
(2) For the most current package and ordering information, see *机械、封装和可订购信息*, or see the TI website at www.ti.com

6 Pin Configuration and Functions

DDC Package
5-Pin SOT
Top View



DRV Package
6-Pin SON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	No. QFN-6	No. TSOT23-5		
EN	4	3	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
FB	3	4	I	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In the fixed-output-voltage option, connect this terminal directly to the output capacitor.
GND	6	2	—	GND supply pin
MODE	2	N/A	I	This pin is only available as a QFN package option. MODE pin = high forces the device to operate in the fixed-frequency PWM mode. MODE pin = low enables the power-save mode with automatic transition from PFM mode to fixed-frequency PWM mode.
SW	1	5	O	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this pin and the output capacitor.
V_{IN}	5	1	—	V_{IN} power-supply pin
Exposed Thermal Pad	—	N/A	—	Must be soldered to achieve appropriate power dissipation. Should be connected to GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Input voltage range(2)	–0.3	7	V
	Voltage range at EN, MODE	–0.3	V_{IN} +0.3, ≤ 7	
	Voltage on SW	–0.3	7	
	Peak output current	Internally limited		A
T_J	Maximum operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	
		Machine model	±200	

(1) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal. The machine model is a 200-pF capacitor discharged directly into each terminal.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Supply voltage	2.5	5.5	V
V_{OUT}	Output voltage range for adjustable voltage	0.85	V_{IN}	V
T_A	Operating ambient temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS62560, TPS62562	TPS62561	UNIT
		DRV (SON)	DDC (SOT)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.8	226.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.5	40.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	48.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.6	48.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 4.7 µF 0603, C_{OUT} = 10 µF 0603, L = 2.2 µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_{OUT}	Output current	V_{IN} 2.5 V to 5.5 V			600	mA
I_Q	Operating quiescent current	I_{OUT} = 0 mA, PFM mode enabled (MODE = GND), device not switching		15		µA
		I_{OUT} = 0 mA, PFM mode enabled (MODE = GND), device switching, V_{OUT} = 1.8 V, See (1)		18.5		
		I_{OUT} = 0 mA, switching with no load (MODE = V_{IN}), PWM operation, V_{OUT} = 1.8 V, V_{IN} = 3 V		3.8		mA
I_{SD}	Shutdown current	EN = GND		0.5		µA
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High-level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 5.5 V	1		V_{IN}	V
V_{IL}	Low-level input voltage, EN, MODE	2 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
I_{IN}	Input bias current, EN, MODE	EN, MODE = GND or V_{IN}		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High side MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, T_A = 25°C		252	492	mΩ
	Low side MOSFET on-resistance			194	391	
I_{LIMF}	Forward current limit, high and low side MOSFET	V_{IN} = V_{GS} = 3.6 V	0.8	1	1.2	A
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal-shutdown hysteresis	Decreasing junction temperature		20		
OSCILLATOR						
f_{SW}	Oscillator frequency	2 V ≤ V_{IN} ≤ 5.5 V		2.25		MHz
OUTPUT						
V_{OUT}	Adjustable-output voltage range		0.85		V_{IN}	V
V_{OUT}	TPS62562 fixed output voltage	V_{IN} ≥ 1.8 V		1.8		V
V_{ref}	Reference voltage			600		mV
V_{FB}	Feedback voltage, PWM mode	MODE = V_{IN}, PWM operation, for fixed-output-voltage versions V_{FB} = V_{OUT}, 2.5 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 600 mA (2)	–2.5%	0%	2.5%	
	Feedback voltage, PFM mode	MODE = GND, device in PFM mode, voltage positioning active (1)		1%		
	Load regulation	PWM mode		–1		%/A
$t_{Start\ Up}$	Start-up time	Time from active EN to reach 95% of V_{OUT} nominal		500		µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW terminal	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND (3)		0.5	1	µA

(1) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the section.
(2) For V_{IN} = V_{OUT} + 0.6 V
(3) In fixed-output-voltage versions, the internal resistor divider network is disconnected from the FB terminal.

7.6 Typical Characteristics

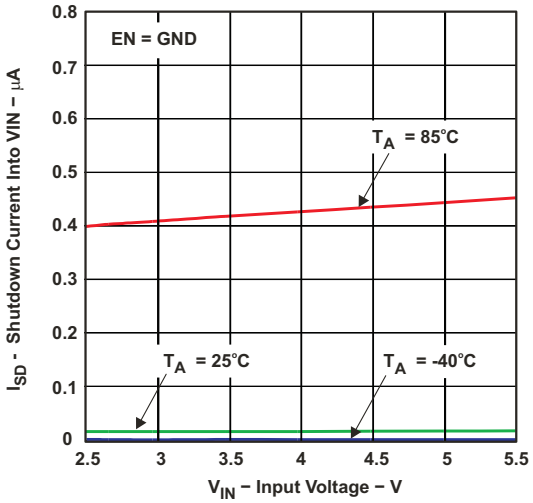


Figure 1. Shutdown Current into VIN vs Input Voltage

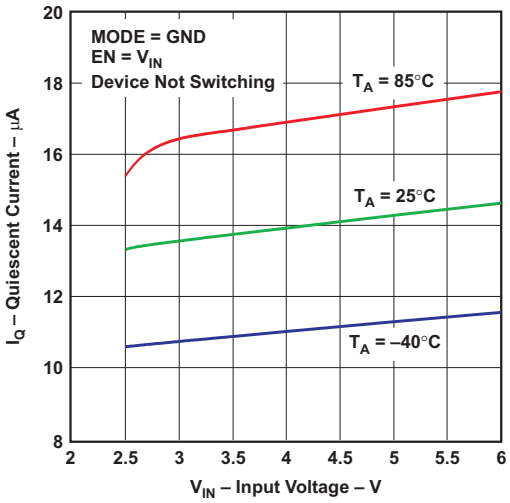


Figure 2. Quiescent Current vs Input Voltage

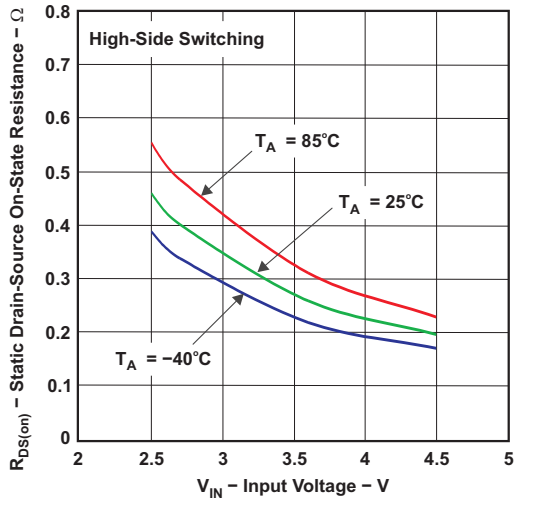


Figure 3. Static Drain-Source ON-State Resistance

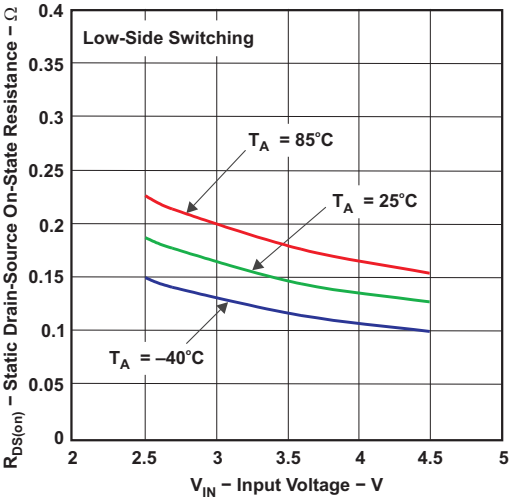


Figure 4. Static Drain-Source ON-State Resistance vs Input Voltage

8 Detailed Description

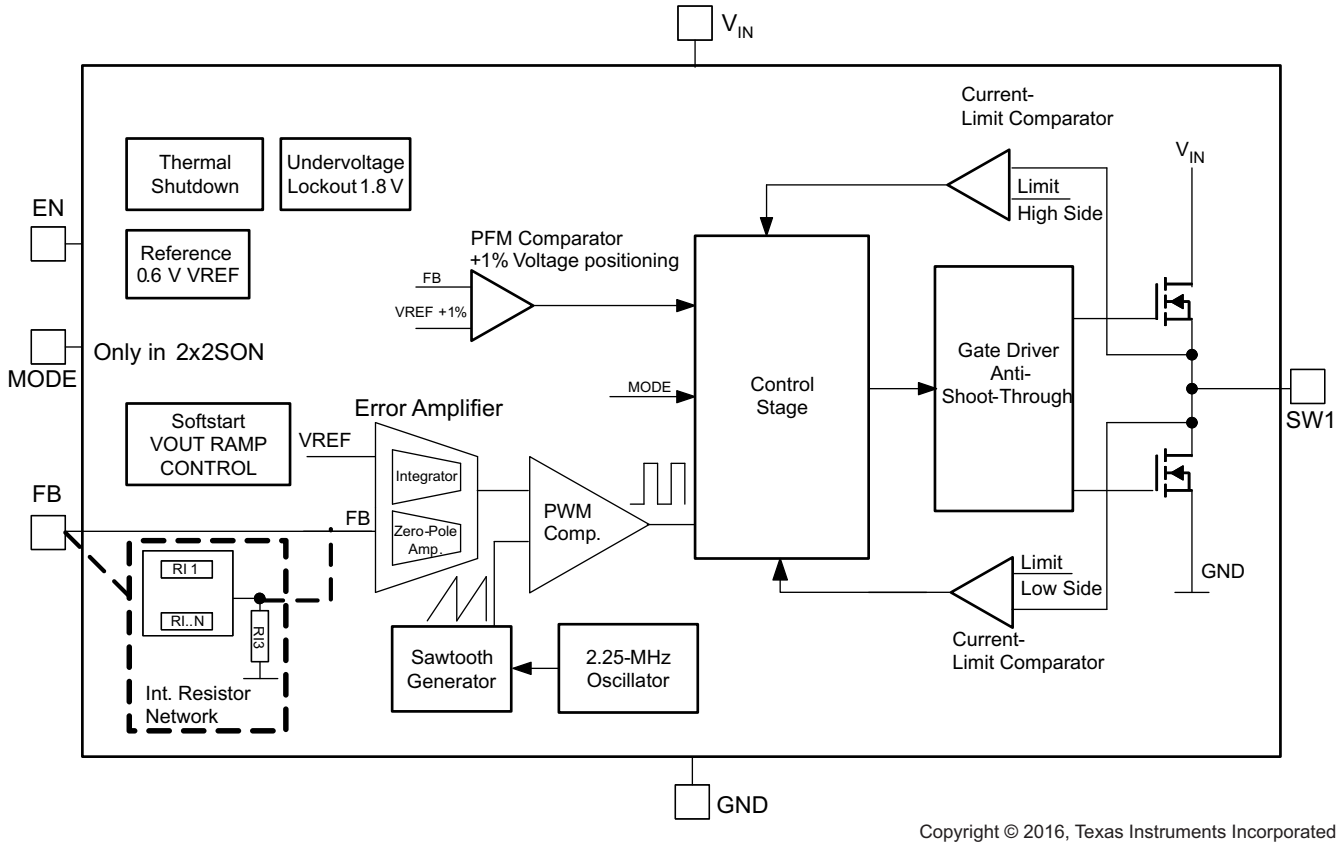
8.1 Overview

The TPS62560/62 step-down converters operate with typically 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power-save mode, and then operates in PFM mode. However, the TPS62561 operates with fixed-frequency PWM only, also at light load conditions.

During PWM operation, the converter uses a unique fast-response voltage-mode control scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows from the input capacitor via the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time, which prevents shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the on the high-side MOSFET switch.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in power-save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

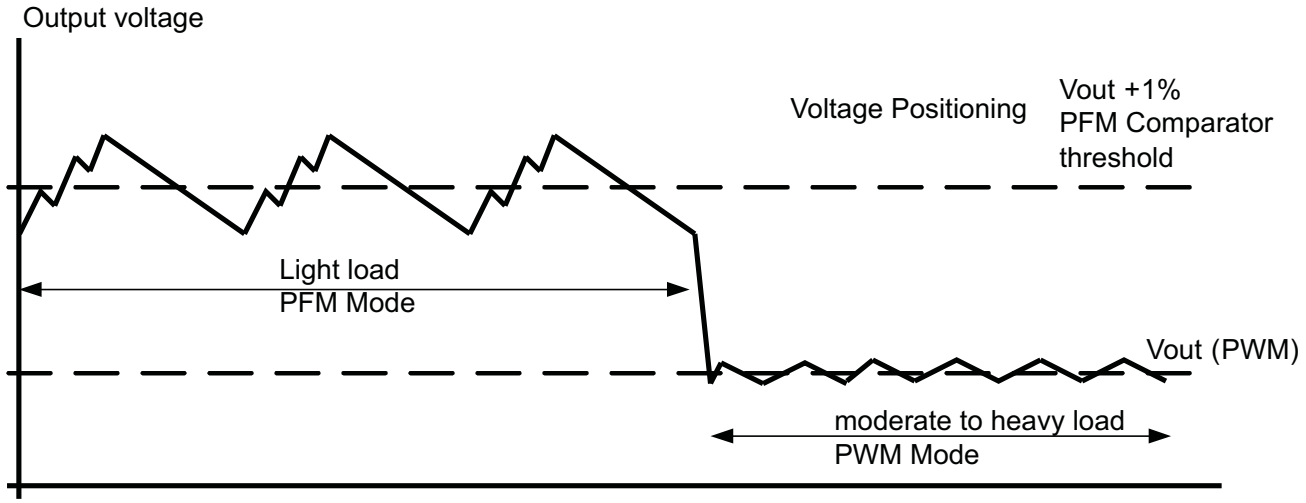


Figure 5. Power Save Mode Operation With Automatic Mode Transition

8.3.2 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

8.3.3 Mode Selection

The MODE terminal allows mode selection between forced-PWM mode and power-save mode.

Connecting this terminal to GND enables the power-save mode with automatic transition between PWM and PFM modes. Pulling the MODE terminal high forces the converter to operate in fixed-frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

The state of the MODE terminal can be changed during operation to allow efficient power management by adjusting the operation mode of the converter to the specific system requirements.

8.3.4 Enable

The device is enabled by setting the EN terminal to high. During the start-up time $t_{Start\ Up}$, the internal circuits are settled and the soft-start circuit is activated. The EN input can be used to control power sequencing in a system with various dc/dc converters. The EN terminal can be connected to the output of another converter, to drive the EN terminal high to achieve a sequencing of the given supply rails. With EN = GND, the device enters shutdown mode, in which all internal circuits are disabled. In fixed-output-voltage versions, the internal resistor divider network is then disconnected from the FB terminal.

8.3.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical), the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

8.4 Device Functional Modes

8.4.1 Soft-Start

The TPS62560 has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value typically within 250 μs. This limits the inrush current into the converter during ramp-up and prevents possible input voltage drops when a battery or high-impedance power source is used. The soft-start circuit is enabled within the start-up time $t_{Start\ Up}$.

8.4.2 Power-Save Mode

The power-save mode is enabled with the MODE terminal set to the low level. If the load current decreases, the converter enters the power-save mode of operation automatically. During power-save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power-save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal + 1%, the device starts a PFM current pulse. The high-side MOSFET switch turns on, and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-μA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses is generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single-threshold comparator, the output-voltage ripple during PFM-mode operation can be kept small. The PFM pulse is time controlled, which allows modifying the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output-voltage ripple and PFM frequency depend primarily on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values minimizes the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

The PFM mode is left and PWM mode entered in case the output current can no longer be supported in PFM mode. The power-save mode can be disabled by setting the MODE terminal to high. The converter then operates in the fixed-frequency PWM mode.

8.4.2.1 100% Duty-Cycle Low-Dropout Operation

The device starts to enter 100% duty-cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN}, the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery-voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage; and, can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times (R_{DS(on)}max + R_L) \quad (1)$$

where

- $I_{OUT}max$ = maximum output current plus inductor ripple current
- $R_{DS(on)}max$ = maximum P-channel switch $R_{DS(on)}$
- R_L = dc resistance of the inductor
- $V_{OUT}max$ = nominal output voltage plus maximum output voltage tolerance

Device Functional Modes (continued)

8.4.2.2 Short-Circuit Protection

The high-side and low-side MOSFET switches are short-circuit protected with maximum switch current = I_{LIMF}. The current in the switches is monitored by current-limit comparators. Once the current in the high-side MOSFET switch exceeds the threshold of its current-limit comparator, it turns off and the low-side MOSFET switch is activated to ramp down the current in the inductor and high-side MOSFET switch. The high-side MOSFET switch can only turn on again after the current in the low-side MOSFET switch has decreased below the threshold of its current-limit comparator.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6256x devices are high-efficiency synchronous step-down DC–DC converter featuring power-save mode or 2.25-MHz fixed frequency operation.

9.2 Typical Application

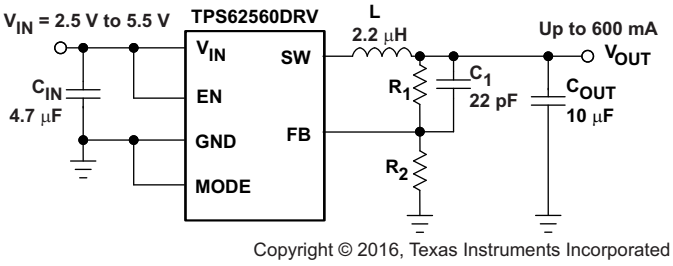


Figure 6. TPS62560DRV Adjustable

9.2.1 Design Requirements

The TPS6256x is a highly integrated DC/DC converter. The output voltage is set with an external voltage divider for the adjustable output voltage version. The output voltage is fixed to 1.8V for the TPS62562. For proper operation a input- and output capacitor and an inductor is required. Table 2 shows the components used for the application characteristic curves.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Setting

For adjustable output voltage versions, the output voltage can be calculated by Equation 2 with the internal reference voltage V_{REF} = 0.6 V typically.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

To minimize the current through the feedback divider network, R_2 should be 180 kΩ or 360 kΩ. The sum of R_1 and R_2 should not exceed ~1 MΩ, to keep the network robust against noise. An external feed-forward capacitor C_1 is required for optimum load transient response. The value of C_1 should be in the range between 22 pF and 33 pF.

In case of using the fixed output voltage version (TPS62562), V_{out} has to be connected to the feedback pin FB.

Typical Application (continued)

Route the FB line away from noise sources, such as the inductor or the SW line.

9.2.2.2 Output Filter Design (inductor and Output Capacitor)

The TPS62560 is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1 µH effective inductance and 3.5 µF effective capacitance.

9.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

The inductor selection also impacts the output voltage ripple in PFM mode. Higher inductor values lead to lower output voltage ripple and higher PFM frequency; lower inductor values lead to a higher output voltage ripple but lower PFM frequency.

Equation 3 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{3}$$

$$I_L\,max = I_{out}\,max + \frac{\Delta I_L}{2} \tag{4}$$

where

- f = Switching frequency (2.25 MHz, typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_L$max = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the dc/dc conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 1. List of Inductors

DIMENSIONS, mm	INDUCTANCE, µH	INDUCTOR TYPE	SUPPLIER(1)
2,5 × 2 × 1 max	2	MIPS2520D2R2	FDK
2,5 × 2 × 1,2 max	2	MIPSA2520D2R2	FDK
2,5 × 2 × 1 max	2.2	KSLI-252010AG2R2	Hitachi Metals
2,5 × 2 × 1,2 max	2.2	LQM2HPN2R2MJ0L	Murata
3 × 3 × 1,5 max	2.2	LPS3015 2R2	Coilcraft

(1) See *Third-Party Products Disclaimer*

9.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TPS62560 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode, and the RMS ripple current is calculated by Equation 5:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2\sqrt{3}} \quad (5)$$

At nominal load current, the device operates in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor shown in Equation 6:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (6)$$

At light load currents, the converter operates in power-save mode, and the output voltage ripple is dependent on the output capacitor and inductor values. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

9.2.2.2.3 Input Capacitor Selection

An input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 4.7-µF to 10-µF ceramic capacitor is recommended. Because a ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended that 10-µF input capacitors be used for input voltages > 4.5 V. The input capacitor can be increased without any limit for better input voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the V_{IN} terminal. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2. List of Capacitors(1)

CAPACITANCE	TYPE	SIZE	SUPPLIER
4.7 µF	GRM188R60J475K	0603—1,6 × 0,8 × 0,8 mm	Murata
10 µF	GRM188R60J106M69D	0603—1,6 × 0,8 × 0,8 mm	Murata

(1) See *Third-Party Products Disclaimer*

9.2.3 Application Curves

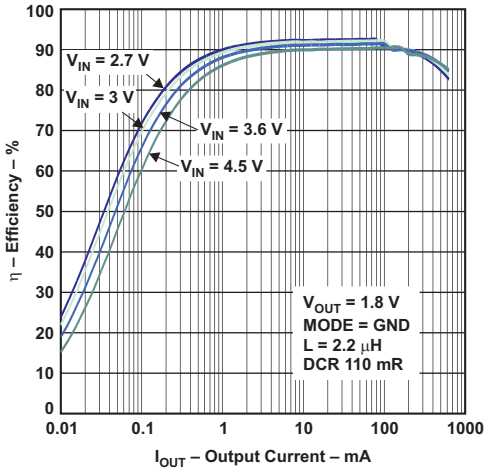


Figure 7. Efficiency vs Output Current

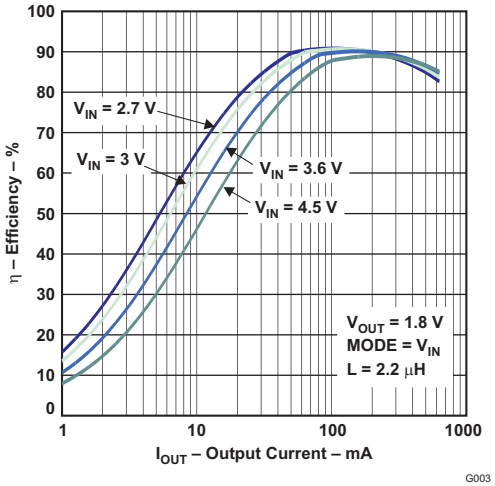


Figure 8. Efficiency vs Output Current

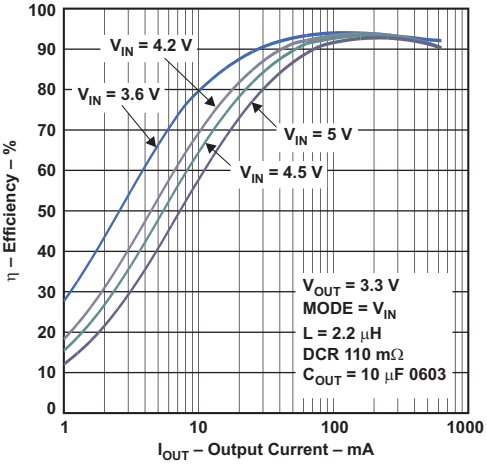


Figure 9. Efficiency vs Output Current

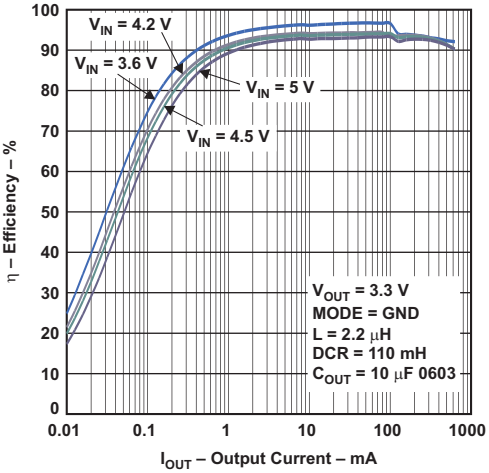


Figure 10. Efficiency vs Output Current

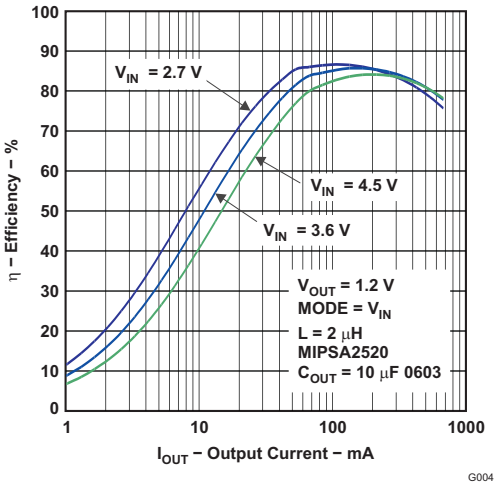


Figure 11. Efficiency vs Output Current

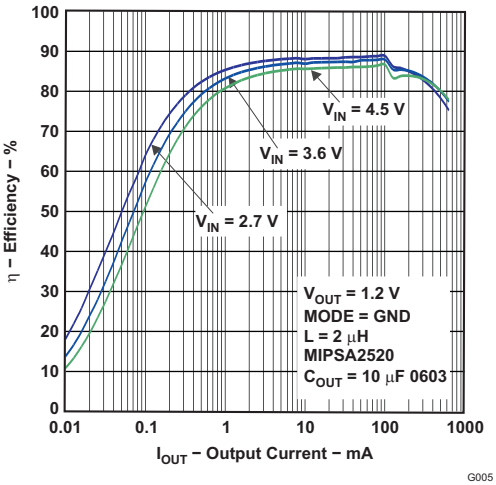


Figure 12. Efficiency vs Output Current

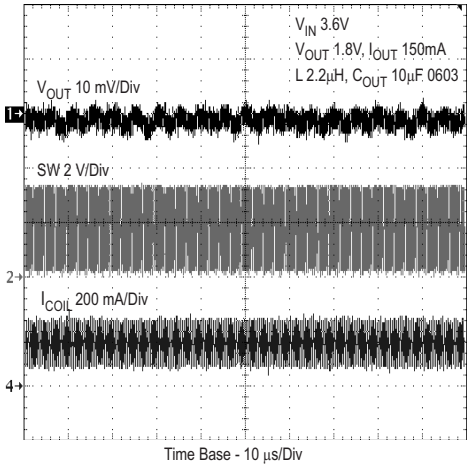


Figure 13. Typical Operation - PWM Mode

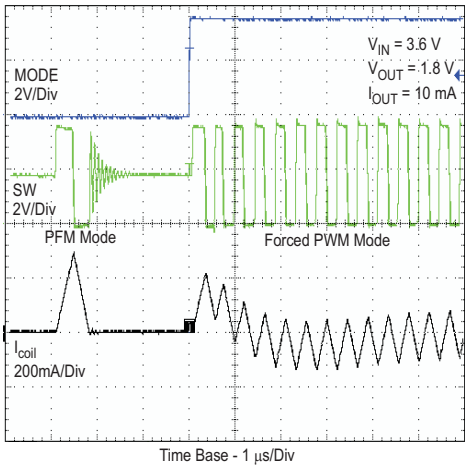


Figure 14. Mode Pin Transition from PFM to FORCED PWM Mode at Light Load

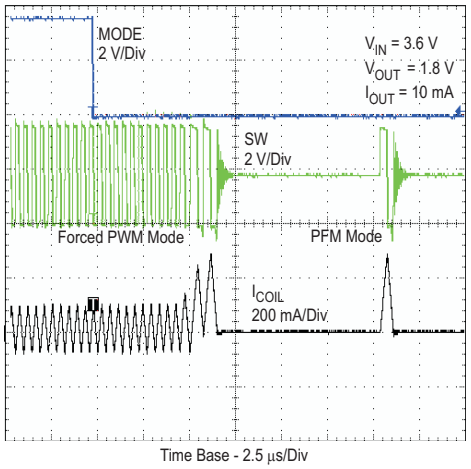


Figure 15. Mode Pin Transition from PWM to PFM MODE at Light Load

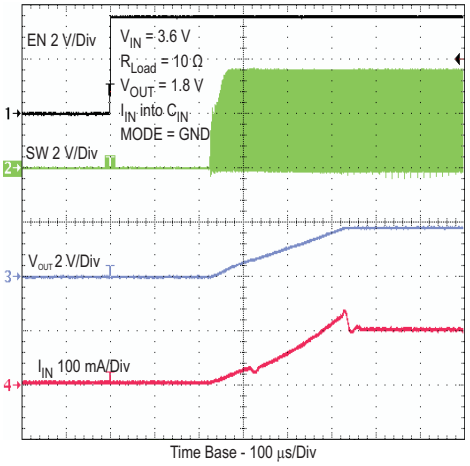


Figure 16. Start-UP Timing

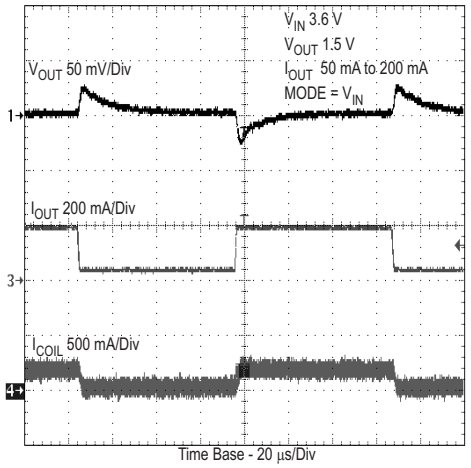


Figure 17. Forced PWM Load Transient

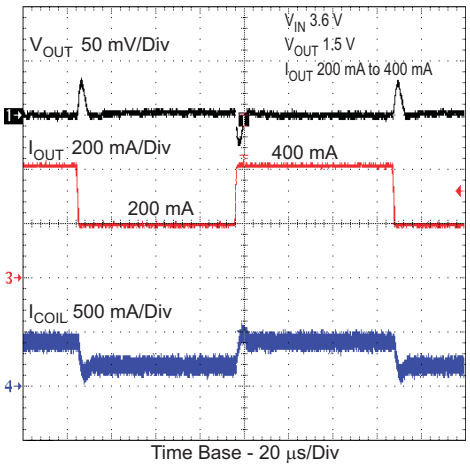


Figure 18. Forced PWM Load Transient

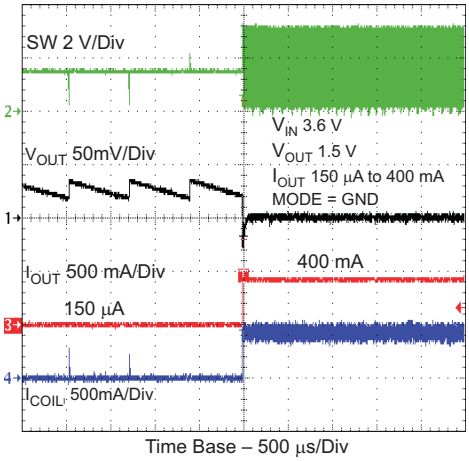


Figure 19. PFM Load Transient

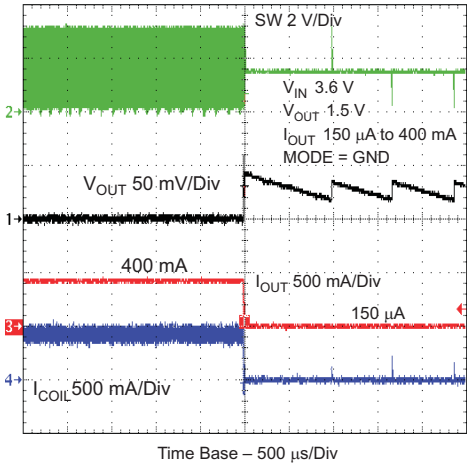


Figure 20. PFM Load Transient

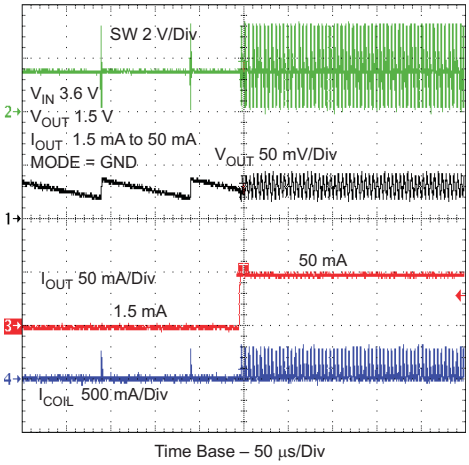


Figure 21. PFM Load Transient

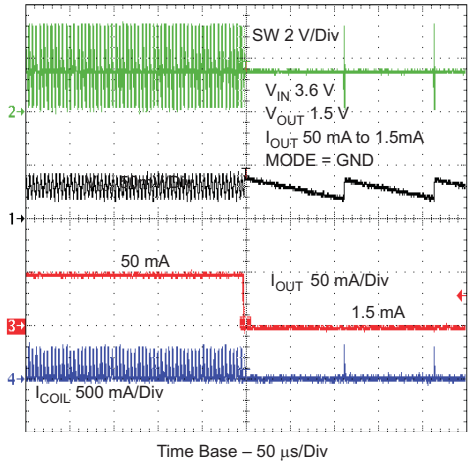


Figure 22. PFM Load Transient

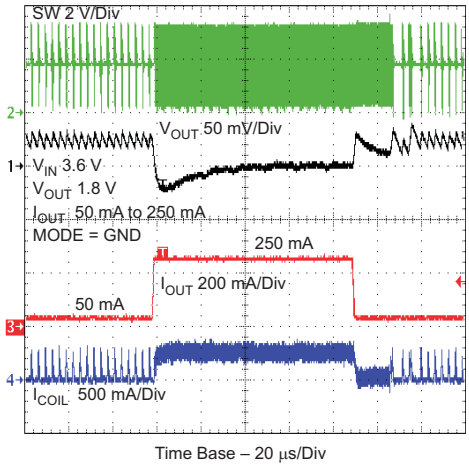


Figure 23. PFM Load Transient

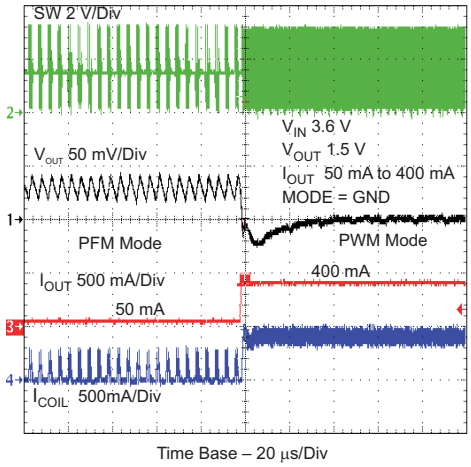


Figure 24. PFM Load Transient

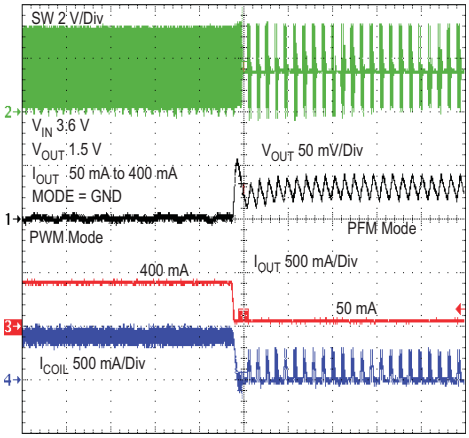


Figure 25. PFM Load Transient

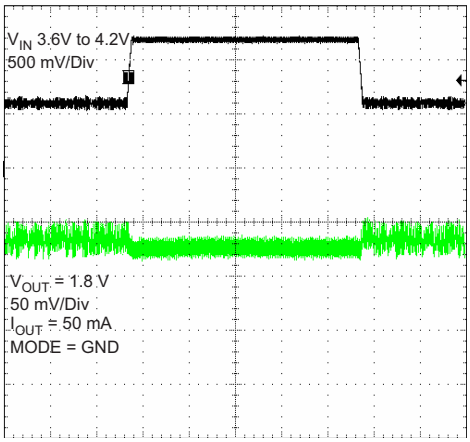


Figure 26. PFM Line Transient

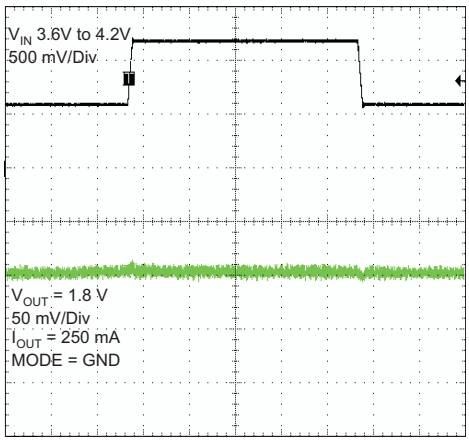


Figure 27. PWM Line Transient

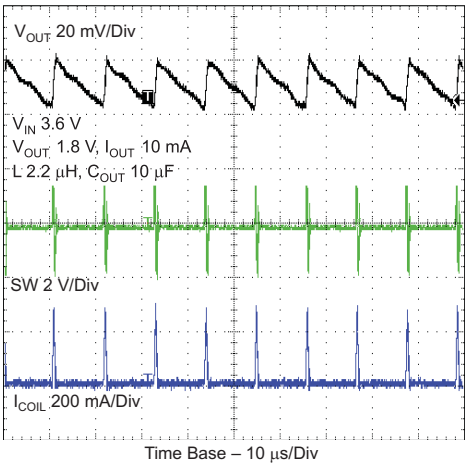


Figure 28. Typical Operation - PFM Mode

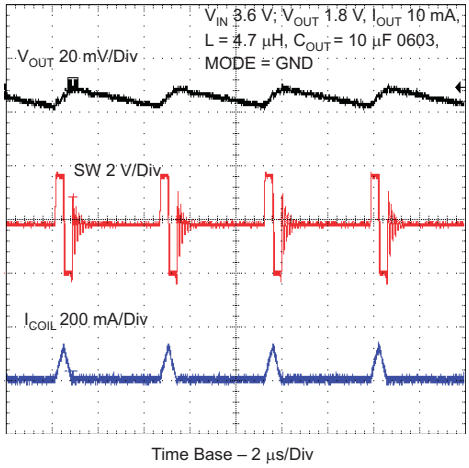


Figure 29. Typical Operation - PFM Mode

9.3 System Examples

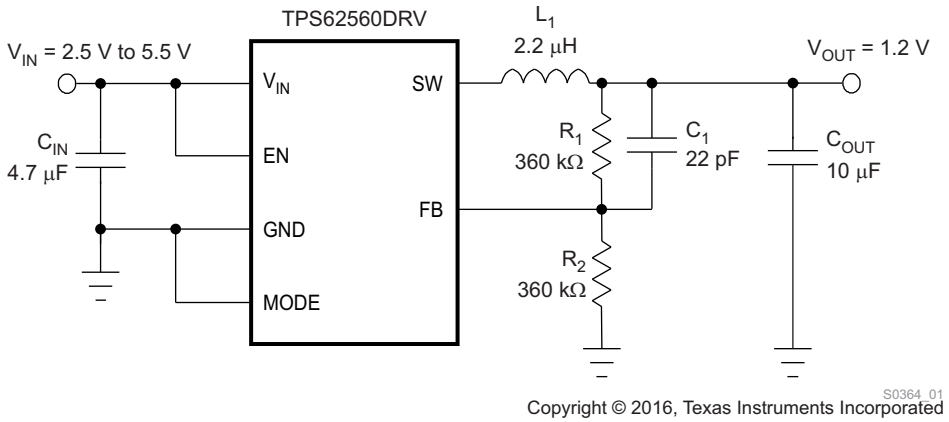


Figure 30. TPS62560 Adjustable 1.2-V Output

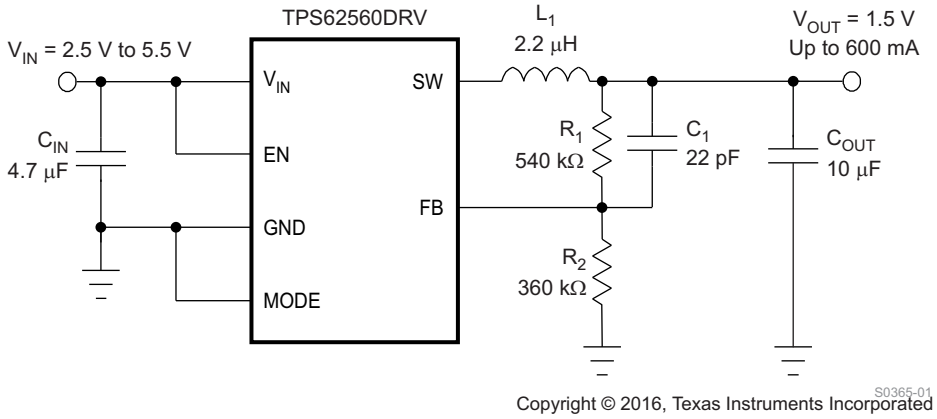


Figure 31. TPS62560 Adjustable 1.5-V Output

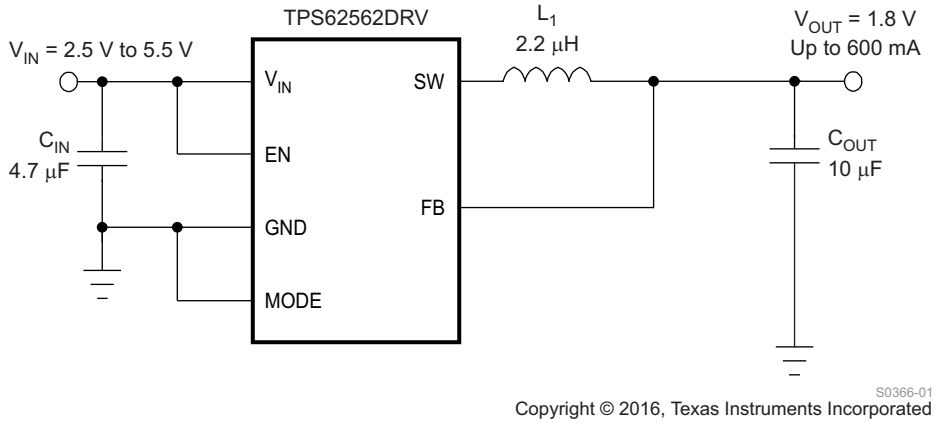


Figure 32. TPS62562 Fixed 1.8-V Output

10 Power Supply Recommendations

The TPS6226x device has no special requirements for its input power supply. The input power supply output current must be rated according to the supply voltage, output voltage, and output current of the TPS6226x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND pin of the device to the exposed thermal pad of the PCB and use this pad as a star point. Use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the exposed thermal pad (star point) underneath the IC. Keep the common path to the GND pin, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected right to the output capacitor and routed away from noisy components and traces (for example, the SW line).

11.2 Layout Examples

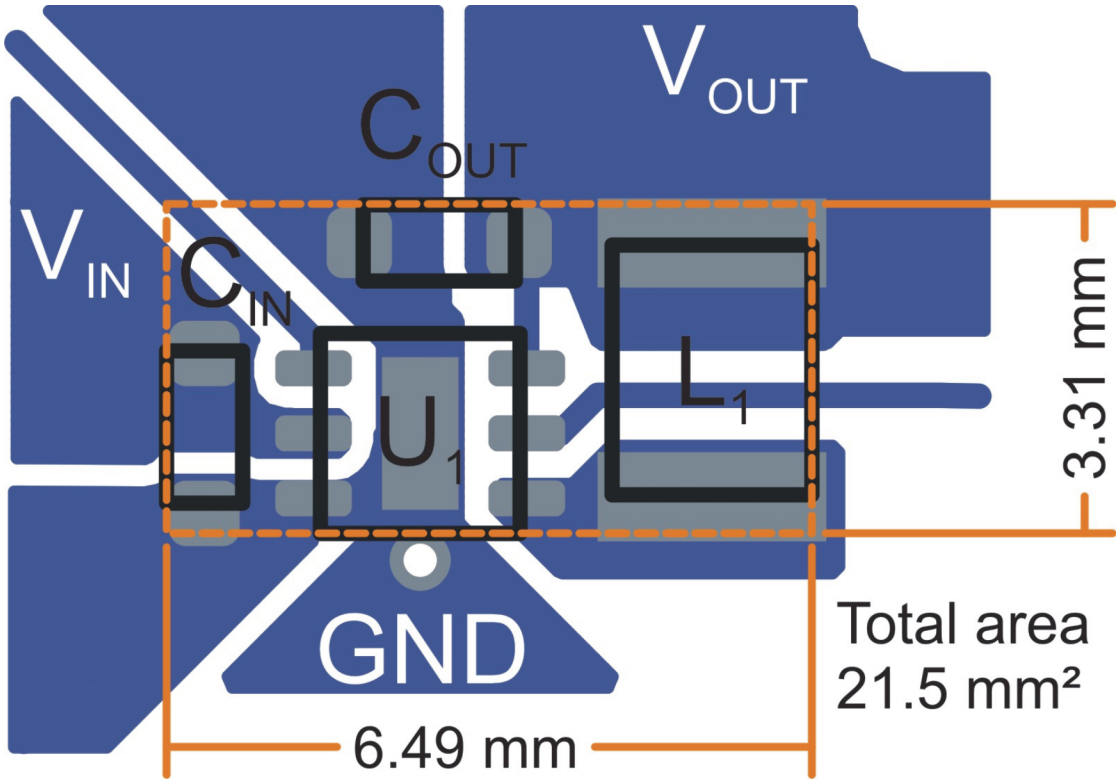


Figure 33. Suggested Layout for Fixed-Output-Voltage Options

Layout Examples (continued)

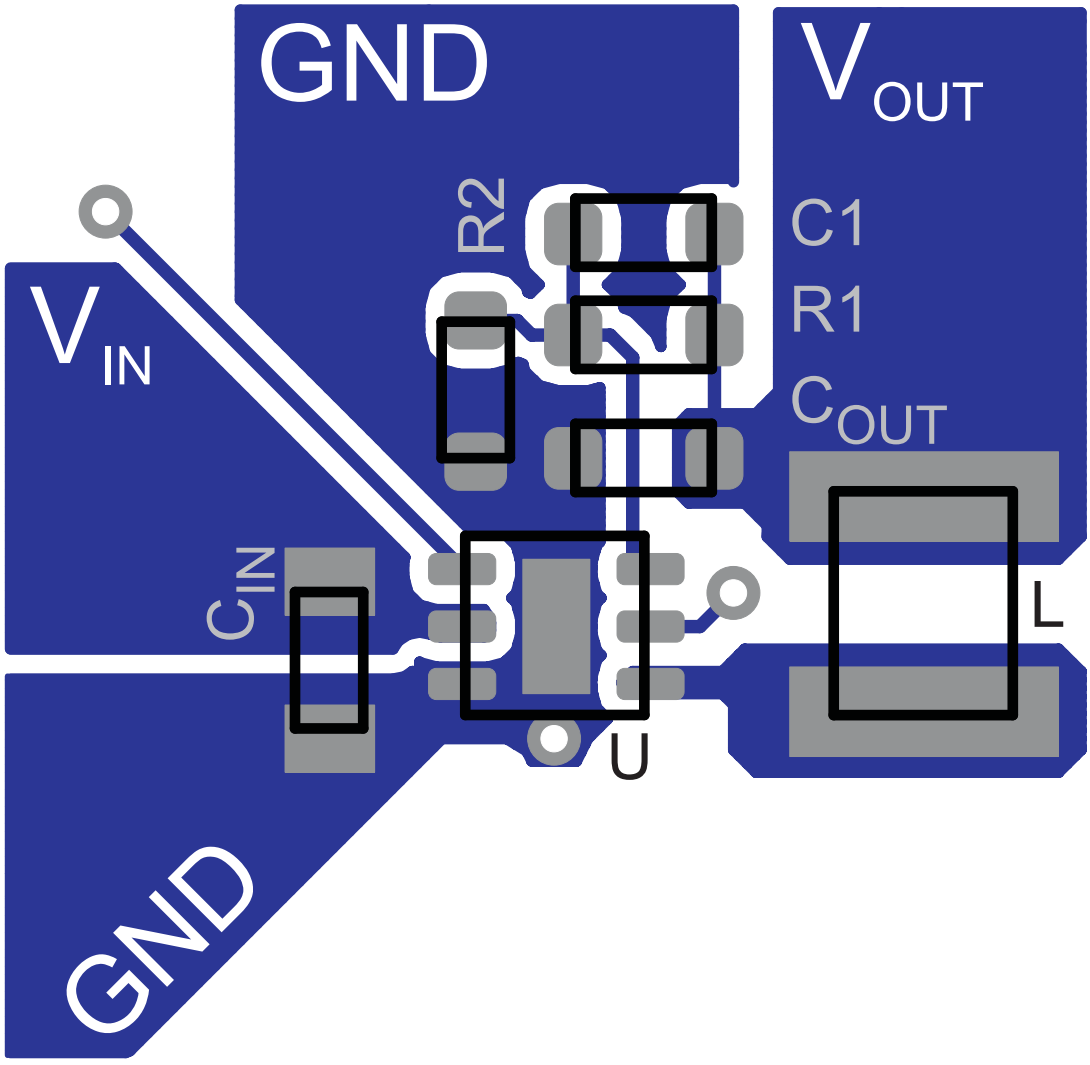


Figure 34. Suggested Layout for Adjustable-Output-Voltage Version

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **3.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS62560	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62561	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62562	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62560DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY	Samples
TPS62560DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CEY	Samples
TPS62561DDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO	Samples
TPS62561DDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVO	Samples
TPS62562DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXT	Samples
TPS62562DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	NXT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

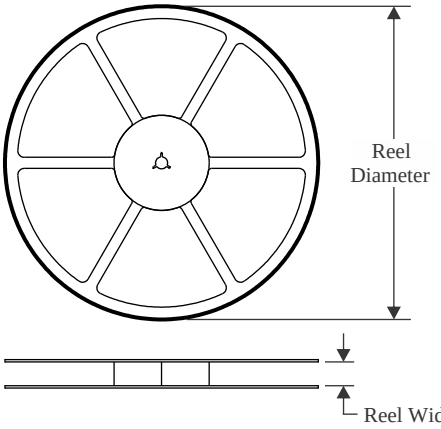
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

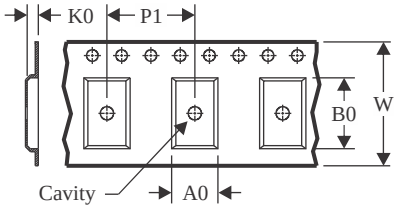
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

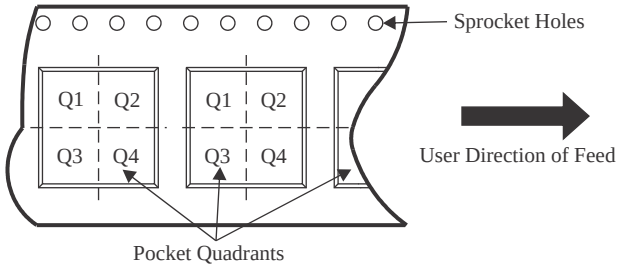


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

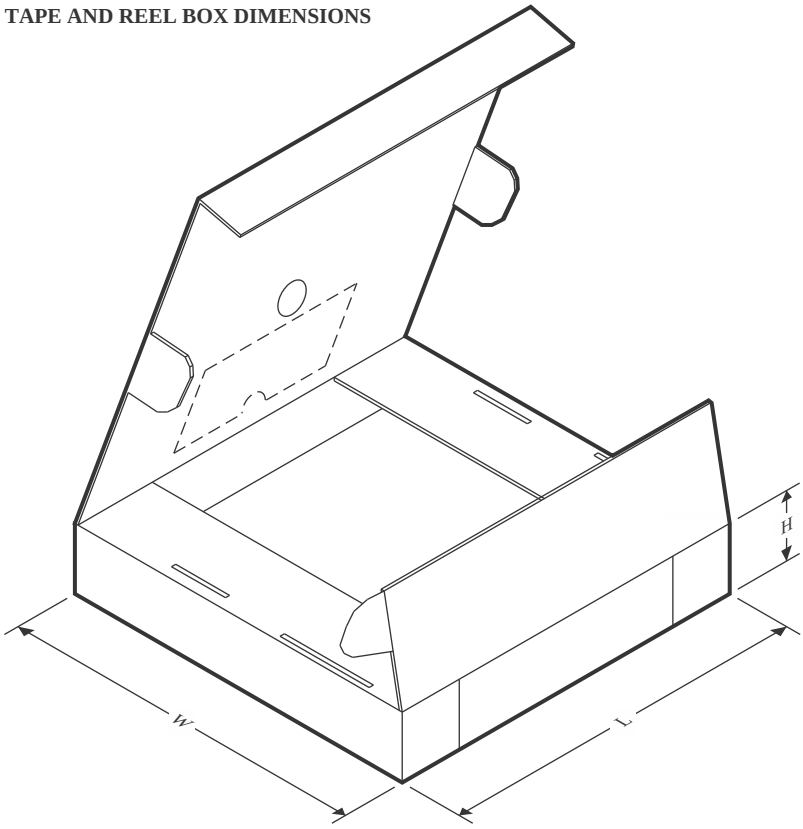
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62560DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62560DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS62561DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62561DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

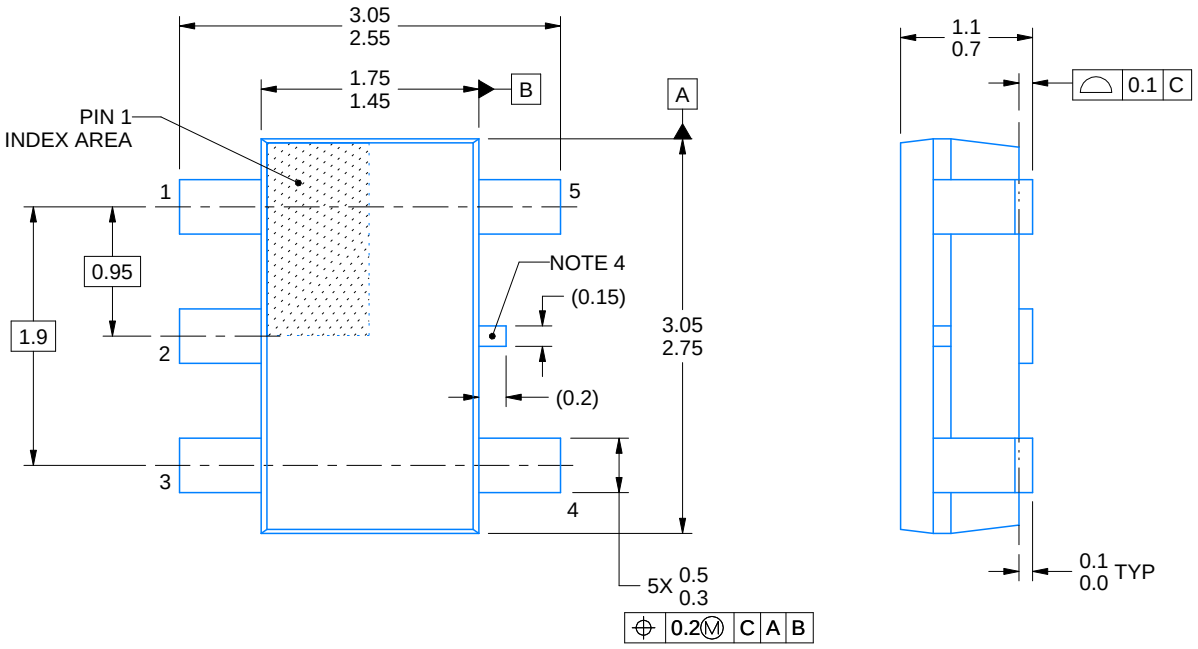
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62560DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS62560DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS62561DDCR	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS62561DDCT	SOT-23-THIN	DDC	5	250	200.0	183.0	25.0

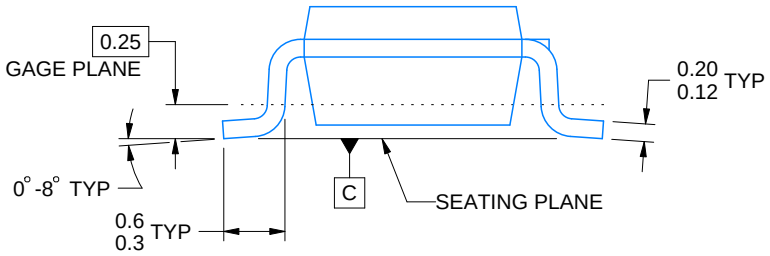
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

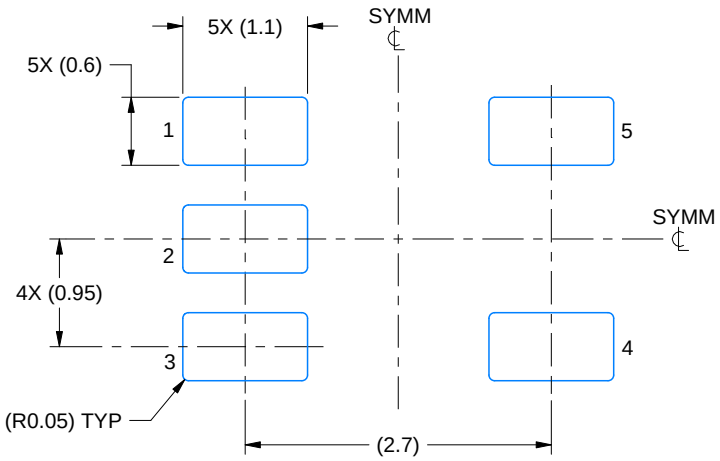




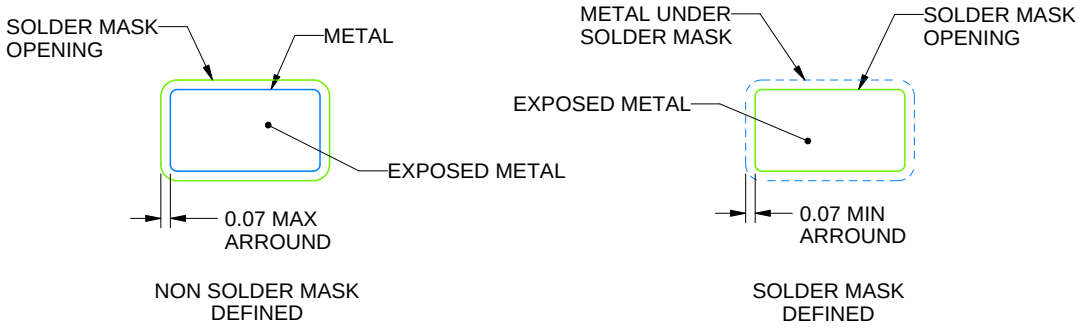
4220752/A 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

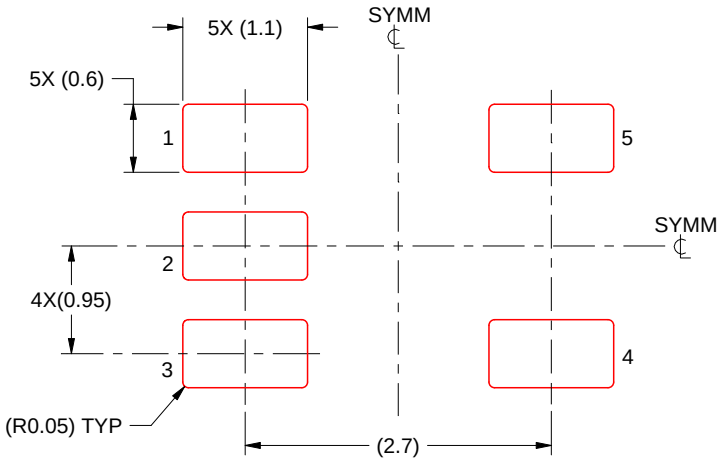


SOLDERMASK DETAILS

4220752/A 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

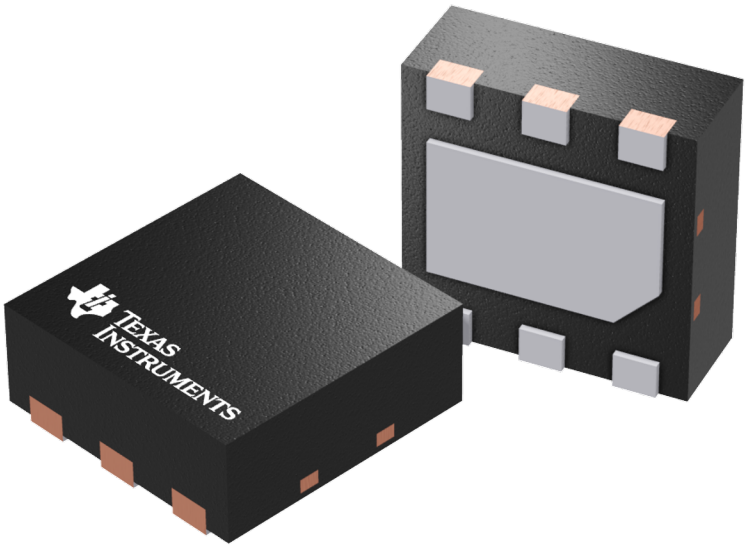
4220752/A 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



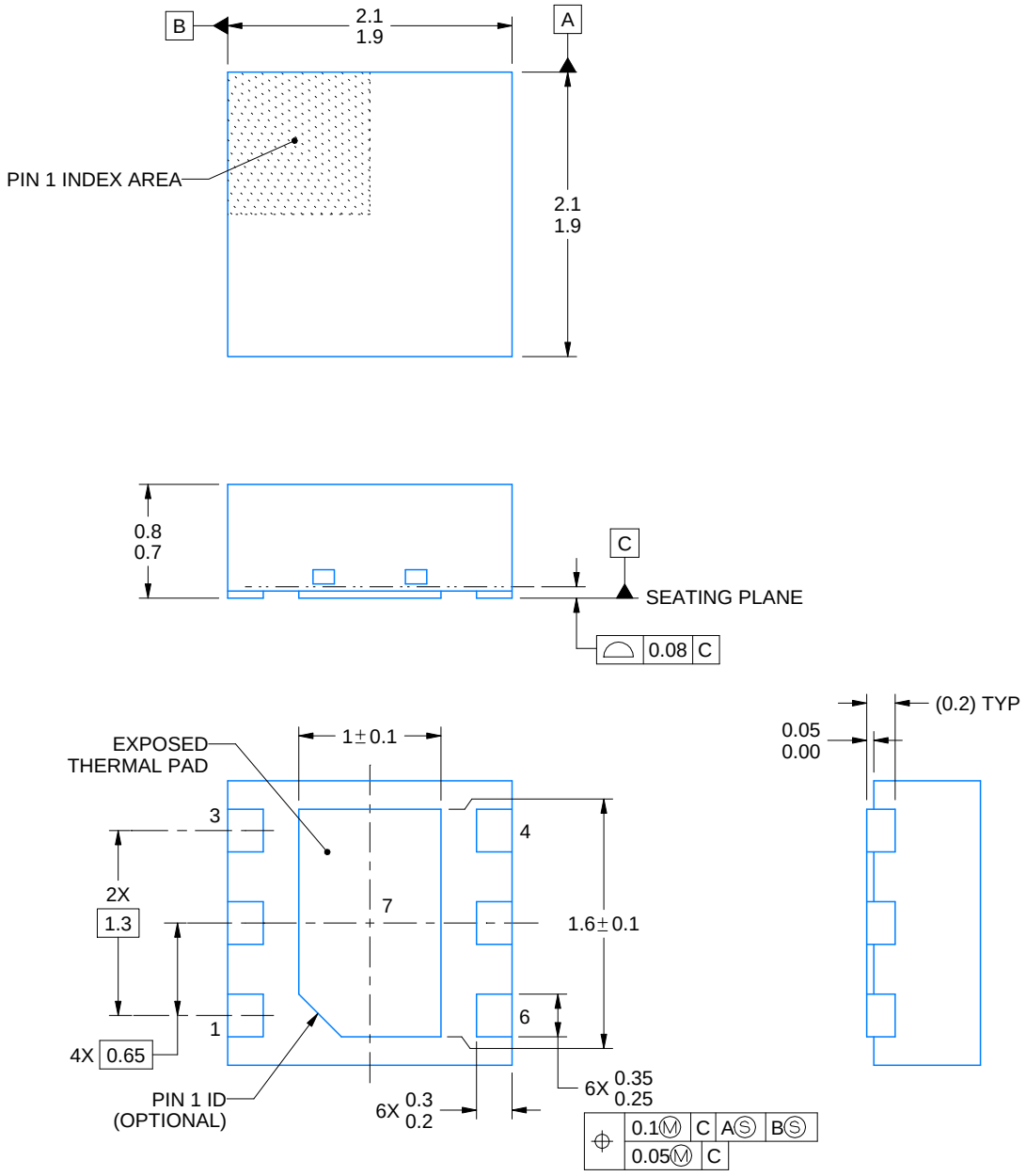
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

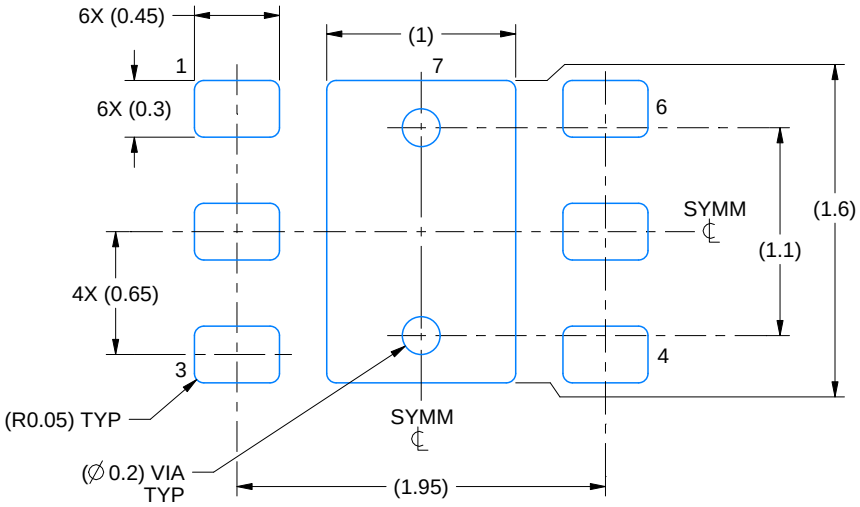
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

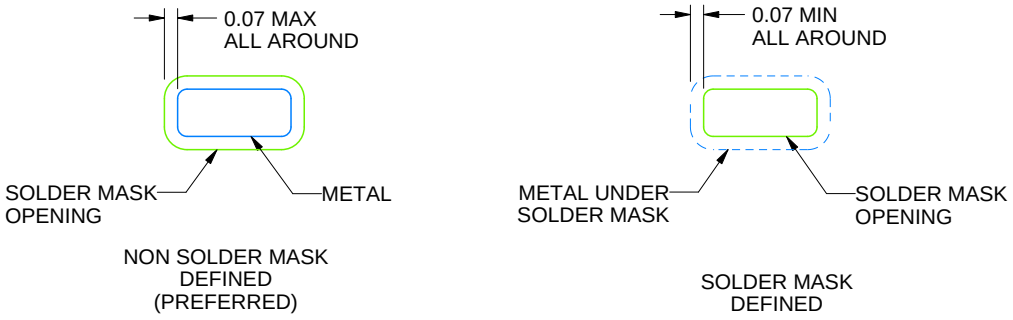


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

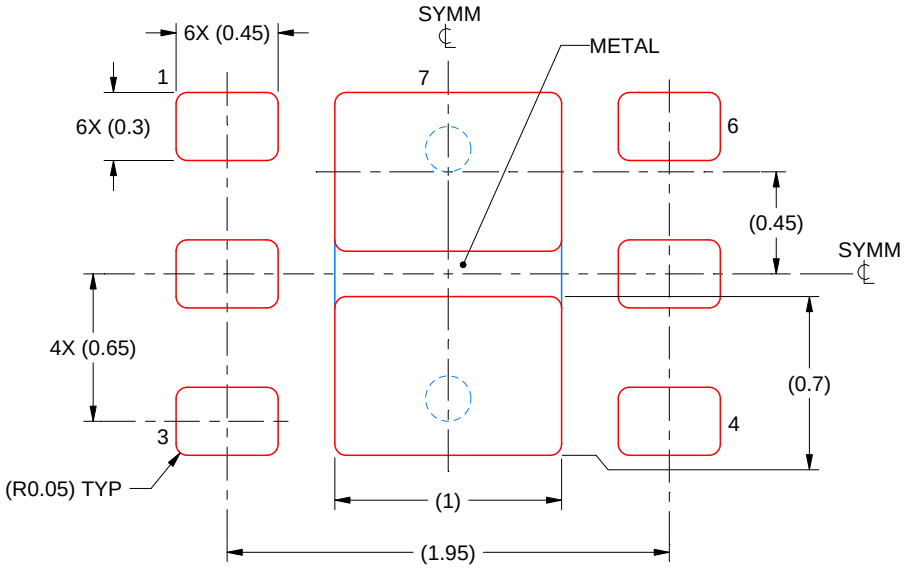
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

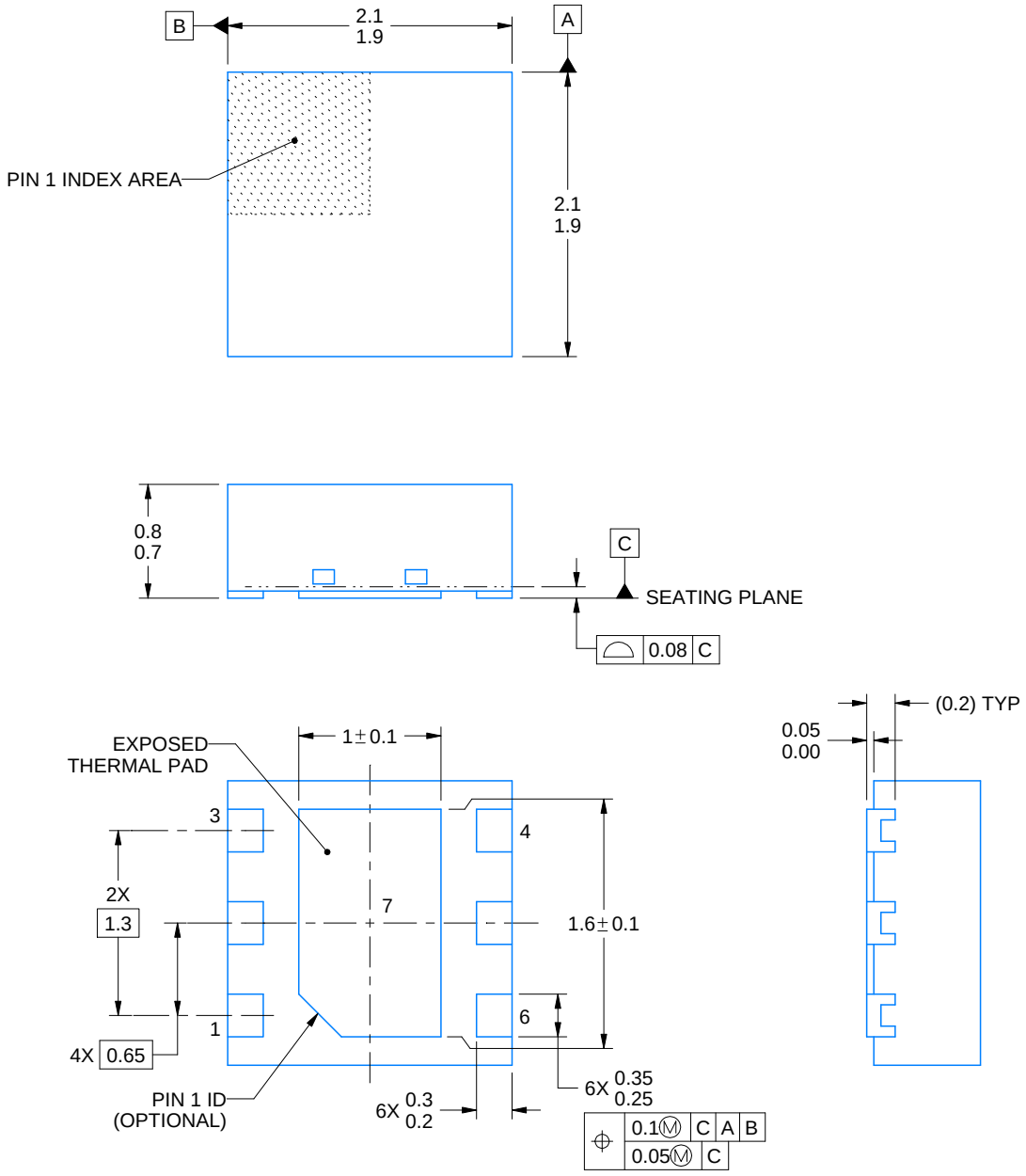
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

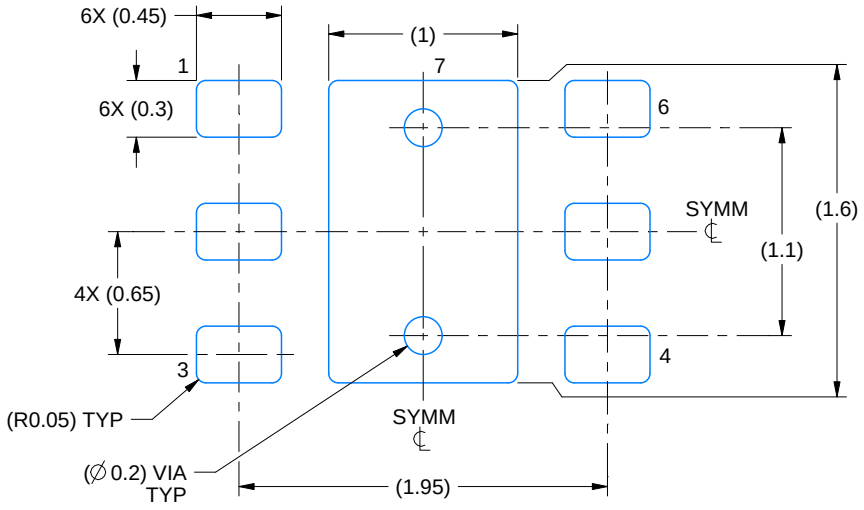
PLASTIC SMALL OUTLINE - NO LEAD



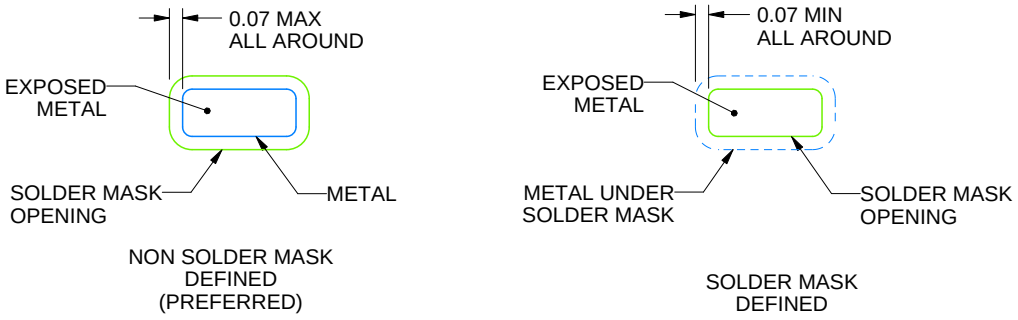
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

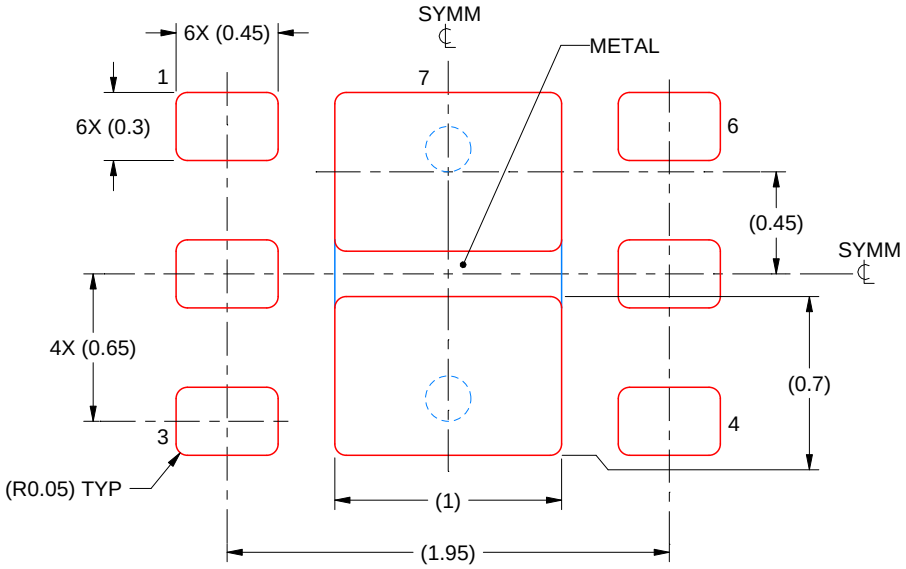


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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