TPS5401 0.5-A, 42-V Input, Step-Down Converter

1 Features

- 3.5-V to 42-V Input Voltage Range
- 200-mΩ High-Side MOSFET
- High Efficiency at Light Loads With a Pulse-Skipping Eco-mode™ Control Scheme
- 116-µA Operating Quiescent Current
- 1.3-µA Shutdown Current
- 100-kHz to 2.5-MHz Switching Frequency
- Synchronizes to External Clock
- Adjustable Slow Start/Sequencing
- UV and OV Power-Good Output
- Adjustable UVLO Voltage and Hysteresis
- 0.8-V ±3.5% Internal Voltage Reference
- MSOP10 With PowerPAD™ Package
- Supported by WEBENCH

2 Applications

- 12-V and 24-V Industrial and Commercial Low-Power Systems
- E-Meters

3 Description

The TPS5401 device is a 42-V, 0.5-A, step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the supply current to 116 µA when outputting regulated voltage with no load. Using the enable pin, shutdown supply current is reduced to 1.3 µA when the enable pin is low.

Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The output voltage start-up ramp is controlled by the slow-start pin that can also be configured for sequencing/tracking. An open-drain power-good signal indicates the output is within 94% to 107% of its nominal voltage.

A wide switching-frequency range allows efficiency and external component size optimization. Frequency foldback and thermal shutdown protect the part during an overload condition.

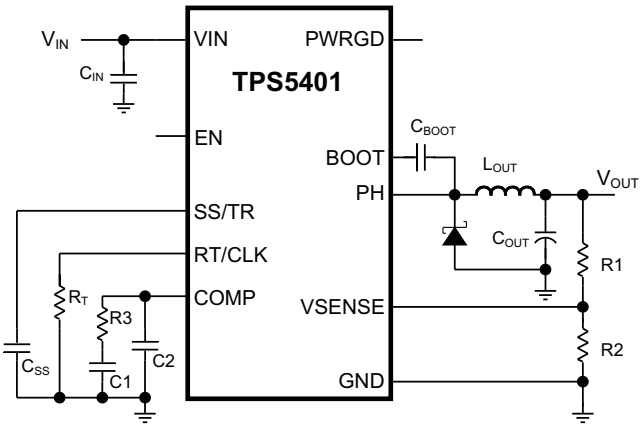
The TPS5401 is available in a 10-pin thermally enhanced MSOP PowerPAD package.

Device Information(1)

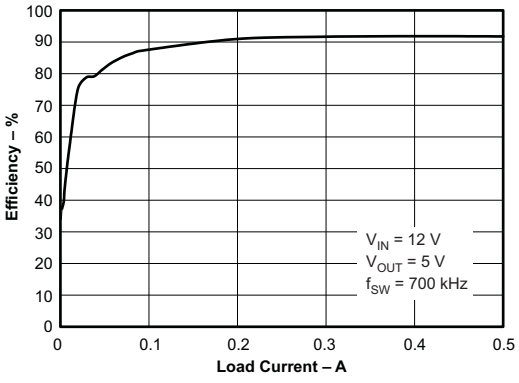
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS5401	MSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency vs. Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2010) to Revision B — **Page**

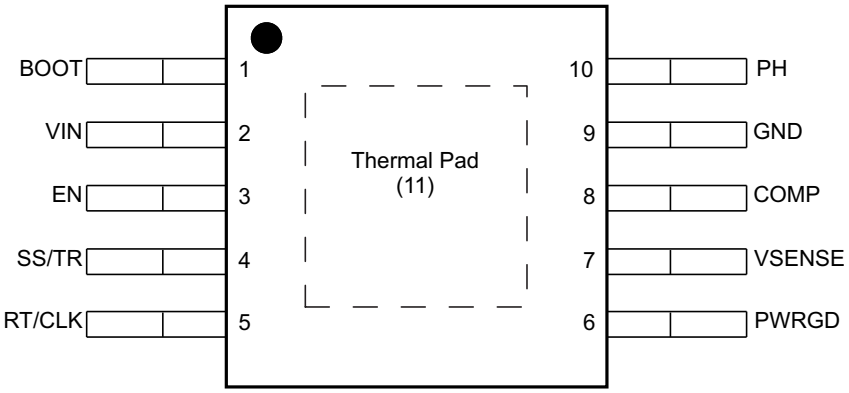
- Deleted SWIFT™ from the data sheet title ... 1
- Deleted Features: "For SWIFT™ Power Products Documentation, see http://www.ti.com/swift ... 1
- Moved the Storage temperature range to the *Absolute Maximum Ratings* ... 4
- Changed the *Handling Ratings* table To: *ESD Ratings* ... 4

Changes from Original (December 2010) to Revision A — **Page**

- Added, updated, or renamed the following sections: Device Information Table, *Application and Implementation*; *Power Supply Recommendations*; *Layout*; *Device and Documentation Support*; *Mechanical, Packaging, and Ordering Information* ... 1

5 Pin Configuration and Functions

DGQ Package
10-Pin MSOP with PowerPAD™
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
GND	9	–	Ground
PH	10	O	The source of the internal high-side power MOSFET
PWRGD	6	O	An open-drain output; asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage or EN shutdown.
RT/CLK	5	I	Resistor timing and external clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high-impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor-set function.
SS/TR	4	I	Slow-start and tracking. An external capacitor connected to this pin sets the output rise time. Because the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
V_{IN}	2	I	Input supply voltage, 3.5 V to 42 V.
VSENSE	7	I	Inverting node of the transconductance (gm) error amplifier.
Thermal pad	(11)	–	GND pin must be electrically connected to the thermal pad on the printed circuit board for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	47	V
	EN	–0.3	5	
	BOOT		55	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	BOOT – PH		8	V
	PH	–0.6	47	
	PH, 10-ns transient	–2	47	
Voltage difference	Thermal pad to GND		±200	mV
Source current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH	Current limit		A
	RT/CLK		100	µA
Sink current	VIN	Current limit		A
	COMP		100	µA
	PWRGD		10	mA
	SS/TR		200	µA
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	÷500	

(1) JEDEC document JEP155 states that 1000-V HBM allows safe manufacturing with a standard ESD control process. QSS 009-105 (JESD22-A114A)
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. QSS 009-147 (JESD22-C101B.01)

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Operating input voltage on the VIN pin	3.5		42	V
T_J	Operating junction temperature	–40		150	°C
	Output voltage	0.8		39	V
	Output current	0		0.5	A

6.4 Thermal Information

THERMAL METRIC[1]		DGQ	UNIT
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	48.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	38.2	
ψ_{JT}	Junction-to-top characterization parameter	2.0	
ψ_{JB}	Junction-to-board characterization parameter	37.9	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	13.6	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN} = 3.5 V to 42 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	Operating input voltage		3.5		42	V
	Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
	Shutdown supply current	V_{EN} = 0 V		1.3	4	µA
	Operating: nonswitching supply current	V_{VSENSE} = 0.83 V, V_{IN} = 12 V, 25°C		116	136	µA
ENABLE AND UVLO (EN PIN)						
	Enable threshold voltage	No voltage hysteresis, rising and falling, 25°C	0.9	1.25	1.55	V
	Input current	Enable threshold 50 mV		–3.8		µA
		Enable threshold –50 mV		–0.9		µA
	Hysteresis current			–2.9		µA
VOLTAGE REFERENCE						
V_{ref}	Voltage reference		0.772	0.8	0.828	V
HIGH-SIDE MOSFET						
	On-resistance	V_{IN} = 3.5 V, $V_{BOOT} – V_{PH}$ = 3 V		300		mΩ
		V_{IN} = 12 V, $V_{BOOT} – V_{PH}$ = 6 V		200	410	mΩ
ERROR AMPLIFIER						
	Input current			50		nA
gm_{EA}	Error amplifier transconductance	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		97		µMhos
	Error amplifier transconductance during slow-start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		26		µMhos
	Error amplifier dc gain	V_{VSENSE} = 0.8 V		10,000		V/V
	Error amplifier bandwidth			2700		kHz
	Error amplifier source/sink	V_{COMP} = 1 V, 100 mV overdrive		±7		µA
gm_{PS}	COMP to switch current transconductance			1.9		A/V
CURRENT LIMIT						
	Current limit threshold	V_{IN} = 12 V, T_J = 25°C	0.6	0.94		A
THERMAL SHUTDOWN						
	Thermal shutdown			182		°C

Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 3.5 V to 42 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching-frequency range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	581	720	kHz
	Switching-frequency range using CLK mode		300		2200	kHz
	Minimum CLK input pulse width			40		ns
	RT/CLK high threshold			1.9	2.2	V
	RT/CLK low threshold		0.5	0.7		V
	RT/CLK falling edge to PH rising edge delay	Measured at 500 kHz with R_T resistor in series		60		ns
	PLL lock-in time	Measured at 500 kHz		100		µs
SLOW-START AND TRACKING (SS/TR PIN)						
	Charge current	$V_{SS/TR}$ = 0.4 V		2		µA
	SS/TR-to-VSENSE matching	$V_{SS/TR}$ = 0.4 V		45		mV
	SS/TR-to-reference crossover	98% nominal		1		V
	SS/TR discharge current (overload)	VSENSE = 0 V, $V_{SS/TR}$ = 0.4 V		112		µA
	SS/TR discharge voltage	V_{VSENSE} = 0 V		54		mV
POWER GOOD (PWRGD PIN)						
	VSENSE low threshold	V_{VSENSE} falling		92%		V_{ref}
		V_{VSENSE} rising		94%		
	VSENSE high threshold	V_{VSENSE} rising		109%		V_{ref}
		V_{VSENSE} falling		107%		
	Hysteresis	V_{VSENSE} falling		2%		
	Output-high leakage	V_{VSENSE} = V_{ref}, V_{PWRGD} = 5.5 V, 25°C		10		nA
	On-resistance	I_{PWRGD} = 3 mA, V_{VSENSE} < 0.77 V		50		Ω
	Minimum V_{IN} for defined output	V_{PWRGD} < 0.5 V, I_{PWRGD} = 100 µA		0.95	1.5	V

6.6 Typical Characteristics

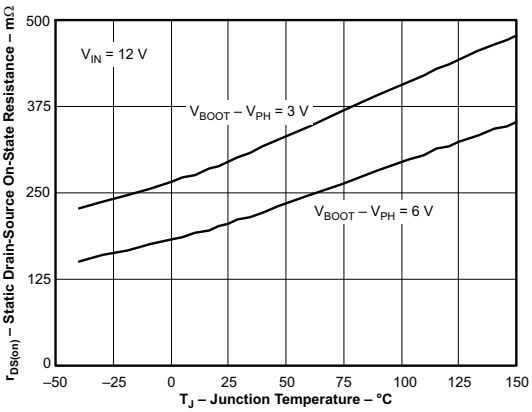


Figure 1. On-resistance vs Junction Temperature

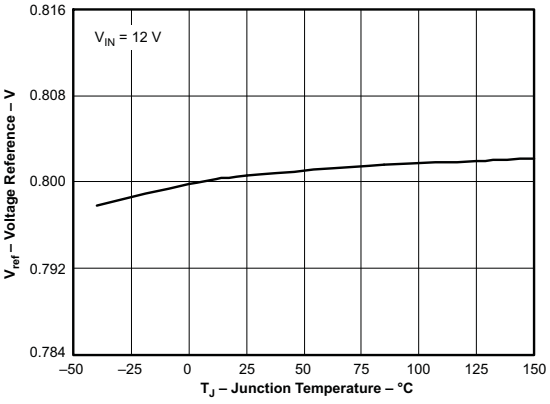


Figure 2. Voltage Reference vs Junction Temperature

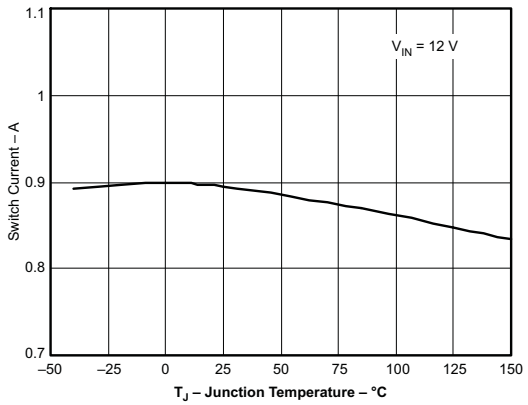


Figure 3. Switch-current Limit vs Junction Temperature

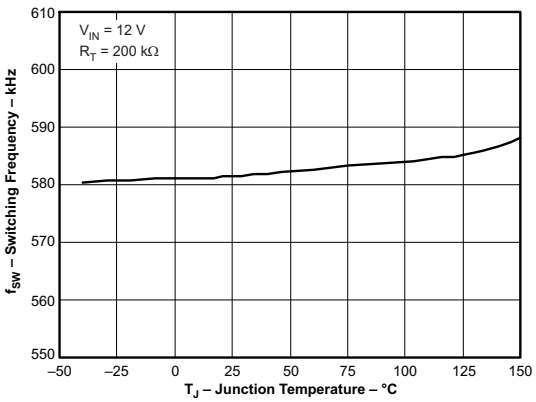


Figure 4. Switching Frequency vs Junction Temperature

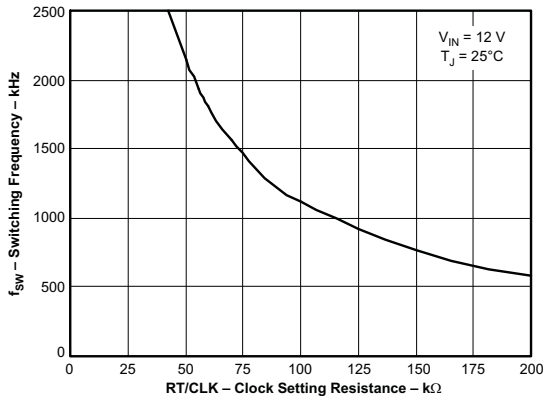


Figure 5. Switching Frequency vs RT/CLK Resistance High-frequency Range

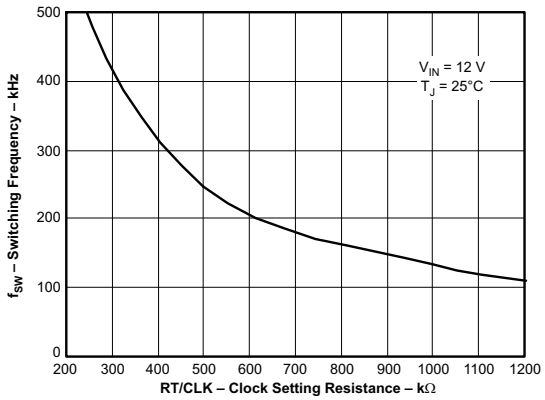


Figure 6. Switching Frequency vs RT/CLK Resistance Low-frequency Range

Typical Characteristics (continued)

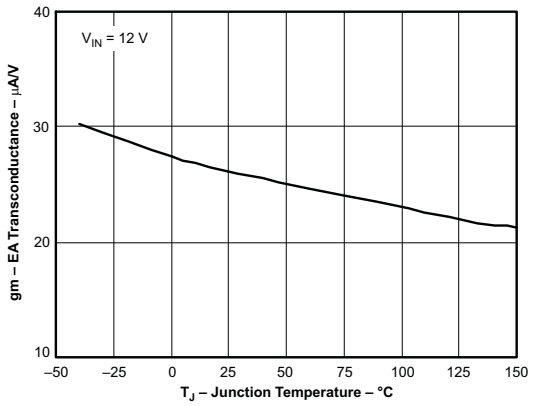


Figure 7. EA Transconductance During Slow-start vs Junction Temperature

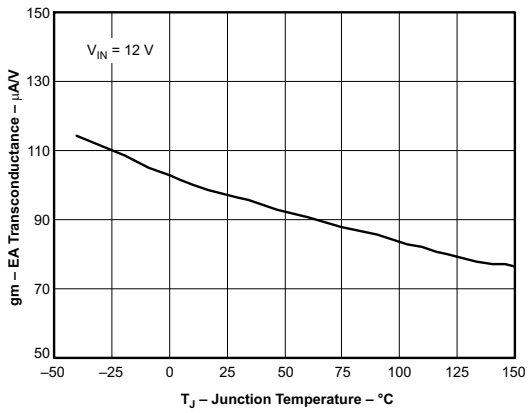


Figure 8. EA Transconductance vs Junction Temperature

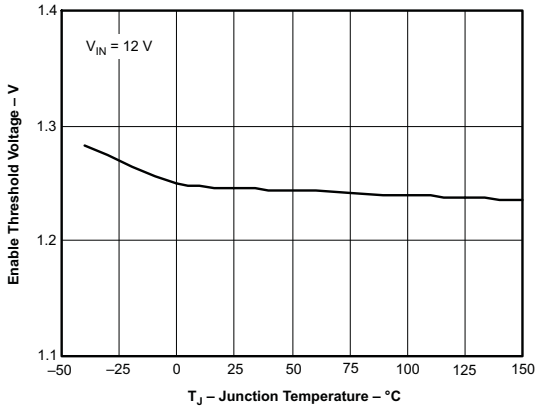


Figure 9. Enable Threshold Voltage vs Junction Temperature

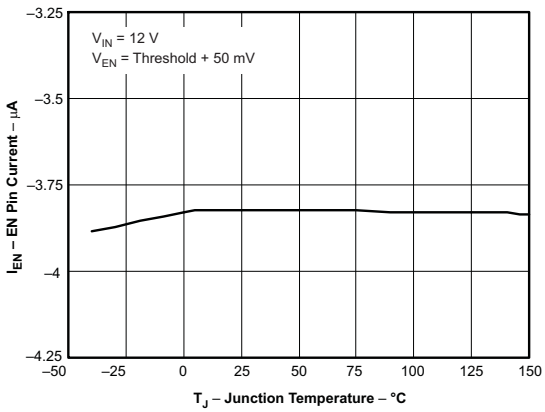


Figure 10. EN Pin Current vs Junction Temperature

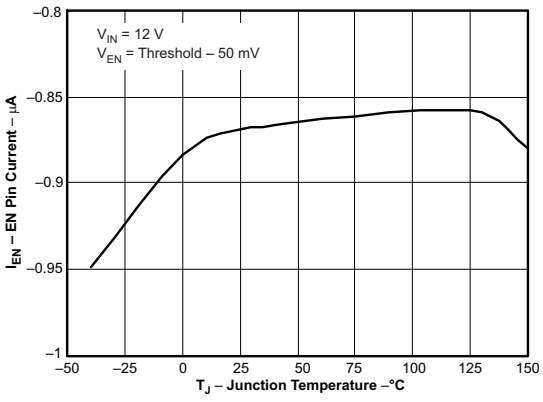


Figure 11. EN Pin Current vs Junction Temperature

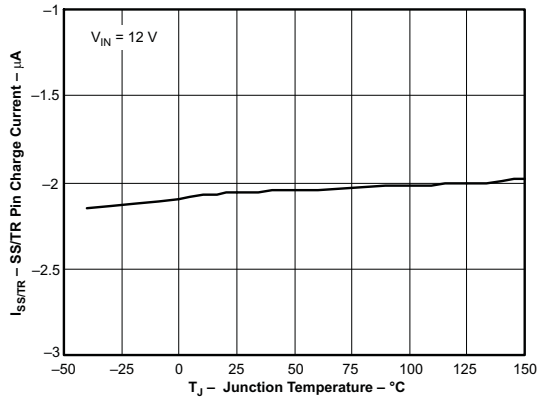


Figure 12. SS/TR Charge Current vs Junction Temperature

Typical Characteristics (continued)

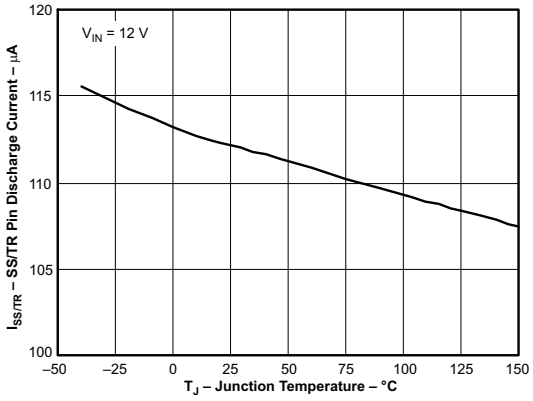


Figure 13. SS/TR Discharge Current vs Junction Temperature

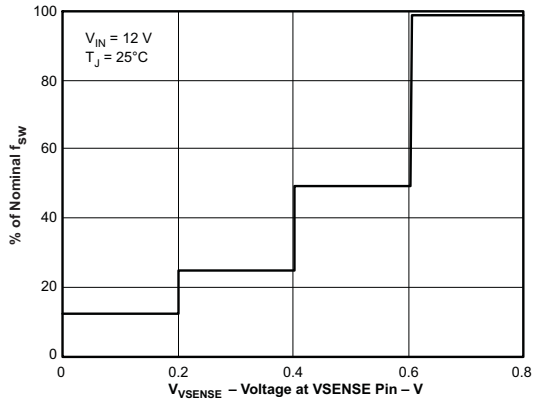


Figure 14. Switching Frequency vs V_{SENSE}

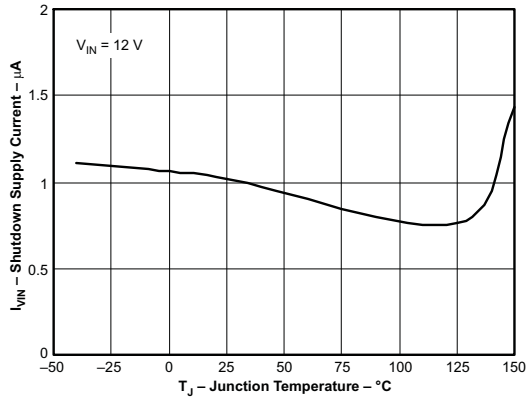


Figure 15. Shutdown Supply Current vs Junction Temperature

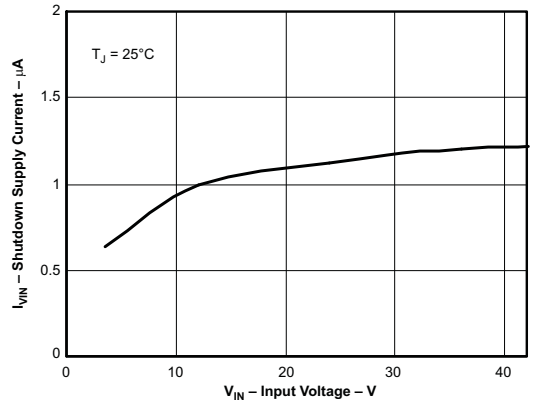


Figure 16. Shutdown Supply Current vs Input Voltage

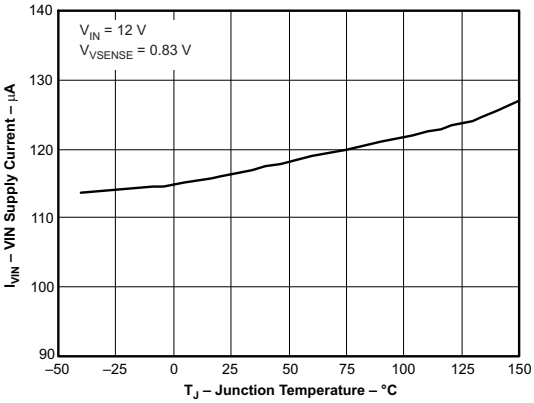


Figure 17. V_{IN} Supply Current vs Junction Temperature

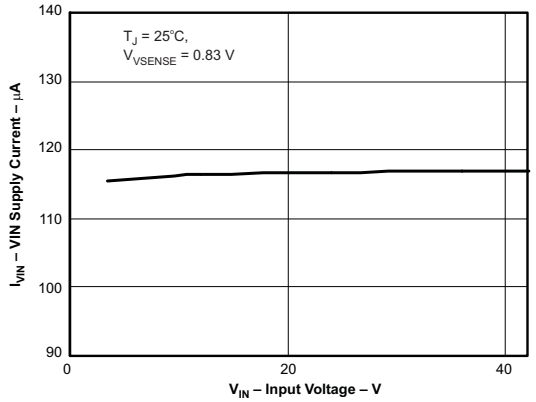


Figure 18. V_{IN} Supply Current vs Input Voltage

Typical Characteristics (continued)

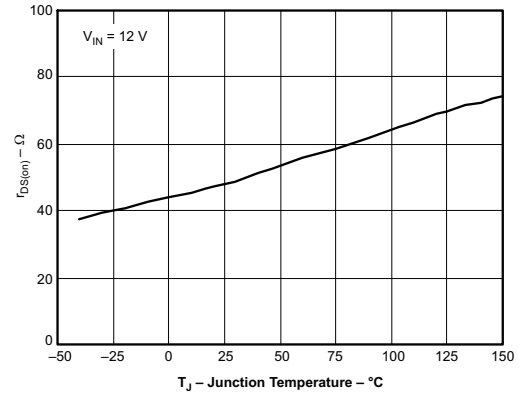


Figure 19. PWRGD On-resistance vs Junction Temperature

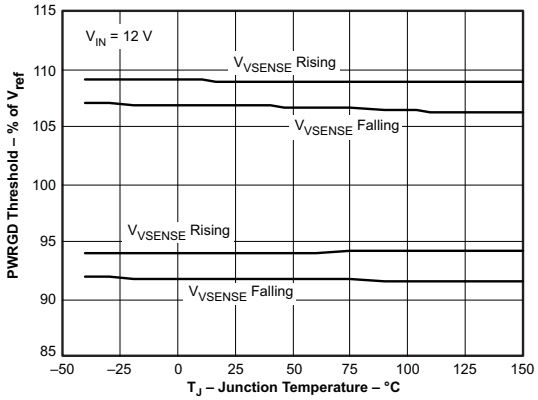


Figure 20. PWRGD Threshold vs Junction Temperature

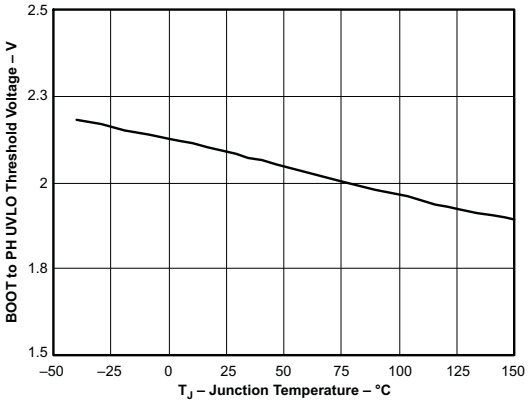


Figure 21. Boot to PH UVLO Threshold vs Junction Temperature

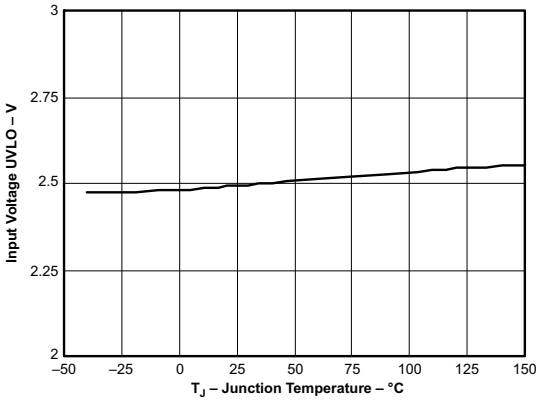


Figure 22. Input Voltage UVLO vs Junction Temperature

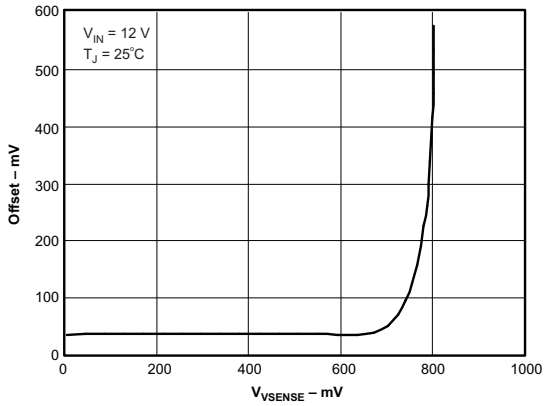


Figure 23. SS/TR to VSENSE Offset vs V_{SENSE} Voltage

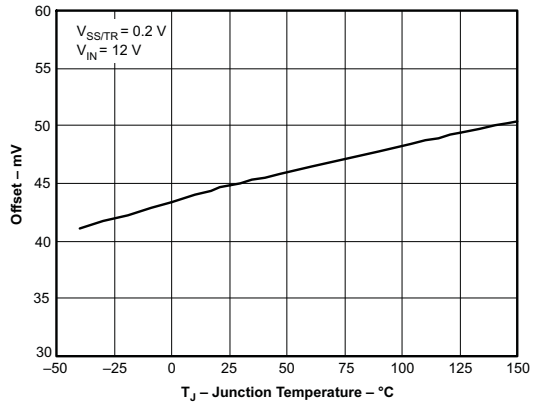


Figure 24. SS/TR to VSENSE Offset vs Temperature

7 Detailed Description

7.1 Overview

The TPS5401 device is a 42-V, 0.5-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency, current-mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching-frequency range of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase-lock loop (PLL) on the RT/CLK pin that is used to synchronize the power-switch turnon to a falling edge of an external system clock.

The TPS5401 device has a default start-up voltage of approximately 2.5 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) threshold with two external resistors. In addition, the pullup current provides a default condition. When the EN pin is floating, the device operates. The operating current is 116 µA when not switching and under no load. When the device is disabled, the supply current is 1.3 µA.

The integrated 200-mΩ high-side MOSFET allows for high-efficiency power-supply designs capable of delivering 0.5 amperes of continuous current to a load. The TPS5401 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor from the BOOT pin to the PH pin. The boot capacitor voltage is monitored by a UVLO circuit and turns the high-side MOSFET off when the boot voltage falls below a preset threshold. The TPS5401 can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8-V reference.

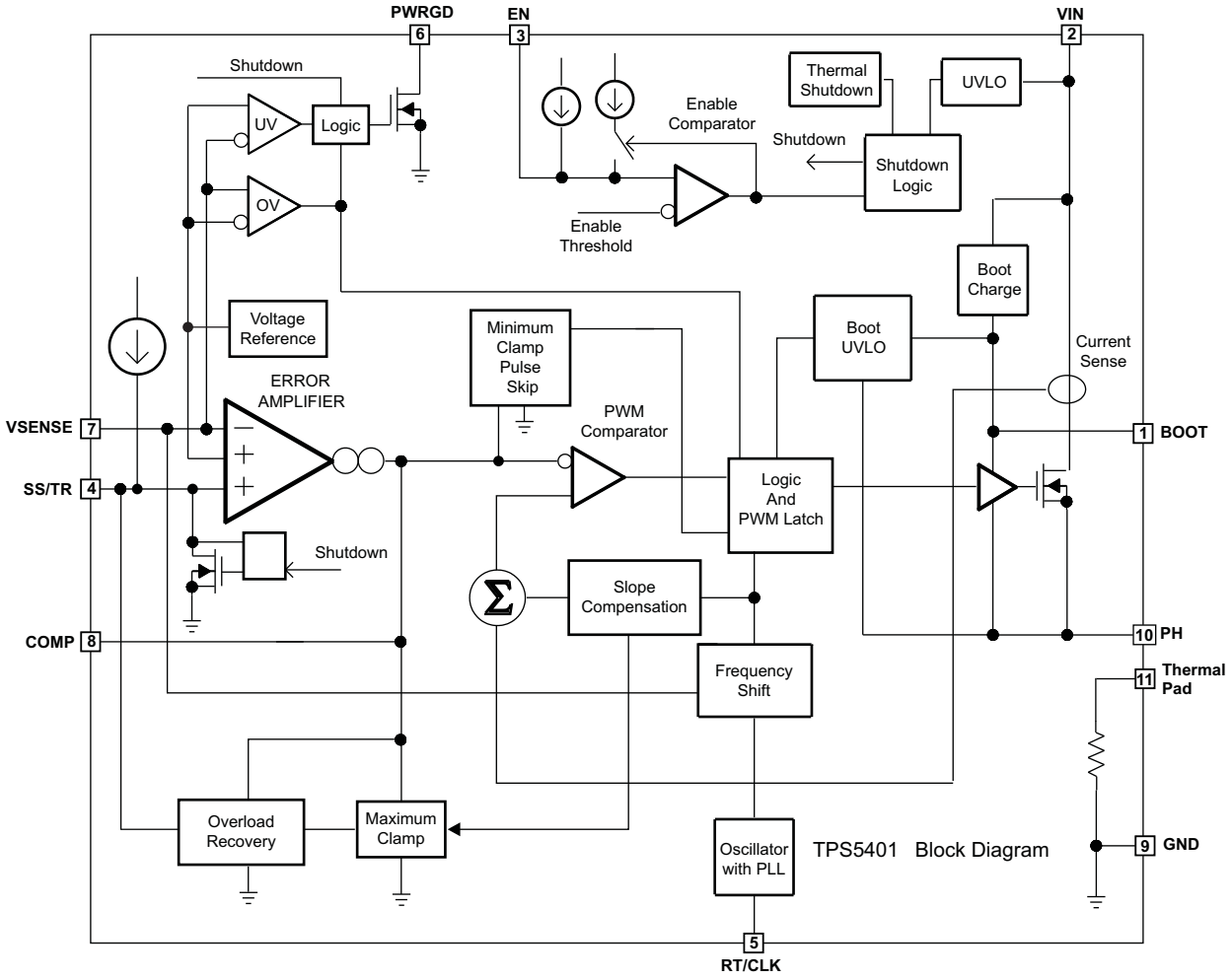
The TPS5401 has a power-good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open-drain output which deasserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage, allowing the pin to transition high when a pullup resistor is used.

The TPS5401 minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power-good comparator. When the OV comparator is activated, the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS/TR (slow-start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power up. A small-value capacitor should be coupled to the pin to adjust the slow-start time. A resistor divider can be coupled to the pin for critical power-supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an overtemperature fault, UVLO fault, or a disabled condition.

The TPS5401 also discharges the slow-start capacitor during overload conditions with an overload recovery circuit. The overload recovery circuit slow-starts the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency-foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help control the inductor current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS5401 uses an adjustable fixed-frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The error amplifier output is compared to the high-side power-switch current. When the power-switch current reaches the level set by the COMP voltage, the power switch is turned off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The Eco-mode control scheme is implemented with a minimum clamp on the COMP pin.

7.3.2 Slope Compensation Output Current

The TPS5401 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty-cycle range.

Feature Description (continued)

7.3.3 Low-Dropout Operation and Bootstrap Voltage (BOOT)

The TPS5401 has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low-side diode conducts. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve dropout, the TPS5401 device is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1 V. When the voltage from BOOT to PH drops below 2.1 V, the high-side MOSFET is turned off using an UVLO circuit, which allows the low-side diode to conduct and refresh the charge on the BOOT capacitor. Because the supply current sourced from the BOOT capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and printed circuit board resistance. During operating conditions in which the input voltage drops and the regulator is operating in continuous conduction mode, the high-side MOSFET can remain on for 100% of the duty cycle to maintain output regulation, until the BOOT-to-PH voltage falls below 2.1 V.

Attention must be taken in maximum-duty-cycle applications which experience extended time periods with light loads or no load. When the voltage across the BOOT capacitor falls below the 2.1-V UVLO threshold, the high-side MOSFET is turned off, but there may not be enough inductor current to pull the PH pin down to recharge the BOOT capacitor. The high-side MOSFET of the regulator stops switching because the voltage across the BOOT capacitor is less than 2.1 V. The output capacitor then decays until the difference in the input voltage and output voltage is greater than 2.1 V, at which point the BOOT UVLO threshold is exceeded, and the device starts switching again until the desired output voltage is reached. This operating condition persists until the input voltage and/or the load current increases. It is recommended to adjust the VIN stop voltage greater than the BOOT UVLO trigger condition at the minimum load of the application using the adjustable VIN UVLO feature with resistors on the EN pin.

The start and stop voltages for typical 3.3-V and 5-V output applications are shown in Figure 25 and Figure 26. The voltages are plotted versus load current. The start voltage is defined as the input voltage needed to regulate the output voltage within 3.5%. The stop voltage is defined as the input voltage at which the output drops by 5% or stops switching.

During high-duty-cycle conditions, the inductor current ripple increases while the BOOT capacitor is being recharged, resulting in an increase in ripple voltage on the output. This is due to the recharge time of the boot capacitor being longer than the typical high-side off time, when switching occurs every cycle.

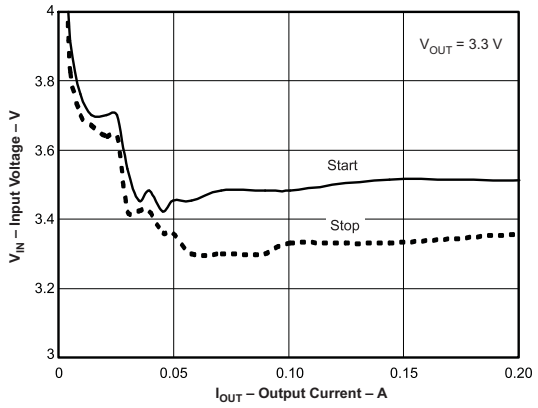


Figure 25. 3.3-V Start/Stop Voltage

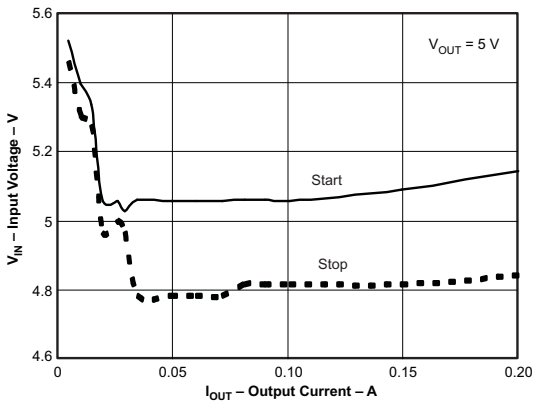


Figure 26. 5-V Start/Stop Voltage

Feature Description (continued)

7.3.4 Error Amplifier

The TPS5401 has a transconductance amplifier as the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 97 µA/V during normal operation. During the slow-start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the VSENSE pin is below 0.8 V and the device is regulating using the SS/TR voltage, the gm is 26 µA/V.

The frequency compensation components (series resistor and capacitor) are connected between the COMP pin and ground.

7.3.5 Voltage Reference

The voltage reference system produces a precise ±3.5% voltage reference over temperature by scaling the output of a temperature-stable bandgap circuit.

7.3.6 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with 10 kΩ for the R2 resistor and use Equation 1 to calculate R1. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator becomes more susceptible to noise, and voltage errors from the VSENSE input current become noticeable.

$$R1 = R2 \times \left(\frac{V_{OUT} - 0.8\ V}{0.8\ V} \right) \quad (1)$$

7.3.7 Enabling and Adjusting Undervoltage Lockout

The TPS5401 is disabled when the VIN pin voltage falls below 2.5 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 27 to adjust the input voltage UVLO by using the two external resistors. Though it is not necessary to use the UVLO adjust resistors, for operation it is highly recommended to provide consistent power-up behavior. The EN pin has an internal pullup current source, I_1, of 0.9 µA that provides the default condition of the TPS5401 operating when the EN pin floats. Once the EN pin voltage exceeds the enable threshold voltage (V_{ENA}) of 1.25 V, an additional 2.9 µA of hysteresis, I_{HYS}, is added. This additional current facilitates input-voltage hysteresis. Use Equation 2 to calculate R1 which sets the external hysteresis for the input voltage. Use Equation 3 to calculate R2 which sets the input start voltage.

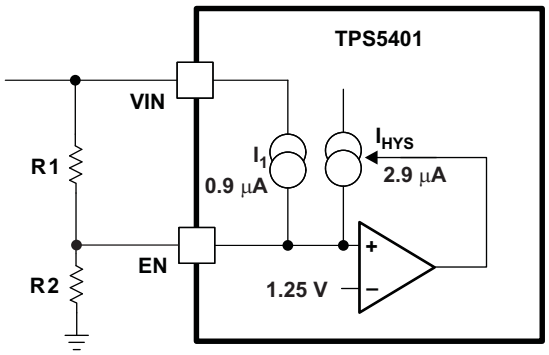


Figure 27. Adjustable Undervoltage Lockout (UVLO)

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \quad (3)$$

Feature Description (continued)

7.3.8 Slow-Start/Tracking Pin (SS/TR)

The TPS5401 effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the power-supply reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS5401 has an internal pullup current source of 2 µA that charges the external slow-start capacitor. The calculations for the slow-start time (10% to 90%) are shown in Equation 4. The voltage reference (V_{ref}) is 0.8 V and the slow-start current (I_{SS}) is 2 µA. The slow-start capacitor should remain lower than 0.47 µF and greater than 0.47 nF.

$$C_{ss}\ (nF) = \frac{t_{ss}\ (ms) \times I_{ss}\ (\mu A)}{V_{ref}\ (V) \times 0.8} \quad (4)$$

At power up, the TPS5401 does not start switching until the slow-start pin is discharged to less than 40 mV to ensure a proper power up; see Figure 28.

Also, during normal operation, the TPS5401 stops switching and SS/TR must be discharged to 40 mV when the VIN UVLO is exceeded, the EN pin is pulled below 1.25 V, or a thermal shutdown event occurs.

The VSENSE voltage follows the SS/TR pin voltage with a 45-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% of the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 1.7 V.

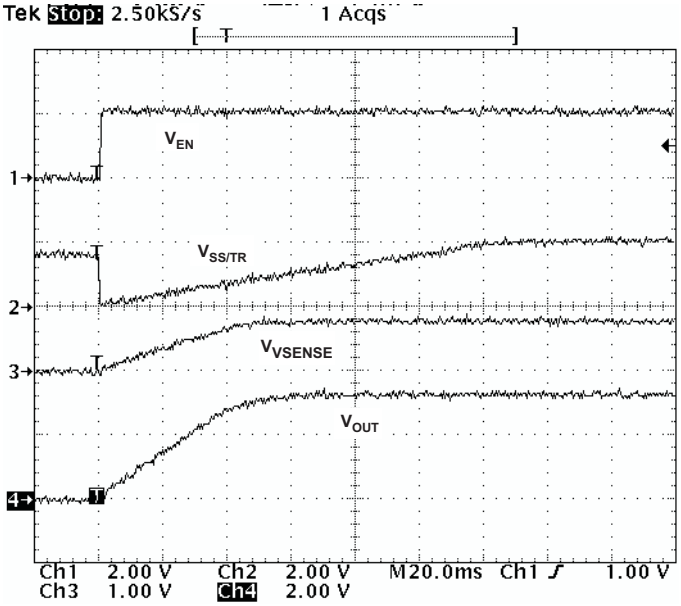


Figure 28. Operation of SS/TR Pin When Starting

7.3.9 Overload Recovery Circuit

The TPS5401 has an overload recovery (OLR) circuit. The OLR circuit slow-starts the output from the overload voltage to the nominal regulation voltage once the fault condition is removed. The OLR circuit discharges the SS/TR pin to a voltage slightly greater than the VSENSE pin voltage, using an internal pulldown of 100 µA when the error amplifier is changed to a high voltage from a fault condition. When the fault condition is removed, the output slow-starts from the fault voltage to nominal output voltage.

Feature Description (continued)

7.3.10 Sequencing

Many of the common power-supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins. The sequential method can be implemented using an open-drain output of a power-on-reset pin of another device. The sequential method is illustrated in Figure 29 using two TPS5401 devices. The power good is coupled to the EN pin on the TPS5401, which enables the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provides a 1-ms start-up delay. Figure 30 shows the results of Figure 29.

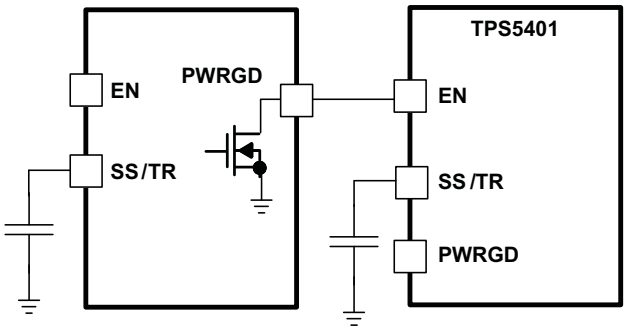


Figure 29. Schematic for Sequential Start-Up Sequence

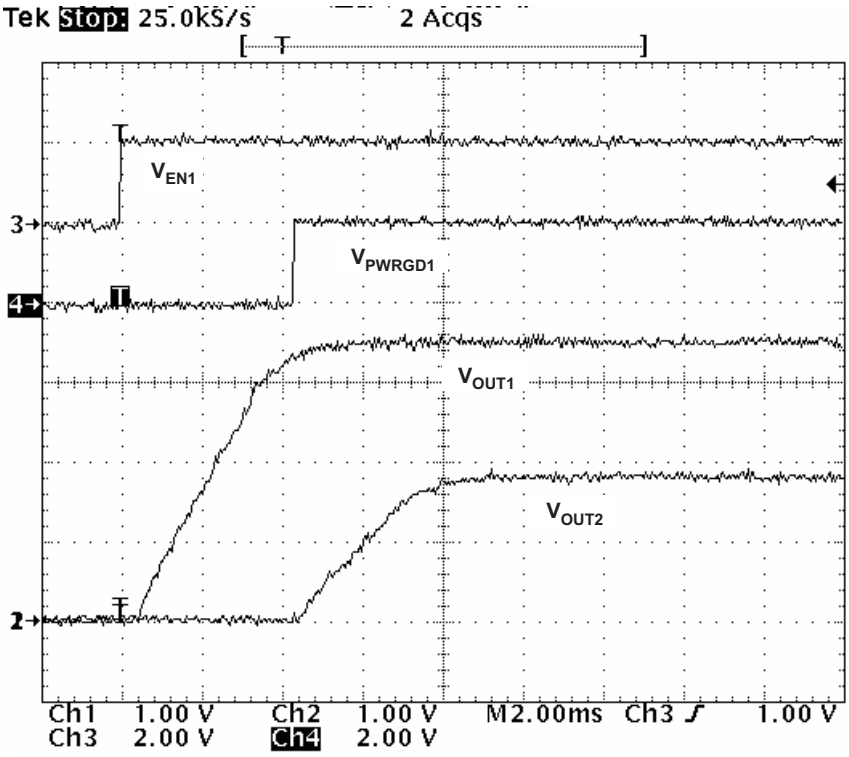


Figure 30. Sequential Start-Up Using EN and PWRGD

Feature Description (continued)

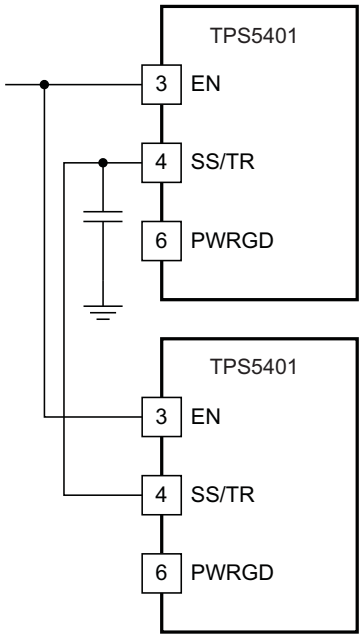


Figure 31. Schematic for Ratiometric Start-Up Sequence

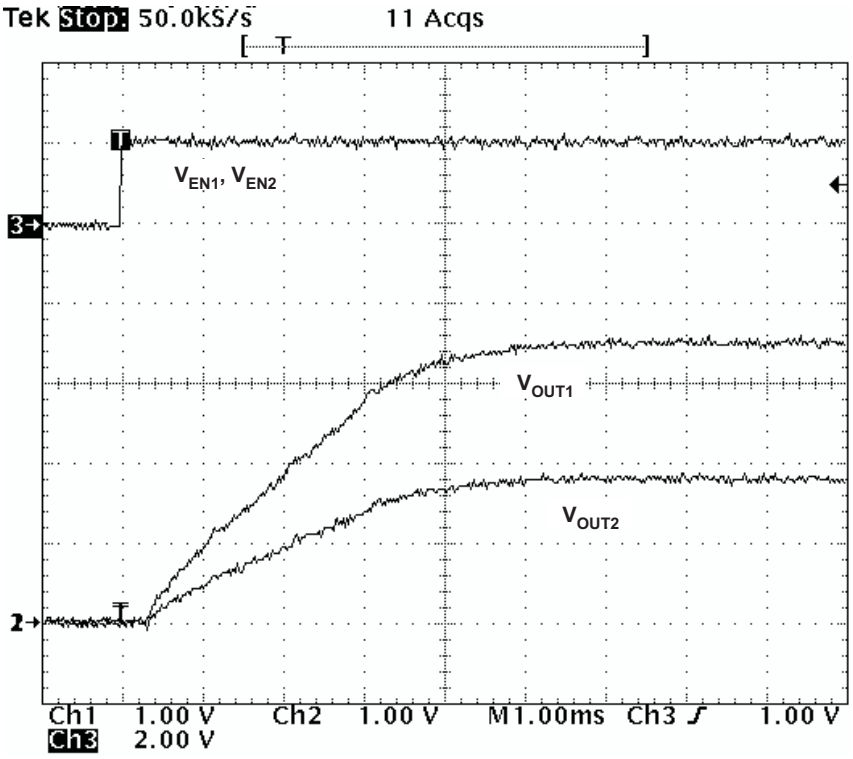


Figure 32. Ratiometric Start-Up Using Coupled SS/TR Pins

Feature Description (continued)

Figure 31 shows a method for ratiometric start-up sequence by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, the pullup current source must be doubled in Equation 4. Figure 32 shows the results of Figure 31.

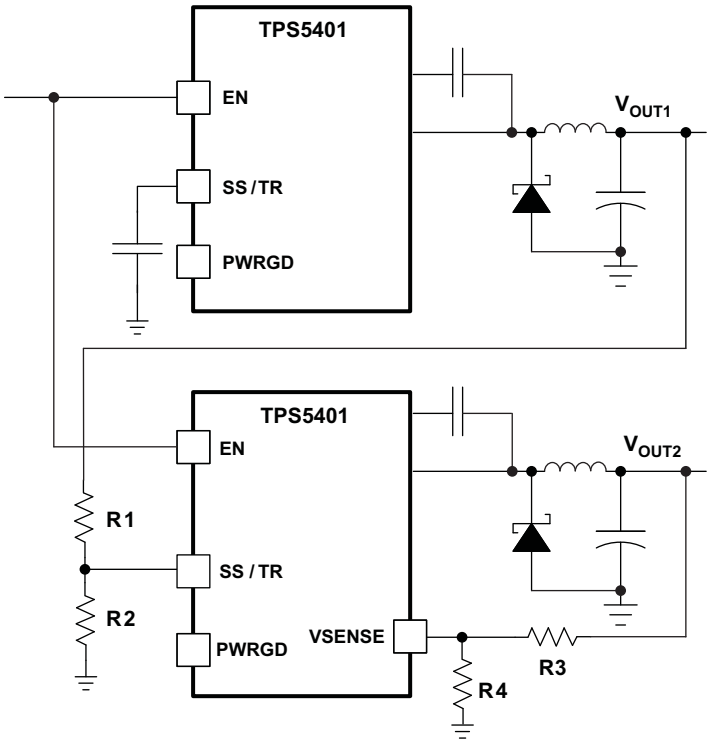


Figure 33. Schematic for Ratiometric and Simultaneous Start-Up Sequence

Ratiometric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 33 to the output of the power supply that must be tracked or to another voltage reference source. Using Equation 5 and Equation 6, the tracking resistors can be calculated to initiate the V_{OUT2} slightly before, after, or at the same time as V_{OUT1}. Equation 7 is the voltage difference between V_{OUT1} and V_{OUT2} at the 95% of nominal output regulation.

The ΔV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset ($V_{ssoffset}$) in the slow-start circuit and the offset created by the pullup current source (I_{ss}) and tracking resistors, the $V_{ssoffset}$ and I_{ss} are included as variables in the equations. Figure 36 shows the result when ΔV = 0 V.

To design a ratiometric start-up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 5 through Equation 7 for ΔV. Equation 7 results in a positive number for applications in which V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved. Figure 34 and Figure 35 show the start-up waveforms for negative and positive ΔV, respectively.

Because the SS/TR pin must be pulled below 40 mV before starting after an EN, UVLO, or thermal shutdown fault, careful selection of the tracking resistors is needed to ensure the device can restart after a fault. Make sure the calculated R1 value from Equation 5 is greater than the value calculated in Equation 8 to ensure the device can recover from a fault.

Feature Description (continued)

As the SS/TR voltage becomes more than 85% of the nominal reference voltage, the $V_{ssoffset}$ becomes larger as the slow-start circuits gradually hand off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.3 V for a complete handoff to the internal voltage reference as shown in Figure 23.

$$R1 = \frac{V_{OUT2} + \Delta V}{V_{ref}} \times \frac{V_{ssoffset}}{I_{ss}} \quad (5)$$

$$R2 = \frac{V_{ref} \times R1}{V_{OUT2} + \Delta V - V_{ref}} \quad (6)$$

$$\Delta V = V_{OUT1} - V_{OUT2} \quad (7)$$

$$R1 > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (8)$$

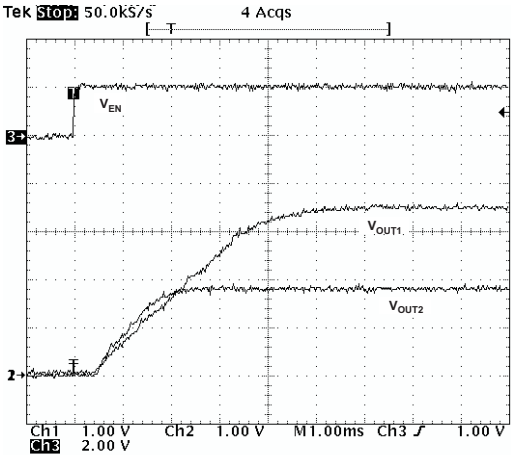


Figure 34. Ratiometric Start-Up With V_{OUT2} Leading V_{OUT1}

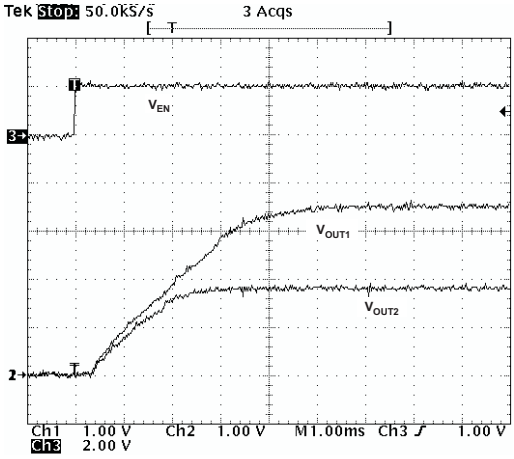


Figure 35. Ratiometric Start-Up With V_{OUT1} Leading V_{OUT2}

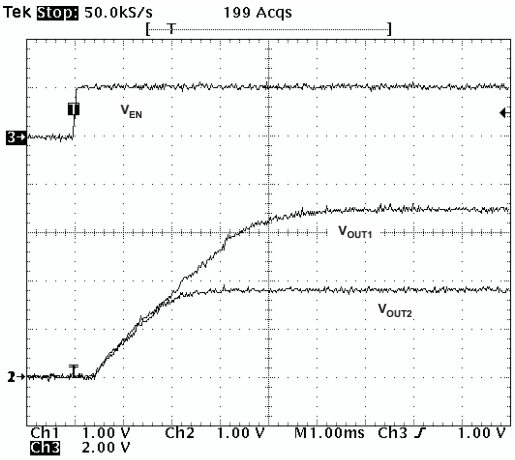


Figure 36. Simultaneous Start-Up

Feature Description (continued)

7.3.11 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS5401 is adjustable over a wide range from approximately 100 kHz to 2500 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 9 or the curves in Figure 5 or Figure 6. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage, and minimum controllable on-time should be considered.

The minimum controllable on-time is typically 130 ns and limits the maximum operating input voltage.

The maximum switching frequency is also limited by the frequency-shift circuit. More discussion on the details of the maximum switching frequency is located as follows.

$$R_T(k\Omega) = \frac{206{,}003}{f_{SW}(kHz)^{1.0888}} \quad (9)$$

7.3.12 Overcurrent Protection and Frequency Shift

The TPS5401 implements current-mode control, which uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. Each cycle, the switch current and COMP pin voltage are compared. When the peak switch current intersects the COMP voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch-current limit.

To increase the maximum operating switching frequency at high input voltages, the TPS5401 implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on the VSENSE pin.

The device implements a digital frequency shift to enable synchronizing to an external clock during normal start-up and fault conditions. Because the device can only divide the switching frequency by 8, there is a maximum input voltage limit in which the device operates and still has frequency-shift protection.

During short-circuit events (particularly with high-input-voltage applications), the control loop has a finite minimum controllable on-time, and the output has a low voltage. During the switch on-time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on-time. During the switch off-time, the inductor current would normally not have enough off-time and output voltage to ramp down by the ramp-up amount. The frequency shift effectively increases the off-time, allowing the current to ramp down.

7.3.13 Selecting the Switching Frequency

The switching frequency that is selected should be the lower value of the two equations, Equation 10 and Equation 11. Use Equation 10 to calculate the maximum switching frequency limitation set by the minimum controllable on-time. Setting the switching frequency above this value causes the regulator to skip switching pulses.

Equation 11 is the maximum switching frequency limit set by the frequency-shift protection. To have adequate output short-circuit protection at high input voltages, the switching frequency should be set to be less than the $f_{SW(maxshift)}$ frequency. Equation 11. To calculate the maximum switching frequency in Equation 11, account for the output voltage decrease from the nominal voltage to 0 volts and the f_{DIV} integer increase from 1 to 8, which corresponds to the frequency shift.

Feature Description (continued)

In Figure 37, the solid line illustrates a typical safe operating area regarding frequency shift and assumes an output voltage of zero volts, an inductor resistance of 0.13 Ω, FET on-resistance of 0.2 Ω, and a diode voltage drop of 0.5 V. The dashed line is the maximum switching frequency to avoid pulse skipping. Enter these equations in a spreadsheet or other software or use the WEBENCH design software to determine the switching frequency.

$$f_{SW(max\,skip)} = \frac{1}{t_{on(min)}} \times \left(\frac{I_L \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \quad (10)$$

where

- $t_{on(min)}$ is the minimum controllable on-time
- I_L is the inductor current
- R_{dc} is the inductor resistance
- $V_d$is the diode voltage drop
- V_{IN} is the maximum input voltage
- V_{OUT} is the output voltage
- $R_{DS(on)}$ is the switch-on resistance

$$f_{SWshift} = \frac{f_{DIV}}{t_{on(min)}} \times \left(\frac{I_L \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \quad (11)$$

where

- f_{DIV} is the frequency divide, which equals 1, 2, 4, or 8
- $V_{OUT(sc)}$ is the output voltage during short

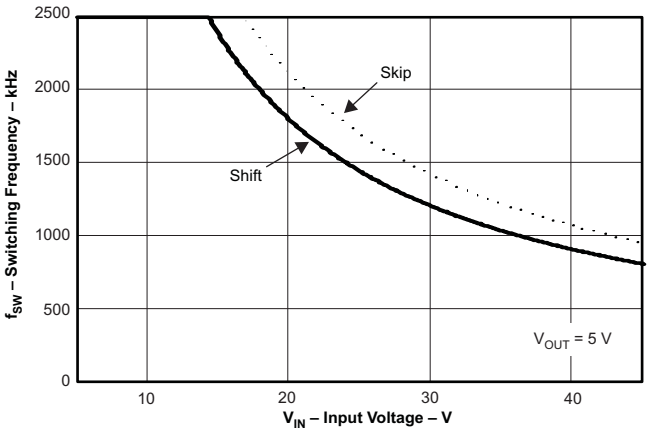


Figure 37. Maximum Switching Frequency vs. Input Voltage

7.3.14 How to Interface to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature, connect a square wave to the RT/CLK pin as shown in Figure 38. The square-wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and have an on-time greater than 40 ns and an off-time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of the PH signal is synchronized to the falling edge of the RT/CLK pin signal.

Feature Description (continued)

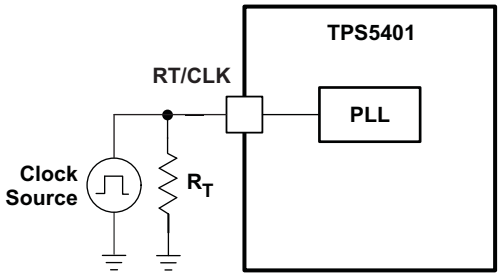


Figure 38. Synchronizing to a System Clock

7.3.15 Power Good (PWRGD Pin)

The PWRGD pin is an open-drain output. Once the VSENSE pin is between 94% and 107% of the internal voltage reference, the PWRGD pin is de-asserted and the pin floats. It is recommended to use a pullup resistor between the values of 10 kΩ and 100 kΩ connected to a voltage source that is 5.5 V or less. PWRGD is in a defined state once the VIN input voltage is greater than 1.5 V, but with reduced current-sinking capability. PWRGD achieves full current-sinking capability as the VIN input voltage approaches 3 V.

The PWRGD pin is pulled low when VSENSE is lower than 92% or greater than 109% of the nominal internal reference voltage. Also, PWRGD is pulled low if the UVLO or thermal shutdown is asserted or the EN pin is pulled low.

7.3.16 Overvoltage Transient Protection

The TPS5401 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power-supply designs with low-value output capacitance. For example, when the power-supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error-amplifier output to a high voltage, thus requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state duty cycle. In some applications, the power-supply output voltage can respond faster than the error-amplifier output can respond, which leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot when using a low-value output capacitor by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold, which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

7.3.17 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 182°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 182°C, the device reinitiates the power-up sequence by discharging the SS/TR pin.

Feature Description (continued)

7.3.18 Current-Mode Compensation Design

To simplify design efforts using the TPS5401, the typical designs for common applications are listed in Table 1. For designs using ceramic output capacitors, TI recommends proper derating of ceramic output capacitance when conducting the stability analysis because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. Advanced users may see the *Detailed Design Procedure* in for detailed guidelines or use the WEBENCH tool.

Table 1. Typical Designs(1)

V_{IN} (V)	V_{OUT} (V)	f_{SW} (kHz)	L_{OUT} (µH)	C_{OUT}	R1 (kΩ)	R2 (kΩ)	C2 (pF)	C1 (pF)	R3 (kΩ)
7.5 V–35 V	5	700	47	Aluminum, 220 µF/260 mΩ	52.3	10	82	3300	698
7.5 V–35 V	5	700	47	Ceramic, 47 µF/10V	52.3	10	5.6	3300	75
12 V–42 V	5	700	47	Aluminum, 100 µF/300 mΩ	52.3	10	100	3300	316
12 V–42 V	3.3	700	33	Ceramic, 33 µF/10 V	30.9	10	10	3300	47
8 V–14 V	5	700	33	Ceramic, 47 µF/10 V	52.3	10	5.6	3300	75

(1) Refer to Simplified Schematic.

7.4 Device Functional Modes

7.4.1 Pulse-Skip Eco-mode Control Scheme

The TPS5401 operates in a pulse-skip Eco-mode control scheme at light load currents to improve efficiency by reducing switching and gate-drive losses. The TPS5401 is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse-skipping current threshold, the device enters the Eco-mode control scheme. This current threshold is the current level corresponding to a nominal COMP voltage of 500 mV.

When in the Eco-mode control scheme, the COMP pin voltage is clamped at 500 mV, and the high-side MOSFET is inhibited. Further decreases in load current or increases in output voltage cannot drive the COMP pin below this clamp voltage level.

Because the device is not switching, the output voltage begins to decay. As the voltage control loop compensates for the falling output voltage, the COMP pin voltage begins to rise. At this time, the high-side MOSFET is enabled, and a switching pulse initiates on the next switching cycle. The peak current is set by the COMP pin voltage. The output voltage recharges the regulated value (see Figure 39); then the peak switch current starts to decrease and eventually falls below the Eco-mode control-scheme threshold, at which time the device again enters the Eco-mode control scheme.

For Eco-mode control-scheme operation, the TPS5401 senses peak current, not average or load current, so the load current where the device enters the Eco-mode control scheme is dependent on the output inductor value. For example, the circuit in Figure 40 enters the Eco-mode control scheme at about 20 mA of output current. When the load current is low and the output voltage is within regulation, the device enters a sleep mode and draws only 116 µA of input quiescent current. The internal PLL remains operating when in sleep mode. When operating at light load currents in the pulse-skip mode, the switching transitions occur synchronously with the external clock signal.

Device Functional Modes (continued)

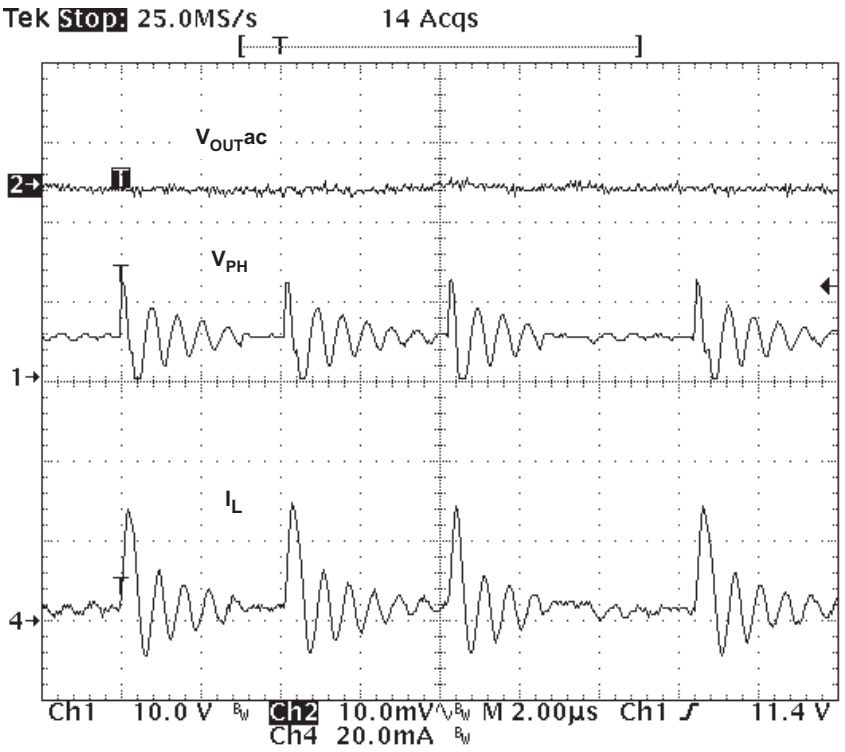


Figure 39. Pulse-Skip Mode Operation

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS5401 is good for the E-meter application. The power supply design is a challenge work to E-meter designers because it must get enough output current from a wide input voltage range with a limited input power. For example, in China, a single-phase or three-phase E-meter must work properly with an input AC electricity voltage range from 0.7 Un to 1.9 Un. Here Un is the phase voltage of 220 V. The input active power limit is 1.5 W. A typical power supply design uses a transformer followed by a rectifier bridge to get a low unregulated dc voltage. Then a voltage regulator generates 5 V for the whole system. Considering the ac transformer has large internal dc resistance and the following rectifier has a voltage drop, the output voltage of the rectifier circuit is different between empty load and heavy load. So the input voltage for the voltage regulator within the whole ac input voltage range may have a maximum-to-minimum ratio of 4. In this situation, a linear regulator is not suitable due to its very low efficiency at high input voltage.

8.2 Typical Application

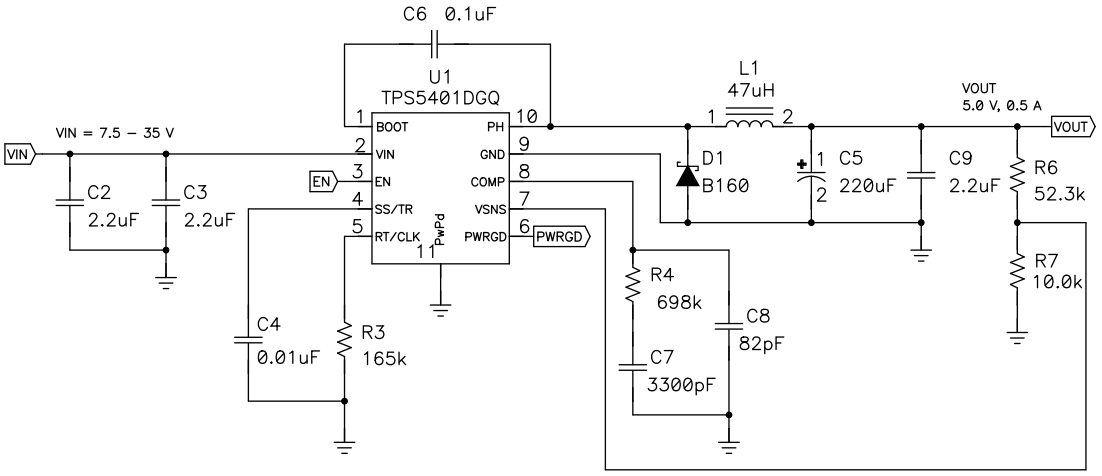


Figure 40. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Figure 40 shows a typical TPS5401 application schematic for this requirement. The input range is set to 7.5 V to 35 V. With such a wide input voltage range, an inexpensive transformer with high dc resistance can be used to save total cost.

8.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS5401. Alternately, the WEBENCH software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process. To begin the design process, a few parameters must be decided upon. Table 2 lists the parameters the designer needs to know.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	7.5 V to 35 V
Output voltage	5 V
Input ripple voltage	300 mV
Output ripple voltage	1% of V_{OUT}
Output transient response for 0 to 500-mA load step	4% of V_{OUT}
Maximum output current	500 mA

8.2.2.1 Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user may want to choose the highest switching frequency possible, because this produces the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. Alternatively, the user may choose a lower switching frequency to improve efficiency. At lower switching frequencies, switching losses are minimized. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage, and the frequency shift limitation.

Equation 10 and Equation 11 must be used to find the maximum switching frequency for the regulator. Choose the lower value of the two equations. Switching frequencies higher than these values result in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on-time, $t_{on(min)}$, is 130 ns for the TPS5401. For this example, the output voltage is 5 V and the maximum input voltage is 35 V, which allows for a maximum switch frequency up to 1213 kHz when including the inductor resistance, on-resistance, and diode voltage in Equation 10. To ensure overcurrent runaway is not a concern during short circuits in your design, use Equation 11 or the solid curve in Figure 37 to determine the maximum switching frequency. With a maximum input voltage of 35 V, assuming a diode voltage of 0.5 V, inductor resistance of 130 mΩ, switch resistance of 400 mΩ, a current-limit value of 0.94 A, and a short-circuit output voltage of 0.1 V, the maximum switching frequency is approximately 1265 kHz. Choosing high frequency can reduce external component size but results in higher switching loss. To achieve a balanced design, a switching frequency of 700 kHz is used. To determine the timing resistance for a given switching frequency, use Equation 9 to get a nearest standard resistance of 165 kΩ. The switching frequency is set to 698 kHz by the resistor R3 shown in Figure 40.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPS5401 is externally adjustable using a resistor divider network. In the application circuit of Figure 40, this divider network is comprised of R6 and R7. The relationship of the output voltage to the resistor divider is given by Equation 12:

$$R6 = \left(\frac{V_{OUT}}{V_{ref}} - 1 \right) \text{ x } R7 \tag{12}$$

Choosing R7 = 10 kΩ, R6 is calculated to be 52.3 kΩ for an output voltage of 5 V.

Due to current leakage of the VSENSE pin, the current flowing through the feedback network should be greater than 1 µA in order to maintain the output voltage accuracy. This requirement makes the maximum value of R7 equal to 800 kΩ. Choosing higher resistor values decreases quiescent current and improve efficiency at low output currents but may introduce noise immunity problems.

8.2.2.3 Input Capacitor

The TPS5401 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor with at least 3 µF of effective capacitance, and in some applications additional bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input-current ripple of the TPS5401. Use Equation 13 to calculate the input voltage ripple.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 60-V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V, and 100 V, so a 100-V capacitor should be selected. For this example, two 2.2-µF, 100-V capacitors in parallel have been selected. Table 3 shows a selection of high-voltage capacitors. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 14.

Using the design example values, $I_{OUT(max)}$ = 0.5 A, C_{IN} = 4.4 µF,and f_{SW} = 700 kHz, yields an input voltage ripple of 40.6 mV and a maximum rms input ripple current of 0.25 A when V_{IN} is equal to 10 V, which is 2 times the output voltage of 5 V.

$$I_{INRMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN}-V_{OUT})}{V_{IN}}} \quad (13)$$

$$V_{INRIPPLE} = \frac{I_{OUT(max)} \times 0.25}{C_{IN} \times f_{SW}} \quad (14)$$

Table 3. Capacitor Types

VENDOR	VALUE (µF)	EIA Size	VOLTAGE	DIELECTRIC	COMMENTS
Murata	1 to 2.2	1210	100 V	X7R	GRM32 series
	1 to 4.7		50 V		
	1	1206	100 V		GRM31 series
	1 to 2.2		50 V		
Vishay	1 to 1.8	2220	50 V		VJ X7R series
	1 to 1.2		100 V		
	1 to 3.9	2225	50 V		
	1 to 1.8		100 V		
TDK	1 to 2.2	1812	100 V		C series C4532
	1.5 to 6.8		50 V		
	1. to 2.2	1210	100 V		C series C3225
	1 to 3.3		50 V		
AVX	1 to 4.7	1210	50 V		X7R dielectric series
	1		100 V		
	1 to 4.7	1812	50 V		
	1 to 2.2		100 V		

8.2.2.4 Output Inductor Selection

To calculate the minimum value of the output inductor, use Equation 15.

$$L_{OUT(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \quad (15)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer. However, the following guidelines may be used.

For designs using low-ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.4 may be used. When using higher-ESR output capacitors, K_{IND} = 0.2 yields better results. Because the inductor ripple current is part of the PWM control system, the TPS5401 requires ripple current that is always greater than 30 mA for dependable operation. In a wide-input voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum. The maximum value of the input inductance is limited by Equation 16.

$$L_{OUT(max)} = \frac{V_{IN(min)} - V_{OUT}}{30mA} \times \frac{V_{OUT}}{V_{IN(min)} \times f_{SW}} \quad (16)$$

For this design example, use K_{IND} = 0.3, and the minimum inductor value is calculated to be 42 µH. The nearest standard value was chosen: 47 µH. For the output-filter inductor, it is important that the root-mean-square (rms) current and saturation current ratings not be exceeded. The rms and peak inductor current can be found from Equation 17 to Equation 19.

$$I_{LRIPPLE} = \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)} \times L_{OUT} \times f_{SW}} \quad (17)$$

$$I_{L(RMS)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)} \times L_{OUT} \times f_{SW}} \right)^2} \quad (18)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (19)$$

As the equation set demonstrates, lower ripple currents reduce the output voltage ripple of the regulator but require a larger value of inductance. Selecting higher ripple currents increases the output voltage ripple of the regulator but allows for a lower inductance value. The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current. For this design, $I_{LRIPPLE}$ = 0.1303 A, $I_{L(RMS)}$ = 0.501 A and $I_{L(peak)}$ = 0.565 A. The inductor used is a Coilcraft MSS1048-473ML type, with a saturation current rating of 1.44 A and an rms current rating of 1.83 A.

8.2.2.5 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator also is temporarily unable to supply sufficient output current if there is a large, fast increase in the current needs of the load, such as when transitioning from no load to a full load. The regulator usually requires two or more clock cycles for the control loop to detect the change in load

current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of drop in the output voltage. Equation 20 shows the minimum output capacitance necessary to accomplish this.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \left(\Delta V_{OUT} - \Delta I_{OUT} \times R_{ESR}\right)}$$

where

- ΔI_{OUT} is the change in output current
- f_{SW} is the regulator switching frequency
- ΔV_{OUT} is the allowable change in the output voltage
- R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor (20)

Equation 20 indicates the ESR must be less than $\Delta V_{OUT}/\Delta I_{OUT}$. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 0 A (no load) to 0.5 A (full load). In addition, ΔI_{OUT} = 0.5A and ΔV_{OUT} = 0.04 × 5 V = 0.2 V. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account. Using these numbers gives a minimum capacitance of 7.14 µF for ceramic capacitor and 20.4 µF for electrolytic capacitor with 260 mΩ ESR.

The catch diode of the regulator cannot sink current, so any stored energy in the inductor produces an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that gets stored in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 21 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value, where L_{OUT} is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_{FIN} is the final peak output voltage, and V_{INI} is the initial capacitor voltage. For this example, the worst-case load step is from 0.5 A to 0 A. The output voltage increases during this load transition, and the stated maximum in our specification is 4% of the output voltage. This makes V_{FIN} = 1.04 × 5 V = 5.2 V. V_{INI} is the initial capacitor voltage, which is the nominal output voltage of 5 V. Using these numbers in Equation 21 yields a minimum capacitance of 5.76 µF.

$$C_{OUT} > L_{OUT} \times \frac{I_{OH}^2 - I_{OL}^2}{V_{FIN}^2 - V_{INI}^2} \quad (21)$$

Equation 22 calculates the minimum output capacitance needed to meet the output-voltage ripple specification, where f_{SW} is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and $I_{LRIPPLE}$ is the inductor ripple current. Equation 22 shows the ESR of the output capacitor must be less than $V_{ORIPPLE}/I_{LRIPPLE}$ to meet the output-voltage ripple requirement. Low-ESR capacitors are preferred to keep the output-voltage ripple low. If a high-ESR electrolytic capacitor is used, a small ESR ceramic capacitor is recommended to be in parallel with the electrolytic capacitor to minimize the output voltage ripple. In this application, an aluminum electrolytic capacitor is chosen as the output capacitor. It has 260 mΩ ESR. Equation 22 yields 1.44 µF.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{ORIPPLE}}{I_{LRIPPLE}} - R_{ESR}} \quad (22)$$

The most stringent criterion for the output capacitor is 20.5 µF of capacitance to keep the output voltage in regulation during a load transient in this example.

Additional capacitance de-ratings for aging, temperature and dc bias should be factored in, which increases this minimum value. For this example, a 220 µF electrolytic capacitor with 260 mΩ of ESR can be used for low cost target.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root-mean-square (rms) value of the maximum ripple current. Equation 23 can be used to calculate the rms ripple current the output capacitor must support. For this application, Equation 23 yields 37.6 mA.

$$I_{CO(RMS)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_{OUT} \times f_{SW}} \quad (23)$$

8.2.2.6 Catch Diode

The TPS5401 requires an external catch diode between the PH pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(MAX)}$. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode, due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, when the voltage and current ratings for the diode are higher, then the forward voltage is higher. Because the design example has an input voltage up to 42 V, a diode with a minimum of 42-V reverse voltage is selected.

For the example design, the B160A Schottky diode is selected for its lower forward voltage, and it comes in a larger package size which has good thermal characteristics over small devices. The typical forward voltage of the B160A is 0.5 V.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode, which equals the conduction losses of the diode. At higher switch frequencies, the ac losses of the diode must be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery. Equation 24 is used to calculate the total power dissipation, conduction losses plus ac losses, of the diode.

The B160A has a junction capacitance (C_J) of 110 pF. Using Equation 24, the selected diode dissipates 0.29 W. This power dissipation, depending on mounting techniques, should produce a 5.9°C temperature rise in the diode when the input voltage is 42 V and the load current is 0.5 A.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times V_{FD}}{V_{IN(max)}} + \frac{C_J \times f_{SW} \times \left(V_{IN(max)} + V_{FD}\right)^2}{2} \quad (24)$$

8.2.2.7 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage-slew rate. This is also used if the output capacitance is large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS5401 reach the current limit, whereas excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage-slew rate solves both of these problems.

The slow-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Equation 25 can be used to find the minimum slow-start time, t_{SS}, necessary to charge the output capacitor, C_{OUT}, from 10% to 90% of the output voltage, V_{OUT}, with an average slow-start current of I_{SSAVG}. In the example, to charge the 220 µF output capacitor up to 5 V while only allowing the average input current I_{SSAVG} to be 0.2 A would require a 4.4-ms slow-start time.

$$t_{SS} > \frac{C_{OUT} \times V_{OUT} \times 0.8}{I_{SSAVG}} \tag{25}$$

When the slow-start time is known, the slow-start capacitor value can be calculated using Equation 4. For the example circuit, the slow-start time is set to a value of 3.2 ms, which requires a 0.01-µF capacitor.

8.2.2.8 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10-V or higher voltage rating.

8.2.2.9 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS5401. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. The supply should turn on and start switching once the input voltage increases above power-up threshold (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below the power-down threshold (UVLO stop).

The programmable UVLO and enable voltages are set using a resistor divider between V_{IN} and ground to the EN pin. Equation 2 through Equation 3 can be used to calculate the resistance values necessary. For the example application, because the minimum input voltage is 7.5 V, when the maximum input voltage is 35 V, the voltage at the EN pin exceeds the absolute voltage rating of the EN pin. So the UVLO is not set externally in this design.

8.2.2.10 Compensation

The external compensation used with the TPS5401 allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric is supported. This design example uses an aluminum electrolytic output capacitor. A design example with the ceramic dielectric output capacitors can be found in the TPS54040 data sheet (SLVS918). More accurate designs can be found in the WEBENCH software.

The peak-current mode PWM modulator and the output filter generate a pair of power stage pole and zero which are determined using Equation 26 and Equation 27.

$$f_{Pmod} = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}} \tag{26}$$

$$f_{Zmod} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{27}$$

A type 2A compensation scheme is recommended for the TPS5401. As R_C, C_C, C_P shown in Figure 41, the compensation components are chosen to set the desired loop crossover frequency and phase margin for output filter components. The type 2A compensation has the following characteristics: a dc gain, a low-frequency pole, and a mid-frequency zero / pole pair.

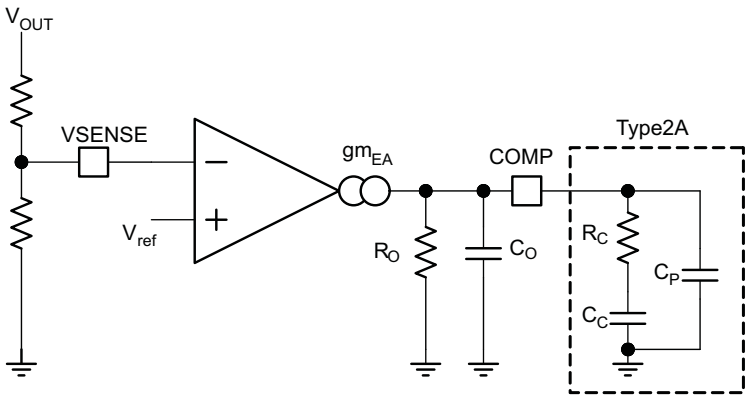


Figure 41. The Compensation Recommended for the TPS5401

The dc gain is determined by Equation 28:

$$G_{DCEA} = A_{DCEA} \times \frac{V_{ref}}{V_{OUT}} \quad (28)$$

where

- A_{DCEA} is the error amplifier open-loop dc gain. It is 10,000 V/V.

The low-frequency pole is determined by Equation 29:

$$f_{P0} = \frac{1}{2\pi \times R_O \times C_C} \quad (29)$$

where

- R_O is the output resistance of the error amplifier. It can be calculated by Equation 30.

$$R_0 = \frac{A_{DCEA}}{gm_{EA}} \quad (30)$$

The mid-frequency zero is determined by Equation 31.

$$f_{Z1} = \frac{1}{2\pi \times R_C \times C_C} \quad (31)$$

Additionally, the mid-frequency pole is given by Equation 32.

$$f_{P1} = \frac{1}{2\pi \times R_C \times C_P} \quad (32)$$

The first step is to choose the closed-loop crossover frequency f_{CO}. In general, the closed-loop crossover frequency could be less than 1/10 of the minimum operating frequency. For the TPS5401, the maximum closed-loop crossover frequency must not be not greater than 40 kHz. For this example, we choose 15-kHz crossover frequency. Next, by definition, the magnitude of the loop gain at the crossover frequency is 0 dB. By placing the compensation zero at the power stage pole, and the mid-compensation pole at the power stage zero, the R_C, C_C and C_P can be approximately calculated by Equation 33 through Equation 35.

$$R_C = \frac{2\pi \times f_{CO} \times C_{OUT}}{gm_{PS}} \times \frac{V_{OUT}}{V_{ref} \times gm_{EA}} \quad (33)$$

$$C_C = \frac{1}{2\pi \times f_{Pmod}} \quad (34)$$

$$C_P = \frac{1}{2\pi \times f_{Zmod}}$$

where

- gm_{PS} is the power-stage transconductance. It is 1.9 A/V
- gm_{EA} is the error-amplifier transconductance. It is 97 µA/V (35)

For this design, the calculated values are as follows:

- R3 = 37.4 kΩ
- C6 = 2200 pF
- C7 = 22 pF

8.2.2.11 Discontinuous Mode and Eco-mode Control-Scheme Boundary

With an input voltage of 34 V, the power supply enters discontinuous mode when the output current is less than 50 mA. The power supply enters Eco-mode control scheme when the output current is lower than 30 mA.

8.2.2.12 Power Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous-conduction mode (CCM) operation. These equations should not be used if the device is working in discontinuous-conduction mode (DCM).

The power dissipation of the IC includes conduction loss (P_{CON}), switching loss (P_{sw}), gate-drive loss (P_{GD}), and supply current (P_{SUP}).

$$P_{con} = I_{OUT}^2 \times r_{DS(on)} \times \frac{V_{OUT}}{V_{IN}} \quad (36)$$

$$P_{sw} = V_{IN}^2 \times I_{OUT} \times 0.25 \times 10^{-9} \times f_{SW} \quad (37)$$

$$P_{GD} = V_{IN} \times 3 \times 10^{-9} \times f_{SW} \quad (38)$$

$$P_{SUP} = 116 \times 10^{-6} \times V_{IN} \quad (39)$$

Therefore, total power dissipation is:

$$P_{TOT} = P_{CON} + P_{SW} + P_{GD} + P_{SUP} \quad (40)$$

For a given ambient temperature T_A, the junction temperature T_J can be estimated by Equation 41.

$$T_J = T_A - \theta_{JA} \times P_{TOT} \quad (41)$$

where

- $R_{\theta JA}$ is the thermal resistance of the package (°C/W)

For given T_J(max) = 150°C, the maximum allowed ambient temperature can be estimated by Equation 42.

$$T_{A(max)} = T_{J(max)} - \theta_{JA} \times P_{TOT} \quad (42)$$

There are additional power losses in the regulator circuit due to the inductor ac and dc losses, the catch diode and trace resistance that impact the overall efficiency of the regulator.

8.2.3 Application Curves

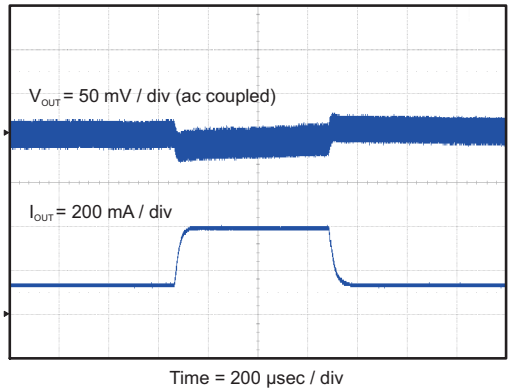


Figure 42. Load Transient (100 mA to 350 mA)

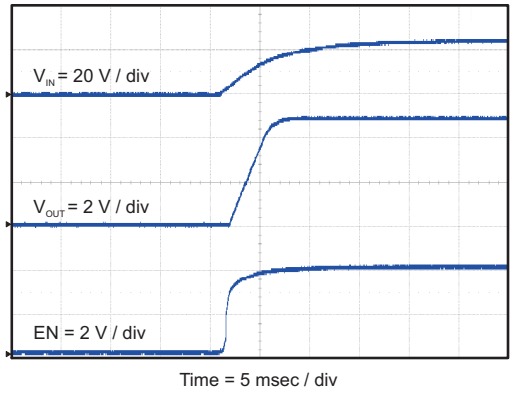


Figure 43. Start-Up With Input Voltage

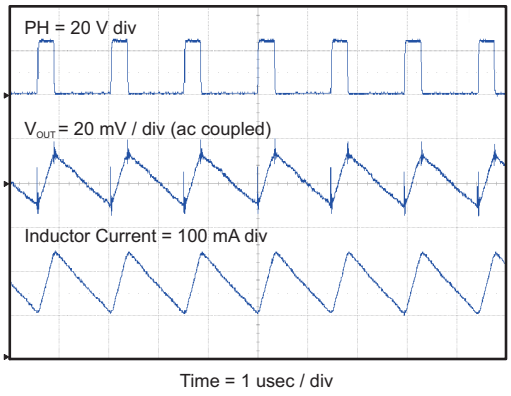


Figure 44. Output Ripple, CCM

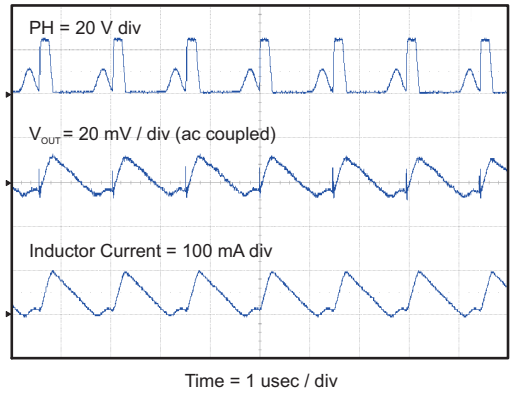


Figure 45. Output Ripple, DCM

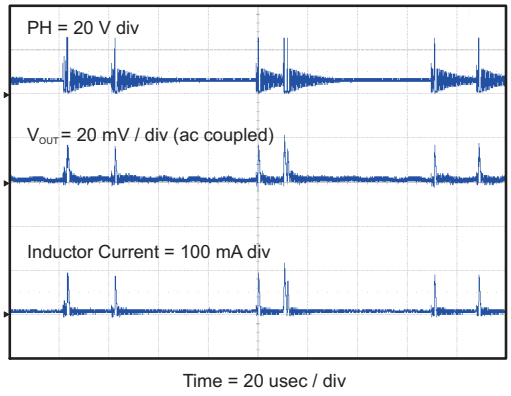


Figure 46. Output Ripple, PSM

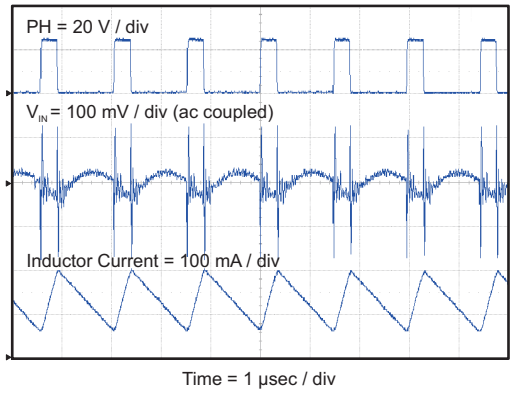


Figure 47. Input Ripple, CCM

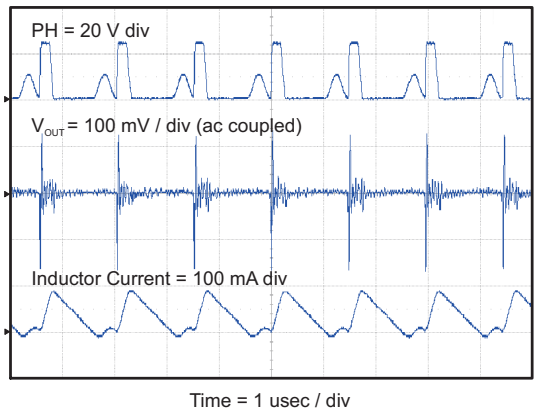


Figure 48. Input Ripple, DCM

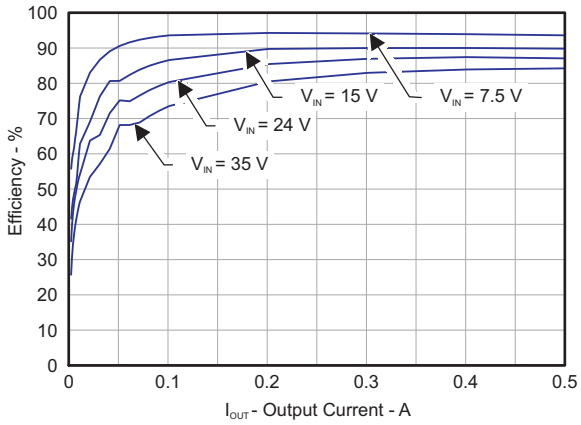


Figure 49. Efficiency vs Load Current

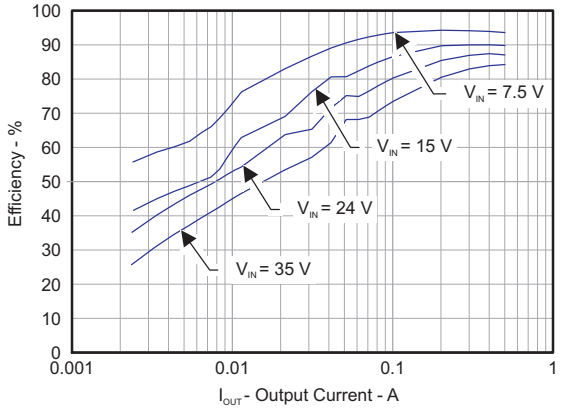


Figure 50. Light-Load Efficiency

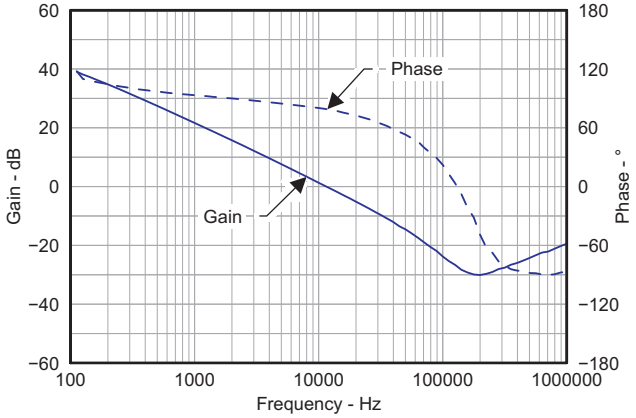


Figure 51. Overall Loop-Frequency Response

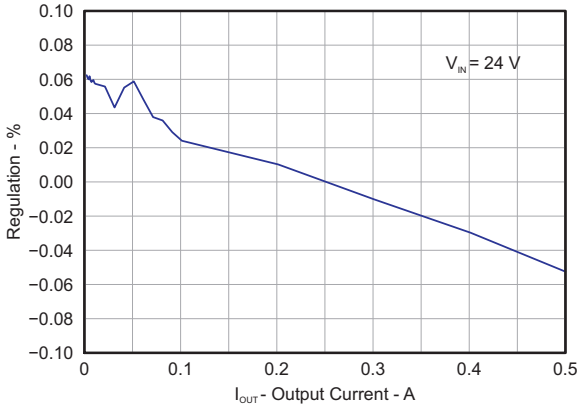


Figure 52. Regulation vs Load Current

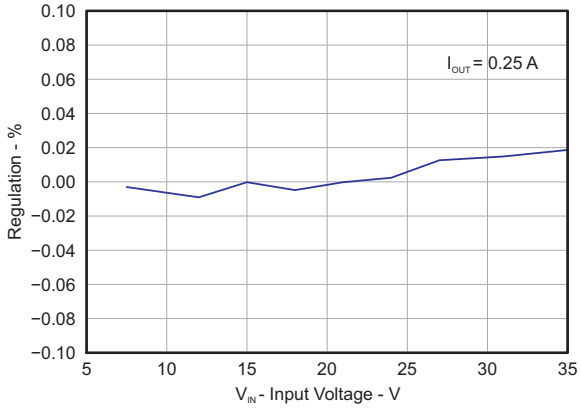


Figure 53. Regulation vs Input Voltage

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 3.5 V and 42 V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 54 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC.

The thermal pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top-side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise, so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however, this layout has been shown to produce good results and is meant as a guideline.

10.2 Layout Example

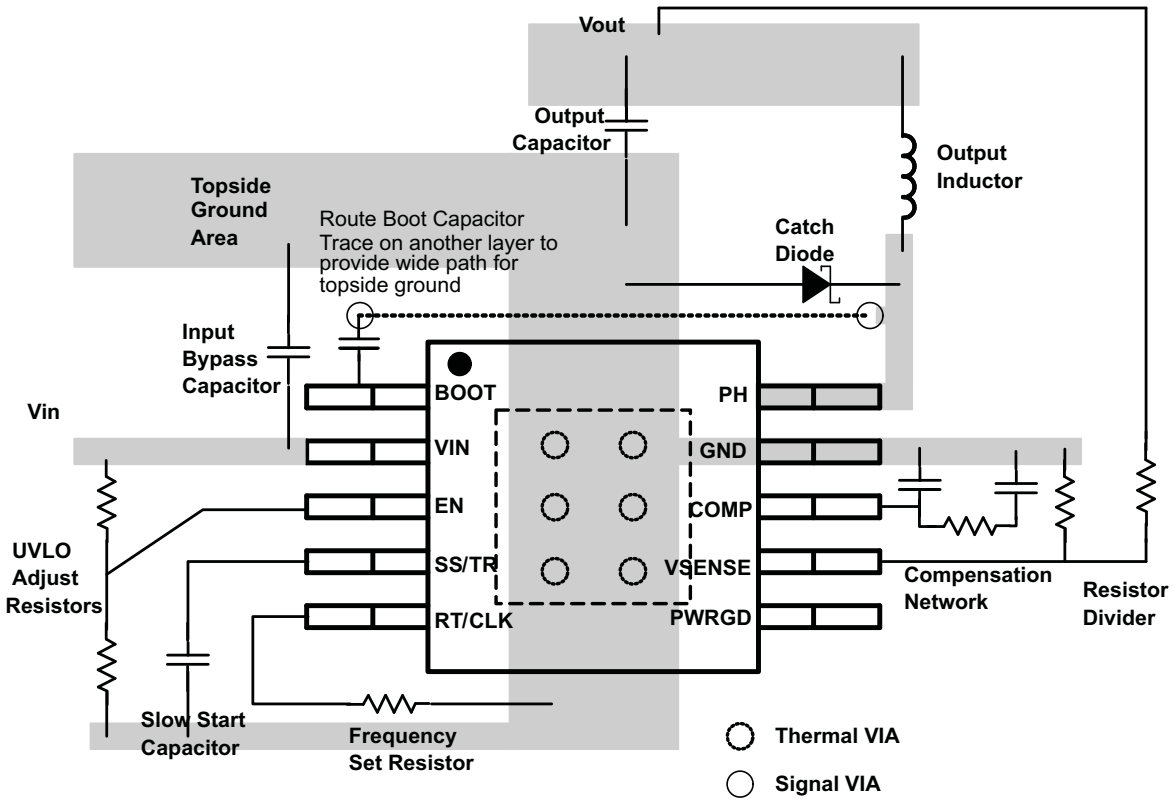


Figure 54. PCB Layout Example

10.3 Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of Figure 40 is 0.55 in^2 (3.55 cm^2). This area does not include test points or connectors.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

- WEBENCH

11.1.2 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

- *Semiconductor and IC Package Thermal Metrics* (SPRA953).
- *TPS54040 0.5-A, 42V Step Down DC/DC Converter with Eco-Mode* data sheet (SLVS918).

11.3 Trademarks

Eco-mode, PowerPAD are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5401DGQ	ACTIVE	HVSSOP	DGQ	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	5401	Samples
TPS5401DGQR	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	5401	Samples
TPS5401DGQT	ACTIVE	HVSSOP	DGQ	10	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	5401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

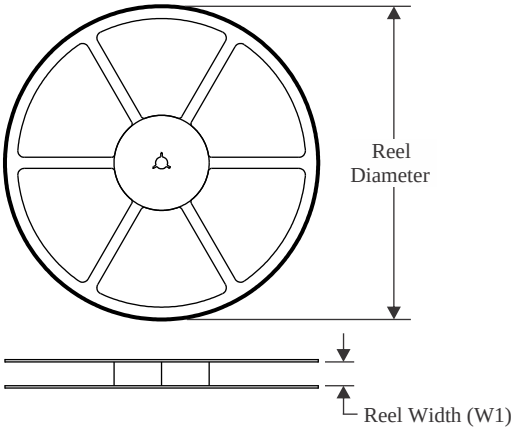
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

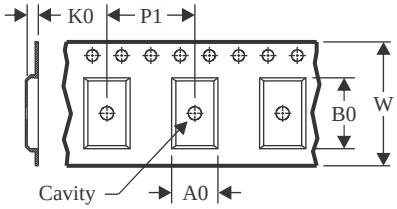
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

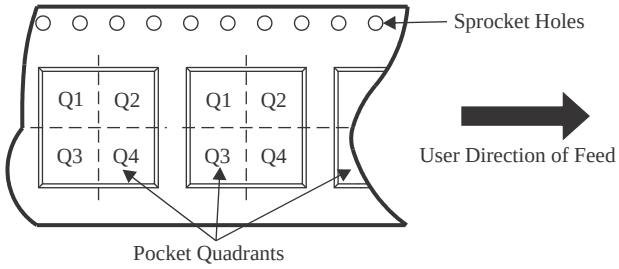


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

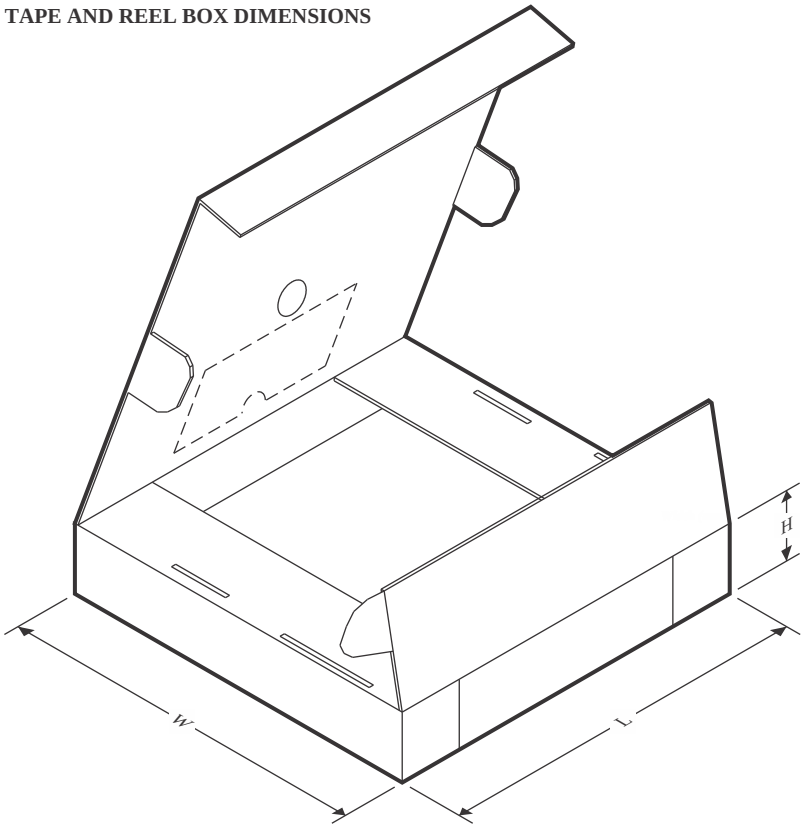
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5401DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS5401DGQT	HVSSOP	DGQ	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

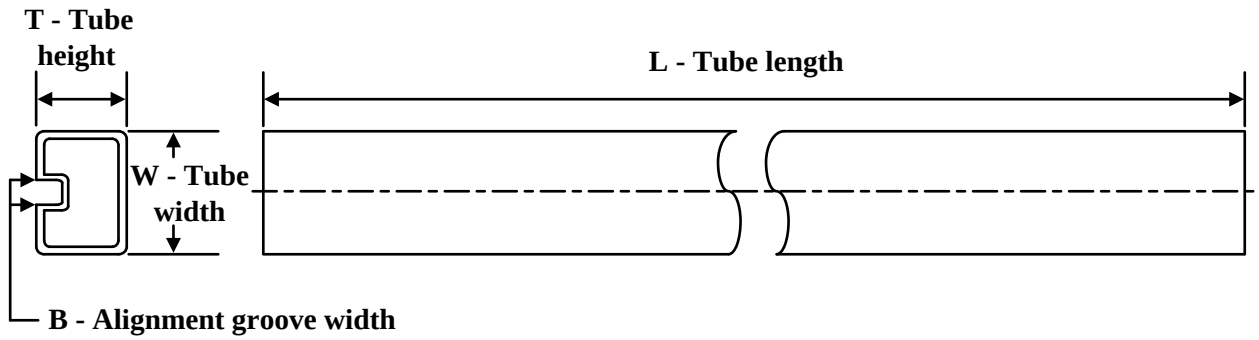
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5401DGQR	HVSSOP	DGQ	10	2500	366.0	364.0	50.0
TPS5401DGQT	HVSSOP	DGQ	10	250	200.0	183.0	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS5401DGQ	DGQ	HVSSOP	10	80	322	6.55	1000	3.01
TPS5401DGQ	DGQ	HVSSOP	10	80	330	6.55	500	2.88

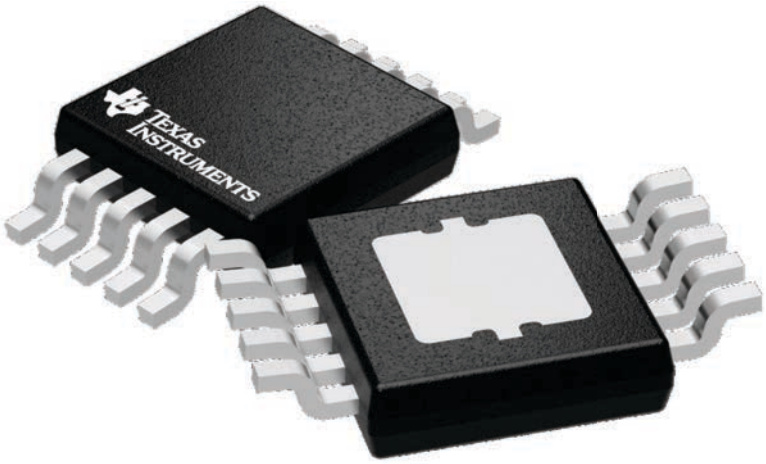
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

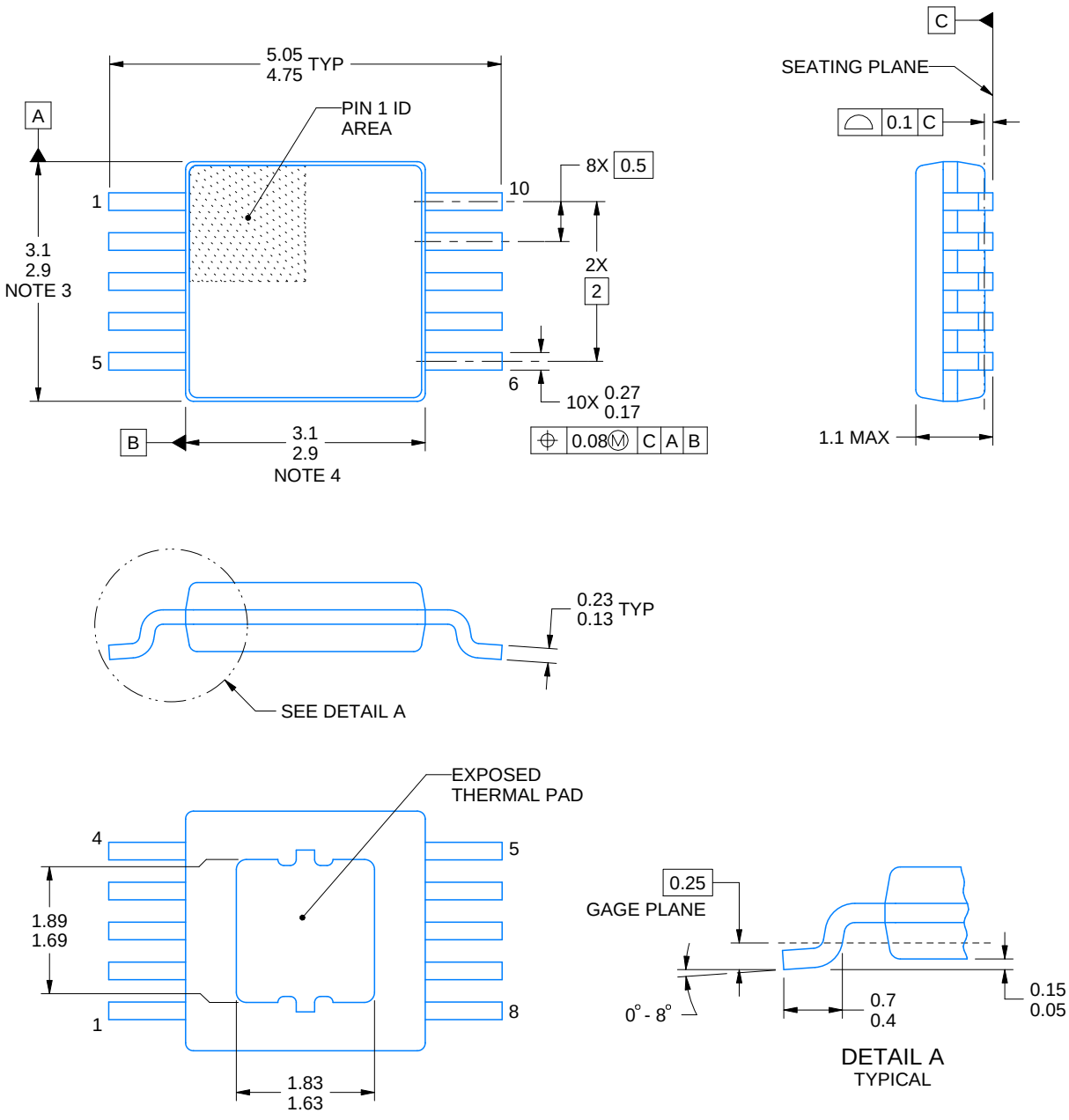
4224775/A

PACKAGE OUTLINE

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE

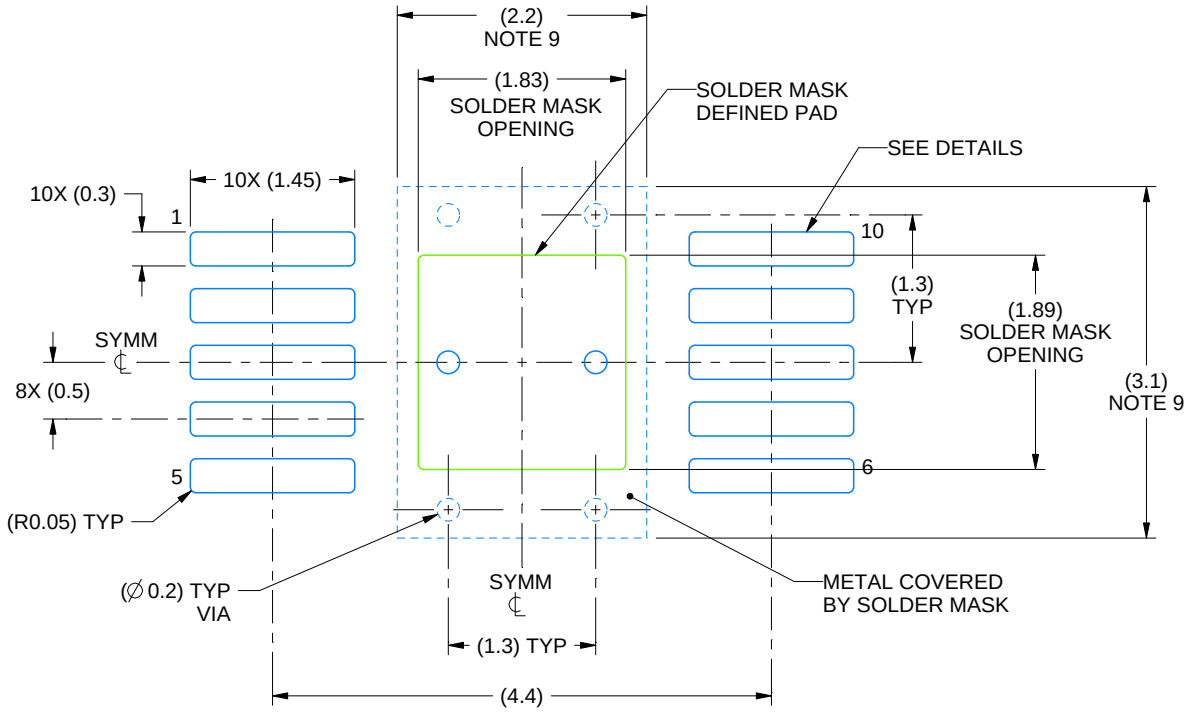


4218842/A 01/2019

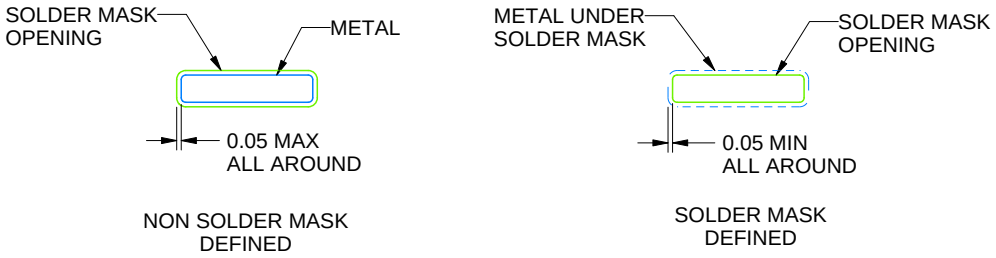
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X

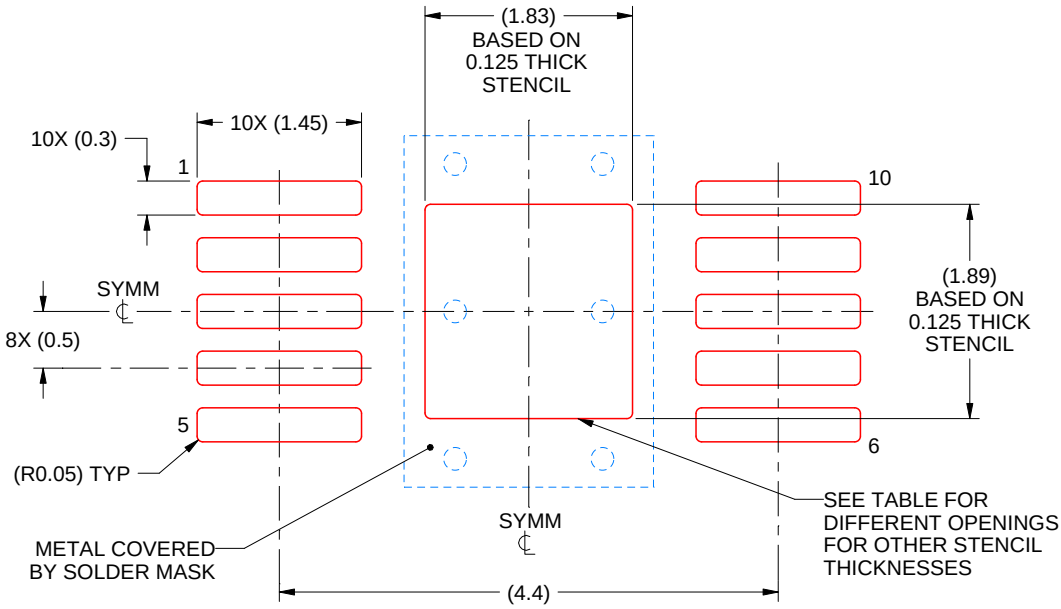


SOLDER MASK DETAILS

4218842/A 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

4218842/A 01/2019

NOTES: (continued)

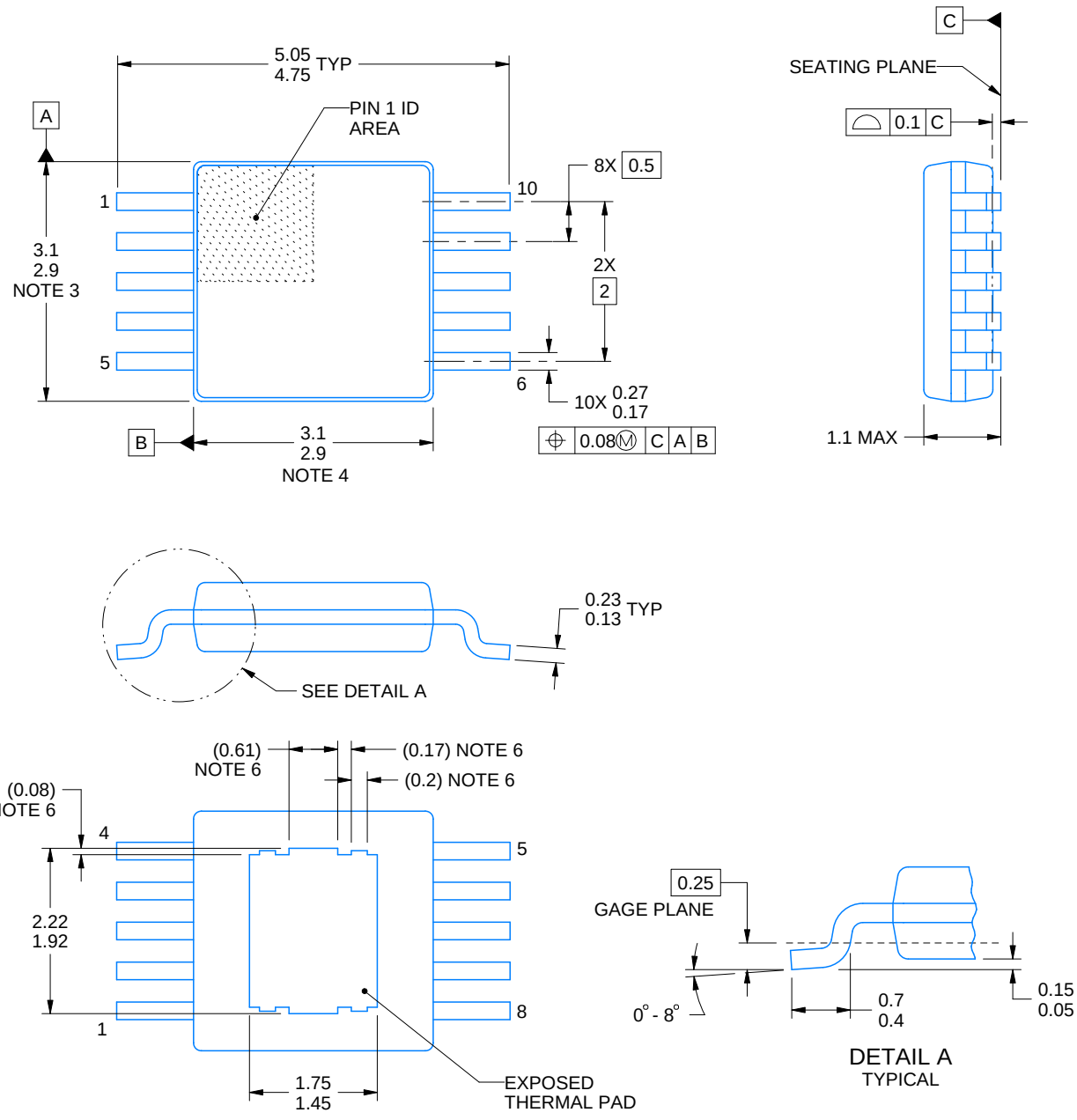
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGQ0010H

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



4226735/B 05/2022

PowerPAD is a trademark of Texas Instruments.

NOTES:

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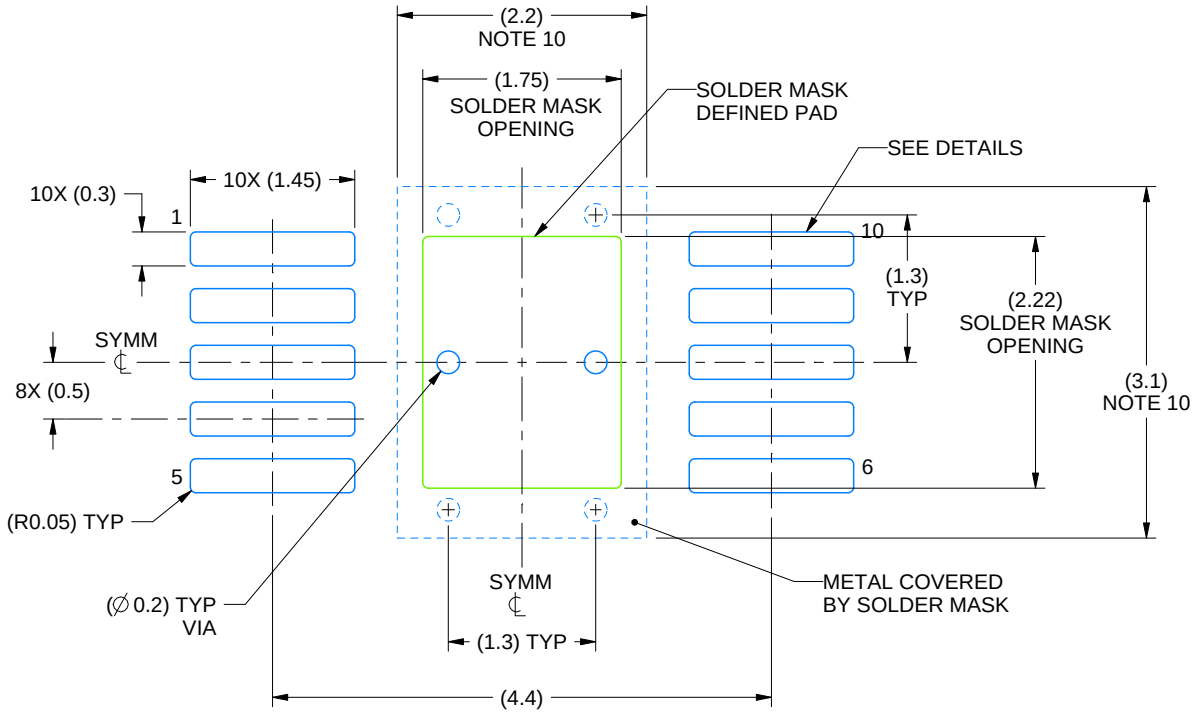
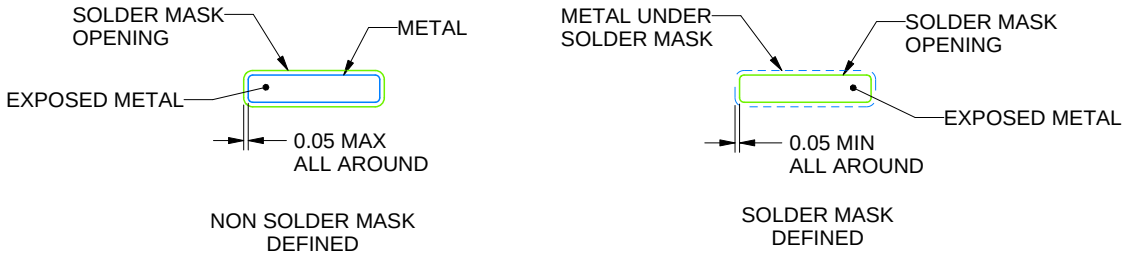
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4226735/B 05/2022

NOTES: (continued)

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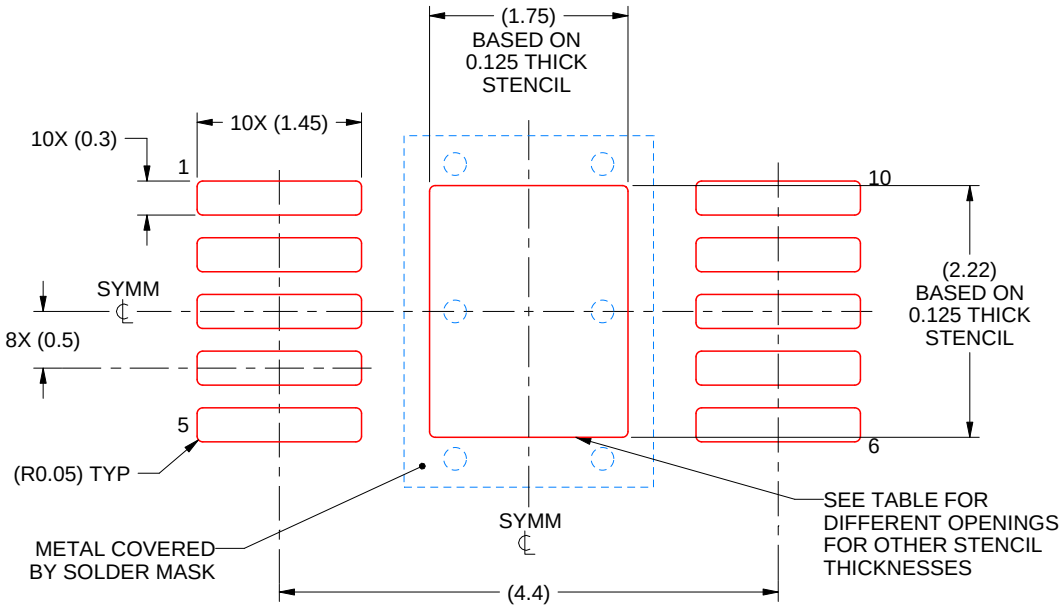
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.100	1.96 X 2.48
0.125	1.75 X 2.22 (SHOWN)
0.150	1.6 X 2.03
0.175	1.48 X 1.88

4226735/B 05/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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