TL07xx 低噪声 FET 输入运算放大器

1 特性

- 高压摆率：20V/μs（TL07xH，典型值）
- 低失调电压：1mV（TL07xH，典型值）
- 低失调电压漂移：2μV/°C
- 低功耗：940μA/ch（TL07xH，典型值）
- 宽共模和差分电压范围
  - 共模输入电压范围包括 V_{CC+}
- 低输入偏置和失调电流
- 低噪声：f = 1kHz 时，V_n = 18nV/√Hz（典型值）
- 输出短路保护
- 低总计谐波失真：0.003%（典型值）
- 宽电源电压：±2.25V 至 ±20V，4.5V 至 40V

2 应用

- 太阳能：串式和中央逆变器
- 电机驱动器：交流和伺服驱动控制及功率级模块
- 单相在线式 UPS
- 三相 UPS
- 专业音频混合器
- 电池测试设备

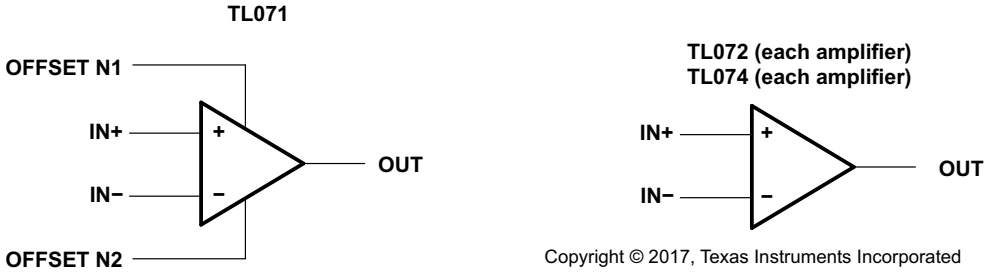
3 说明

TL07xH（TL071H、TL072H 和 TL074H）系列器件是业界通用的 TL07x（TL071、TL072 和 TL074）器件的下一代版本。这些器件为成本敏感型应用提供了卓越的价值，其特性包括低失调电压（1mV，典型值）、高压摆率 (20V/μs) 和正电源的共模输入。得益于高 ESD（1.5kV，HBM）、集成 EMI 和射频滤波器，以及能够在 –40°C 至 125°C 的整个温度范围内运行，TL07xH 器件可用于要求极严苛的应用。

封装信息

器件型号(1)	封装	封装尺寸（标称值）
TL071x	P（PDIP，8）	9.59mm × 6.35mm
	DCK（SC70，5）	2.00mm × 1.25mm
	PS（SO，8）	6.20mm × 5.30mm
	D（SOIC，8）	4.90mm × 3.90mm
	DBV（SOT-23，5)	1.60mm × 1.20mm
TL072x	P（PDIP，8）	9.59mm × 6.35mm
	PS（SO，8）	6.20mm × 5.30mm
	D（SOIC，8）	4.90mm × 3.90mm
	P（SOT-23，8）	2.90mm × 1.60mm
	PW (TSSOP, 8)	4.40mm x 3.00mm
TL072M	JG（CDIP，8）	9.59mm × 6.67mm
	W（CFP，10）	6.12mm × 3.56mm
	FK（LCCC，20）	8.89mm × 8.89mm
TL074x	N（PDIP，14）	19.30mm x 6.35mm
	NS（SO，14）	10.30mm × 5.30mm
	D（SOIC，14）	8.65mm × 3.91mm
	DYY（SOT-23，14）	4.20mm × 2.00mm
	DB（SSOP，14）	6.20mm × 5.30mm
	PW（TSSOP，14）	5.00mm × 4.40mm
TL074M	J（CDIP，14）	19.56mm × 6.92mm
	W（CFP，14）	9.21mm × 6.29mm
	FK（LCCC，20）	8.89mm × 8.89mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



Copyright © 2017, Texas Instruments Incorporated

逻辑符号

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SLOS080

内容

1 特性.....1
2 应用.....1
3 说明.....1
4 修订历史记录.....2
5 引脚配置和功能.....4
6 规格.....11
6.1 绝对最大额定值.....11
6.2 ESD 等级.....11
6.3 建议运行条件.....11
6.4 单通道器件的热性能信息.....12
6.5 双通道器件的热性能信息.....12
6.6 四通道器件的热性能信息.....13
6.7 电气特性：TL07xH.....14
6.8 电气特性（直流）：TL07xC、TL07xAC、TL07xBC、TL07xI、TL07xM.....16
6.9 电气特性（交流）：TL07xC、TL07xAC、TL07xBC、TL07xI、TL07xM.....18
6.10 典型特性：TL07xH.....19
6.11 典型特性：除 TL07xH 之外的所有器件.....26
7 参数测量信息.....30
8 详细说明.....31
8.1 概述.....31
8.2 功能方框图.....31
8.3 特性说明.....31
8.4 器件功能模式.....31
9 应用和实现.....32
9.1 应用信息.....32
9.2 典型应用.....32
9.3 单位增益缓冲器.....33
9.4 系统示例.....34
9.5 电源相关建议.....35
9.6 布局.....35
10 器件和文档支持.....37
10.1 接收文档更新通知.....37
10.2 支持资源.....37
10.3 商标.....37
10.4 静电放电警告.....37
10.5 术语表.....37
11 机械、封装和可订购信息.....37

4 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision U (December 2022) to Revision V (April 2023) — **Page**

- 更新了*概述*、*功能方框图*和*特性说明*部分.....31

Changes from Revision T (December 2021) to Revision U (December 2022) — **Page**

- 通过合并 TL07xH 和 TL07xx 规格更改了*绝对最大额定值*、*ESD 等级*、*建议运行条件和热性能信息*部分.....11
- 通过合并 TL07xC、TL07xAC、TL07xBC、TL07xI 和 TL07xM 规格更改了*电气特性*表.....16
- 将所有非 NS/非 PS 封装和非 TL07xM 器件的增益带宽值从 3MHz 更改为 5.25MHz.....16
- 更改了 TL07xC、TL07xAC、TL07xBC、TL07xI 和 TL07xM *开关特性*表，重命名为*电气特性（交流）*.....18
- 将所有非 PS/非 NS 封装和所有非 TL07xM 器件的 1kHz 输入电压噪声密度更改为 37nV/√Hz.....18
- 将所有非 PS/非 NS 封装和所有非 TL07xM 器件的 THD+N 更改为 0.00012%.....18

Changes from Revision S (July 2021) to Revision T (December 2021) — **Page**

- 更正了*引脚配置和功能*部分的 DCK 引脚图和引脚表.....4

Changes from Revision R (June 2021) to Revision S (July 2021) — **Page**

- 删除了整个数据表中 TL071H SOIC (8)、SOT-23 (5) 和 SC70 (5) 封装的预发布说明.....1

Changes from Revision Q (June 2021) to Revision R (June 2021) — **Page**

- 删除了整个数据表中 TL072H SOIC (8)、SOT-23 (8) 和 TSSOP (8) 封装的预发布说明.....1
- 添加了 TL072H 的 ESD 信息.....11
- 为 TL072H 添加了 I_Q 规格.....14

Copyright © 2023 Texas Instruments Incorporated

Changes from Revision P (November 2020) to Revision Q (June 2021) **Page**

- 删除了*器件信息* 部分中的 VSSOP (8) 封装 1
- 在*引脚配置和功能* 部分中为 TL071H 添加了 DBV、DCK 和 D 封装 4
- 在*引脚配置和功能* 部分中删除了 TL072x 的 DGK 封装 4
- 删除了*规格* 部分中包含重复信息的表 11
- 在“单通道热性能信息：TL071H”部分中添加了 D、DCK 和 DBV 封装热性能信息 12
- 在“双通道热性能信息：TL072H”部分中添加了 D、DDF 和 PW 封装热性能信息 12
- 为单通道 DCK 和 DBV 封装添加了 I_B 和 I_{OS} 规格 14
- 为 TL071H 添加了 I_Q 规格 14
- 从*器件和文档支持* 部分删除了*相关链接* 部分 37

Changes from Revision O (October 2020) to Revision P (November 2020) **Page**

- 在*四通道热性能信息：TL074H* 部分中添加了 SOIC 和 TSSOP 封装*热性能信息* 13
- 在*规格* 部分中添加了*典型特性：TL07xH* 部分 19

Changes from Revision N (July 2017) to Revision O (October 2020) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 向*特性* 部分添加了 TL07xH 的特性 1
- 在*应用* 部分中添加了应用的链接 1
- 在*说明* 部分中添加了 TL07xH 1
- 在*器件信息* 部分中添加了 TL07xH 器件 1
- 在*器件信息* 部分中添加了 SOT-23 (14)、VSSOP (8)、SOT-23 (8)、SC70 (5) 和 SOT-23 (5) 封装 1
- 在*引脚配置和功能* 部分中为 TL072x 添加了 TSSOP、VSSOP 和 DDF 封装 4
- 在*引脚配置和功能* 部分中为 TL074x 添加了 DYY 封装 4
- 删除了*典型特性* 部分中的图形列表 26
- 删除了*布局指南* 部分中对过时文档的参考 35
- 删除了*相关文档* 部分 37

Changes from Revision M (February 2014) to Revision N (July 2017) **Page**

- 根据最新文档和翻译标准更新了数据表文本 1
- 向数据表添加了 TL072M 和 TL074M 器件 1
- 重写了*说明* 部分中的文本 1
- 将*器件信息* 表中 TL07x 8 引脚 PDIP 封装更改为 8 引脚 CDIP 封装 1
- 删除了*器件信息* 表中的 20 引脚 LCCC 封装 1
- 在首页原理图中添加了 2017 年版权声明 1
- 删除了*引脚配置和功能* 部分的 TL071x FK (LCCC) 引脚图和引脚表 4
- 更新了*引脚配置和功能* 部分的引脚图和引脚表 4
- 将 图 6-59 添加到*典型特性* 部分 26
- 添加了*典型应用* 部分的第二条应用曲线 33
- 更改了*布局指南* 部分中的文档参考 35

Changes from Revision L (February 2014) to Revision M (February 2014) **Page**

- 添加了*器件信息* 表、*引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实现* 部分、*电源相关建议* 部分、*布局* 部分 1

5 引脚配置和功能

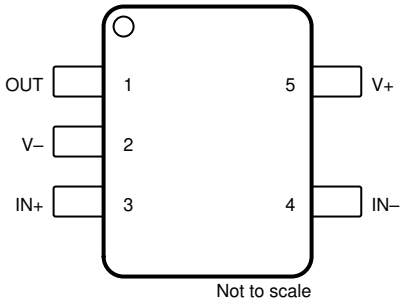


图 5-1. TL071H DBV 封装，5 引脚 SOT-23（顶视图）

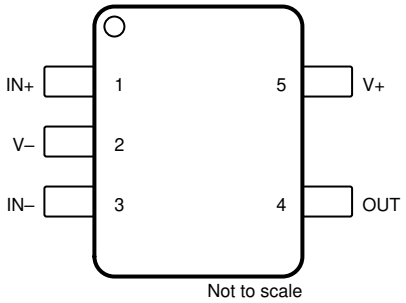
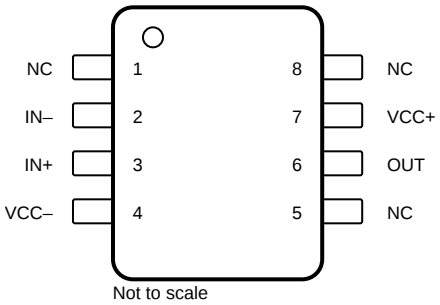


图 5-2. TL071H DCK 封装，5 引脚 SC70（顶视图）



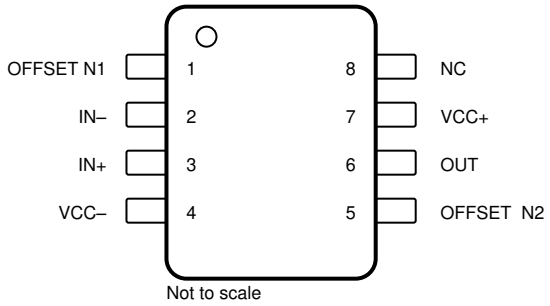
NC = 没有与内部电路连接

图 5-3. TL071H D 封装，8 引脚 SOIC（顶视图）

表 5-1. 引脚功能：TL071H

引脚				I/O	说明
名称	DBV	DCK	D		
IN –	4	3	2	I	反相输入
IN+	3	1	3	I	同相输入
NC	—	—	8	—	不连接
NC	—	—	1	—	不连接
NC	—	—	5	—	不连接
OUT	1	4	6	O	输出
VCC –	2	2	4	—	电源
VCC+	5	5	7	—	电源

Copyright © 2023 Texas Instruments Incorporated



NC = 没有与内部电路连接

图 5-4. TL071x D、P 和 PS 封装，8 引脚 SOIC、PDIP 和 SO（顶视图）

表 5-2. 引脚功能：TL071x

引脚		I/O	说明
名称	编号		
IN –	2	I	反相输入
IN+	3	I	同相输入
NC	8	—	不连接
OFFSET N1	1	—	输入失调电压调节
OFFSET N2	5	—	输入失调电压调节
OUT	6	O	输出
VCC –	4	—	电源
VCC+	7	—	电源

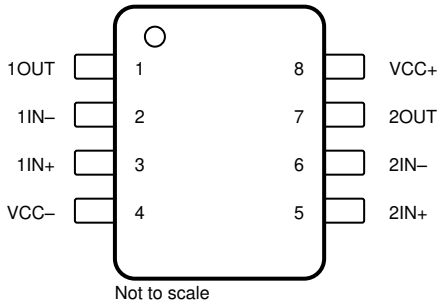
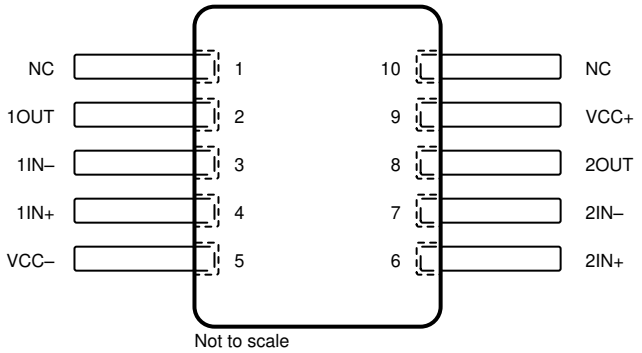


图 5-5. TL072x D、DDF、JG、P、PS 和 PW 封装，8 引脚 SOIC、SOT-23、CDIP、PDIP、SO 和 TSSOP（顶视图）

表 5-3. 引脚功能：TL072x

引脚		I/O	说明
名称	编号		
1IN –	2	I	反相输入
1IN+	3	I	同相输入
1OUT	1	O	输出
2IN –	6	I	反相输入
2IN+	5	I	同相输入
2OUT	7	O	输出
VCC –	4	—	电源
VCC+	8	—	电源

Copyright © 2023 Texas Instruments Incorporated

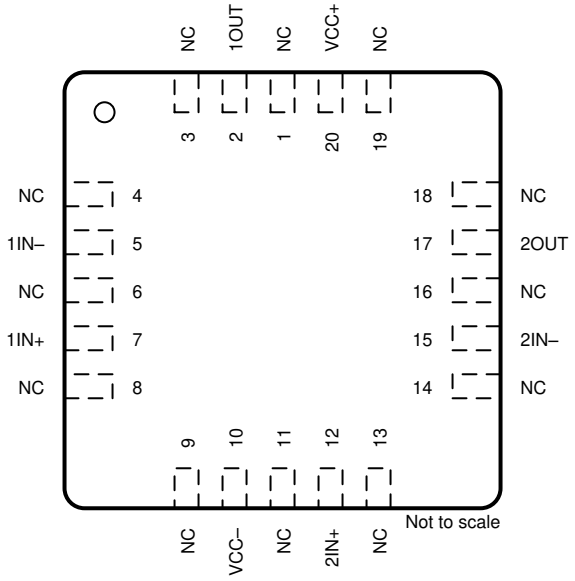


NC = 没有与内部电路连接

图 5-6. TL072x U 封装，
10 引脚 CFP
（顶视图）

表 5-4. 引脚功能：TL072x

引脚		I/O	说明
名称	编号		
1IN –	3	I	反相输入
1IN+	4	I	同相输入
1OUT	2	O	输出
2IN –	7	I	反相输入
2IN+	6	I	同相输入
2OUT	8	O	输出
NC	1、10	—	不连接
VCC –	5	—	电源
VCC+	9	—	电源



NC = 没有与内部电路连接

图 5-7. TL072 FK 封装
20 引脚 LCCC
（顶视图）

表 5-5. 引脚功能：TL072x

引脚		I/O	说明
名称	编号		
1IN –	5	I	反相输入
1IN+	7	I	同相输入
1OUT	2	O	输出
2IN –	15	I	反相输入
2IN+	12	I	同相输入
2OUT	17	O	输出
NC	1、3、4、6、8、9、11、13、14、16、18、19	—	不连接
VCC –	10	—	电源
VCC+	20	—	电源

Copyright © 2023 Texas Instruments Incorporated

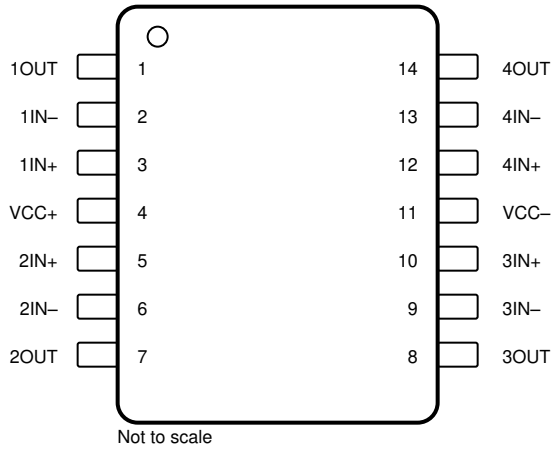
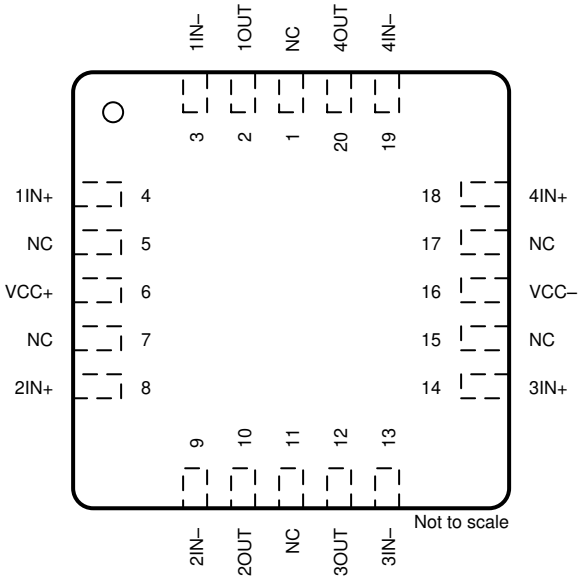


图 5-8. TL074x D、N、NS、PW、J、DYY 和 W 封装，14 引脚 SOIC、PDIP、SO、TSSOP、CDIP、SOT-23 和 CFP（顶视图）

表 5-6. 引脚功能：TL074x

引脚		I/O	说明
名称	编号		
1IN –	2	I	反相输入
1IN+	3	I	同相输入
1OUT	1	O	输出
2IN –	6	I	反相输入
2IN+	5	I	同相输入
2OUT	7	O	输出
3IN –	9	I	反相输入
3IN+	10	I	同相输入
3OUT	8	O	输出
4IN –	13	I	反相输入
4IN+	12	I	同相输入
4OUT	14	O	输出
V_{CC-}	11	—	电源
V_{CC+}	4	—	电源



NC = 没有与内部电路连接

图 5-9. TL074 FK 封装，
20 引脚 LCCC
（顶视图）

表 5-7. 引脚功能：TL074x

引脚		I/O	说明
名称	编号		
1IN –	3	I	反相输入
1IN+	4	I	同相输入
1OUT	2	O	输出
2IN –	9	I	反相输入
2IN+	8	I	同相输入
2OUT	10	O	输出
3IN –	13	I	反相输入
3IN+	14	I	同相输入
3OUT	12	O	输出
4IN –	19	I	反相输入
4IN+	18	I	同相输入
4OUT	20	O	输出
NC	1、5、7、11、15、17	—	不连接
VCC –	16	—	电源
VCC+	6	—	电源

Copyright © 2023 Texas Instruments Incorporated

6 规格

6.1 绝对最大额定值

在工作环境温度范围内（除非另有说明）[1]

			最小值	最大值	单位
电源电压，V_S = (V+) – (V–)		所有 NS 和 PS 封装；所有 TL07xM 器件	-0.3	36	V
		所有其他器件	0	42	V
信号输入引脚	共模电压[3]	所有 NS 和 PS 封装；所有 TL07xM 器件	(V–) – 0.3	(V–) + 36	V
		所有其他器件	(V–) – 0.5	(V+) + 0.5	V
	差分电压[3]	所有 NS 和 PS 封装；所有 TL07xM 器件[4]	(V–) – 0.3	(V–) + 36	V
		所有其他器件		V_S + 0.2	V
	电流[3]	所有 NS 和 PS 封装；所有 TL07xM 器件		50	mA
		所有其他器件	-10	10	mA
输出短路[2]			持续		
工作环境温度，T_A			-55	150	°C
结温，T_J				150	°C
60 秒内的外壳温度 - FK 封装				260	°C
10 秒内距离外壳 1.8mm（1/16 英寸）的引线温度				300	°C
贮存温度，T_{stg}			-65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力等级，这并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间在最大绝对额定条件下运行会影响器件可靠性。
(2) 接地短路，每个封装对应一个放大器。
(3) 输入引脚被二极管钳制至电源轨。摆幅超过电源轨 0.5V 的输入信号的电流必须限制在 10mA 或者更少。
(4) 差分电压仅受输入电压限制。

6.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准[1]	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101[2]	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文件 JEP157 指出：250V CDM 可实现在标准 ESD 控制流程下安全生产。

6.3 建议运行条件

在工作环境温度范围内测得（除非另外注明）

			最小值	最大值	单位
V_S	电源电压，(V+) – (V–)	所有 NS 和 PS 封装；所有 TL07xM 器件[1]	10	30	V
		所有其他器件	4.5	40	V
V_I	输入电压范围	所有 NS 和 PS 封装；所有 TL07xM 器件	(V–) + 2	(V+)+0.1	V
		所有其他器件	(V–) + 4	(V+)+0.1	V
T_A	额定温度	TL07xM	–55	125	°C
		TL07xH	-40	125	°C
		TL07xI	–40	85	°C
		TL07xC	0	70	°C

(1) V+ 和 V– 不要求具有相同的幅度，只要总 V_S (V+ – V–) 介于 10V 与 30V 之间即可。

6.4 单通道器件的热性能信息

热指标 (1)		TL071xx					单位
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	P (PDIP)	PS (SO)	
		8 引脚	5 引脚	5 引脚	8 引脚	8 引脚	
$R_{\theta JA}$	结至环境热阻	158.8	217.5	212.2	85	95	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	98.6	113.1	111.1	–	-	°C/W
$R_{\theta JB}$	结至电路板热阻	102.3	63.8	79.4	–	-	°C/W
ψ_{JT}	结至顶部特征参数	45.8	34.8	51.8	–	-	°C/W
ψ_{JB}	结至电路板特征参数	101.5	63.5	79.0	–	-	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	不适用	不适用	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告，SPRA953。

6.5 双通道器件的热性能信息

热指标 (1)		TL072xx								单位
		D (SOIC)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SO)	PW (TSSOP)	U (CFP)	
		8 引脚	8 引脚	20 引脚	8 个引脚	8 引脚	8 引脚	8 引脚	10 引脚	
$R_{\theta JA}$	结至环境热阻	147.8	181.5	–	-	85	95	200.3	169.8	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	88.2	112.5	5.61	15.05	–	-	89.4	62.1	°C/W
$R_{\theta JB}$	结至电路板热阻	91.4	98.2	–	-	-	-	131.0	176.2	°C/W
ψ_{JT}	结至顶部特征参数	36.8	17.2	–	-	-	-	22.2	48.4	°C/W
ψ_{JB}	结至电路板特征参数	90.6	97.6	–	-	-	-	129.3	144.1	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	–	-	-	-	不适用	5.4	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告，SPRA953。

Copyright © 2023 Texas Instruments Incorporated

6.6 四通道器件的热性能信息

热指标 (1)		TL074xx								单位
		D (SOIC)	DYY (SOT-23)	FK (TSSOP)	J (TSSOP)	N (TSSOP)	NS (TSSOP)	PW (TSSOP)	W (TSSOP)	
		14 引脚	14 引脚	20 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	114.2	153.2	–	-	80	76	-	128.8	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	70.3	88.7	5.61	14.5	–	-	14.5	56.1	°C/W
$R_{\theta JB}$	结至电路板热阻	70.2	65.4	–	-	-	-	-	127.6	°C/W
ψ_{JT}	结至顶部特征参数	28.8	9.5	–	-	-	-	-	29	°C/W
ψ_{JB}	结至电路板特征参数	69.8	65.0	–	-	-	-	-	106.1	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	–	-	-	-	-	0.5	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告，SPRA953。

6.7 电气特性：TL07xH

$V_S = (V_{CC+}) - (V_{CC-}) = 4.5V$ 至 40V（±2.25V 至 ±20V），$T_A = 25°C$，$R_L = 10k\Omega$ 连接至 $V_S/2$，$V_{CM} = V_S/2$，且 $V_{OUT} = V_S / 2$（除非另有说明）。

参数		测试条件		最小值	典型值	最大值	单位
失调电压							
V_{OS}	输入失调电压				±1	±4	mV
			T_A = –40°C 至 125°C			±5	
dV_{OS}/dT	输入失调电压漂移		T_A = –40°C 至 125°C		±2		μV/℃
PSRR	输入失调电压与电源间的关系	V_S = 5V 至 40V，$V_{CM} = V_S/2$	T_A = –40°C 至 125°C		±1	±10	μV/V
	通道分离	f = 0Hz			10		μV/V
输入偏置电流							
I_B	输入偏置电流				±1	±120	pA
			DCK 和 DBV 封装		±1	±300	pA
			T_A = –40°C 至 125°C(1)			±5	nA
I_{OS}	输入失调电流				±0.5	±120	pA
			DCK 和 DBV 封装		±0.5	±250	pA
			T_A = –40°C 至 125°C(1)			±5	nA
噪声							
E_N	输入电压噪声	f = 0.1Hz 至 10Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	输入电压噪声密度	f = 1kHz			37		nV/√Hz
		f = 10kHz			21		
i_N	输入电流噪声	f = 1kHz			80		fA/√Hz
输入电压范围							
V_{CM}	共模电压范围			(V_{CC-}) + 1.5		(V_{CC+})	V
CMRR	共模抑制比	V_S = 40V，(V_{CC-}) + 2.5V < V_{CM} < (V_{CC+}) – 1.5V		100	105		dB
			T_A = –40°C 至 125°C	95			dB
		V_S = 40V，(V_{CC-}) + 2.5V < V_{CM} < (V_{CC+})		90	105		dB
			T_A = –40°C 至 125°C	80			dB
输入电容							
Z_{ID}	差分				100 || 2		MΩ || pF
Z_{ICM}	共模				6 || 1		TΩ || pF
开环增益							
A_{OL}	开环电压增益	V_S = 40V，$V_{CM} = V_S/2$，(V_{CC-}) + 0.3V < V_O < (V_{CC+}) – 0.3V	T_A = –40°C 至 125°C	118	125		dB
A_{OL}	开环电压增益	V_S = 40V，$V_{CM} = V_S/2$，R_L = 2kΩ，(V_{CC-}) + 1.2V < V_O < (V_{CC+}) – 1.2V	T_A = –40°C 至 125°C	115	120		dB
频率响应							
GBW	增益带宽积				5.25		MHz
SR	压摆率	V_S = 40V，G = +1，C_L = 20pF			20		V/μs
t_S	建立时间	精度达到 0.1%，V_S = 40V，V_{STEP} = 10V，G = +1，CL = 20pF			0.63		μs
		精度达到 0.1%，V_S = 40V，V_{STEP} = 2V，G = +1，CL = 20pF			0.56		
		精度达到 0.01%，V_S = 40V，V_{STEP} = 10V，G = +1，CL = 20pF			0.91		
		精度达到 0.01%，V_S = 40V，V_{STEP} = 2V，G = +1，CL = 20pF			0.48		
	相位裕度	G = +1，R_L = 10kΩ，C_L = 20pF			56		°

Copyright © 2023 Texas Instruments Incorporated

6.7 电气特性：TL07xH (continued)

$V_S = (V_{CC+}) - (V_{CC-}) = 4.5V$ 至 40V（±2.25V 至 ±20V），$T_A = 25°C$，$R_L = 10k\Omega$ 连接至 $V_S/2$，$V_{CM} = V_S/2$，且 $V_{OUT} = V_S / 2$（除非另有说明）。

参数		测试条件		最小值	典型值	最大值	单位
	过载恢复时间	V_{IN} × 增益 > V_S			300		ns
THD+N	总谐波失真 + 噪声	$V_S = 40V$，$V_O = 6V_{RMS}$，G = +1，f = 1kHz			0.00012		%
EMIRR	EMI 抑制比	f = 1GHz			53		dB
输出							
	相对于电源轨的电压输出摆幅	正电源轨余量	$V_S = 40V$，$R_L = 10k\Omega$		115	210	mV
			$V_S = 40V$，$R_L = 2k\Omega$		520	965	
		负电源轨余量	$V_S = 40V$，$R_L = 10k\Omega$		105	215	
			$V_S = 40V$，$R_L = 2k\Omega$		500	1030	
I_{SC}	短路电流				±26		mA
C_{LOAD}	容性负载驱动				300		pF
Z_O	开环输出阻抗	f=1MHz，$I_O = 0A$			125		Ω
电源							
I_Q	每个放大器的静态电流	$I_O = 0A$			937.5	1125	μA
		$I_O = 0A$，(TL071H)			960	1156	
		$I_O = 0A$	T_A = –40°C 至 125°C			1130	
		$I_O = 0A$，(TL072H)				1143	
		$I_O = 0A$，(TL071H)				1160	
	开通时间	$T_A = 25°C$，$V_S = 40V$，V_S 升降速率 > 0.3V/μs			60		μs

(1) 根据表征结果指定最大 I_B 和 I_{os}。

6.8 电气特性（直流）：TL07xC、TL07xAC、TL07xBC、TL07xI、TL07xM

对于 $V_S = (V_{CC+}) - (V_{CC-}) = \pm15V$，$T_A = 25°C$ 时（除非另有说明）

参数		测试条件(1) (2)			最小值	典型值	最大值	单位
V_{OS}	输入失调电压	$V_O = 0V$ $R_S = 50\Omega$	TL07xC			3	10	mV
				T_A = 完整范围			13	
			TL07xAC			3	6	
				T_A = 完整范围			7.5	
			TL07xBC			2	3	
				T_A = 完整范围			5	
			TL07xI			3	6	
				T_A = 完整范围			8	
			TL071M、TL072M			3	6	
				T_A = 完整范围			9	
			TL074M			3	9	
				T_A = 完整范围			15	
dV_{OS}/dT	输入失调电压漂移	$V_O = 0V$，$R_S = 50\Omega$	T_A = 完整范围			±18		μV/℃
I_{OS}	输入失调电流	$V_O = 0V$	TL07xC			5	100	pA
				T_A = 完整范围			10	nA
			TL07xAC、TL07xBC、TL07xI			5	100	pA
				T_A = 完整范围			2	nA
			TL07xM			5	100	pA
				T_A = 完整范围			20	nA
I_B	输入偏置电流	$V_O = 0V$	TL07xC、TL07xAC、TL07xBC、TL07xI			65	200	pA
				T_A = 完整范围			7	nA
			TL071M、TL072M			65	200	pA
				T_A = 完整范围			50	nA
			TL074M			65	200	pA
				T_A = 完整范围			20	nA
V_{CM}	共模电压范围				±11	–12 至 15		V
VOM	最大峰值输出电压摆幅	$R_L = 10k\Omega$			±12	±13.5		V
		$R_L \geqslant 10k\Omega$	T_A = 完整范围		±12			
		$R_L \geqslant 2k\Omega$			±10			
A_{OL}	开环电压增益	$V_O = 0V$	TL07xC		25	200		V/mV
				T_A = 完整范围	15			
			TL07xAC、TL07xBC、TL07xI		50	200		
				T_A = 完整范围	25			
			TL07xM		35	200		
				T_A = 完整范围	15			
GBW	增益带宽积	所有 NS 和 PS 封装；所有 TL07xM 器件				3		MHz
		所有其他器件				5.25		
R_{ID}	共模输入电阻					1		TΩ
CMRR	共模抑制比	$V_{IC} = V_{ICR(min)}$ $V_O = 0V$ $R_S = 50\Omega$	TL07xC		70	100		dB
			TL07xAC、TL07xBC、TL07xI		75	100		
			TL07xM		80	86		
PSRR	输入失调电压与电源间的关系	$V_S = \pm9V$ 至 ± 18V $V_O = 0V$ $R_S = 50\Omega$	TL07xC		70	100		dB
			TL07xAC、TL07xBC、TL07xI		80	100		
			TL07xM		80	86		

Copyright © 2023 Texas Instruments Incorporated

6.8 电气特性（直流）：TL07xC、TL07xAC、TL07xBC、TL07xI、TL07xM (continued)

对于 $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15V$，$T_A = 25°C$ 时（除非另有说明）

参数		测试条件[(1) (2)]	最小值	典型值	最大值	单位
I_Q	每个放大器的静态电流	$V_O = 0$ V；空载		1.4	2.5	mA
	通道隔离	f = 0Hz		1		μV/V

(1) 除非另有说明，所有特性均在开环条件下以零共模电压测定。
(2) 对于 TL07xC、TL07xAC 和 TL07xBC，完整范围为 $T_A = 0°C$ 至 70°C；对于 TL07xI，$T_A = -40°C$ 至 85°C；对于 TL07xM，$T_A = -55°C$ 至 125°C。

6.9 电气特性（交流）：TL07xC、TL07xAC、TL07xBC、TL07xI、TL07xM

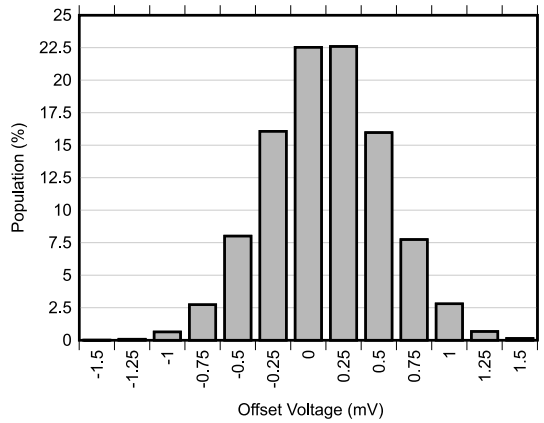
对于 $V_S = (V_{CC+}) - (V_{CC-}) = \pm15V$，$T_A = 25°C$ 时（除非另有说明）

参数		测试条件		最小值	典型值	最大值	单位
SR	压摆率	$V_I = 10V$，$C_L = 100pF$，$R_L = 2k\Omega$	TL07xM	5	20		V/μs
			TL07xC、TL07xAC、TL07xBC、TL07xI	8	20		V/μs
t_S	趋稳时间	$V_I = 20V$，$C_L = 100pF$，$R_L = 2k\Omega$			0.1		μs
					20%		
e_N	输入电压噪声密度	所有 PS 和 NS 封装；所有 TL07xM 器件	$R_S = 20\Omega$，f = 1kHz		18		nV/√Hz
		所有其他器件	f = 1kHz		37		nV/√Hz
			f = 10kHz		21		
E_N	输入电压噪声	所有 PS 和 NS 封装；所有 TL07xM 器件	$R_S = 20\Omega$，f = 10Hz 至 10kHz		4		μV_{RMS}
		所有其他器件	f = 0.1Hz 至 10Hz		1.4		μV_{RMS}
i_N	输入电流噪声	$R_S = 20\Omega$，f = 1kHz			10		fA/√Hz
	相位裕度	TL07xC、TL07xAC、TL07xBC、TL07xI	G = +1，$R_L = 10k\Omega$，$C_L = 20pF$		56		°
	过载恢复时间	V_{IN} × 增益 > V_S			300		ns
THD+N	总谐波失真 + 噪声	所有 PS 和 NS 封装；所有 TL07xM 器件	$V_O = 6V_{RMS}$，$R_L \geqslant 2k\Omega$，f = 1kHz，G = +1，$R_S \leqslant 1k\Omega$		0.003		%
		所有其他器件	$V_S = 40V$，$V_O = 6V_{RMS}$，G = +1，f = 1kHz		0.00012		%
EMIRR	EMI 抑制比	TL07xC、TL07xAC、TL07xBC、TL07xI	f = 1GHz		53		dB
Z_O	开环输出阻抗	TL07xC、TL07xAC、TL07xBC、TL07xI	f=1MHz，$I_O = 0A$		125		Ω

Copyright © 2023 Texas Instruments Incorporated

6.10 典型特性：TL07xH

T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S/2，R_{LOAD} = 10kΩ 连接至 V_S/2，且 C_L = 20pF（除非另外说明）



T_A = 25°C

图 6-1. 失调电压产生分布

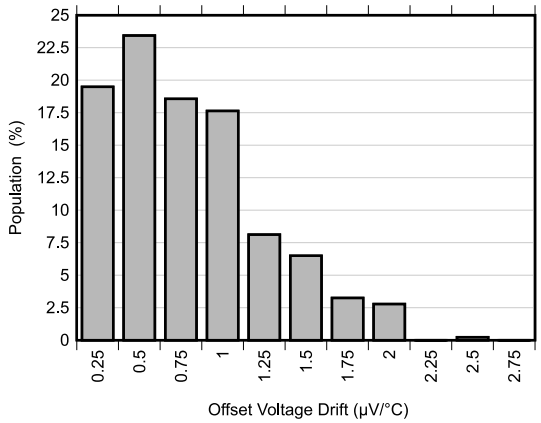
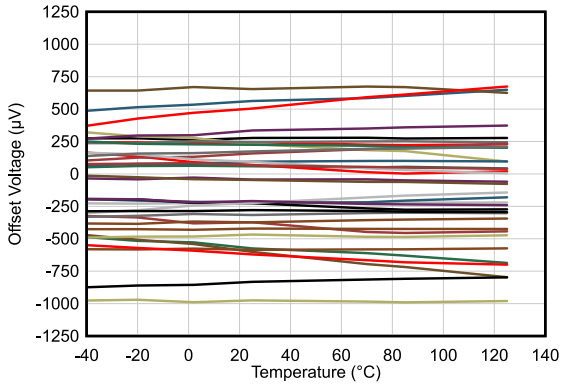
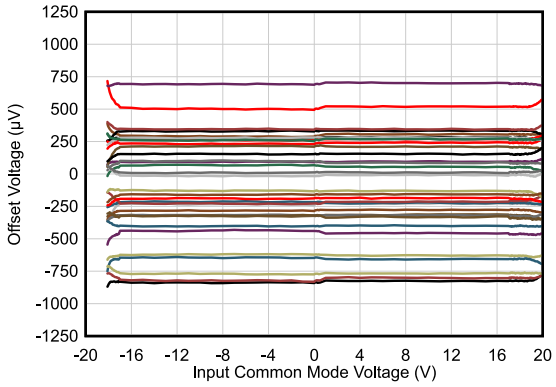


图 6-2. 失调电压漂移分布



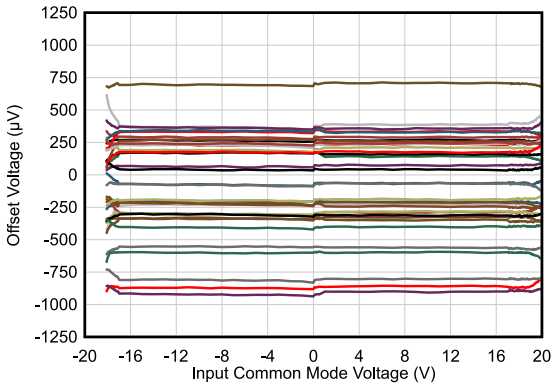
V_{CM} = V_S/2

图 6-3. 失调电压与温度间的关系



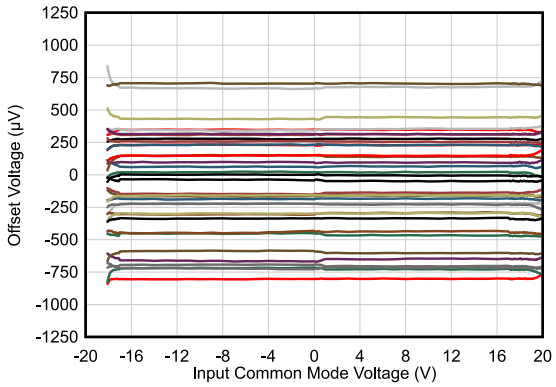
T_A = 25°C

图 6-4. 失调电压与共模电压间的关系



T_A = 125°C

图 6-5. 失调电压与共模电压间的关系



T_A = -40°C

图 6-6. 失调电压与共模电压间的关系

6.10 典型特性：TL07xH (continued)

T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S/2，R_{LOAD} = 10kΩ 连接至 V_S/2，且 C_L = 20pF（除非另外说明）

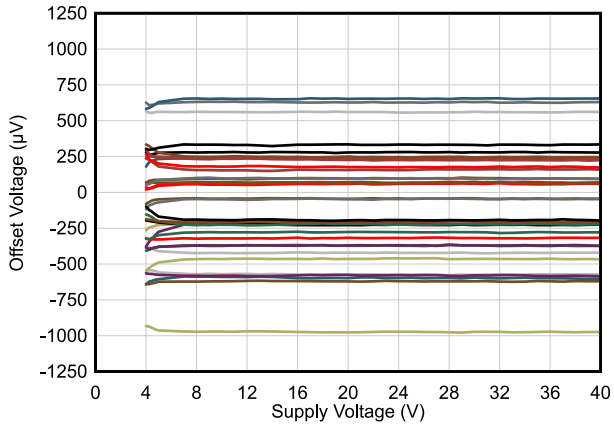


图 6-7. 失调电压与电源间的关系

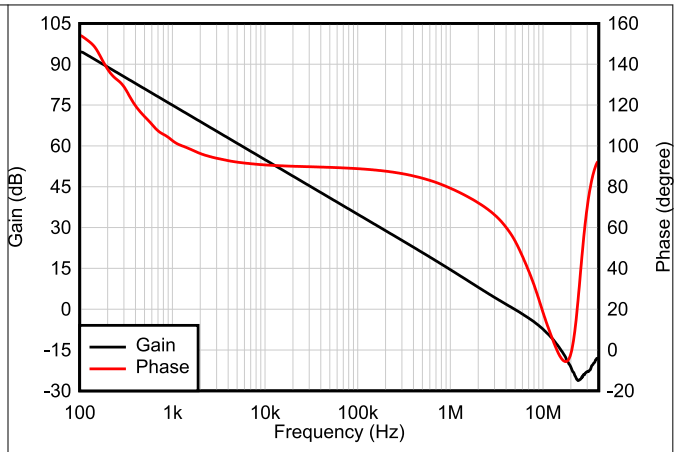


图 6-8. 开环增益和相位与频率间的关系

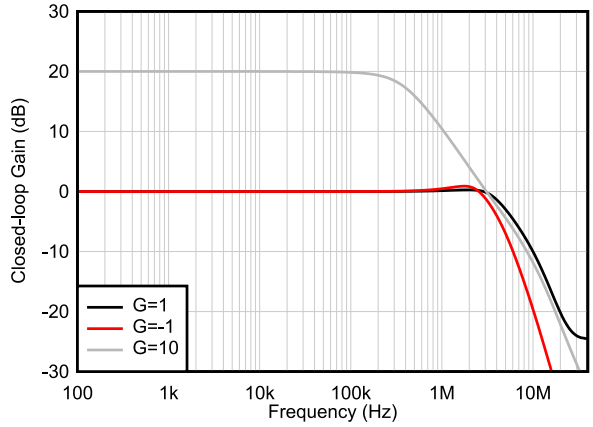


图 6-9. 闭环增益与频率间的关系

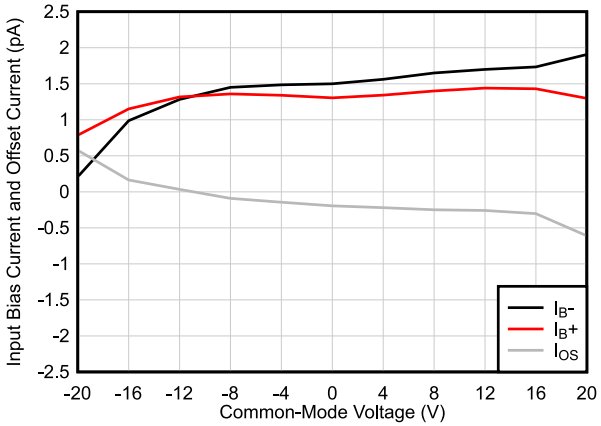


图 6-10. 输入偏置电流与共模电压间的关系

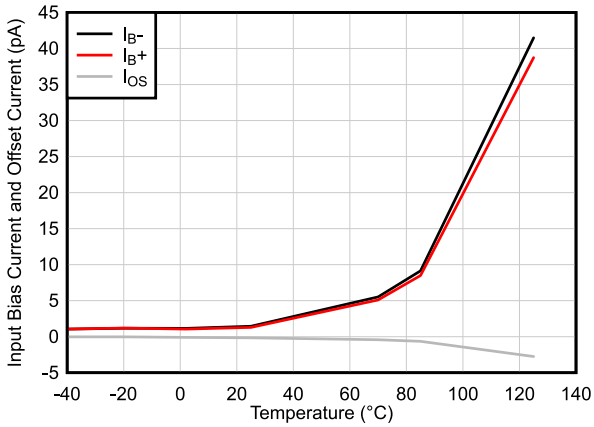


图 6-11. 输入偏置电流与温度间的关系

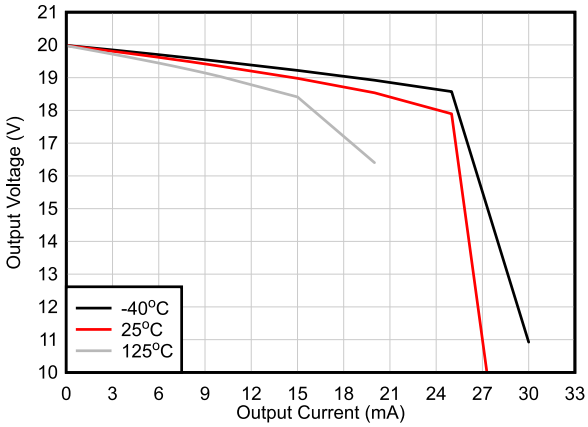


图 6-12. 输出电压摆幅与输出电流（拉电流）间的关系

Copyright © 2023 Texas Instruments Incorporated

6.10 典型特性：TL07xH (continued)

T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S/2，R_{LOAD} = 10kΩ 连接至 V_S/2，且 C_L = 20pF（除非另外说明）

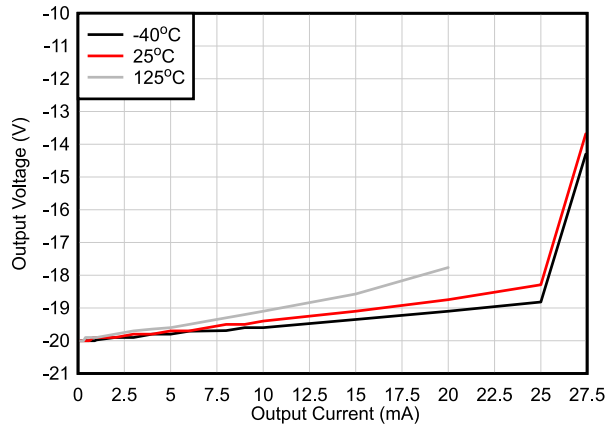


图 6-13. 输出电压摆幅与输出电流（灌电流）间的关系

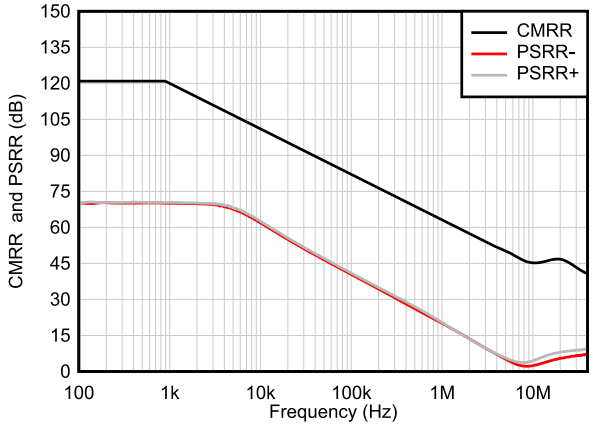
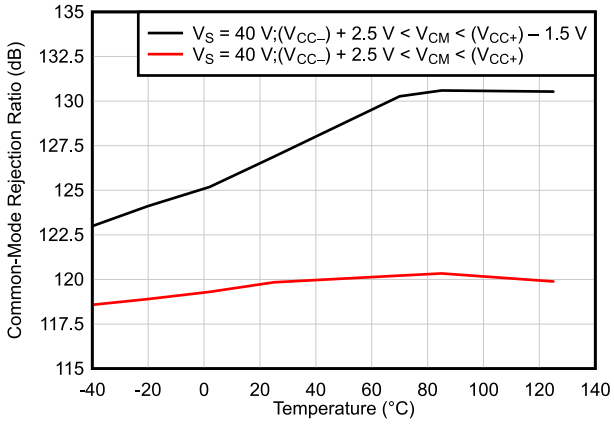
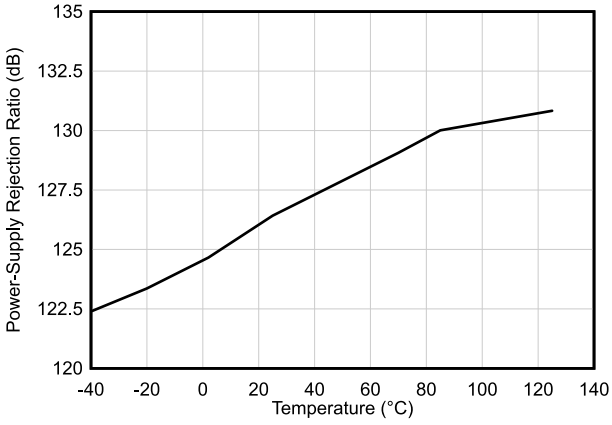


图 6-14. CMRR 和 PSRR 与频率间的关系



f = 0Hz

图 6-15. CMRR 与温度间的关系 (dB)



f = 0Hz

图 6-16. PSRR 与温度间的关系 (dB)

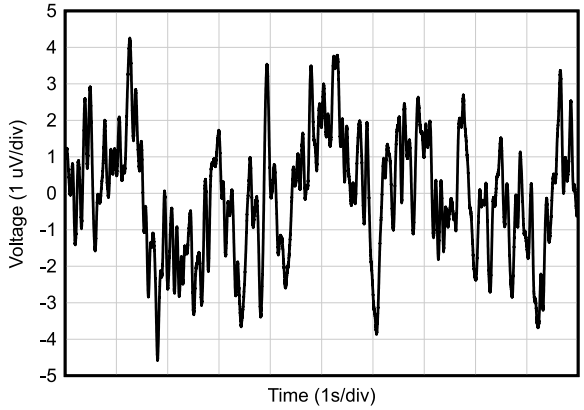


图 6-17. 0.1Hz 至 10Hz 噪声

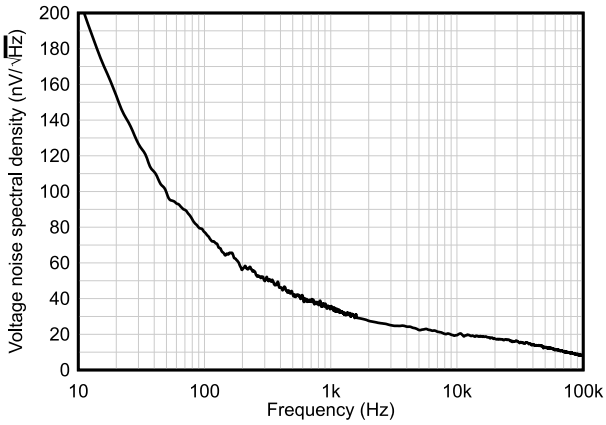
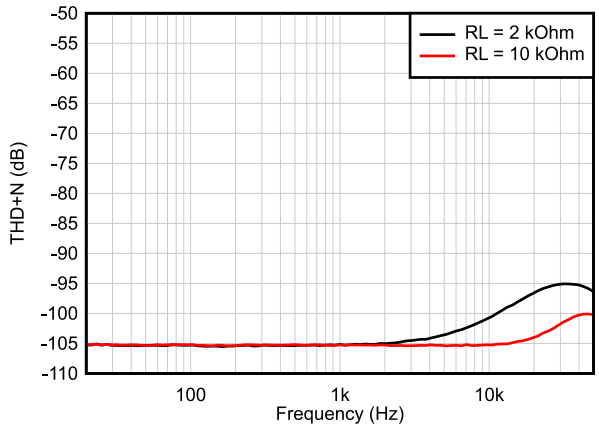


图 6-18. 输入电压噪声频谱密度与频率间的关系

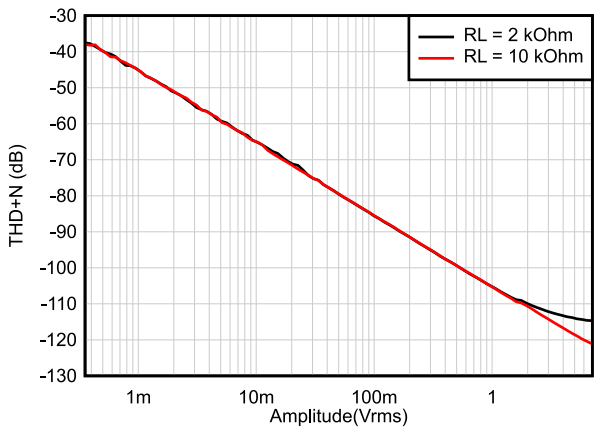
6.10 典型特性：TL07xH (continued)

T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S/2，R_{LOAD} = 10kΩ 连接至 V_S/2，且 C_L = 20pF（除非另外说明）



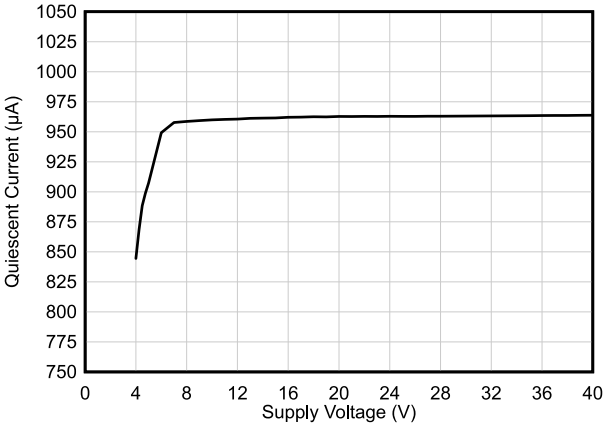
BW = 80kHz，V_{OUT} = 1V_{RMS}

图 6-19. THD+N 比与频率间的关系



BW = 80kHz，f = 1kHz

图 6-20. THD+N 与输出幅度间的关系



V_{CM} = V_S/2

图 6-21. 静态电流与电源电压间的关系

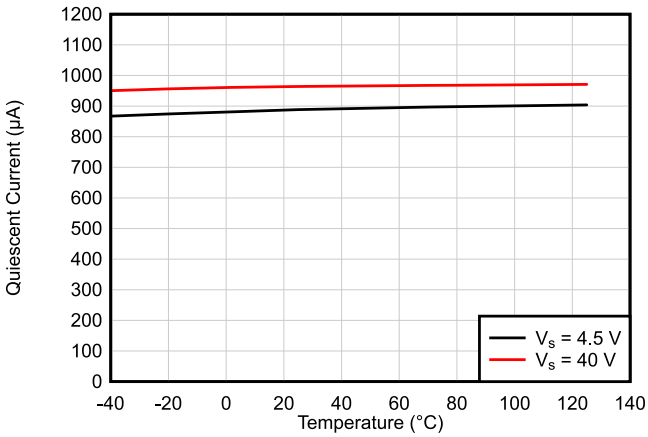


图 6-22. 静态电流与温度间的关系

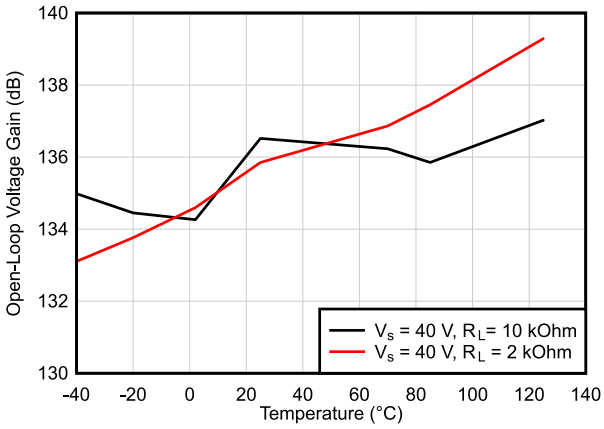


图 6-23. 开环电压增益与温度间的关系 (dB)

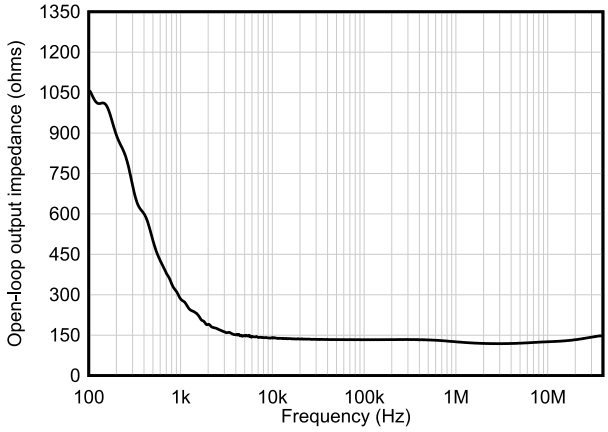
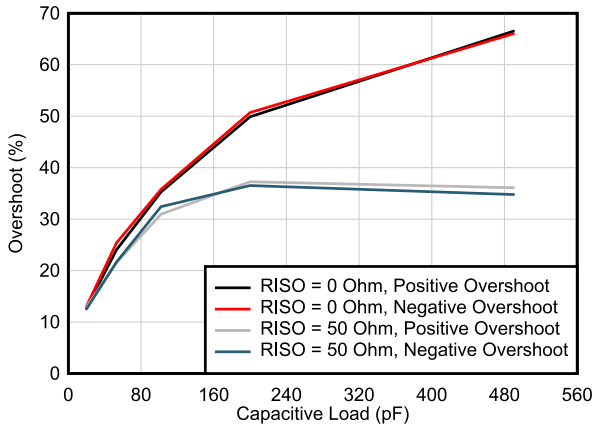


图 6-24. 开环输出阻抗与频率间的关系

Copyright © 2023 Texas Instruments Incorporated

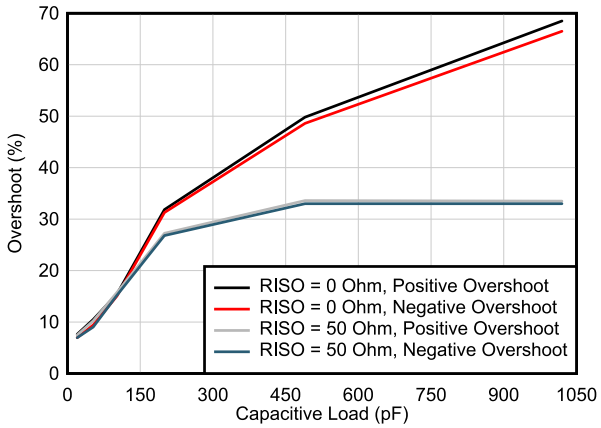
6.10 典型特性：TL07xH (continued)

T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S/2，R_{LOAD} = 10kΩ 连接至 V_S/2，且 C_L = 20pF（除非另外说明）



G = –1，25mV 输出阶跃

图 6-25. 小信号过冲与容性负载间的关系



G = 1，10mV 输出阶跃

图 6-26. 小信号过冲与容性负载间的关系

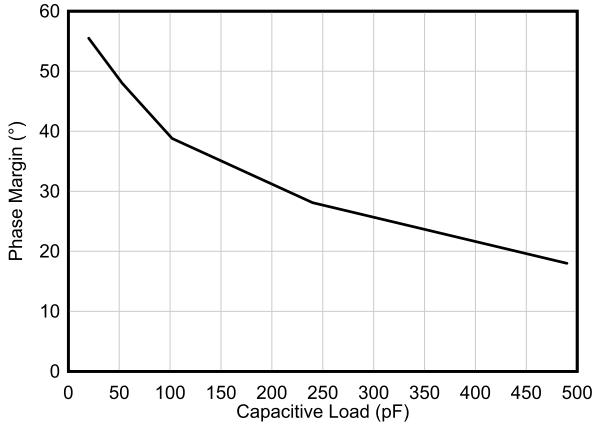
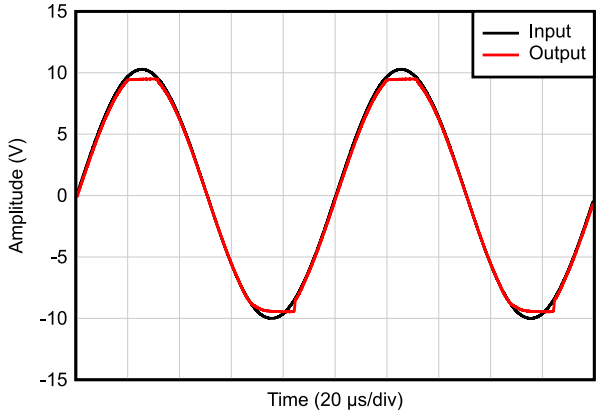
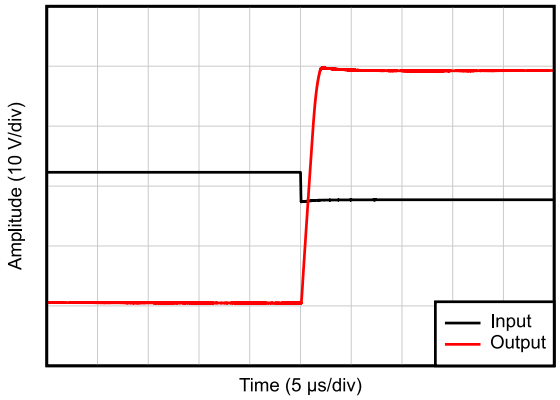


图 6-27. 相位裕度与容性负载间的关系



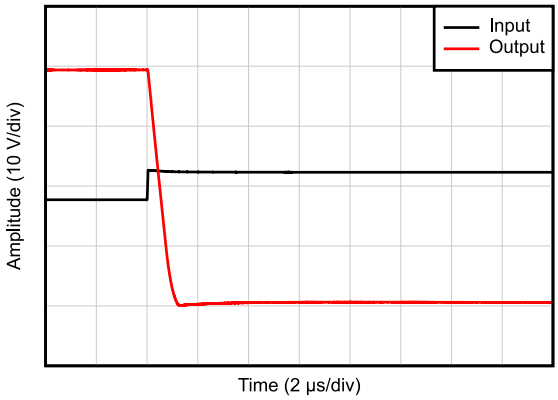
V_S = ±10V，V_{IN} = V_{OUT}

图 6-28. 无相位反转



G = -10

图 6-29. 正过载恢复

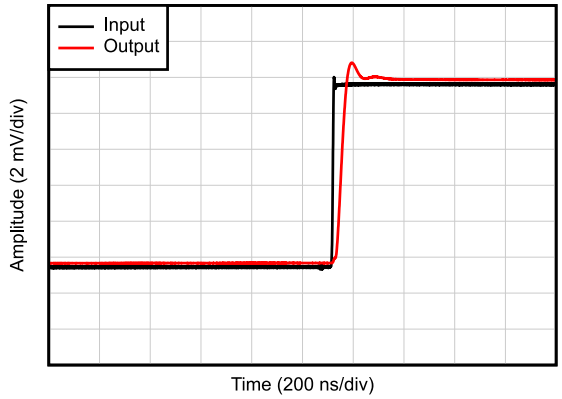


G = -10

图 6-30. 负过载恢复

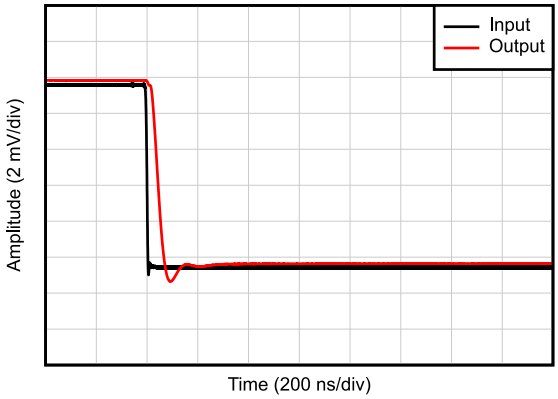
6.10 典型特性：TL07xH (continued)

T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S/2，R_{LOAD} = 10kΩ 连接至 V_S/2，且 C_L = 20pF（除非另外说明）



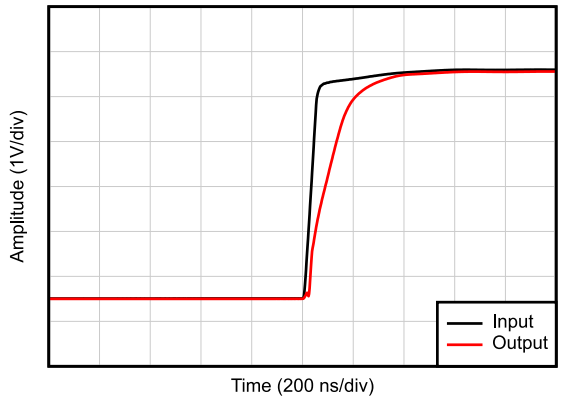
C_L = 20pF，G = 1，10mV 阶跃响应

图 6-31. 小信号阶跃响应，上升



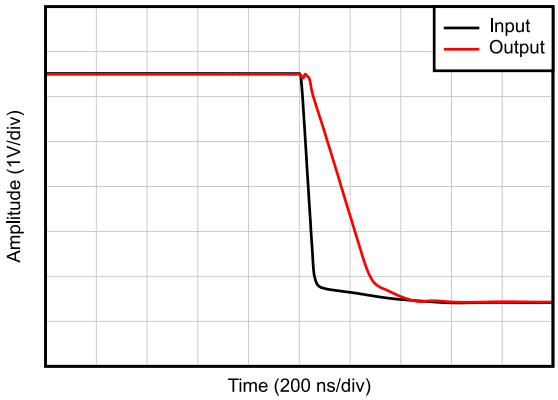
C_L = 20pF，G = 1，10mV 阶跃响应

图 6-32. 小信号阶跃响应，下降



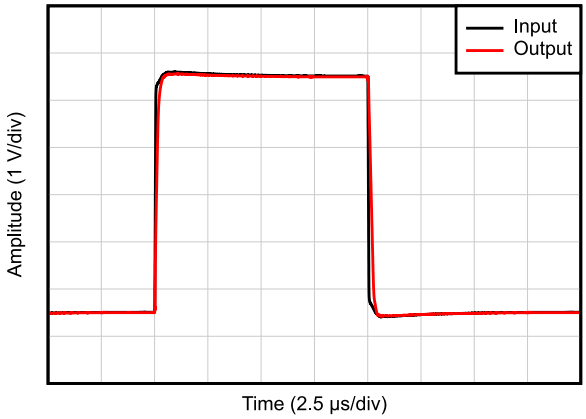
C_L = 20pF，G = 1

图 6-33. 大信号阶跃响应（上升）



C_L = 20pF，G = 1

图 6-34. 大信号阶跃响应（下降）



C_L = 20pF，G = 1

图 6-35. 大信号阶跃响应

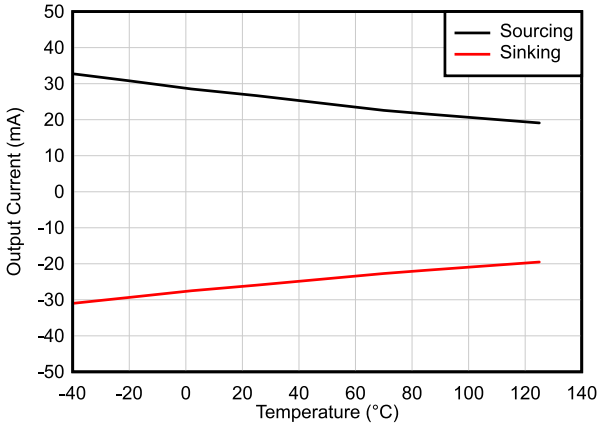


图 6-36. 短路电流与温度间的关系

Copyright © 2023 Texas Instruments Incorporated

6.10 典型特性：TL07xH (continued)

T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S/2，R_{LOAD} = 10kΩ 连接至 V_S/2，且 C_L = 20pF（除非另外说明）

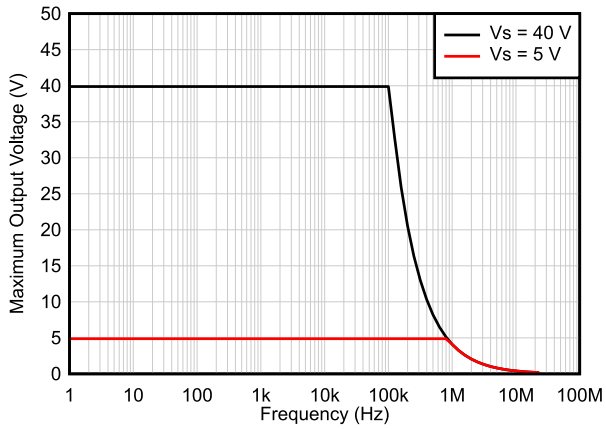


图 6-37. 最大输出电压与频率间的关系

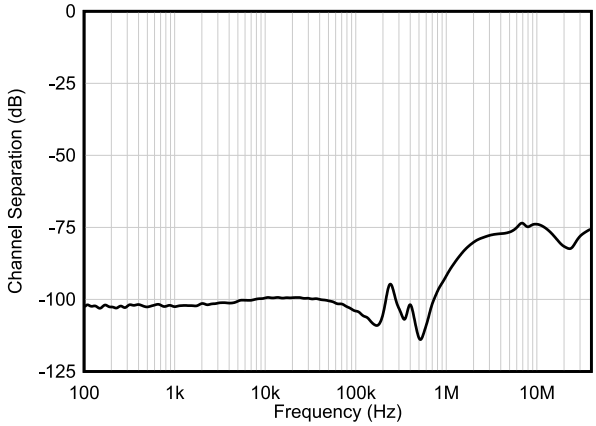


图 6-38. 通道隔离与频率间的关系

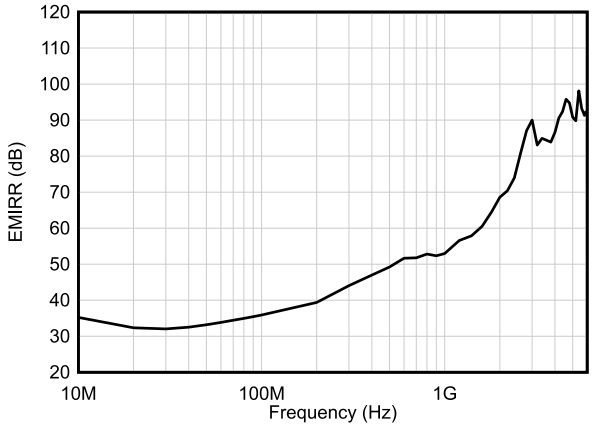


图 6-39. EMIRR（电磁干扰抑制比）与频率间的关系

6.11 典型特性：除 TL07xH 之外的所有器件

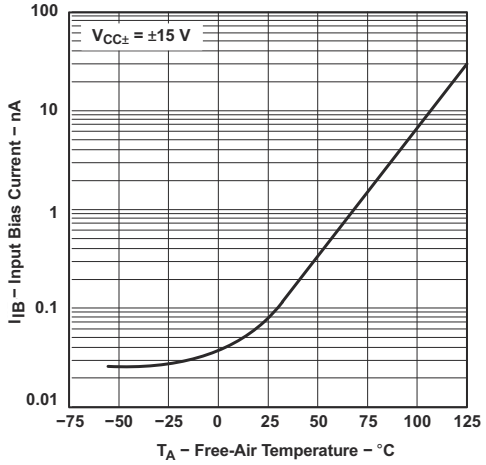


图 6-40. 输入偏置电流与自然通风温度间的关系

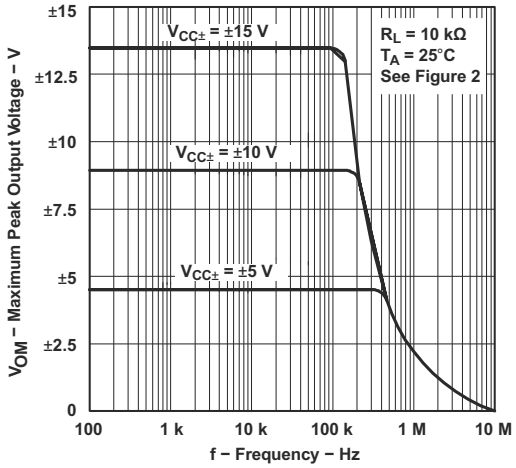


图 6-41. 最大峰值输出电压与频率间的关系

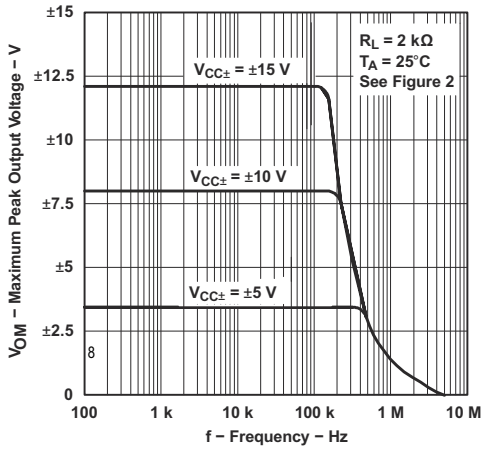


图 6-42. 最大峰值输出电压与频率间的关系

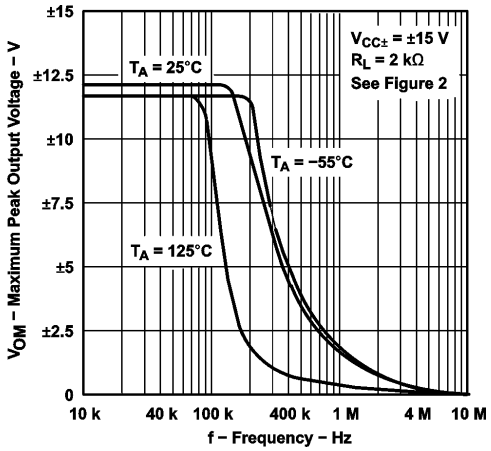


图 6-43. 最大峰值输出电压与频率间的关系

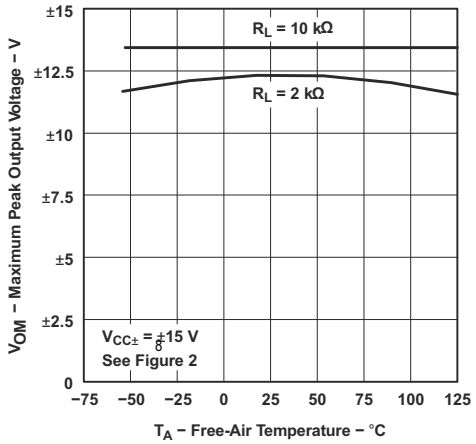


图 6-44. 最大峰值输出电压与自然通风温度间的关系

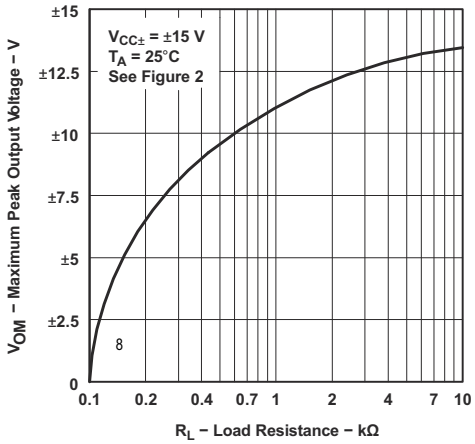


图 6-45. 最大峰值输出电压与负载电阻间的关系

Copyright © 2023 Texas Instruments Incorporated

6.11 典型特性：除 TL07xH 之外的所有器件 (continued)

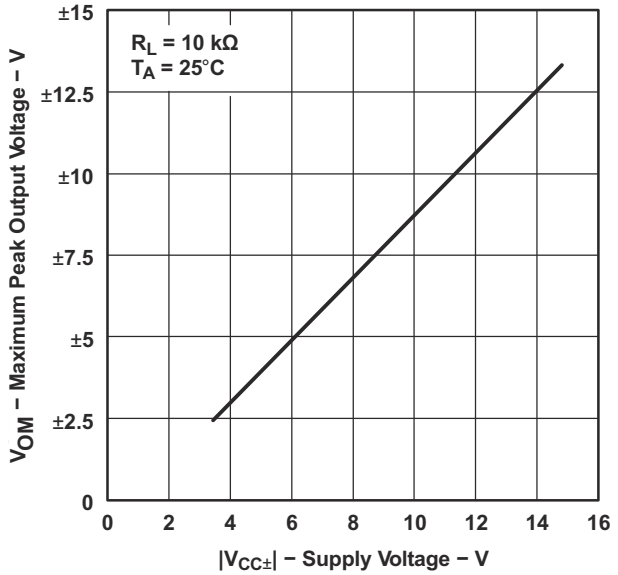


图 6-46. 最大峰值输出电压与电源电压间的关系

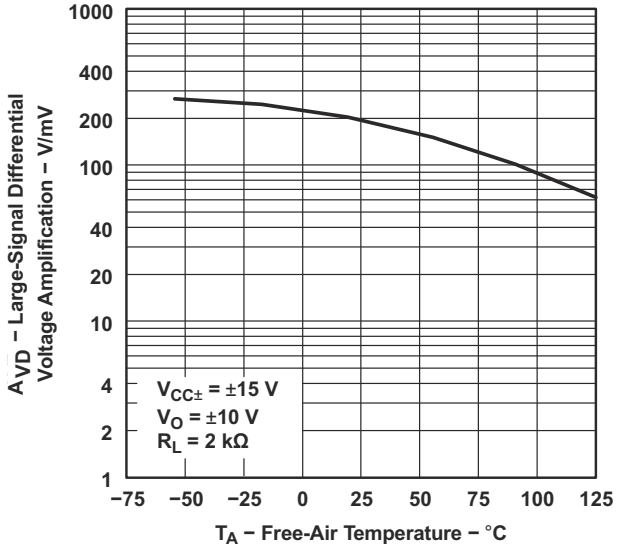


图 6-47. 大信号差分电压放大与自然通风温度间的关系

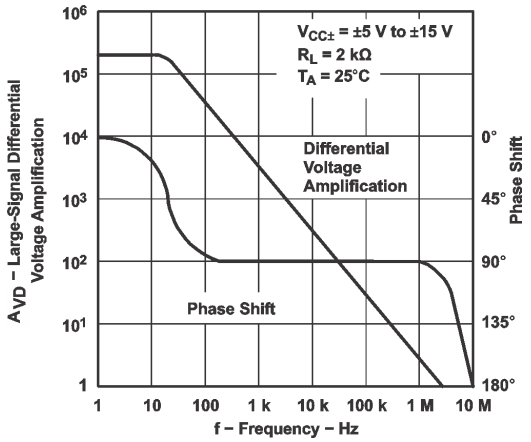


图 6-48. 大信号差分电压放大和相移与频率间的关系

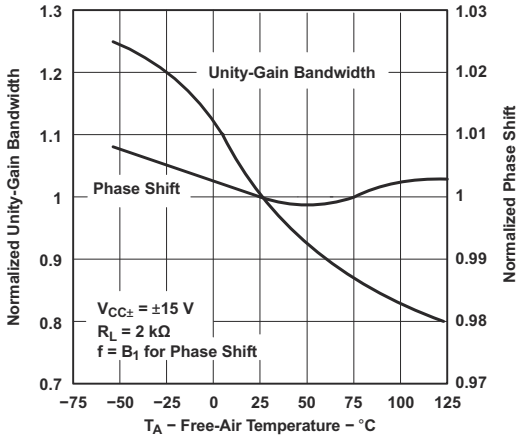


图 6-49. 标称单位增益带宽和相移与自然通风温度间的关系

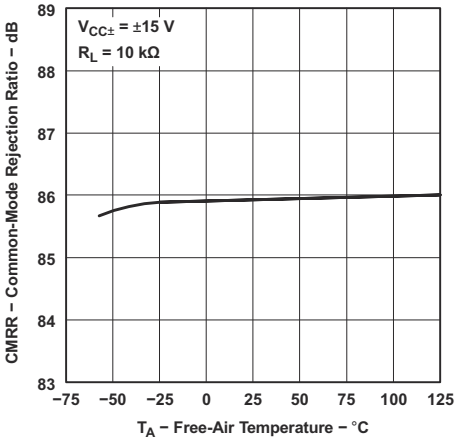


图 6-50. 共模抑制比与自然通风温度间的关系

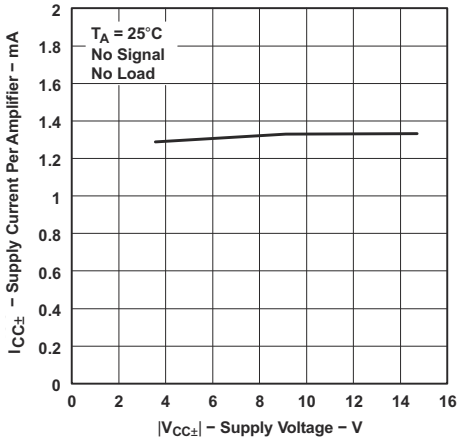


图 6-51. 每个放大器的电源电流与电源电压间的关系

6.11 典型特性：除 TL07xH 之外的所有器件 (continued)

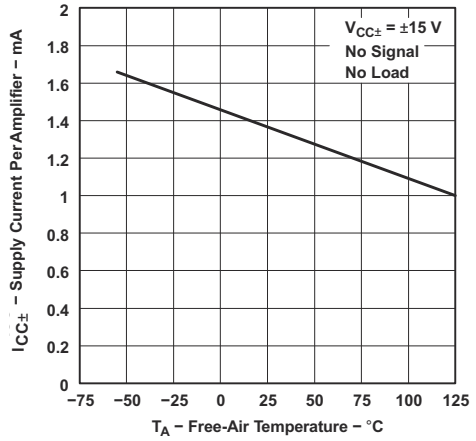


图 6-52. 每个放大器的电源电流与自然通风温度间的关系

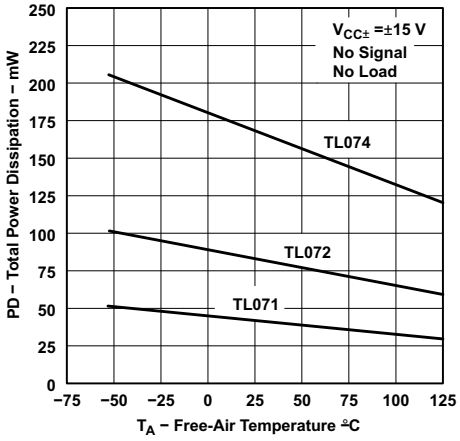


图 6-53. 总功率损耗与自然通风温度间的关系

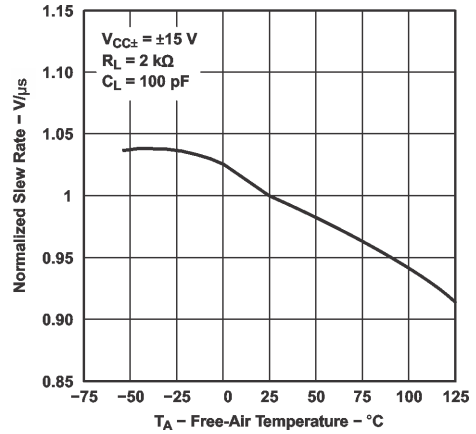


图 6-54. 标称压摆率与自然通风温度间的关系

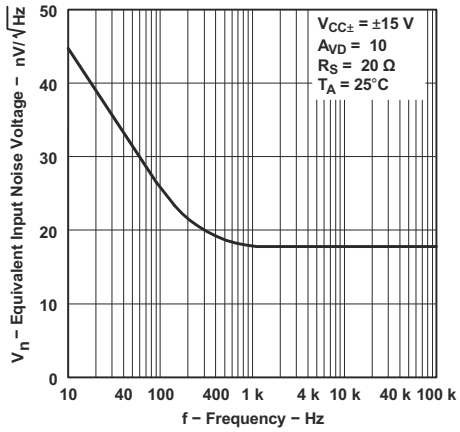


图 6-55. 等效输入噪声电压与频率间的关系

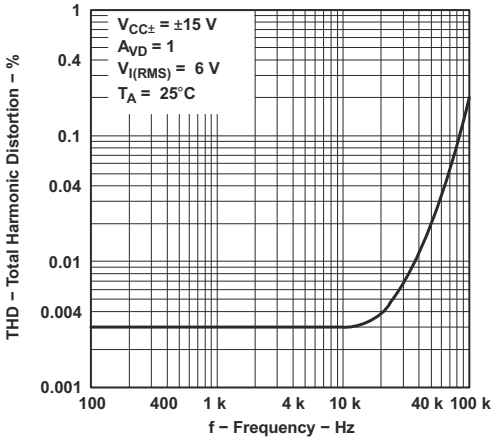


图 6-56. 总谐波失真与频率间的关系

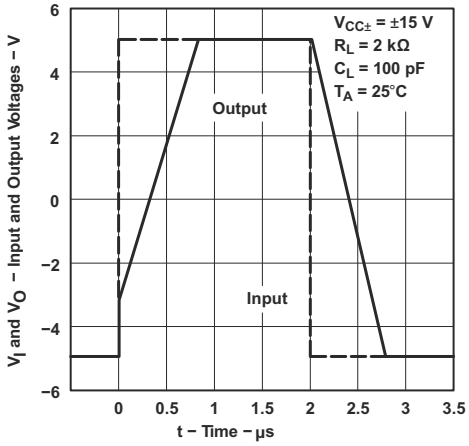


图 6-57. 电压跟随器大信号脉冲响应

Copyright © 2023 Texas Instruments Incorporated

6.11 典型特性：除 TL07xH 之外的所有器件 (continued)

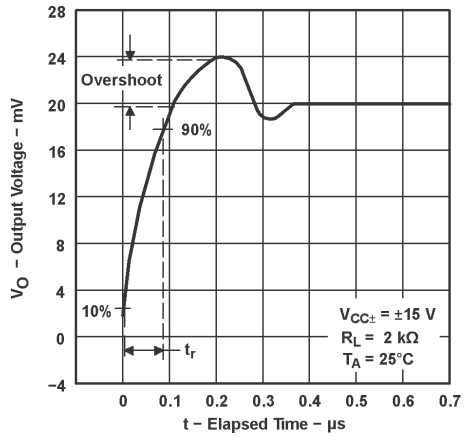


图 6-58. 输出电压与经历时间间的关系

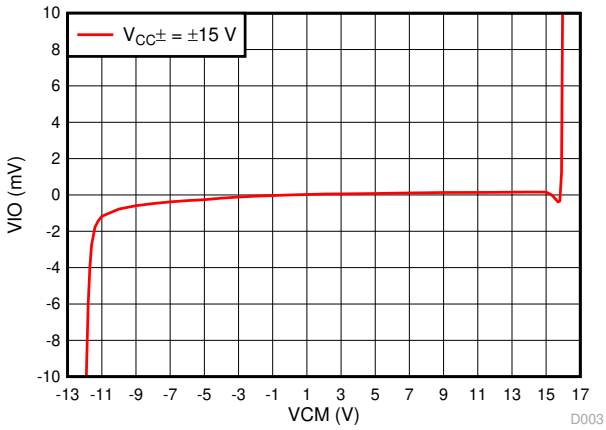


图 6-59. V_{IO} 与 V_{CM} 间的关系

7 参数测量信息

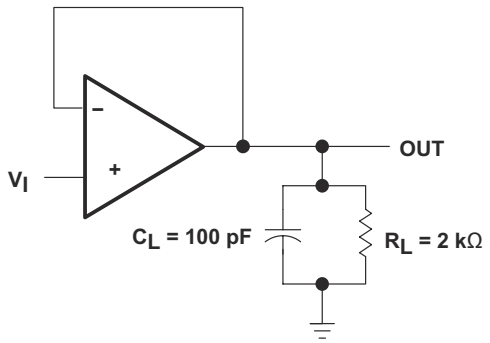


图 7-1. 单位增益放大器

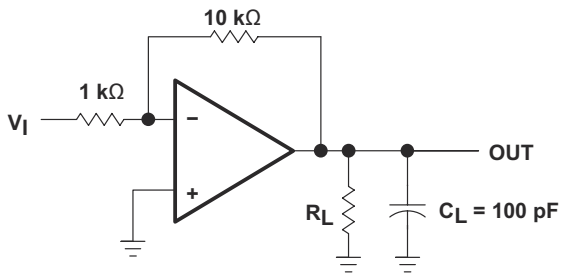


图 7-2. 增益为 10 的反相放大器

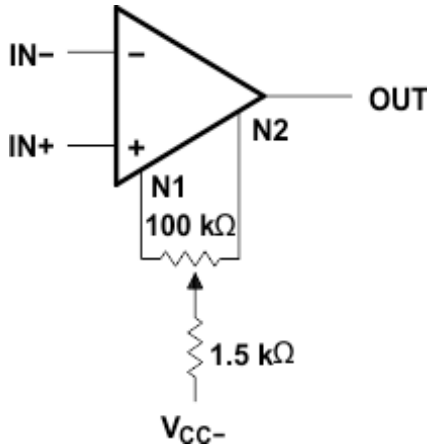


图 7-3. 输入失调电压零点电路

Copyright © 2023 Texas Instruments Incorporated

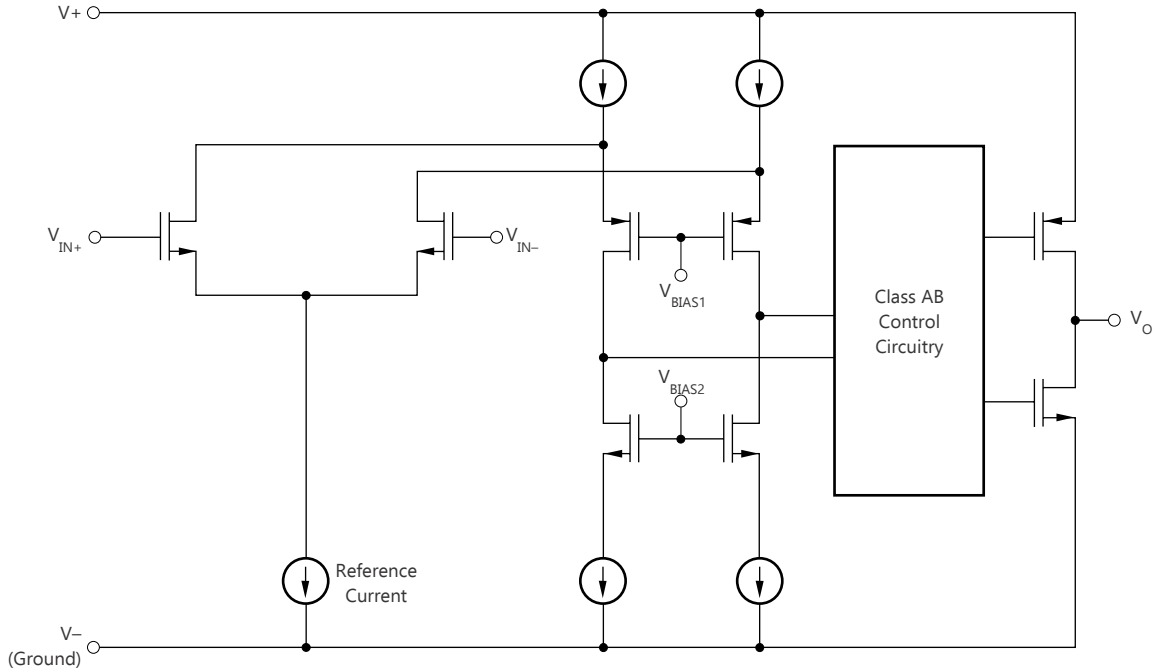
8 详细说明

8.1 概述

TL07xH（TL071H、TL072H 和 TL074H）系列器件是业界通用的 TL07x（TL071、TL072 和 TL074）器件的下一代版本。这些器件为成本敏感型应用提供了卓越的价值，其特性包括低失调电压（1mV，典型值）、高压摆率（20V/μs，典型值）和正电源的共模输入。得益于高 ESD（2kV，HBM）、集成 EMI 和射频滤波器以及 –40°C 至 125°C 的完整运行温度范围，TL07xH 器件可用于要求严苛的应用。

后缀为 C 的器件在 0°C 至 70°C 的温度范围内运行。后缀为 I 的器件在 −40°C 至 +85°C 的温度范围内运行。后缀为 M 的器件在 −55°C 至 +125°C 的完整军用温度范围内运行。

8.2 功能方框图



8.3 特性说明

与业界通用的 TL07x 系列相比，TL07xH 系列器件改进了许多规格。以下各节对这些系列之间的几个主要规格进行比较，展示了 TL07xH 系列的优势。

8.3.1 总谐波失真

音频信号的谐波失真由电路中的电子组件产生。总谐波失真 (THD) 用于衡量音频系统中的信号所累积的谐波失真。这些器件 具有 0.003% 的极低 THD，这意味着 TL07x 器件用在音频信号应用中时几乎不增加谐波失真。

8.3.2 压摆率

压摆率是运算放大器在输入发生变化时可以改变输出的速率。这些器件具有 20V/μs 的压摆率。

8.4 器件功能模式

这些器件会在连接电源时上电。这些器件可根据应用情况作为单电源运算放大器或双电源放大器使用。

9 应用和实现

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 应用信息

运算放大器的典型应用是反相放大器。该放大器在输入端接受正电压，然后使电压变为负电压。该放大器以相同的方式使负输入电压变为正电压。

9.2 典型应用

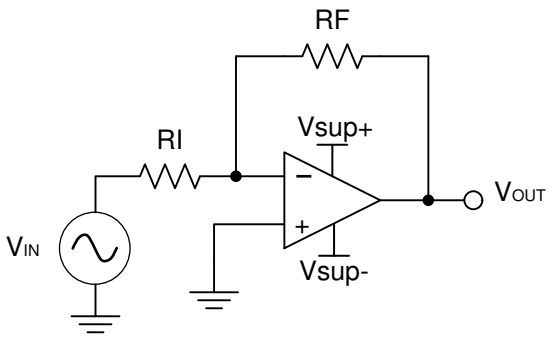


图 9-1. 反相放大器

9.2.1 设计要求

所选用的电源电压必须大于输入电压范围和输出范围。例如，此应用将 ±0.5V 的信号扩展到了 ±1.8V。将电源设置在 ±12V 就足以满足此应用的要求。

9.2.2 详细设计过程

$$V_o = (V_i + V_{io}) \times \left(1 + \frac{1M\Omega}{1k\Omega}\right) \tag{1}$$

确定反相放大器所需的增益：

$$A_V = \frac{VOUT}{VIN} \tag{2}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{3}$$

确定所需增益后，请选择 RI 或 RF 的值。由于放大器电路使用毫安级的电流，因此通常需要选择千欧姆级的值。这样可以确保该器件不会消耗过多电流。此示例使用的 RI 为 10kΩ，这意味着对 RF 使用的值为 36kΩ。这是由方程式 4 算出的。

$$A_V = -\frac{RF}{RI} \tag{4}$$

Copyright © 2023 Texas Instruments Incorporated

9.2.3 应用曲线

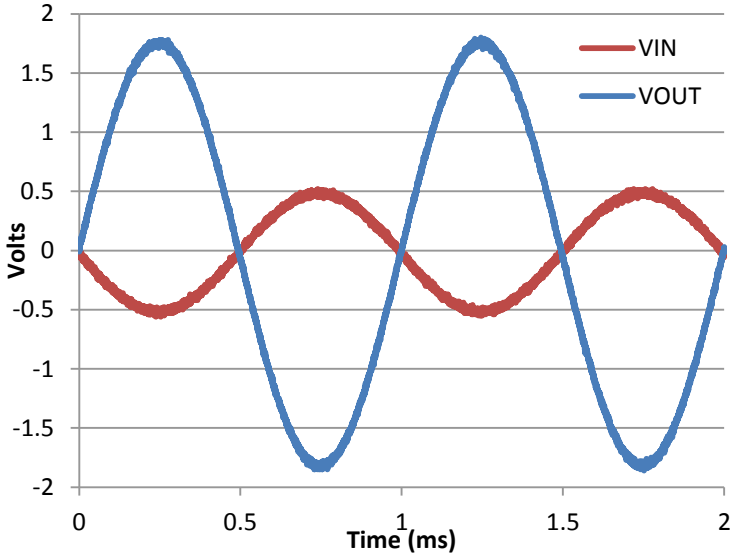
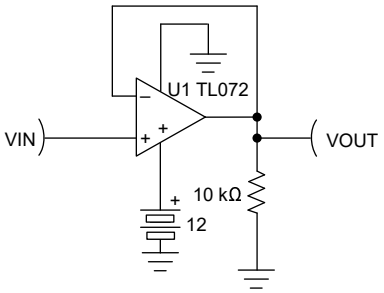


图 9-2. 反相放大器的输入和输出电压

9.3 单位增益缓冲器



Copyright © 2017, Texas Instruments Incorporated

图 9-3. 单电源单位增益放大器

9.3.1 设计要求

- V_{CC} 必须处于*建议运行条件*规定的有效范围内。此示例使用的 V_{CC} 值为 12V。
- 输入电压必须处于建议的共模范围内，如*建议运行条件*中所示。有效的共模范围为 4V 至 12V（V_{CC-} + 4V 至 V_{CC+}）。
- 输出受制于输出范围，通常为 1.5V 至 10.5V，即 V_{CC-} + 1.5V 至 V_{CC+} – 1.5V。

9.3.2 详细设计过程

- 避免输入电压值低于 1V，从而防止输出变高时出现相位反转。
- 避免输入值低于 4V，从而防止降级的 V_{IO} 导致视在增益大于 1。这种情况可能会导致一些二阶滤波器设计出现不稳定。

9.3.3 应用曲线

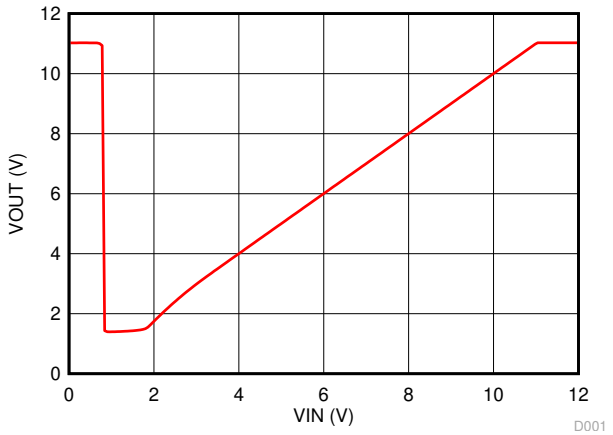


图 9-4. 输出电压与输入电压间的关系

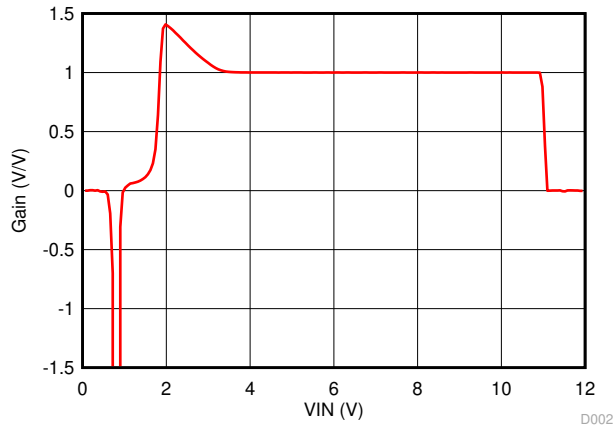


图 9-5. 增益与输入电压间的关系

9.4 系统示例

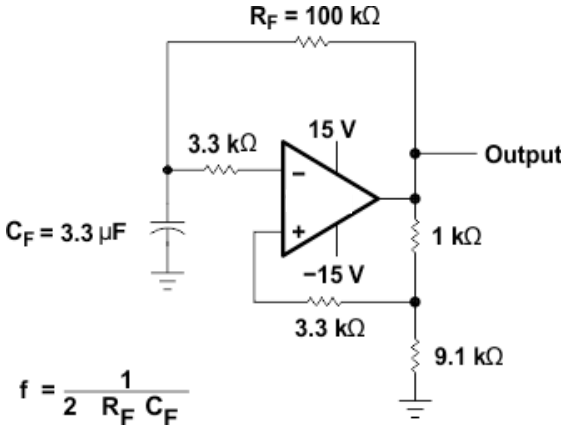


图 9-6. 0.5Hz 方波振荡器

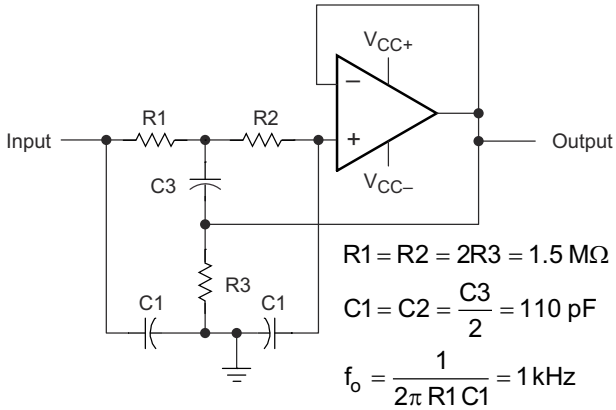


图 9-7. 高 Q 值陷波滤波器

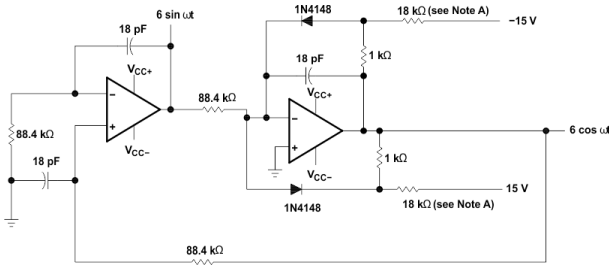


图 9-8. 100kHz 正交振荡器

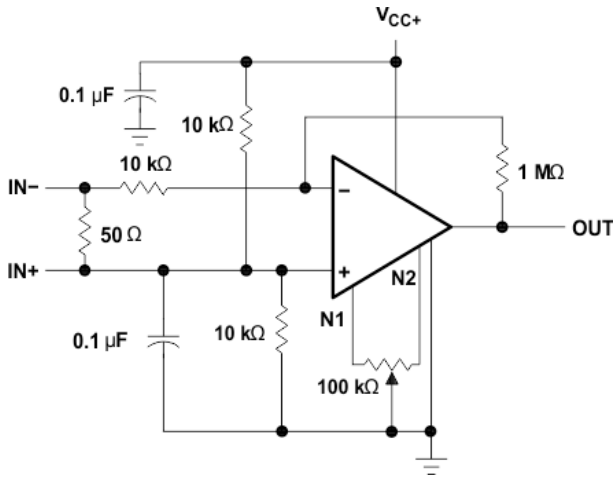


图 9-9. 交流放大器

Copyright © 2023 Texas Instruments Incorporated

9.5 电源相关建议

CAUTION

单电源的电源电压超过 36V 或双电源的电源电压范围超出 ±18V 可能会对器件造成损坏（请参阅节 6.1）。

将 0.1 μF 旁路电容器置于电源引脚附近，可减少从高噪声电源或高阻抗电源中耦合进来的误差。有关旁路电容器放置的更多详细信息，请参阅节 9.6。

9.6 布局

9.6.1 布局指南

为了实现器件的卓越运行性能，应使用良好的 PCB 布局规范，包括：

- 噪声可通过全部电路电源引脚以及运算放大器自身传入模拟电路。旁路电容器通过提供位于模拟电路本地的低阻抗电源来降低耦合噪声。
  - 在每个电源引脚和接地端之间连接低 ESR 0.1 μF 陶瓷旁路电容器，放置位置尽量靠近器件。从 V_{CC+} 到接地端的单个旁路电容器适用于单通道电源应用。
- 将电路的模拟和数字部分单独接地是简单有效的噪声抑制方法之一。通常将多层 PCB 中的一层或多层专门作为接地层。接地平面有助于散热和降低 EMI 噪声拾取。请小心地对数字接地和模拟接地进行物理隔离，同时应注意接地电流。
- 为了减少寄生耦合，请让输入走线尽可能远离电源或输出走线。如果这些迹线不能保持分离状态，最好让敏感走线与有噪声的走线垂直相交，而不是平行相交。
- 外部组件的位置应尽量靠近器件。使 RF 和 RG 接近反相输入可尽可能减小寄生电容。详细信息请参见 节 9.6.2。
- 尽可能缩短输入走线的长度。切记：输入走线是电路中最敏感的部分。
- 考虑在关键走线周围设定驱动型低阻抗保护环。这样可显著减少附近走线在不同电势下产生的漏电流。

9.6.2 布局示例

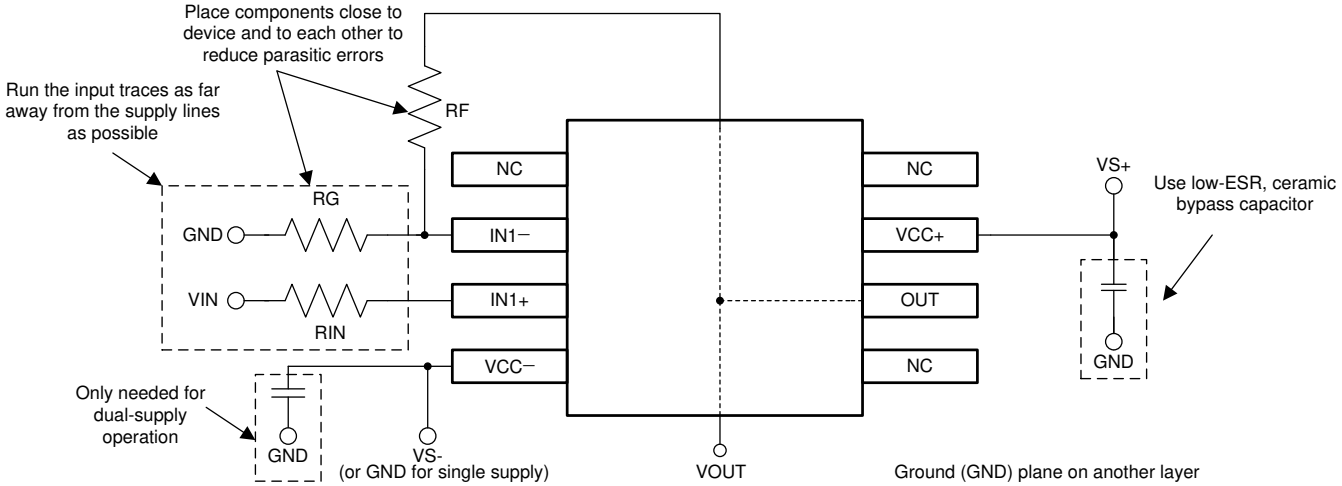


图 **9-10.** 同相配置的运算放大器电路板布局布线

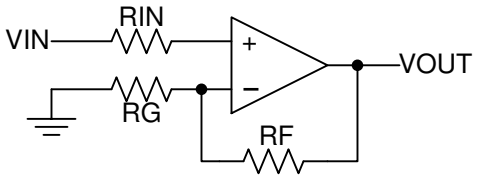


图 **9-11.** 同相配置的运算放大器原理图

Copyright © 2023 Texas Instruments Incorporated

10 器件和文档支持

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023052A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
8102305HA	ACTIVE	CFP	U	10	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
8102305PA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
81023062A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
8102306CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
8102306DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples
JM38510/11905BPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
M38510/11905BPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
TL071ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	Samples
TL071BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	Samples
TL071CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDRE4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL071CDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL071CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70		Samples
TL071CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL071HIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T71V	Samples
TL071HIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1IO	Samples
TL071HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL071D	Samples
TL071IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples
TL071IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP	Samples
TL072ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072ACPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70		Samples
TL072ACPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072A	Samples
TL072BCD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	072BC	
TL072BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples
TL072CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	TBD	Call TI	Call TI	0 to 70		Samples
TL072CPWRG4	ACTIVE	TSSOP	PW	8	2000	TBD	Call TI	Call TI	0 to 70		Samples
TL072HIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O72F	Samples
TL072HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072D	Samples
TL072HIPWR	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	072HPW	Samples
TL072IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072IPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	-40 to 85		Samples
TL072MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
TL072MJG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL072MJG	Samples
TL072MJGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
TL072MUB	ACTIVE	CFP	U	10	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
TL074ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	Samples
TL074BCD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	TL074BC	
TL074BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074CD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	TL074C	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074CDBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	0 to 70	T074	
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074HIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID	Samples
TL074HIDYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T074HDYY	Samples
TL074HIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074PW	Samples
TL074ID	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	TL074I	
TL074IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN	Samples
TL074MFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MFK	Samples
TL074MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
TL074MJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MJ	Samples
TL074MJB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074MWB	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :

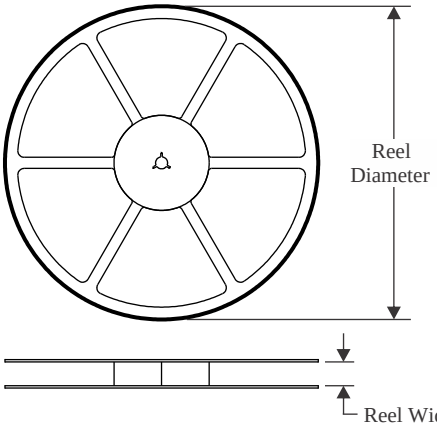
- Catalog : TL072, TL074
- Enhanced Product : TL072-EP, TL072-EP, TL074-EP, TL074-EP
- Military : TL072M, TL074M

NOTE: Qualified Version Definitions:

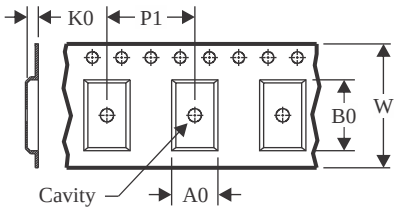
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

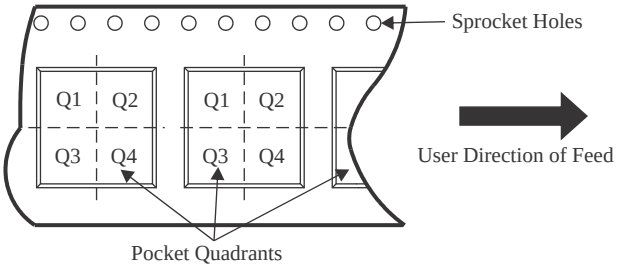


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

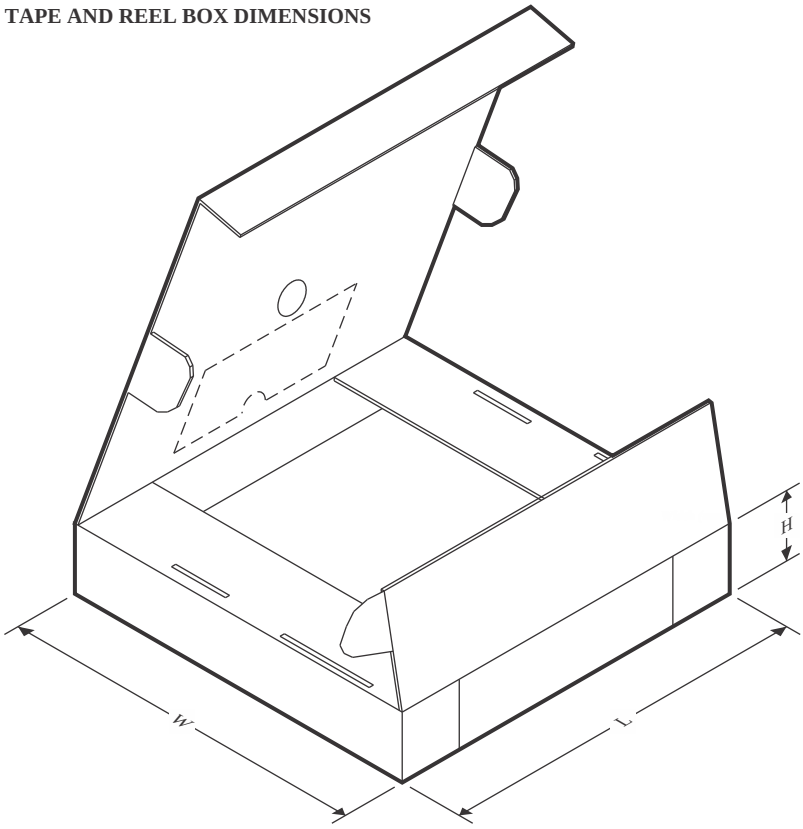


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL071HIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL071HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL071HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL072HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL074HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

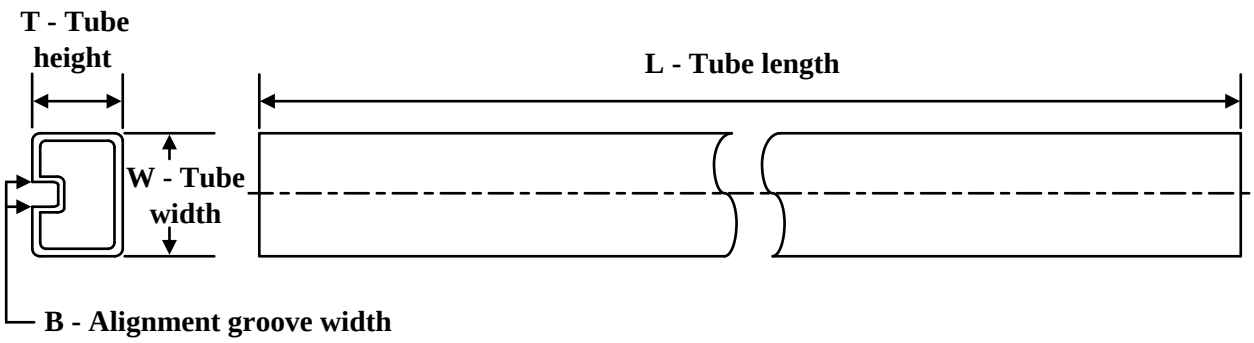


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL071ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071BCDR	SOIC	D	8	2500	356.0	356.0	35.0
TL071BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL071CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL071HIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL071HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL071HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL071IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072ACDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072BCDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL072CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL072CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL072HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL072HIPWR	TSSOP	PW	8	3000	356.0	356.0	35.0
TL072IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL072IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL074ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074ACDR	SOIC	D	14	2500	356.0	356.0	35.0
TL074ACNSR	SO	NS	14	2000	356.0	356.0	35.0
TL074BCDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074BCDR	SOIC	D	14	2500	356.0	356.0	35.0
TL074CDBR	SSOP	DB	14	2000	356.0	356.0	35.0
TL074CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL074CDR	SOIC	D	14	2500	356.0	356.0	35.0
TL074CDRG4	SOIC	D	14	2500	356.0	356.0	35.0
TL074CNSR	SO	NS	14	2000	356.0	356.0	35.0
TL074CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL074CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL074HIDR	SOIC	D	14	2500	356.0	356.0	35.0
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL074HIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL074IDR	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



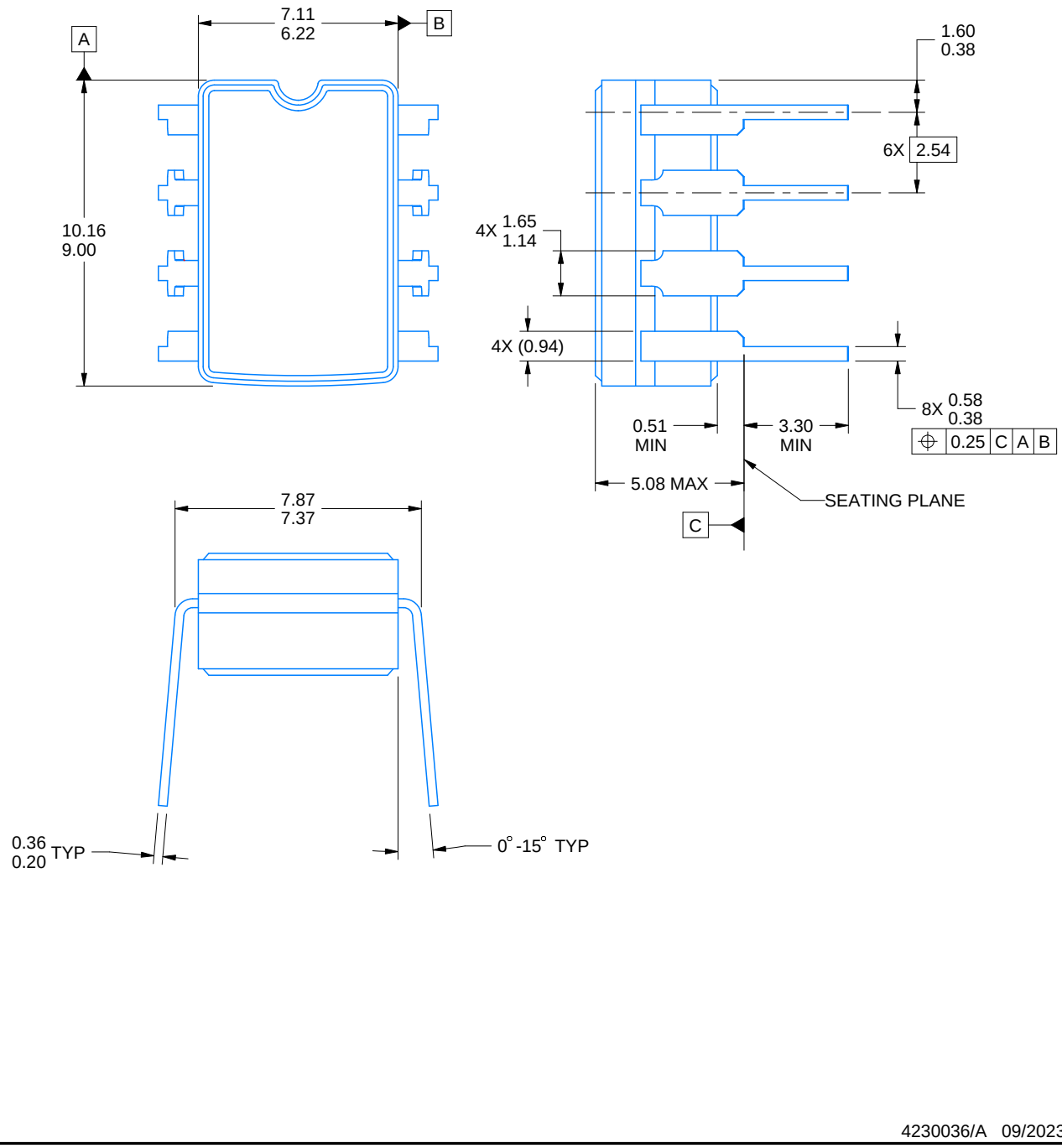
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
81023052A	FK	LCCC	20	55	506.98	12.06	2030	NA
8102305HA	U	CFP	10	25	506.98	26.16	6220	NA
81023062A	FK	LCCC	20	55	506.98	12.06	2030	NA
8102306DA	W	CFP	14	25	506.98	26.16	6220	NA
TL071ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL071BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CP	P	PDIP	8	50	506	13.97	11230	4.32
TL071IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL072MUB	U	CFP	10	25	506.98	26.16	6220	NA
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074IN	N	PDIP	14	25	506	13.97	11230	4.32
TL074MFK	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL074MWB	W	CFP	14	25	506.98	26.16	6220	NA

JG0008A

CDIP - 5.08 mm max height

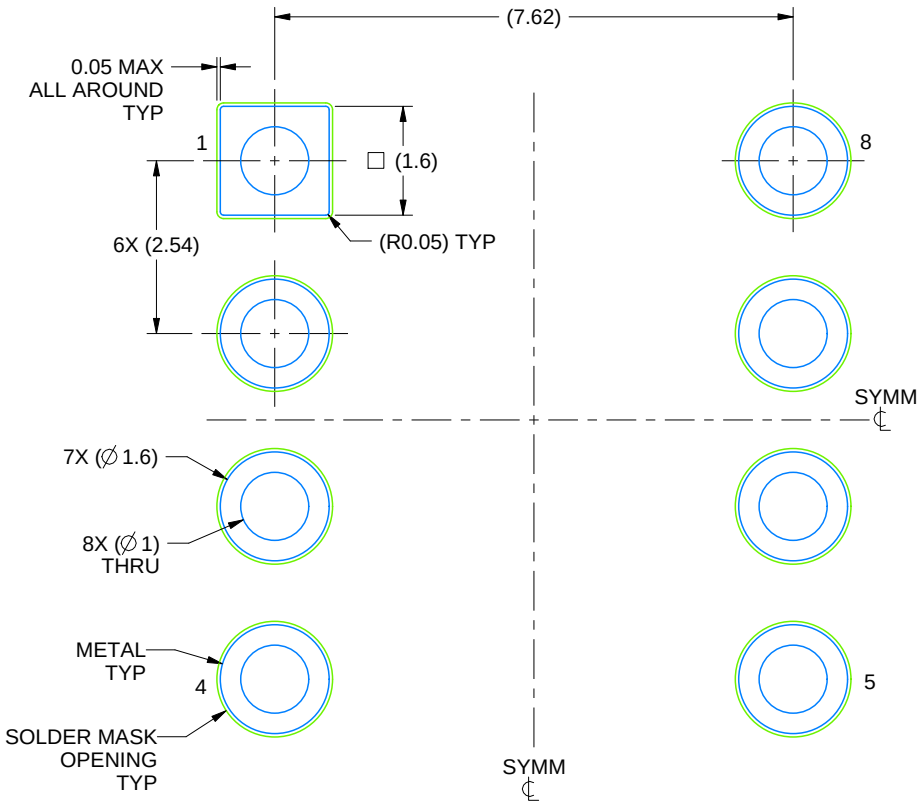
CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

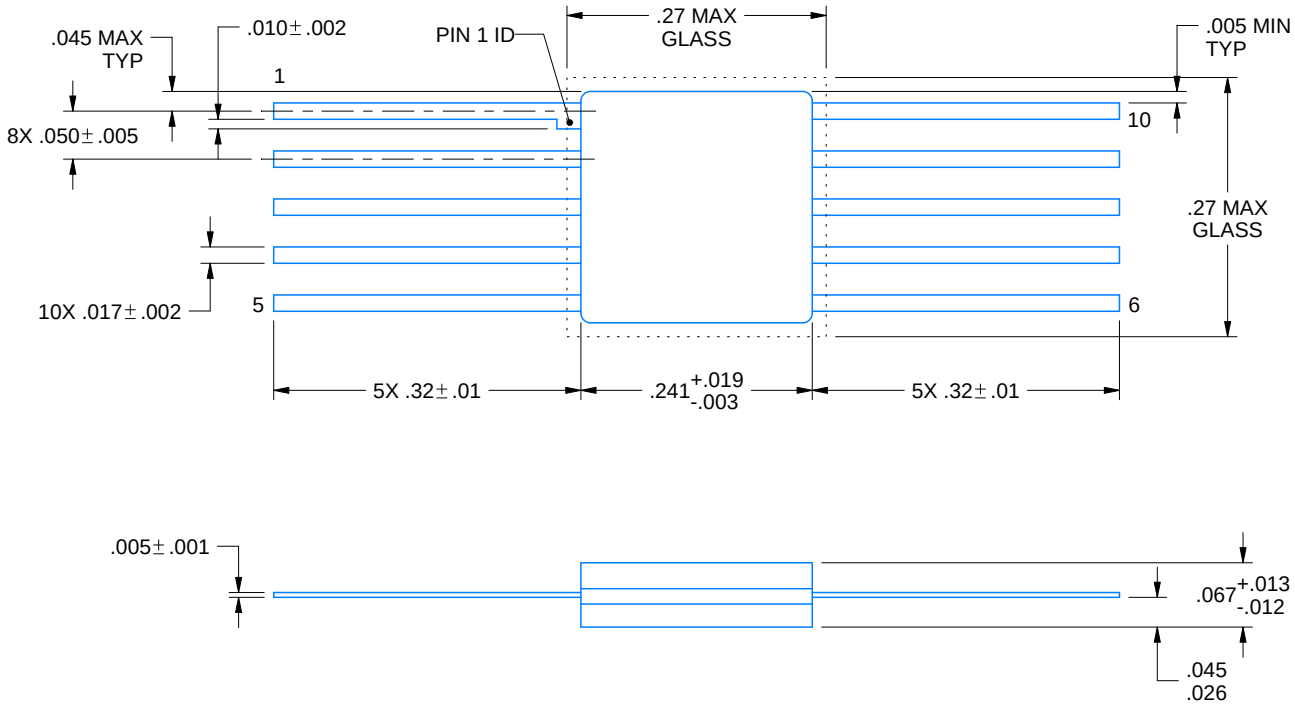
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

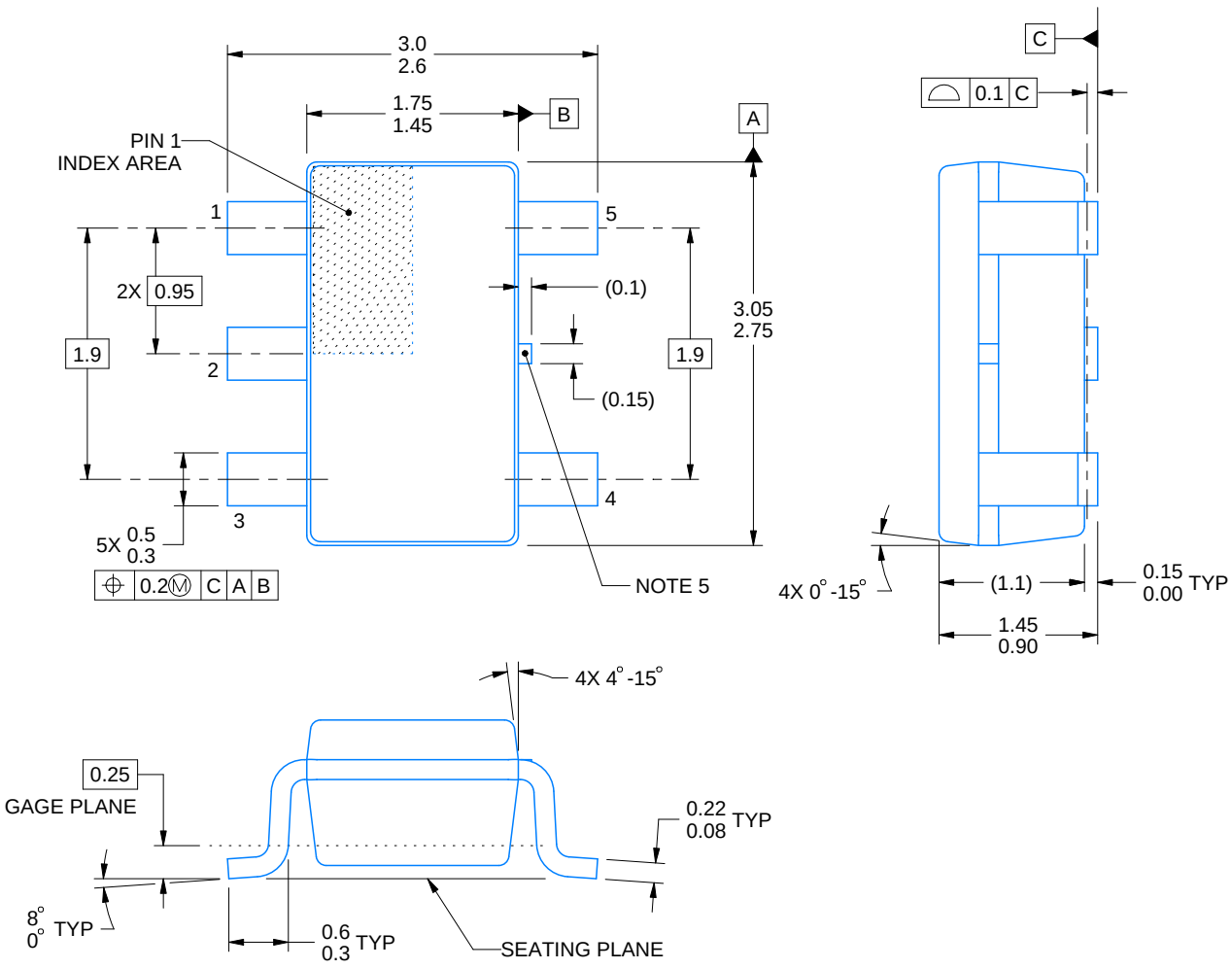
4230036/A 09/2023



4225582/A 01/2020

NOTES:

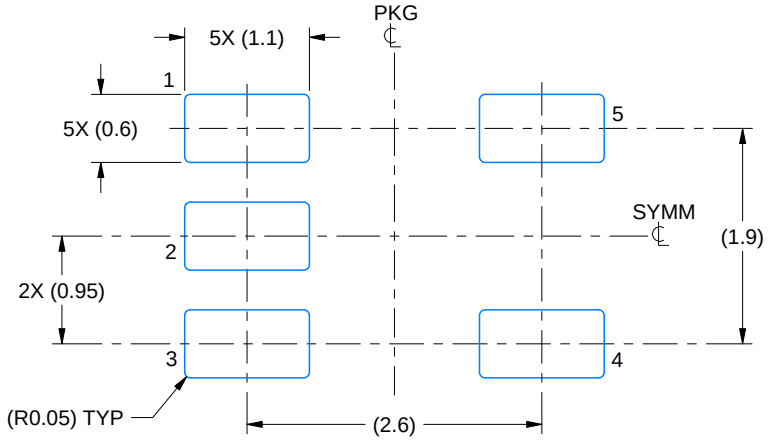
1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



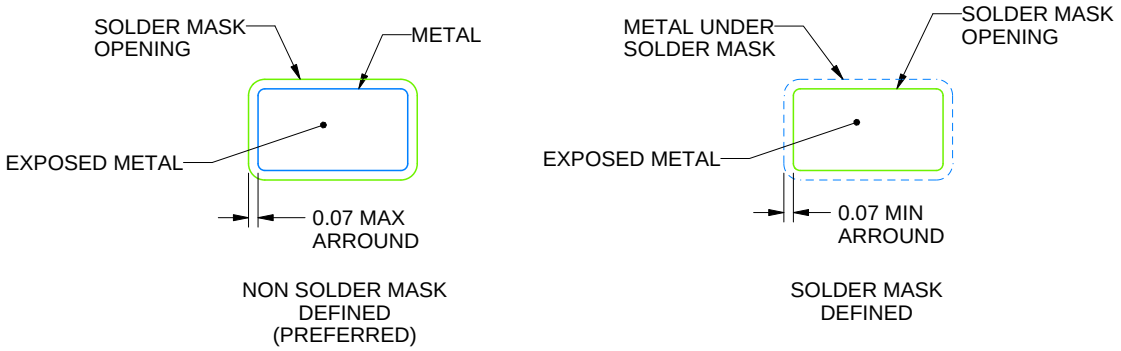
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

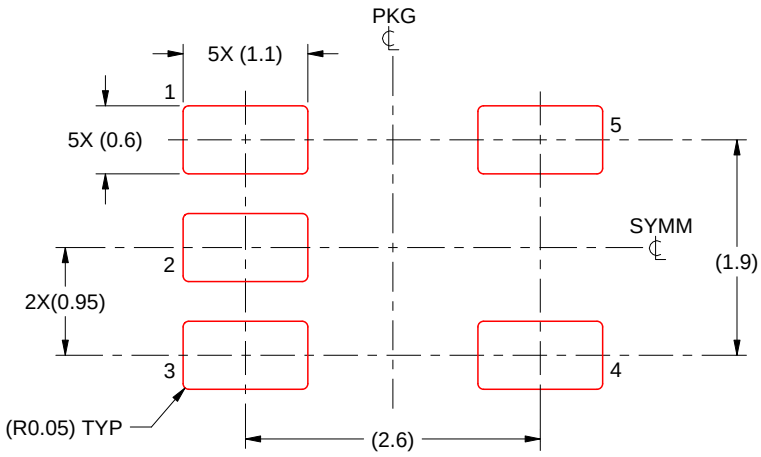


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

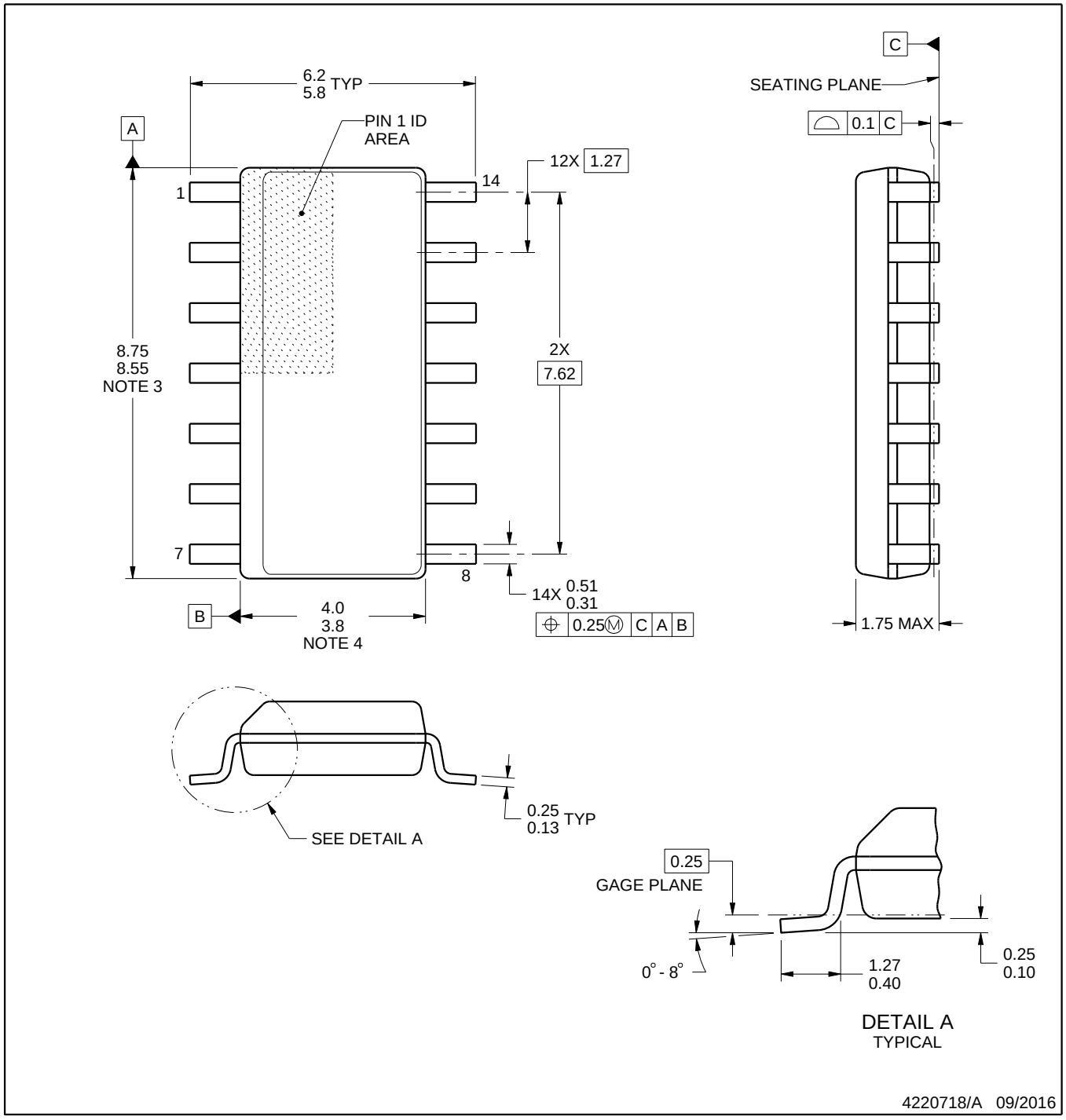


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

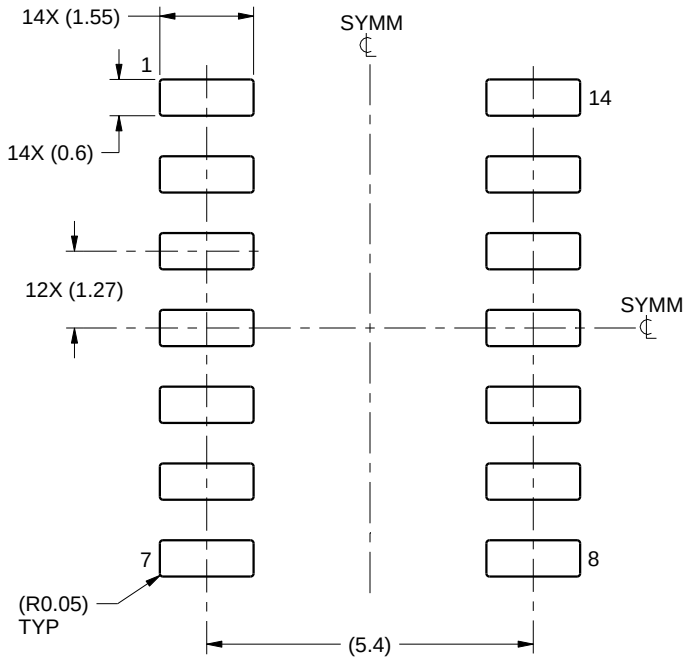
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

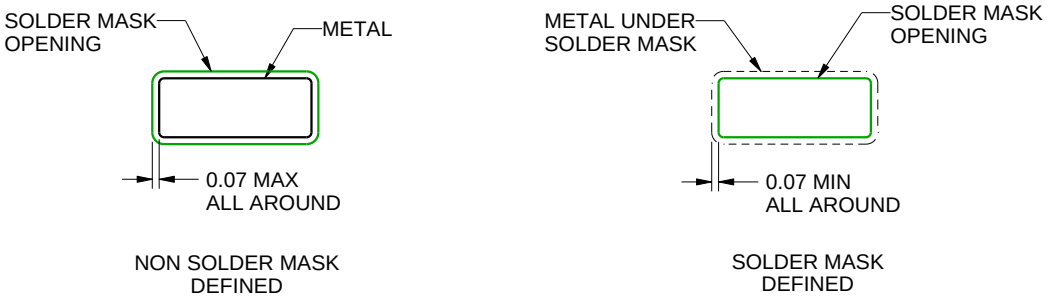


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

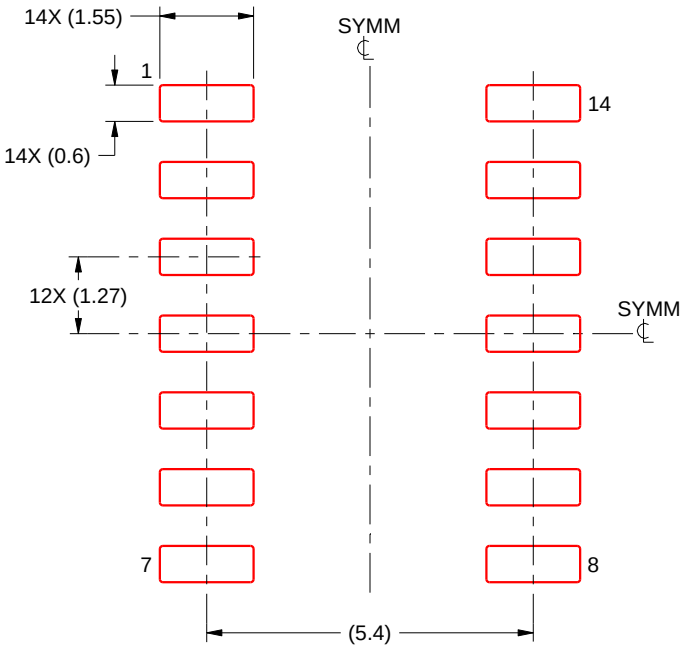


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

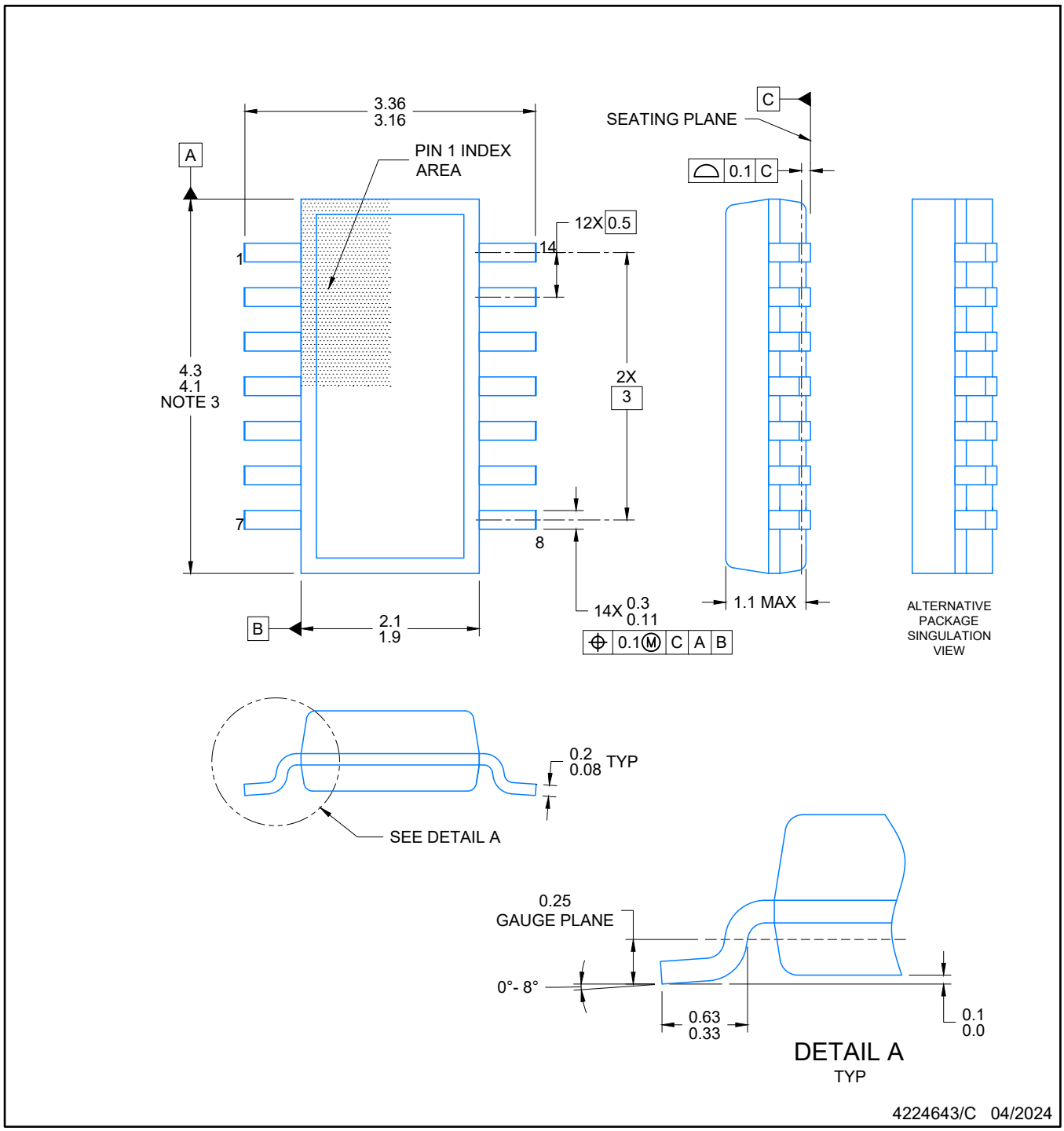


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

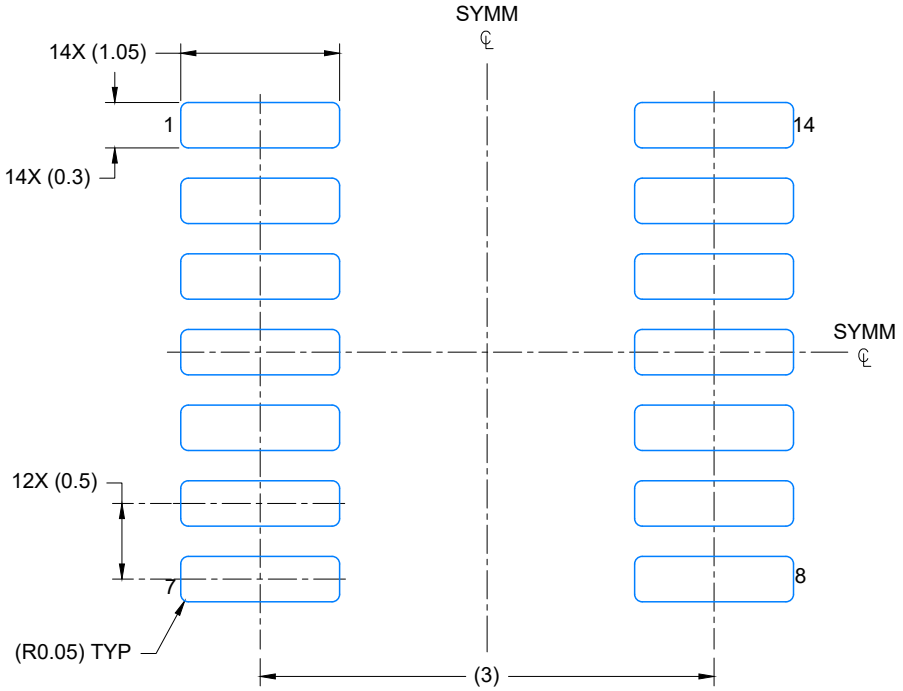
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

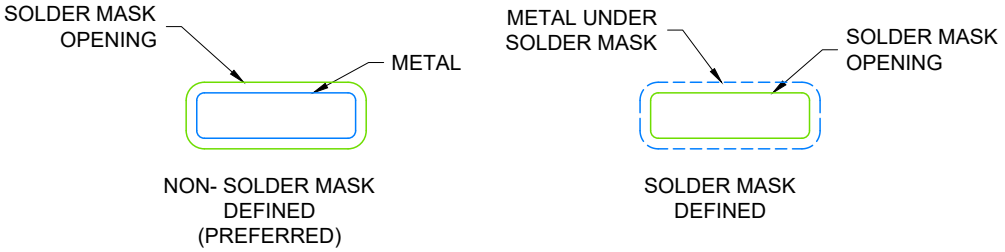


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

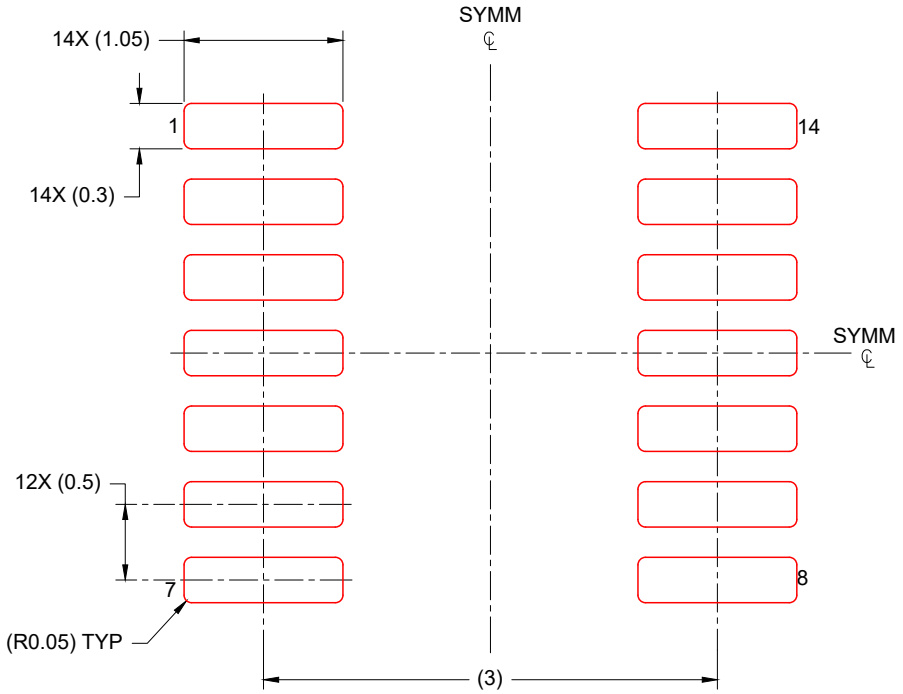


SOLDER MASK DETAILS

4224643/C 04/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/C 04/2024

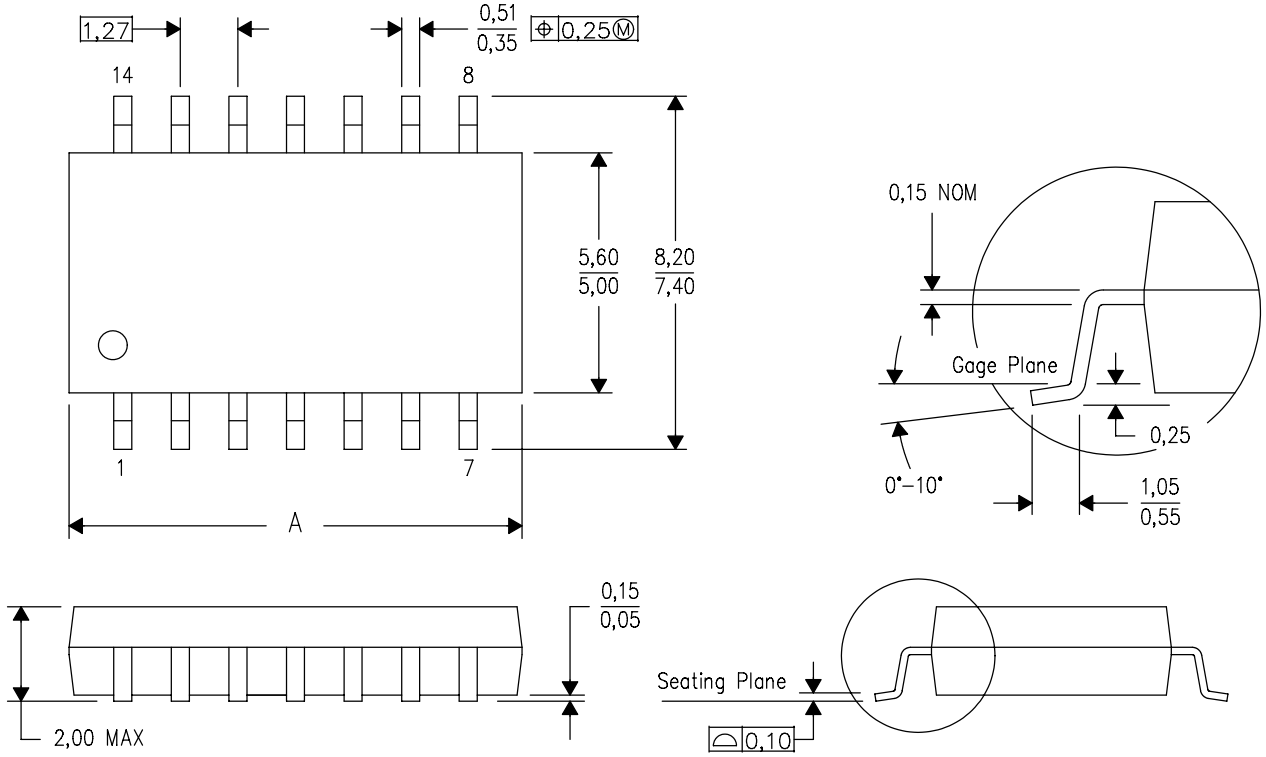
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

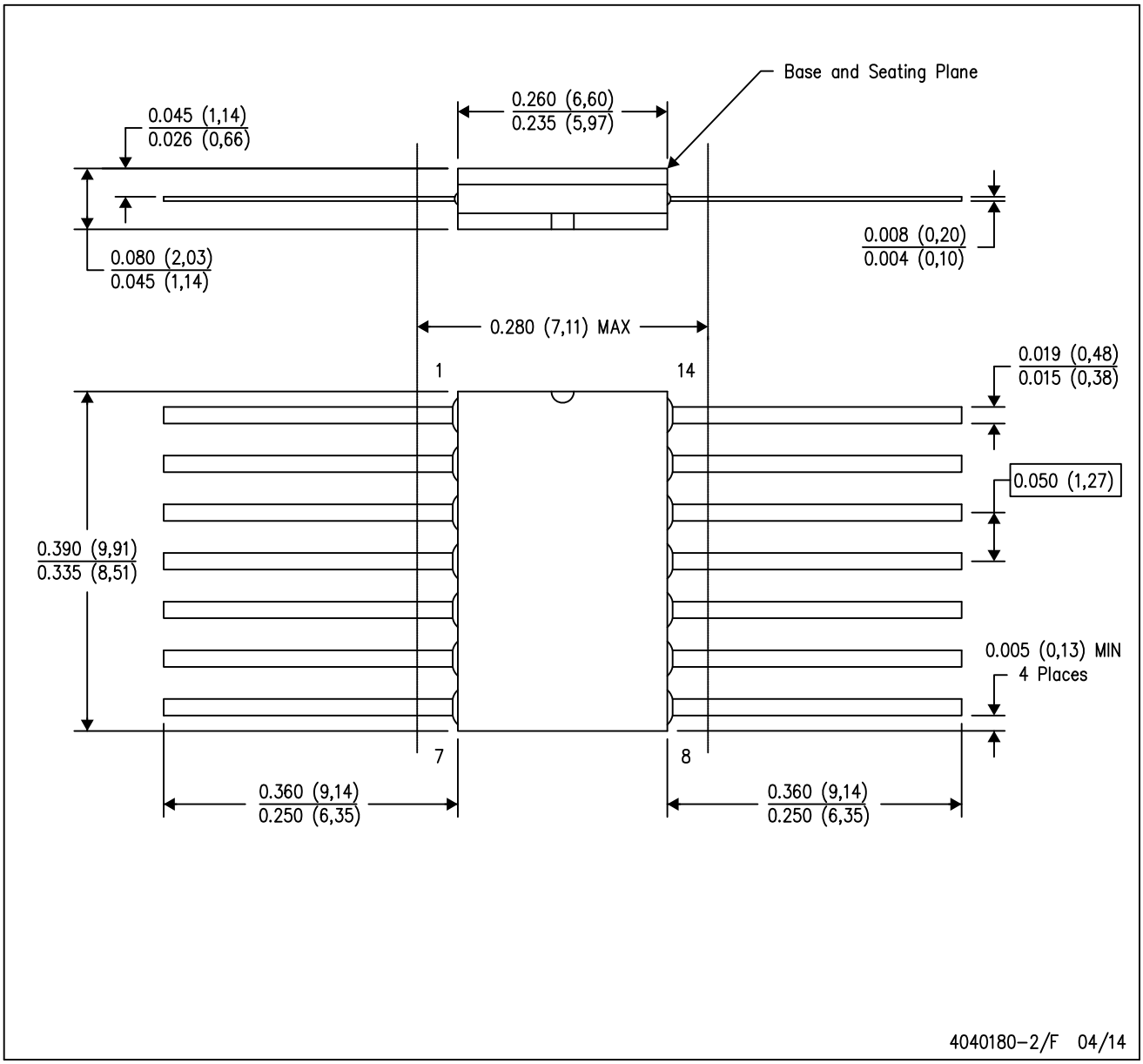


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

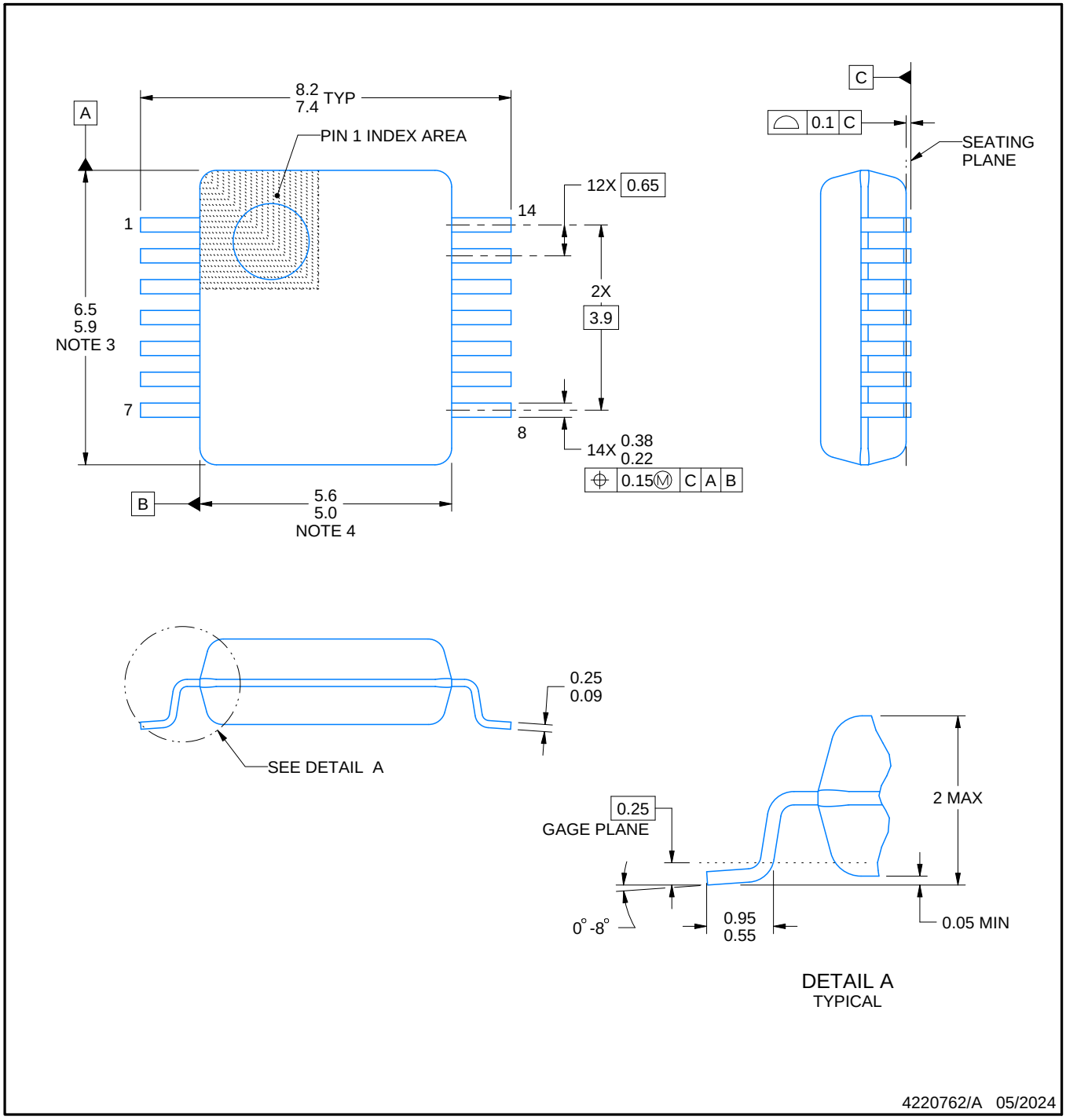
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

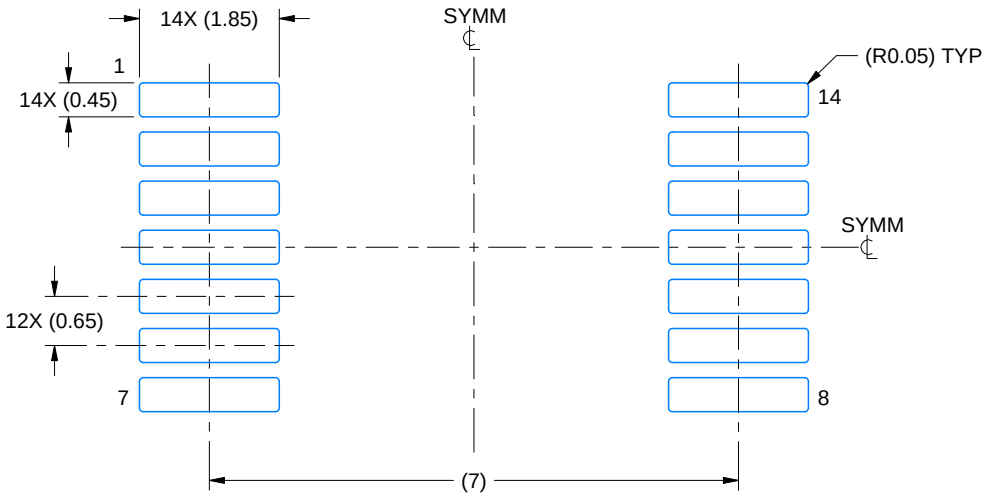


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

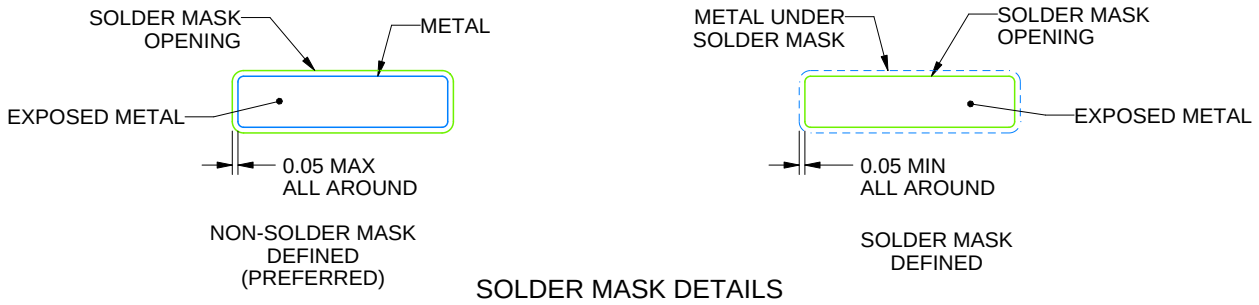


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

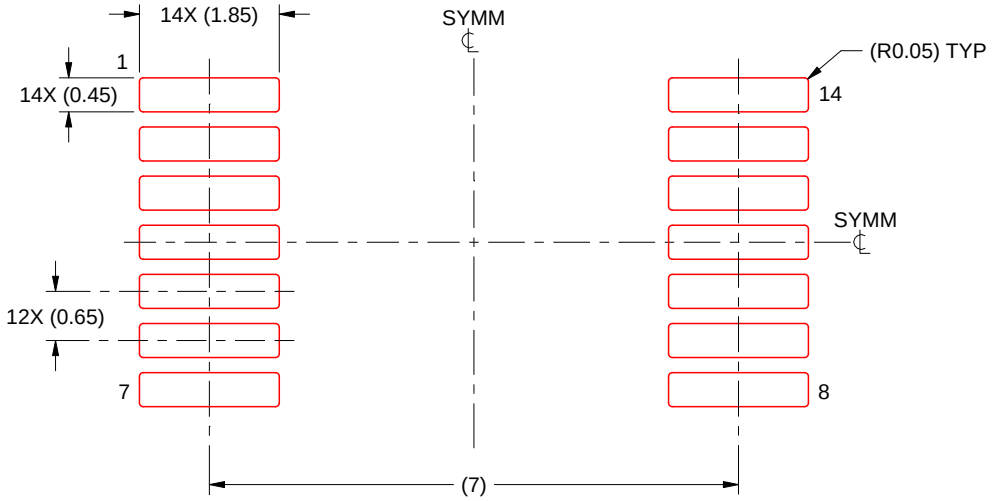


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

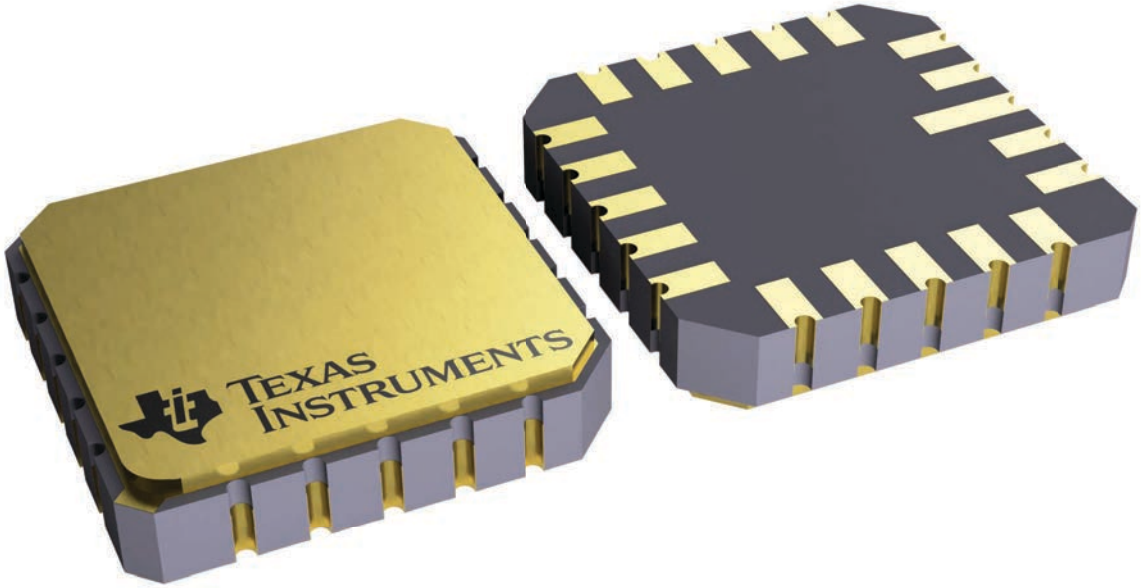
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

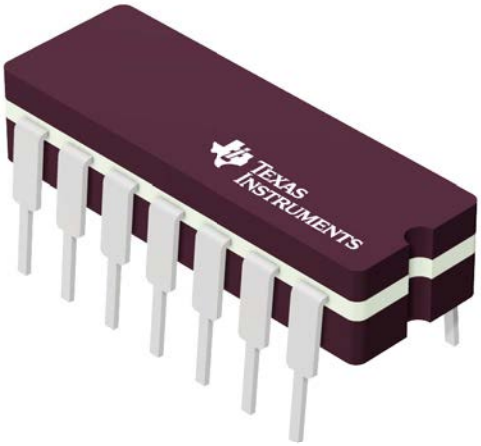
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

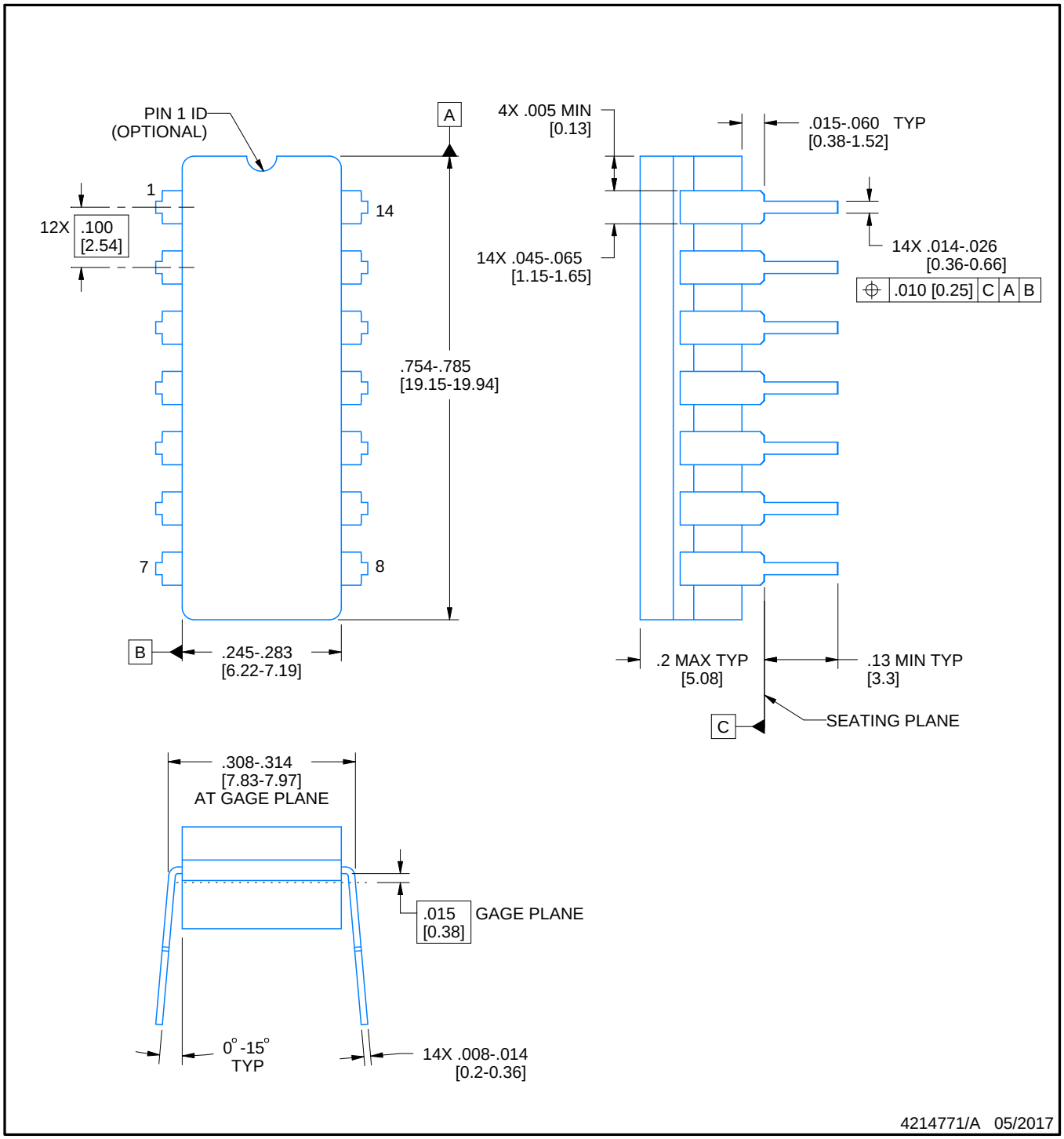
4040083-5/G

PACKAGE OUTLINE

J0014A

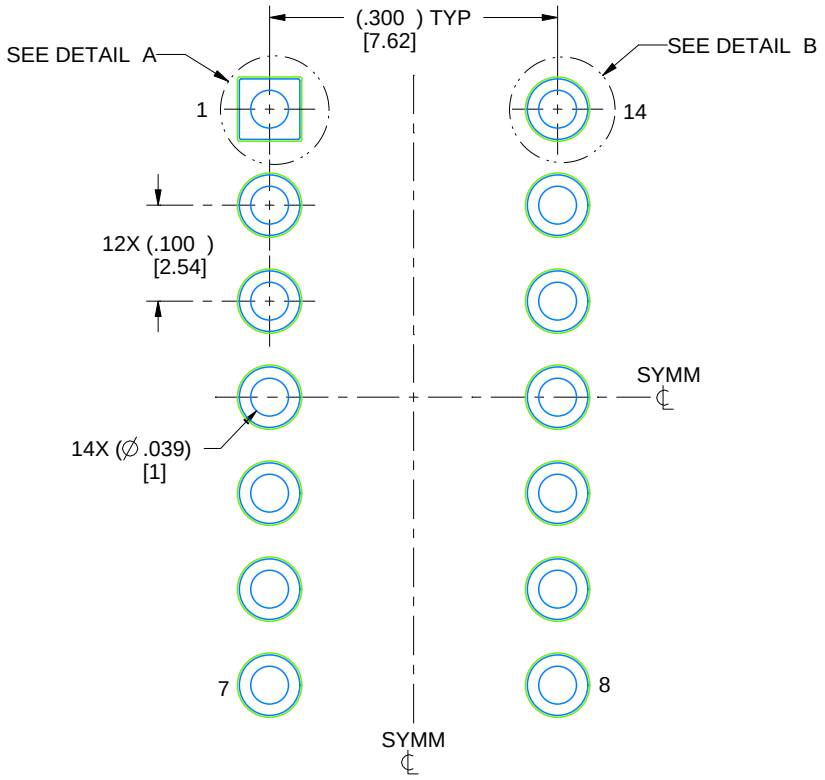
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

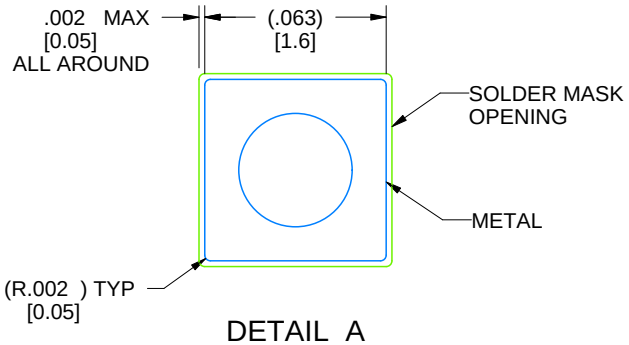


NOTES:

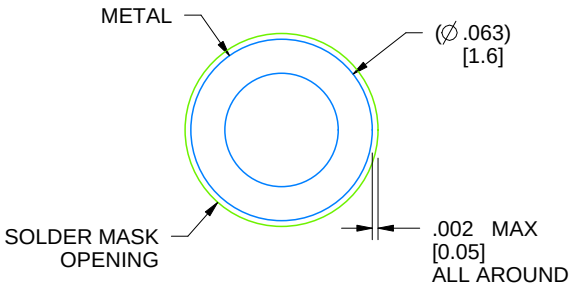
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

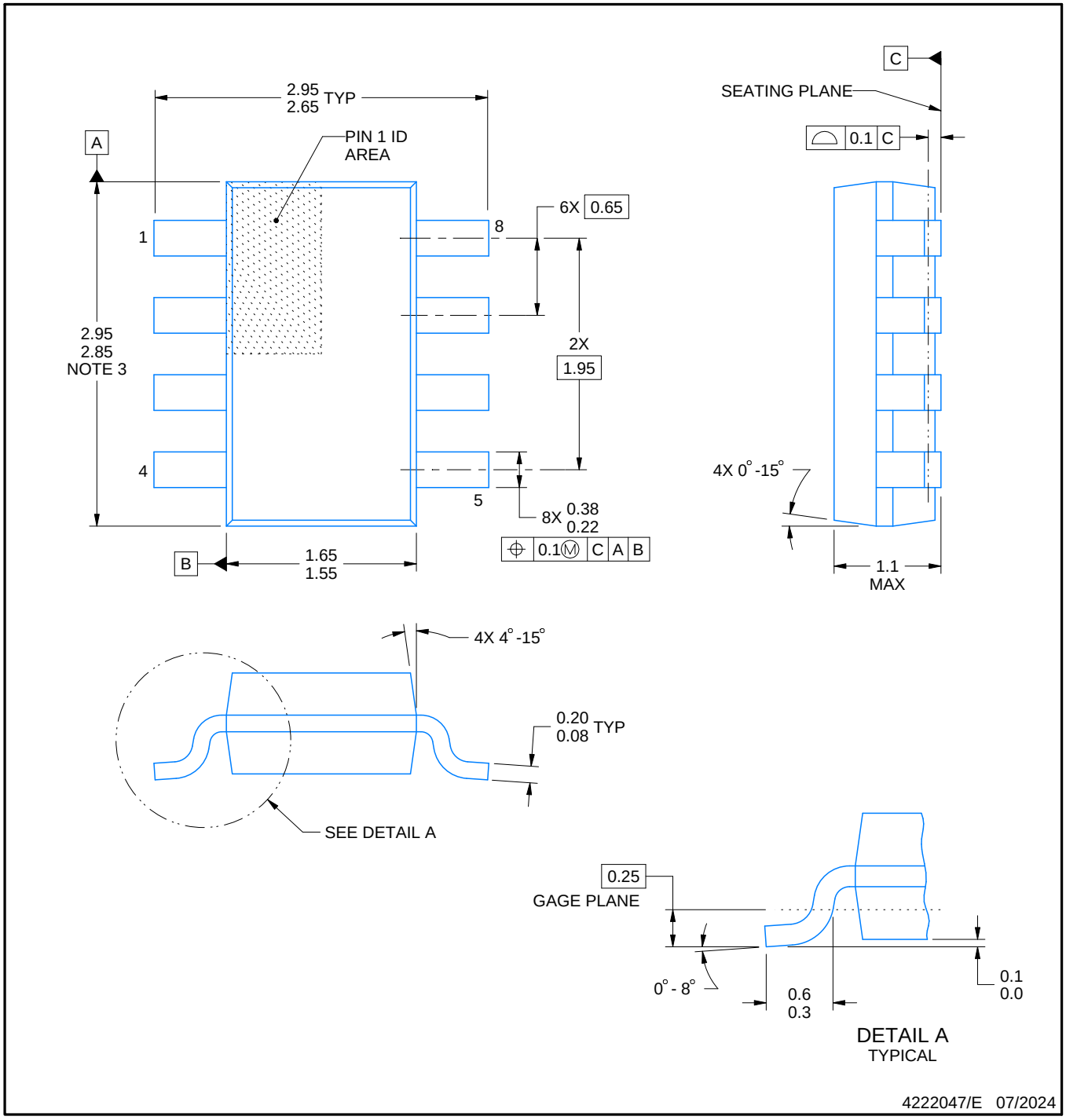


DETAIL A
SCALE: 15X



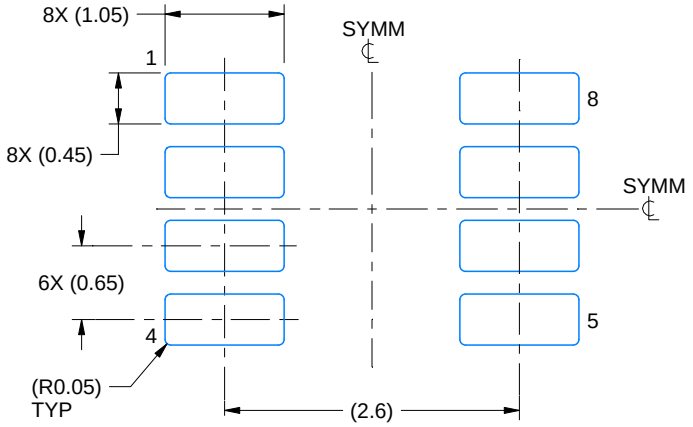
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

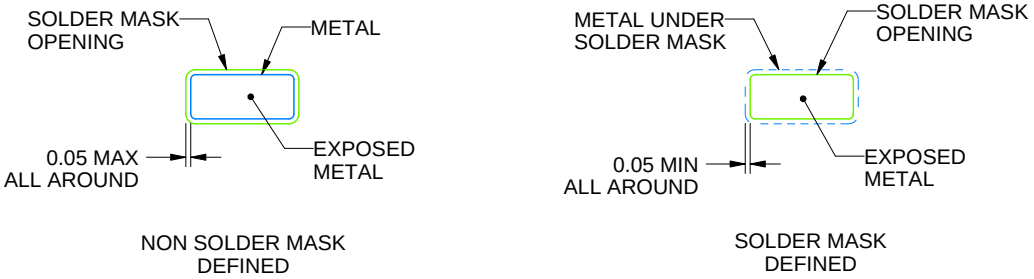


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

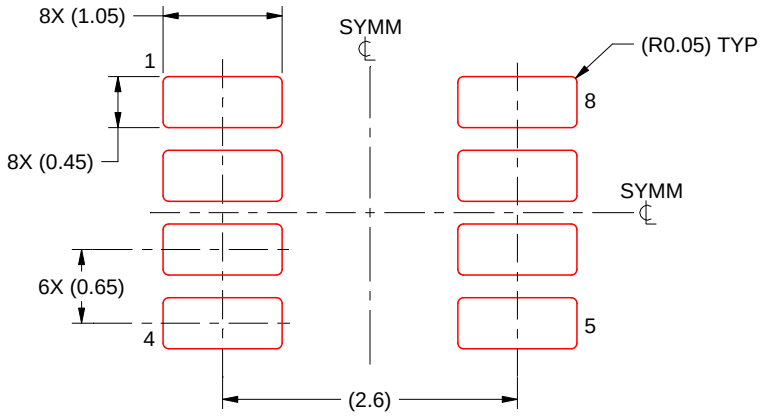


SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

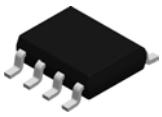


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

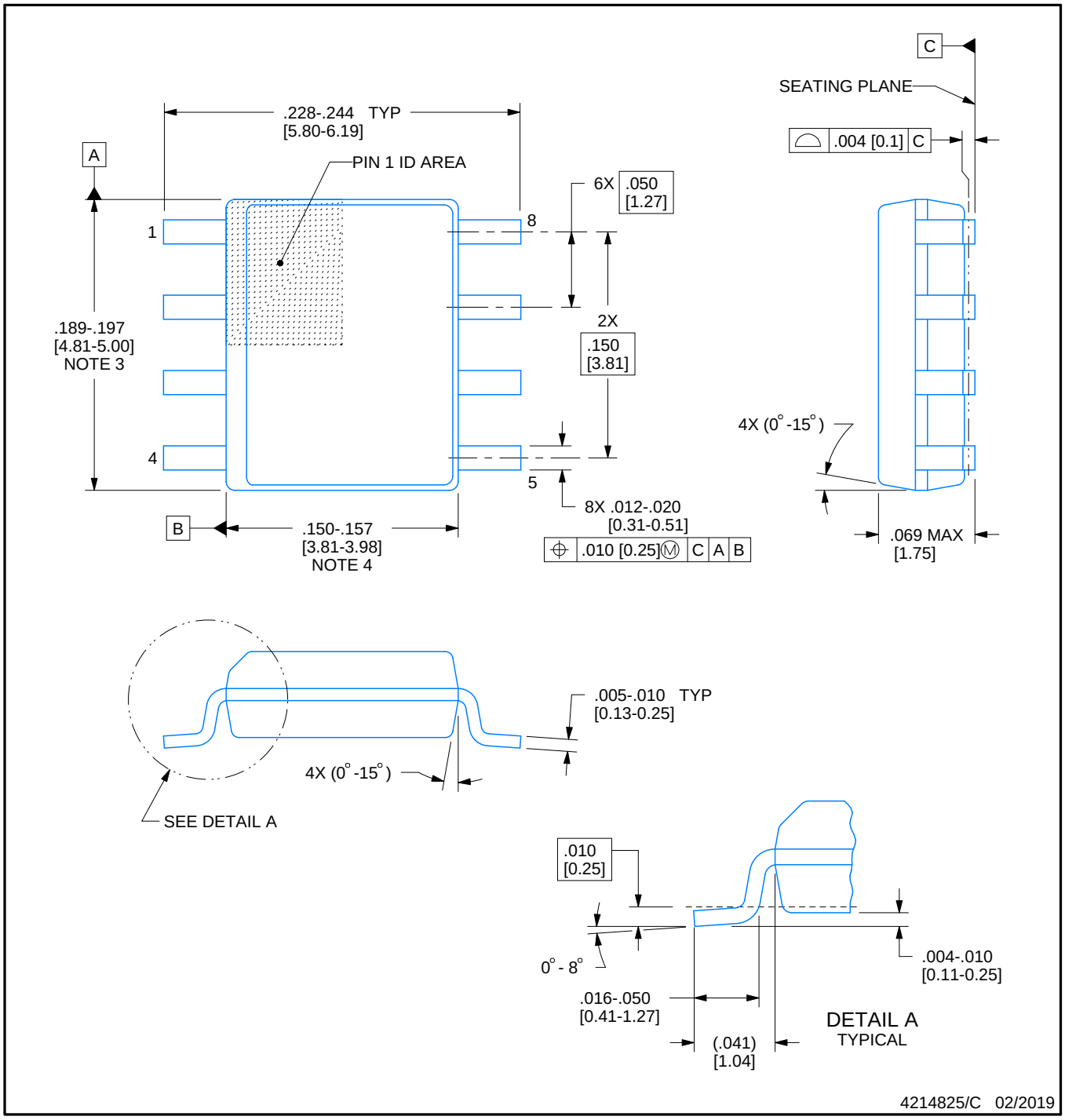


PACKAGE OUTLINE

D0008A

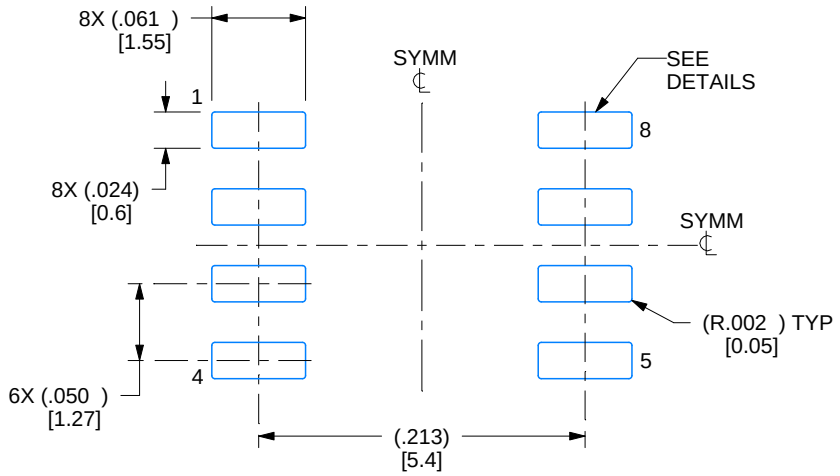
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

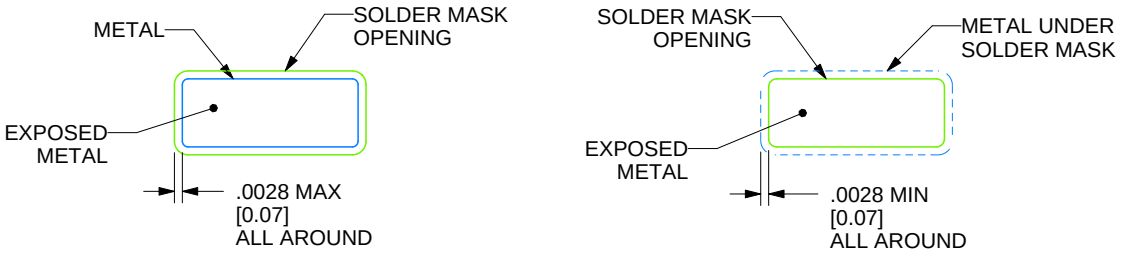


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

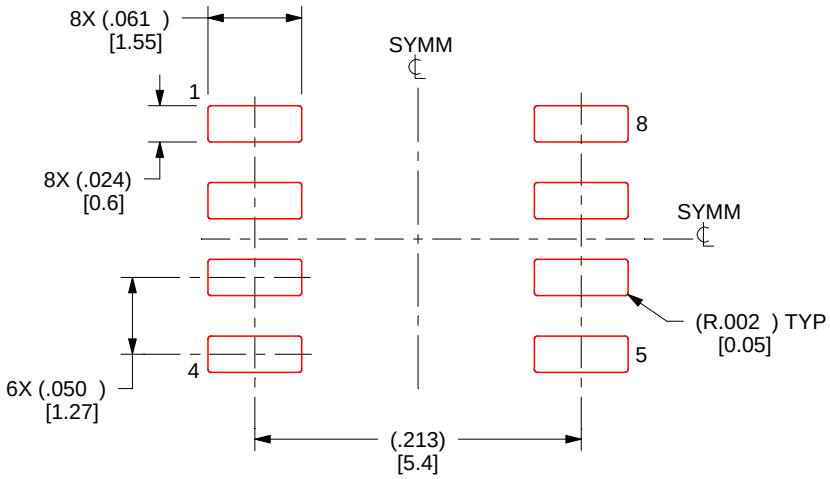


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

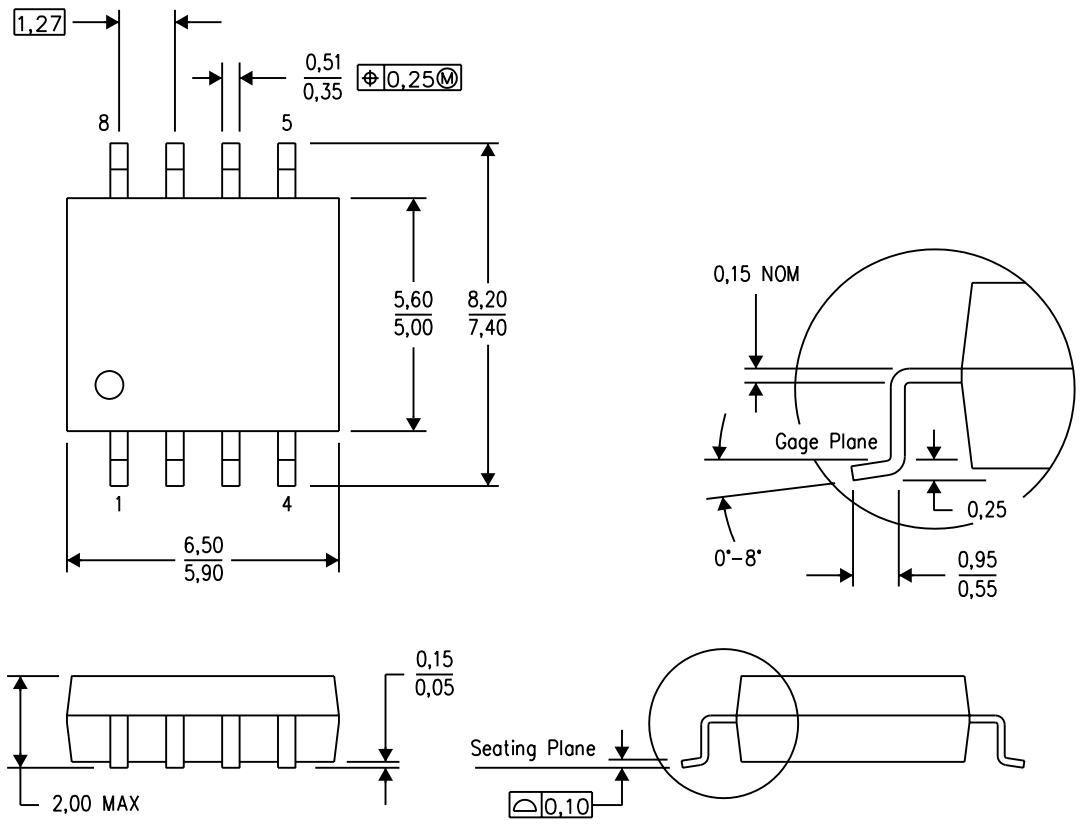
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

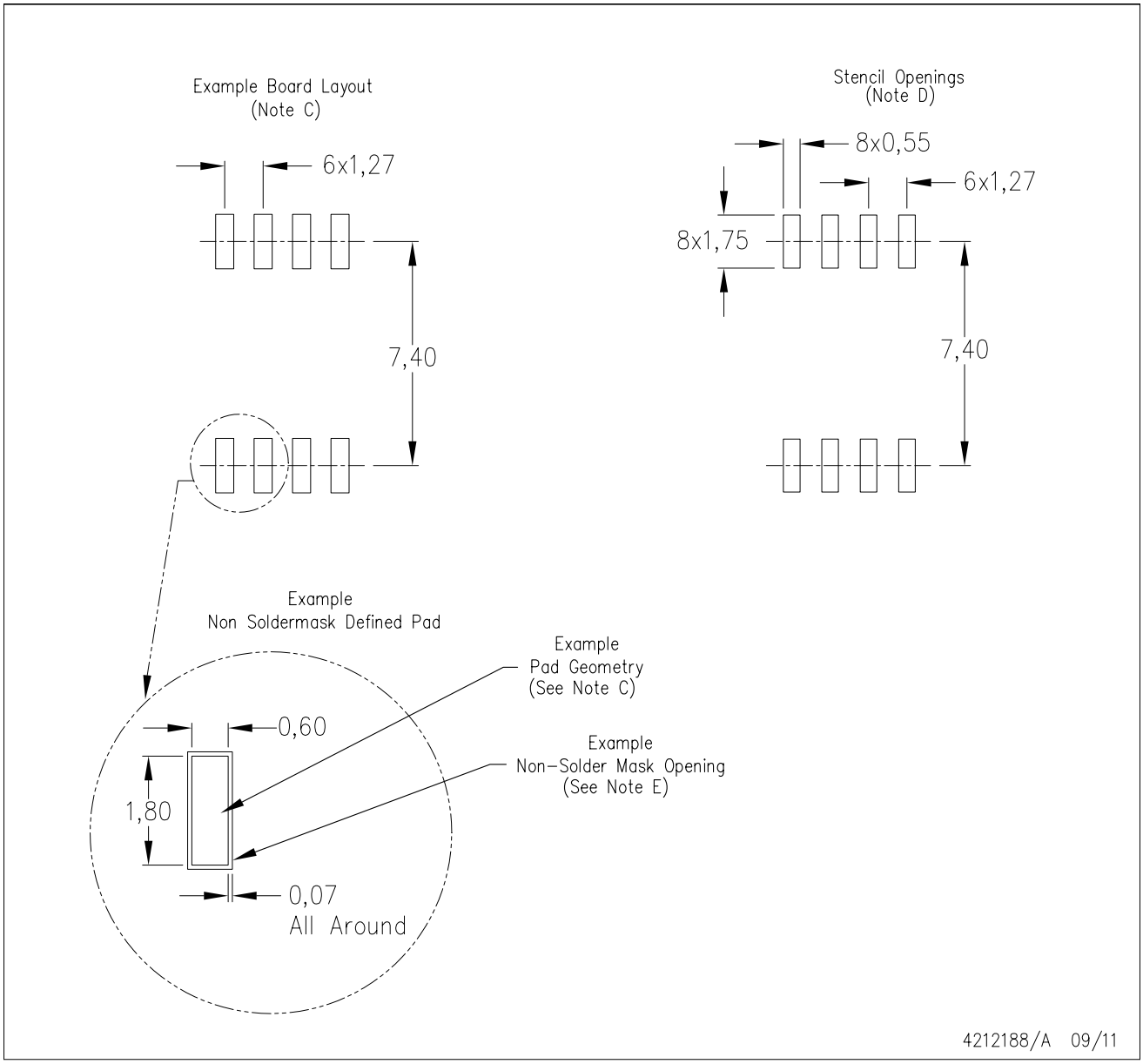
MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



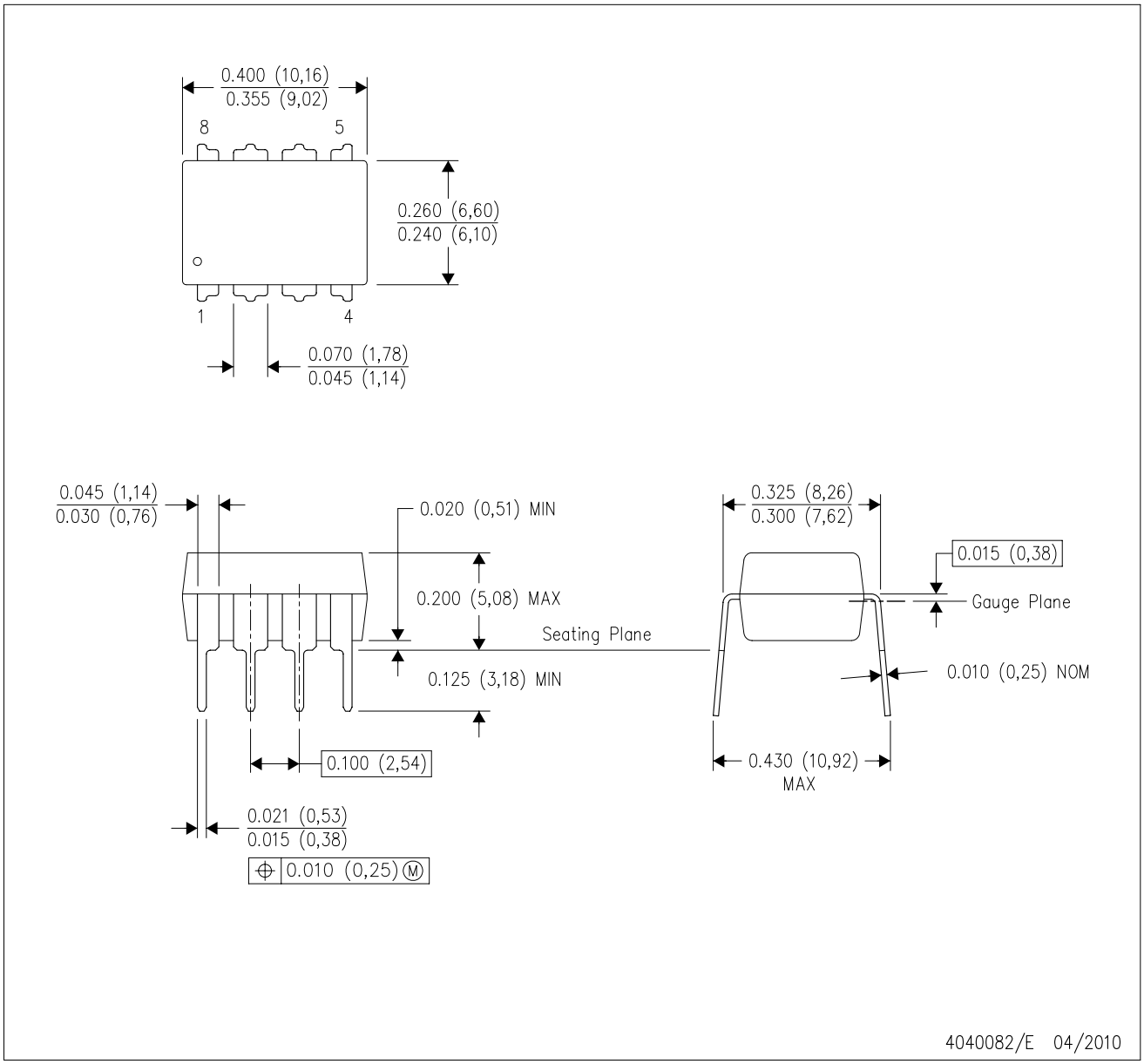
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

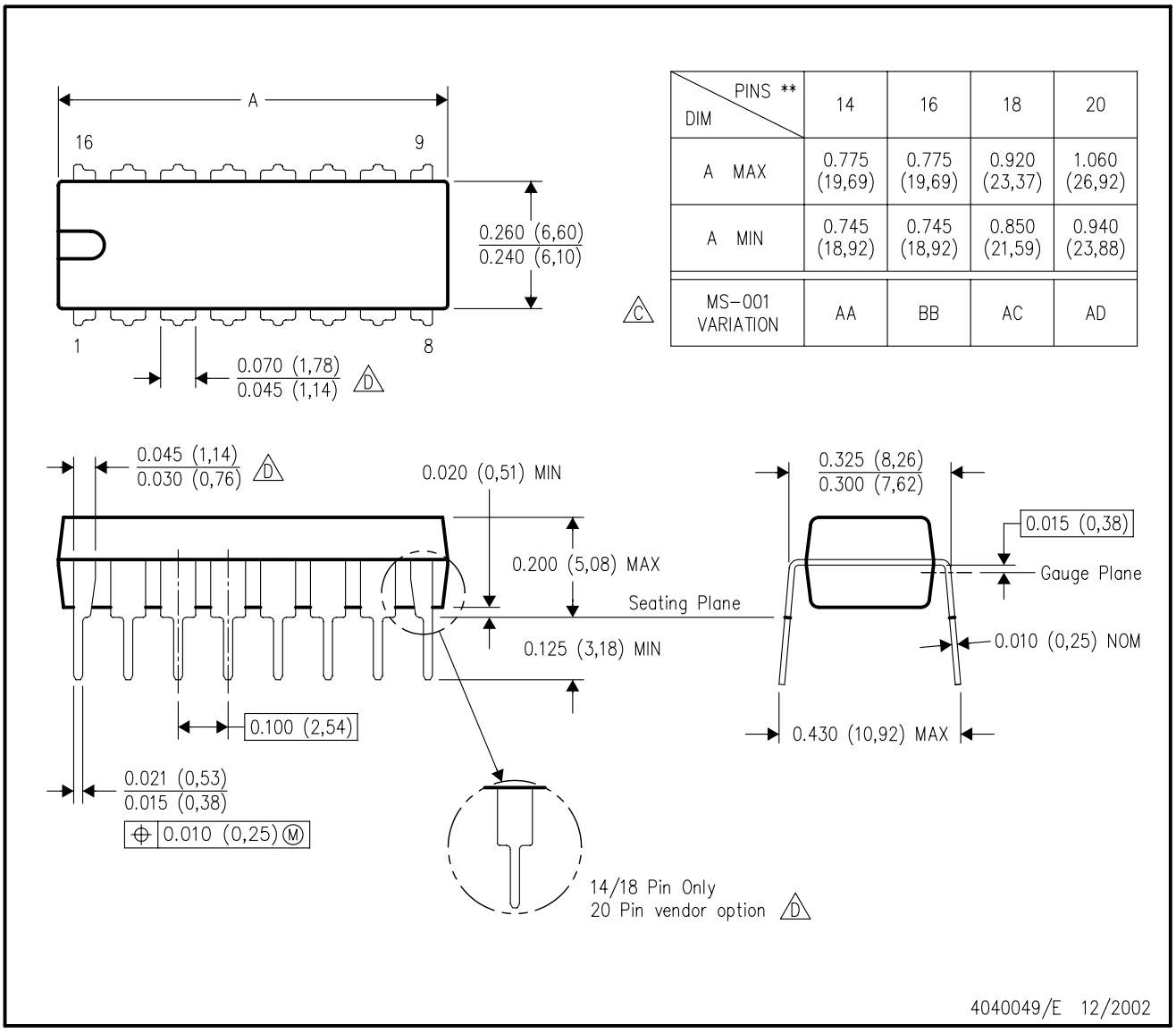
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

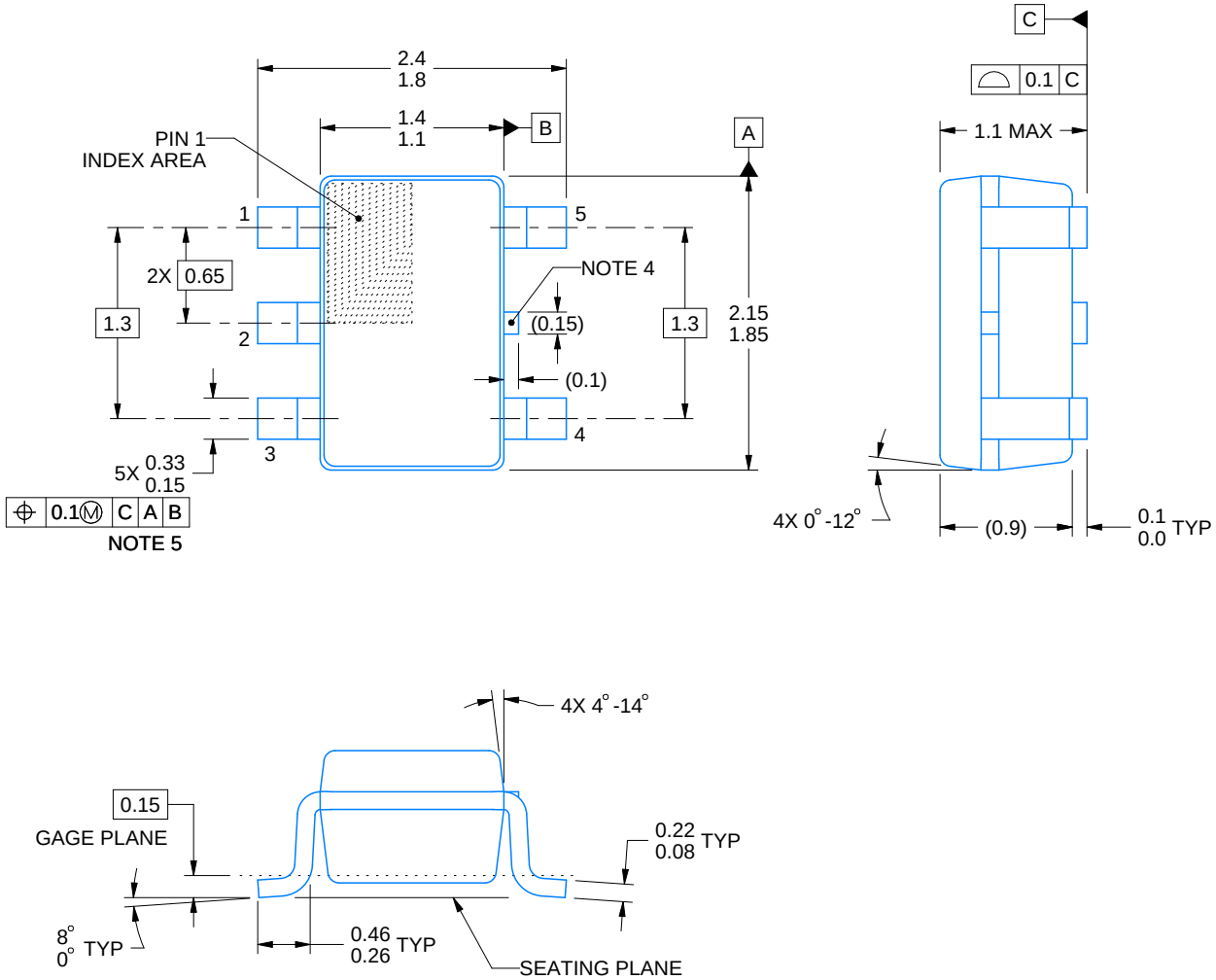
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

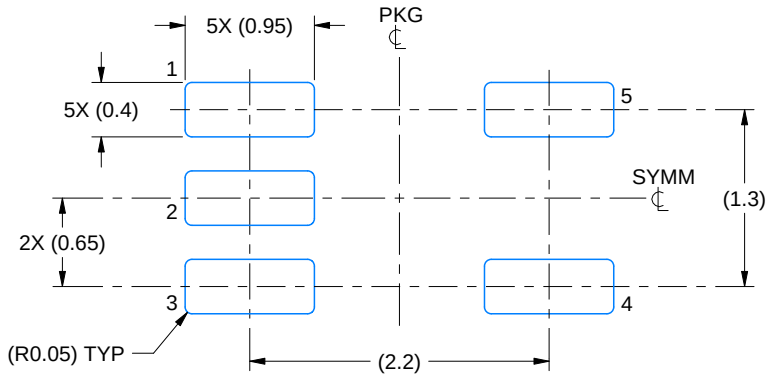
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.



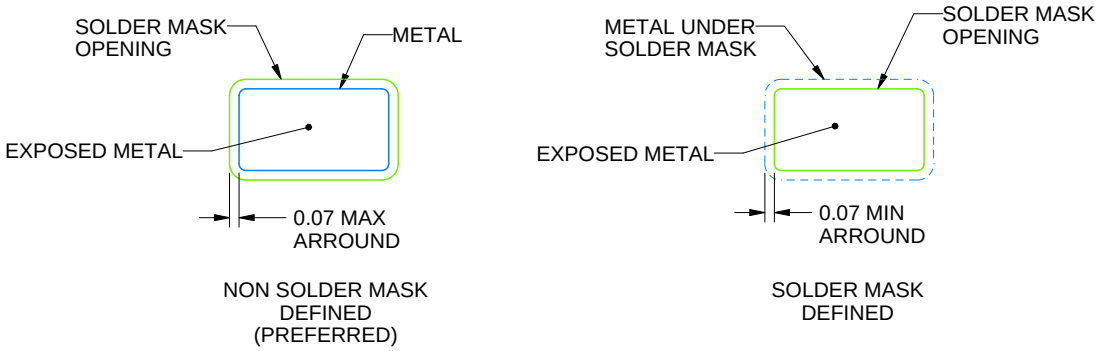
4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

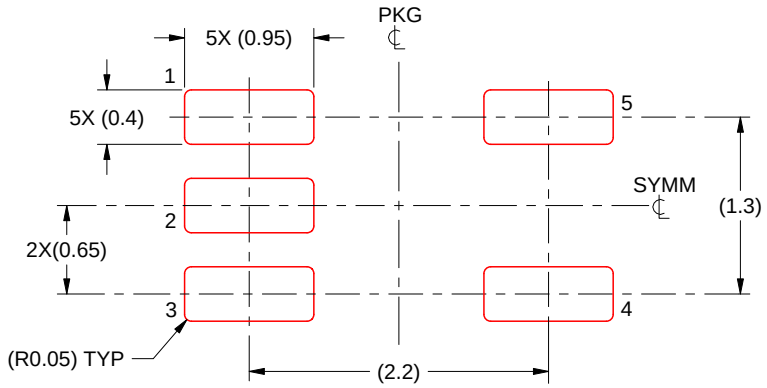


SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



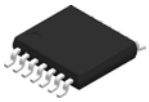
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

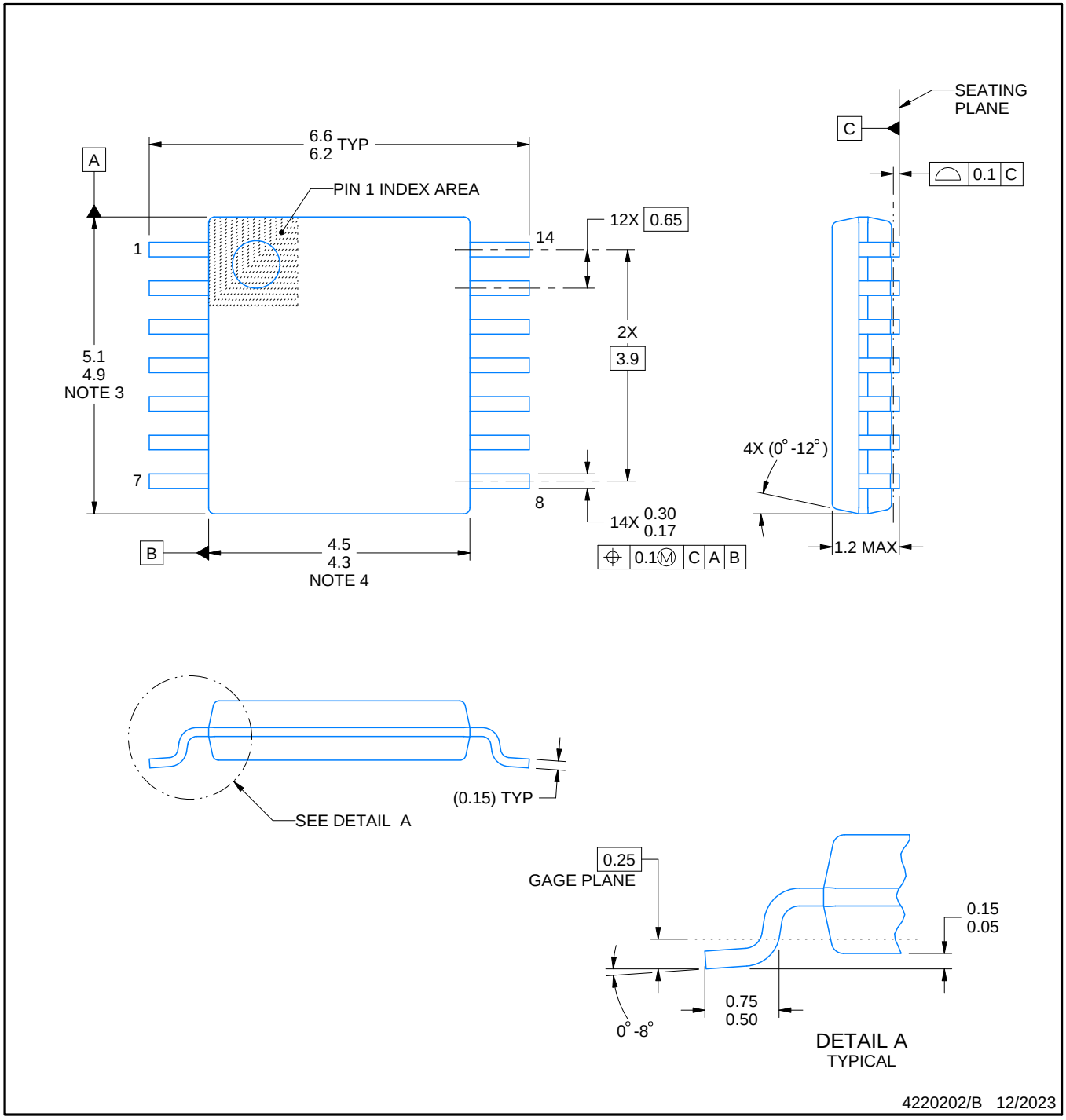
PW0014A



PACKAGE OUTLINE

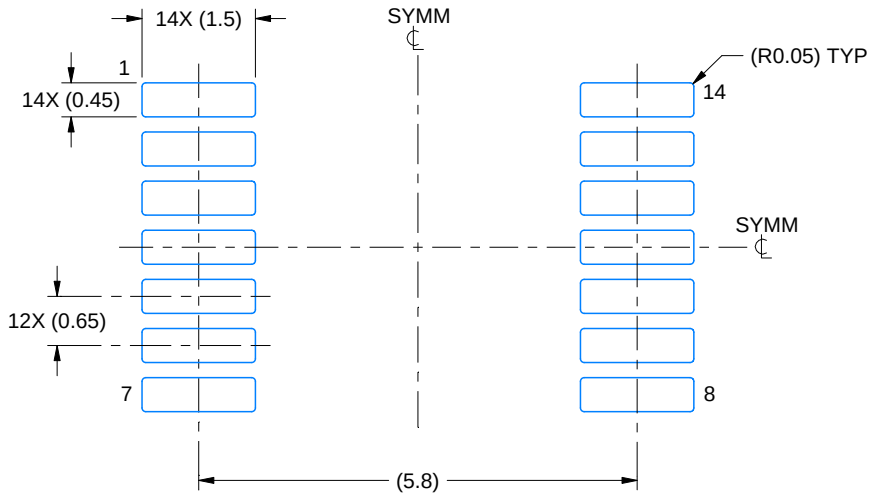
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

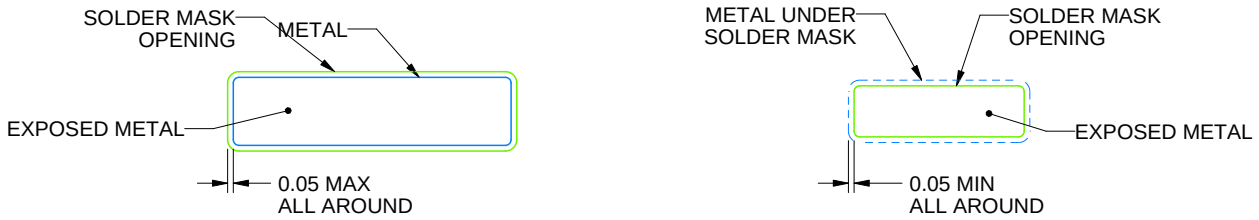


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

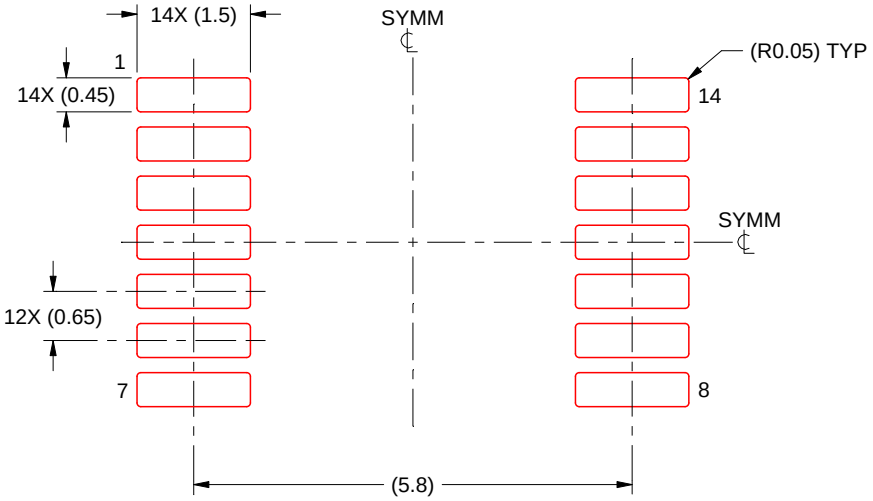
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

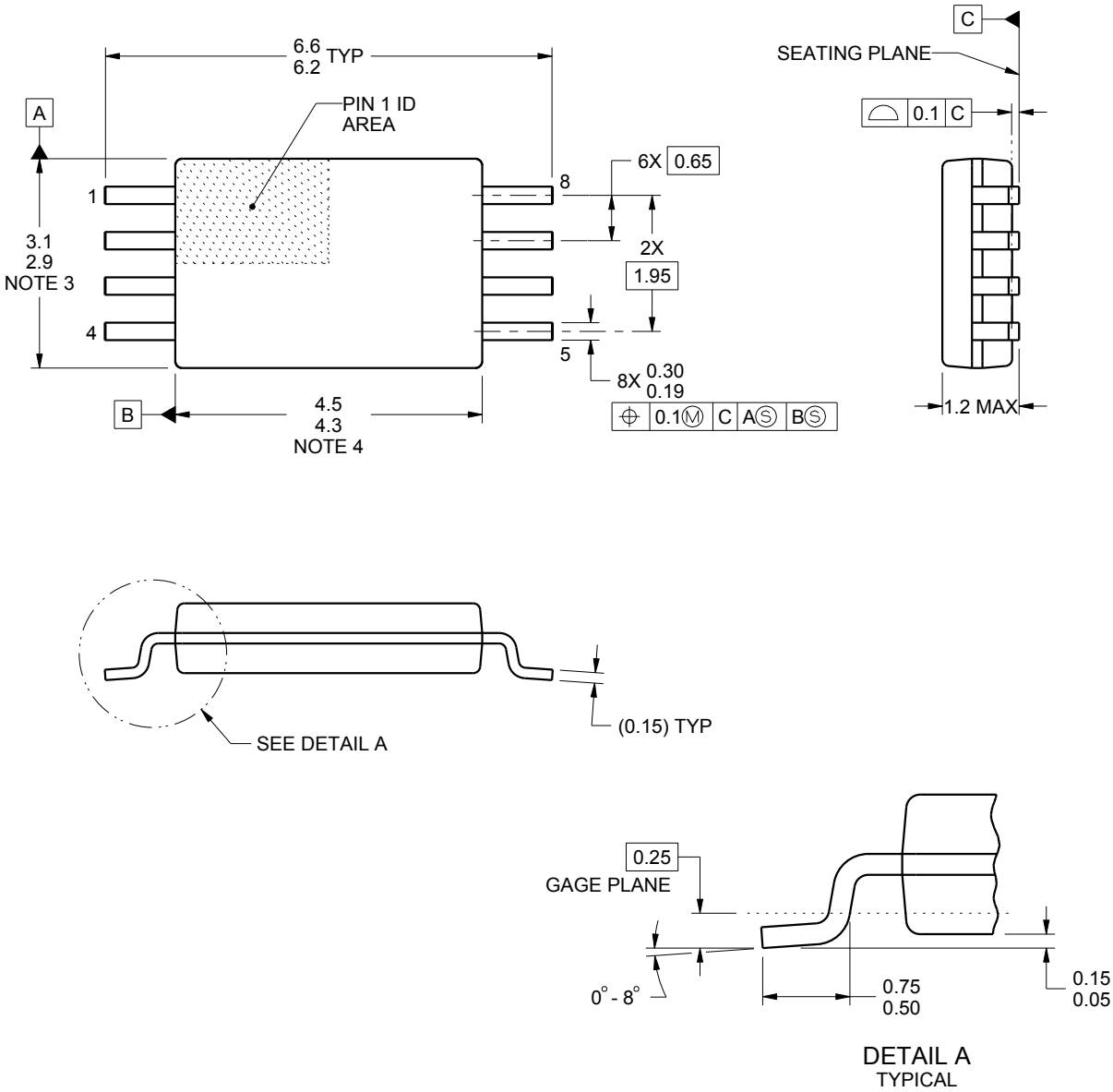


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

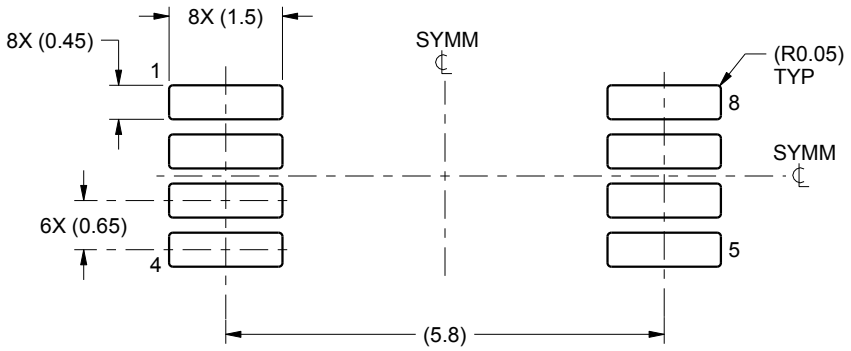
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

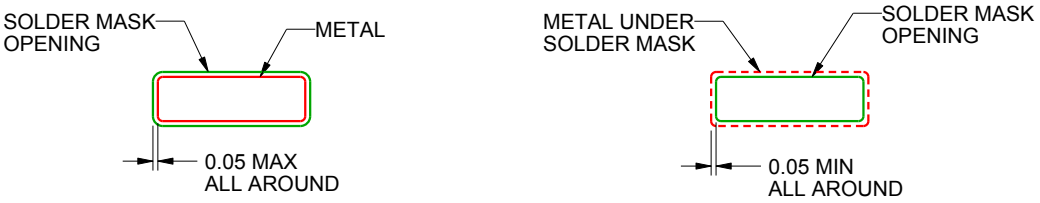


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

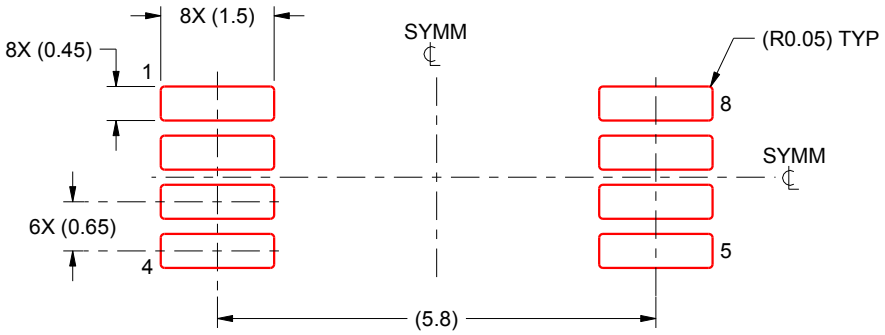
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024，德州仪器 (TI) 公司