

FEATURES

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT™ and Compatibles**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Supports Data Rates up to 120 kbit/s**
- **ESD Protection Meets or Exceeds 10 kV on RS-232 Pins and 3.5 kV on All Other Pins (Human-Body Model)**
- **Pin-to-Pin Compatible With the SN75C185**

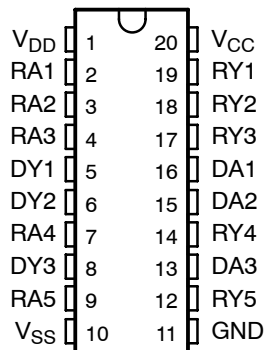
DESCRIPTION/ORDERING INFORMATION

The SN75185 combines three drivers and five receivers from the TI SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of IBM™ PC/AT™ and compatibles. The bipolar circuits and processing of the SN75185 provide a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

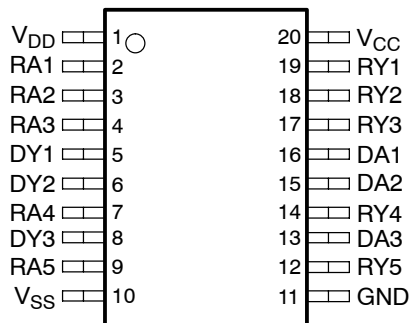
The SN75185 complies with the requirements of the TIA/EIA-232-F and ITU v.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75185 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates to 120 kbit/s, use of TIA/EIA-423-B (ITU v.10) and TIA/EIA-422-B (ITU v.11) standards is recommended.

The SN75185 is characterized for operation over the temperature range of 0°C to 70°C.

**N PACKAGE
(TOP VIEW)**



**DB, DW, OR PW PACKAGE
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

IBM, PC/AT are trademarks of IBM Corporation.

SN75185

MULTIPLE RS-232 DRIVERS AND RECEIVERS

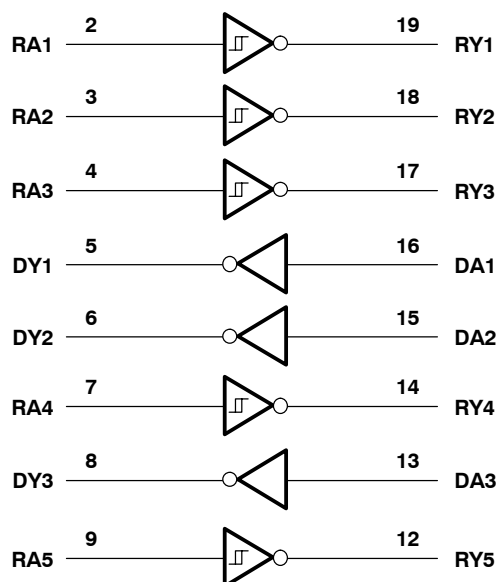
SLLS181D–DECEMBER 1994–REVISED JANUARY 2006

ORDERING INFORMATION

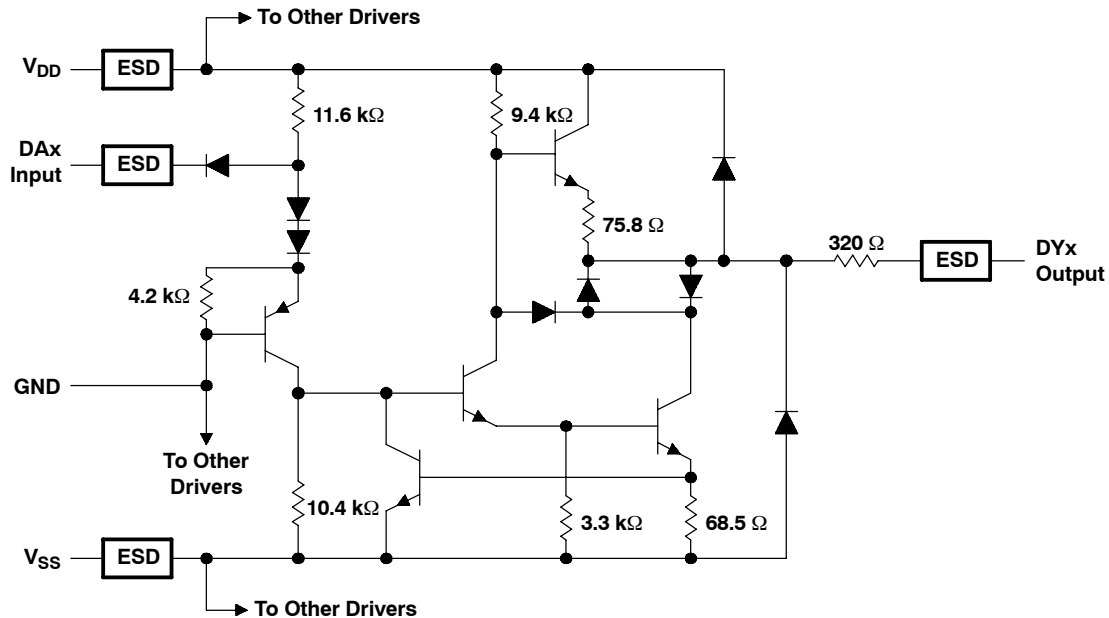
T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN75185N	SN75185N
	SOIC – DW	Tube of 25	SN75185DW	SN75185
		Reel of 2000	SN75185DWR	
	SSOP – DB	Tube of 70	SN75185DB	A185
		Reel of 2000	SN75185DBR	
	TSSOP – PW	Tube of 70	SN75185PW	A185
		Reel of 2000	SN75185PWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

LOGIC DIAGRAM (POSITIVE LOGIC)

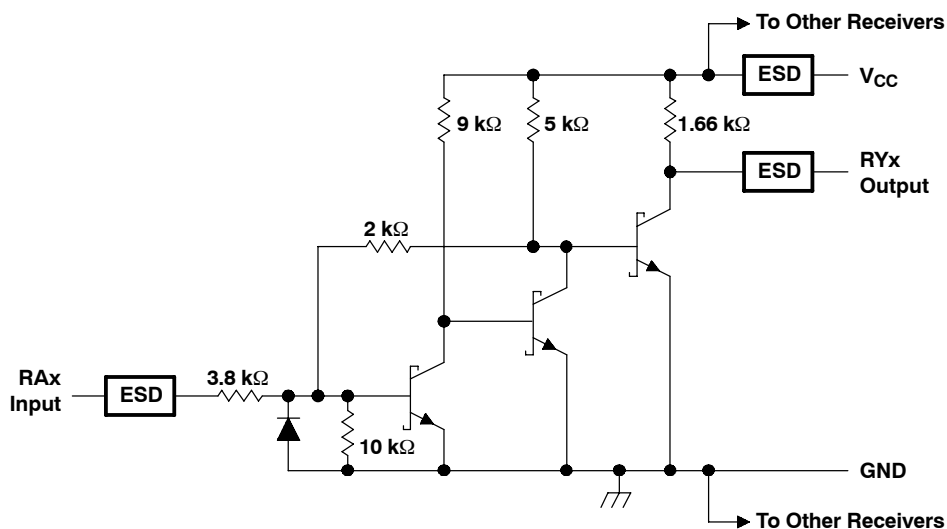


SCHEMATIC OF DRIVERS



Resistor values shown are nominal.

SCHEMATIC (EACH RECEIVER)



Resistor values shown are nominal.

SN75185

MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS181D–DECEMBER 1994–REVISED JANUARY 2006

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾			10	V
V _{DD}	Supply voltage ⁽²⁾			15	V
V _{SS}	Supply voltage ⁽²⁾			−15	V
Input voltage range		Driver	−15	7	V
		Receiver	−30	30	
Driver output voltage range			−15	15	V
Receiver low-level output current				20	mA
θ _{JA}	Package thermal impedance ^{(3) (4)}	DB package		70	°C/W
		DW package		58	
		N package		69	
		PW package		83	
T _J	Operating virtual junction temperature			150	°C
Electrostatic discharge		Human-Body Model	RS-232 pins, class 3, A ⁽⁵⁾	10	kV
			All pins, class 3, A ⁽⁶⁾	3.5	
		Machine Model	RS-232 pins, class 3, B ⁽⁷⁾	600	V
			All pins, class 3, B ⁽⁵⁾	250	
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the network ground terminal.
- (3) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) RS-232 pins are tested with respect to ground and to each other.
- (6) Per MIL-PRF-38535
- (7) RS-232 pins are tested with respect to ground.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	7.5	9	15	V
V_{SS}	Supply voltage	-7.5	-9	-15	V
V_{IH}	High-level input voltage (drivers only)	1.9			V
V_{IL}	Low-level input voltage (drivers only)			0.8	V
I_{OH}	High-level output current	Drivers		-6	mA
		Receivers		-0.5	
I_{OL}	Low-level output current	Drivers		6	mA
		Receivers		16	
T_A	Operating free-air temperature	0		70	°C

Supply Currents

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	All inputs at 5 V,	No load, $V_{CC} = 5$ V		30	mA
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V	15	mA
				$V_{DD} = 12$ V, $V_{SS} = -12$ V	19	
				$V_{DD} = 15$ V, $V_{SS} = -15$ V	25	
		All inputs at 0.8 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V	4.5	
				$V_{DD} = 12$ V, $V_{SS} = -12$ V	5.5	
				$V_{DD} = 15$ V, $V_{SS} = -15$ V	9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V	-15	mA
				$V_{DD} = 12$ V, $V_{SS} = -12$ V	-19	
				$V_{DD} = 15$ V, $V_{SS} = -15$ V	-25	
		All inputs at 0.8 V,	No load	$V_{DD} = 9$ V, $V_{SS} = -9$ V	-3.2	
				$V_{DD} = 12$ V, $V_{SS} = -12$ V	-3.2	
				$V_{DD} = 15$ V, $V_{SS} = -15$ V	-3.2	

SN75185

MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS181D–DECEMBER 1994–REVISED JANUARY 2006



DRIVER SECTION

Electrical Characteristics

over recommended operating free-air temperature range, $V_{DD} = 9\text{ V}$, $V_{SS} = -9\text{ V}$, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$V_{IL} = 0.8\text{ V}$, $R_L = 3\text{ k}\Omega$, See Figure 1	6	7.5		V
V_{OL} Low-level output voltage ⁽¹⁾	$V_{IH} = 1.9\text{ V}$, $R_L = 3\text{ k}\Omega$, See Figure 1		-7.5	-6	V
I_{IH} High-level input current	$V_I = 5\text{ V}$, See Figure 2			10	μA
I_{IL} Low-level input current	$V_I = 0$, See Figure 2			-1.6	mA
$I_{OS(H)}$ High-level short-circuit output current ⁽²⁾	$V_{IL} = 0.8\text{ V}$, $V_O = 0$, See Figure 1	-4.5	-12	-19.5	mA
$I_{OS(L)}$ Low-level short-circuit output current	$V_{IH} = 2\text{ V}$, $V_O = 0$, See Figure 1	4.5	12	19.5	mA
r_o Output resistance ⁽³⁾	$V_{CC} = V_{DD} = V_{SS} = 0$, $V_O = -2\text{ V to } 2\text{ V}$	300			Ω

- (1) The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if -10 V is maximum, the typical value is a more negative voltage).
- (2) Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
- (3) Test conditions are those specified by TIA/EIA-232-F and as listed above.

Switching Characteristics

$V_{CC} = 5\text{ V}$, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$		315	500	ns
t_{PHL} Propagation delay time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$		75	175	ns
t_{TLH} Transition time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$		60	100	ns
	$C_L = 2500\text{ pF}$ ⁽¹⁾		1.7	2.5	μs
t_{THL} Transition time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $C_L = 15\text{ pF}$		40	75	ns
	$C_L = 2500\text{ pF}$ ⁽²⁾		1.5	2.5	μs

- (1) Measured between -3 V and 3 V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.
- (2) Measured between 3 V and -3 V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

RECEIVER SECTION

Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{T+}	Positive-going threshold voltage	See Figure 5	T _A = 25°C	1.75	1.9	2.3	V
			T _A = 0°C to 70°C	1.55		2.3	
V _{T-}	Negative-going threshold voltage			0.75	0.97	1.25	V
V _{hys}	Input hysteresis (V _{T+} – V _{T-})			0.5			V
V _{OH}	High-level output voltage	I _{OH} = –0.5 mA	V _{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V _{OL}	Low-level input voltage	I _{OL} = 10 mA,	V _I = 3 V		0.2	0.45	V
I _{IH}	High-level input current	V _I = 25 V,	See Figure 5	3.6		8.3	mA
		V _I = 3 V,	See Figure 5	0.43			
I _{IL}	Low-level output current	V _I = –25 V,	See Figure 5	–3.6		–8.3	mA
		V _I = –3 V,	See Figure 5	–0.43			
I _{OS}	Short-circuit output current	See Figure 4			–3.4	–12	mA

(1) All typical values are at $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 9\text{ V}$, and $V_{SS} = -9\text{ V}$.

Switching Characteristics

$V_{CC} = 5\text{ V}$, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $T_A = 25^{\circ}\text{C}$ (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$		107	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$		42	150	ns
t_{TLH}	Transition time, low- to high-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$		175	525	ns
t_{THL}	Transition time, high- to low-level output	$C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$		16	60	ns

PARAMETER MEASUREMENT INFORMATION

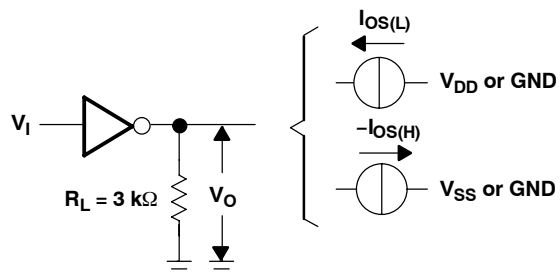


Figure 1. Driver Test Circuit for V_{OH} , V_{OL} , $I_{OS(H)}$, and $I_{OS(L)}$

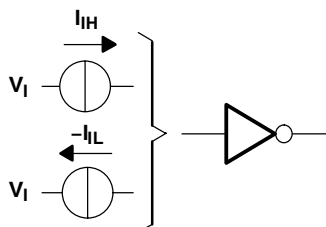
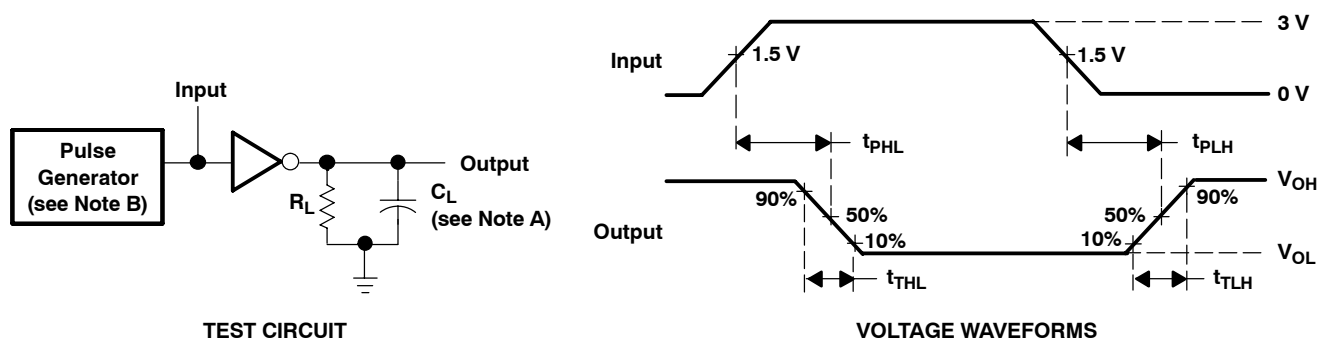


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $t_w = 25\text{ }\mu\text{s}$, $\text{PRR} = 20\text{ kHz}$, $Z_O = 50\text{ }\Omega$, $t_r = t_f < 50\text{ ns}$.

Figure 3. Driver Test Circuit and Voltage Waveforms

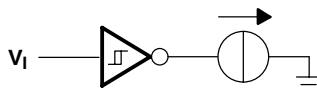


Figure 4. Receiver Test Circuit for I_{OS}

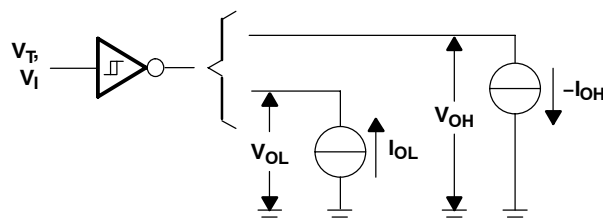
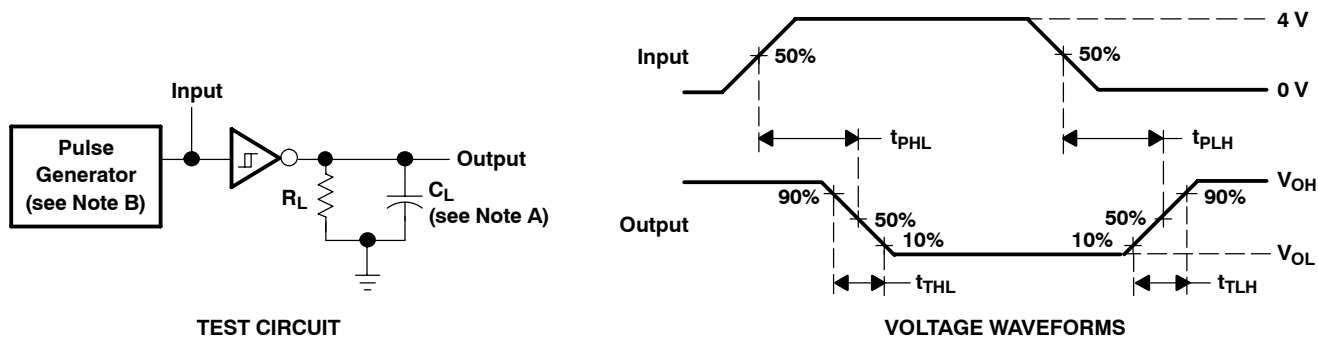


Figure 5. Receiver Test Circuit for V_T , V_{OH} , and V_{OL}

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

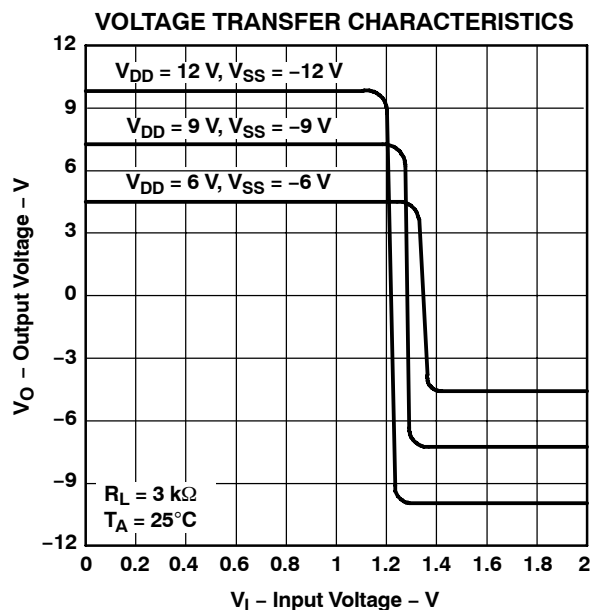


Figure 7.

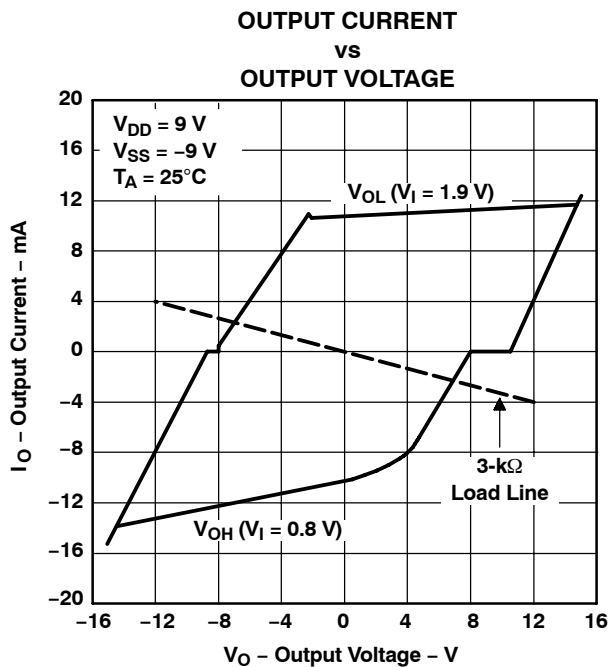


Figure 8.

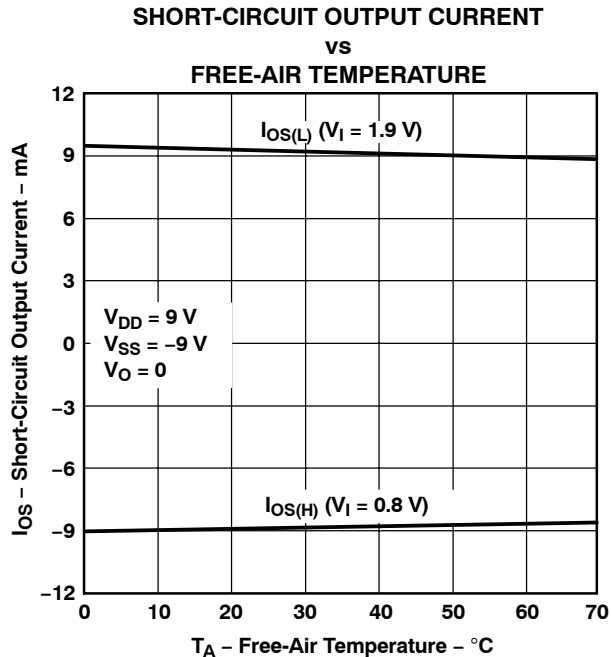


Figure 9.

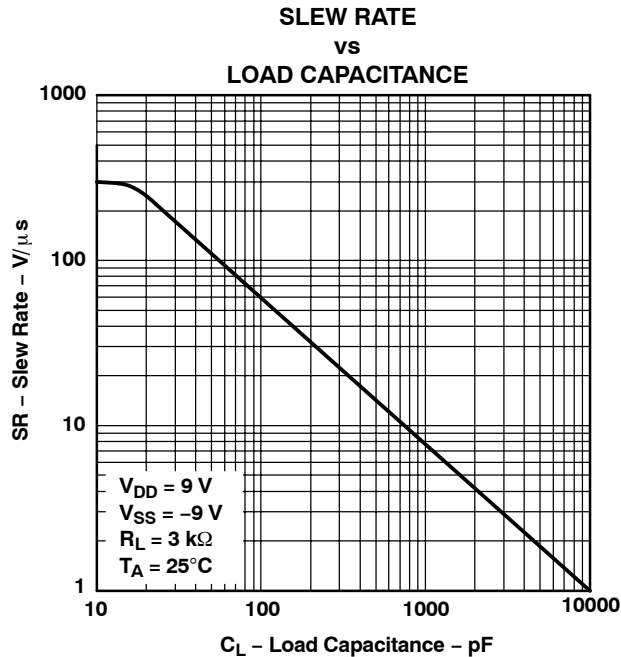


Figure 10.

TYPICAL CHARACTERISTICS

RECEIVER SECTION

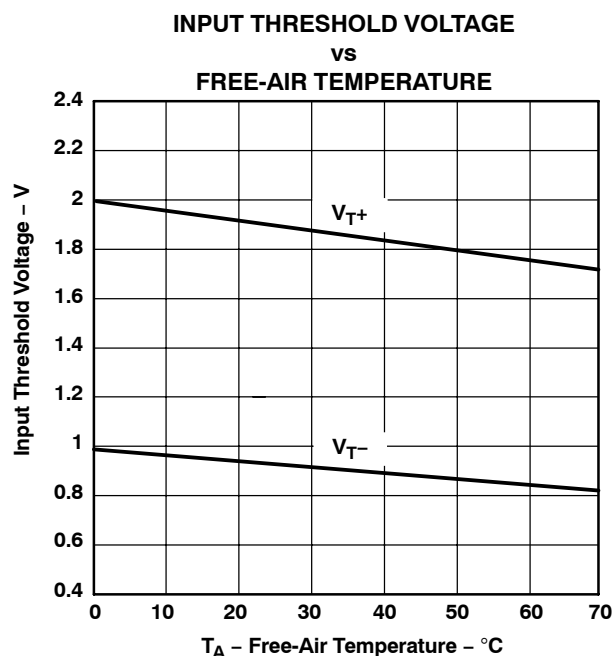


Figure 11.

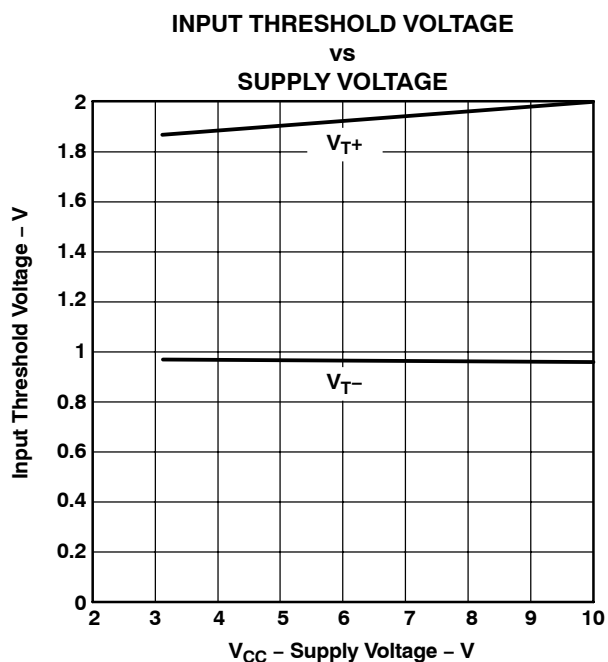
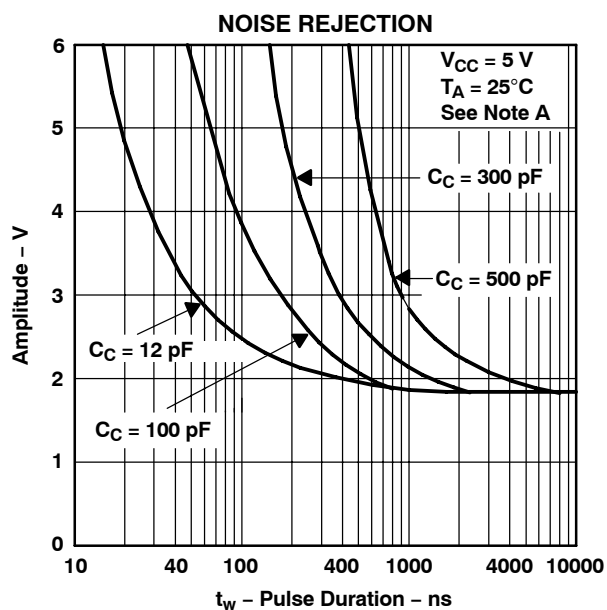


Figure 12.



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 13.

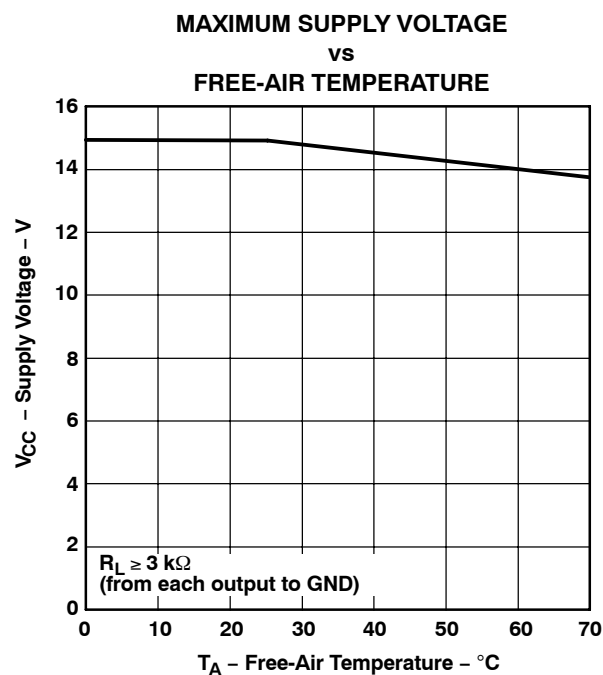


Figure 14.

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75185 in the fault condition. In the fault condition, the device outputs are shorted to ± 15 V, and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

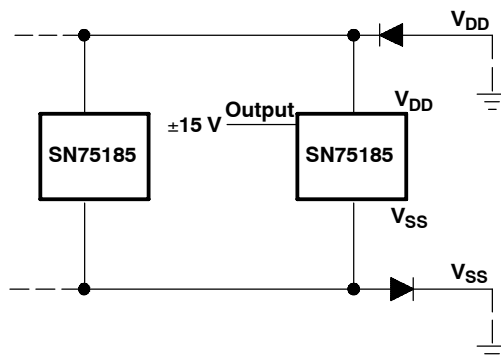
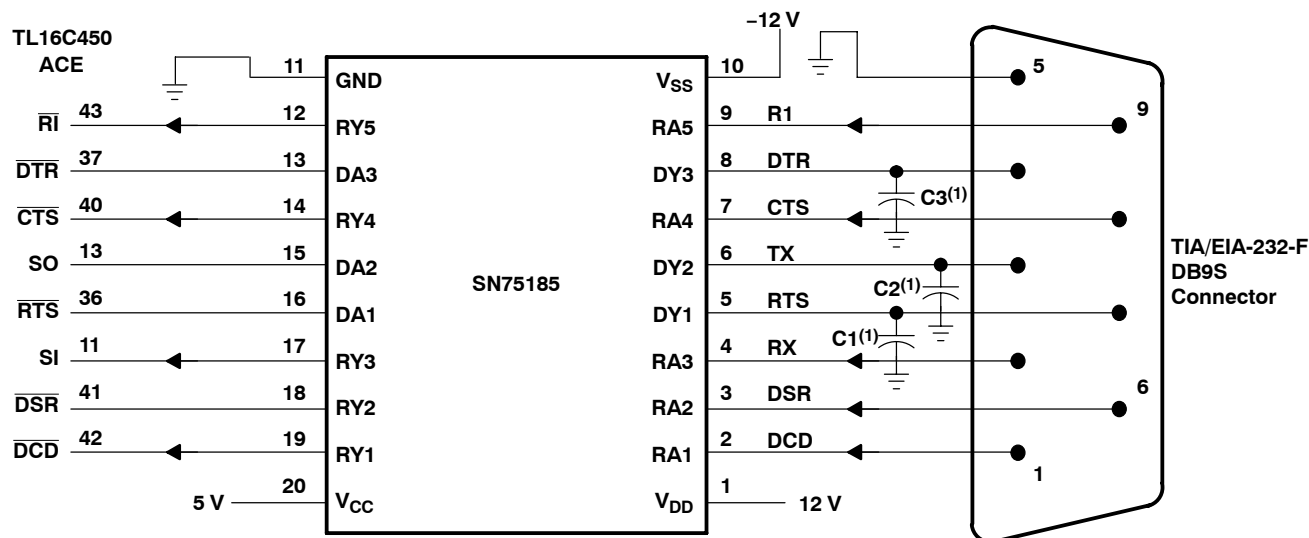


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



- (1) See Figure 10 to select the correct values for the loading capacitors (C1, C2, and C3), which are required to meet the RS-232 maximum slew-rate requirement of 30 V/ μ s. The value of the loading capacitors required depends on the line length and desired slew rate, but typically is 330 pF.

Figure 16. Typical Connection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75185DB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	Samples
SN75185DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	Samples
SN75185DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185	Samples
SN75185N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75185N	Samples
SN75185PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A185	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75185DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75185DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75185PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75185DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN75185DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75185PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).



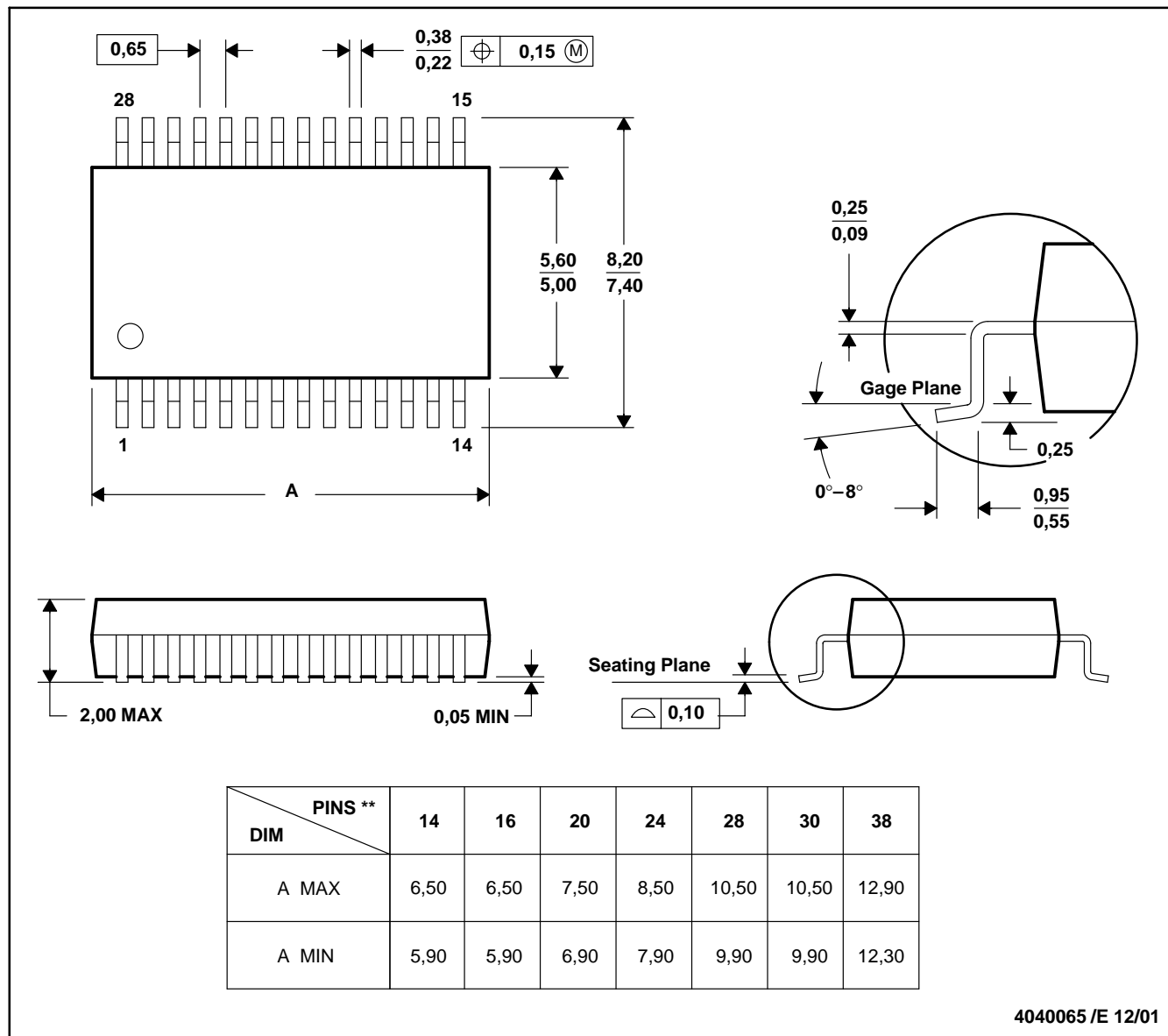
4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com