

SNx4HC374 具有三态输出的八路边沿触发 D 类触发器

1 特性

- 2V 至 6V 的宽工作电压范围
- 高电流三态真实输出最多可驱动 15 个 LSTTL 负载
- 单个封装中包含八路 D 类触发器
- 针对负载的完全并行访问
- 低功耗， I_{CC} 最大 80 μ A
- t_{pd} 典型值 = 14 ns
- ± 6 mA 输出驱动 (电压为 5V 时)
- 低输出电流，最大值 1 μ A

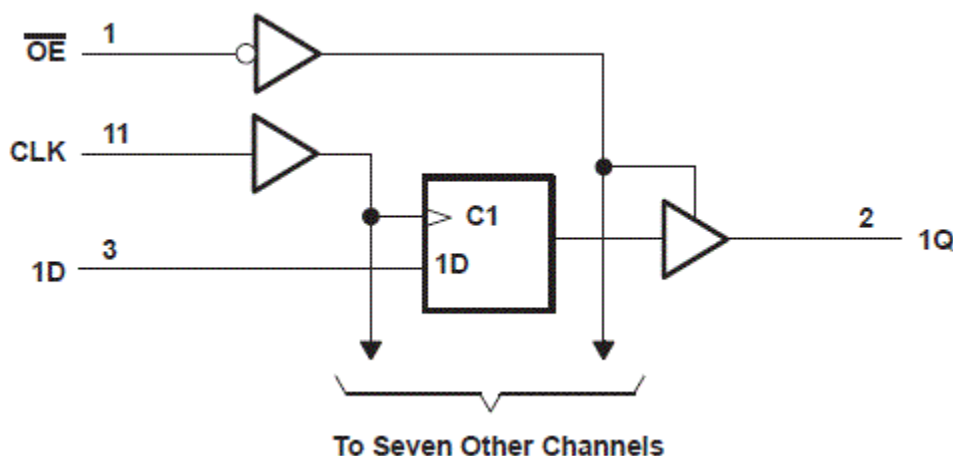
2 说明

这些 8 位触发器具有专门设计用于驱动高电容或相对低阻抗负载的三态输出。它们特别适合于实现缓冲寄存器、I/O 端口、双向总线驱动器和工作寄存器。

器件信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 (标称值) |
|-------------|-------------------|--------------------|
| SN74HC374DW | SOIC (20) | 12.80mm × 7.50mm |
| SN74HC374DB | SSOP (20) | 7.20mm × 5.30mm |
| SN74HC374N | PDIP (20) | 25.40mm × 6.35mm |
| SN74HC374NS | SO (20) | 15.00 mm × 5.30 mm |
| SN74HC374PW | TSSOP (20) | 6.50mm × 4.40mm |
| SN54HC374J | CDIP (20) | 26.92mm × 6.92mm |
| SN54HC374FK | LCCC (20) | 8.89mm × 8.89mm |
| SN54HC374W | CFP (20) | 13.09 mm × 6.92 mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图



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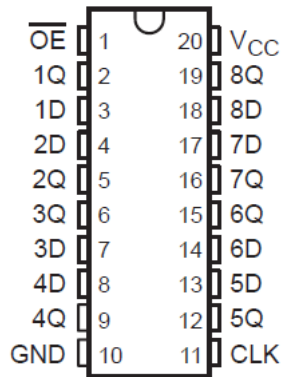
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

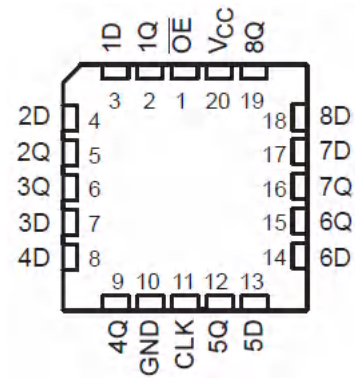
| Changes from Revision F (December 2021) to Revision G (April 2022) | Page |
|--|-------------|
| • Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, DB was 70 is now 122.7, N was 69 is now 84.6, NS was 60 is now 113.4, PW was 83 is now 131.8..... | 4 |

| Changes from Revision E (August 2003) to Revision F (December 2021) | Page |
|--|-------------|
| • 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准..... | 1 |

4 Pin Configuration and Functions



J, W, DB, DW, N, NS, or PW package
20-Pin CDIP, CFP, SSOP, SOIC, PDIP, SO, or TSSOP
Top View



FK package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--|-----|--------|
| V _{CC} | Supply voltage range | - 0.5 | 7 | V |
| I _{IK} | Input clamp current ⁽²⁾ | V _I < 0 or V _I > V _{CC} | | ±20 mA |
| I _{OK} | Output clamp current ⁽²⁾ | V _O < 0 or V _O > V _{CC} | | ±20 mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±35 mA |
| | Continuous current through V _{CC} or GND | | | ±70 mA |
| T _J | Junction temperature | | | 150 °C |
| T _{stg} | Storage temperature range | - 65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

| | | SN54HC374 | | | SN74HC374 | | | UNIT |
|-----------------|-------------------------------------|-------------------------|-----|-----------------|-----------|-----------------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | | 1.5 | 1.5 | | V | |
| | | V _{CC} = 4.5 V | | 3.15 | 3.15 | | | |
| | | V _{CC} = 6 V | | 4.2 | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | | 0.5 | 0.5 | V | |
| | | V _{CC} = 4.5 V | | | 1.35 | 1.35 | | |
| | | V _{CC} = 6 V | | | 1.8 | 1.8 | | |
| V _I | Input voltage | 0 | | V _{CC} | 0 | V _{CC} | V | |
| V _O | Output voltage | 0 | | V _{CC} | 0 | V _{CC} | V | |
| Δt/Δv | Input transition rise and fall time | V _{CC} = 2 V | | | 1000 | 1000 | ns | |
| | | V _{CC} = 4.5 V | | | 500 | 500 | | |
| | | V _{CC} = 6 V | | | 400 | 400 | | |
| T _A | Operating free-air temperature | - 55 | | 125 | - 40 | 85 | °C | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

| THERMAL METRIC | | SN74HC374 | | | | | UNIT |
|-----------------------|---|-----------|-----------|----------|---------|------------|------|
| | | DW (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽¹⁾ | 109.1 | 122.7 | 84.6 | 113.4 | 131.8 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 76 | 81.6 | 72.5 | 78.6 | 72.2 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 77.6 | 77.5 | 65.3 | 78.4 | 82.8 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 51.5 | 46.1 | 55.3 | 47.1 | 21.5 | °C/W |

5.3 Thermal Information (continued)

| THERMAL METRIC | | SN74HC374 | | | | | UNIT |
|----------------------|--|-----------|-----------|----------|---------|------------|------|
| | | DW (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| Ψ_{JB} | Junction-to-board characterization parameter | 77.1 | 77.1 | 65.2 | 78.1 | 82.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC374 | | SN74HC374 | | UNIT |
|-----------|--------------------------------|----------------------------|--------------------------|------------|-----------|-----------|------------|------------|---------------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V_{OH} | $V_I = V_{IH}$ or V_{IL} | $I_{OH} = -20 \mu\text{A}$ | 2 V | 1.9 | 1.998 | | 1.9 | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | 5.9 | | |
| | | $I_{OH} = -6 \text{ mA}$ | 4.5 V | 3.98 | 4.3 | | 3.7 | 3.84 | | |
| | | $I_{OH} = -7.8 \text{ mA}$ | 6 V | 5.48 | 5.8 | | 5.2 | 5.34 | | |
| V_{OL} | $V_I = V_{IH}$ or V_{IL} | $I_{OL} = 20 \mu\text{A}$ | 2 V | | 0.002 | 0.1 | | 0.1 | V | |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | |
| | | $I_{OL} = 6 \text{ mA}$ | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 |
| | | $I_{OL} = 7.8 \text{ mA}$ | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 |
| I_I | $V_I = V_{CC}$ or 0 | 6 V | | ± 0.1 | ± 100 | | ± 1000 | ± 1000 | nA | |
| I_{OZ} | $V_O = V_{CC}$ or 0 | 6 V | | ± 0.01 | ± 0.5 | | ± 10 | ± 5 | μA | |
| I_{CC} | $V_I = V_{CC}$ or 0, $I_O = 0$ | 6 V | | | 8 | | 160 | 80 | μA | |
| C_i | | 2 V to 6 V | | 3 | 10 | | 10 | 10 | pF | |

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | V_{CC} | $T_A = 25^\circ\text{C}$ | | SN54HC374 | | SN74HC374 | | UNIT |
|---|----------|--------------------------|-----|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} Clock frequency | 2 V | | 6 | | 4 | | 5 | MHz |
| | 4.5 V | | 30 | | 20 | | 24 | |
| | 6 V | | 35 | | 24 | | 28 | |
| t_w Pulse duration, CLK high or low | 2 V | | 80 | | 120 | | 100 | ns |
| | 4.5 V | | 16 | | 24 | | 20 | |
| | 6 V | | 14 | | 20 | | 17 | |
| t_{su} Setup time, data before CLK \uparrow | 2 V | | 100 | | 150 | | 125 | ns |
| | 4.5 V | | 20 | | 30 | | 25 | |
| | 6 V | | 17 | | 25 | | 21 | |
| t_h Hold time, data after CLK \uparrow | 2 V | | 10 | | 13 | | 12 | ns |
| | 4.5 V | | 5 | | 5 | | 5 | |
| | 6 V | | 5 | | 5 | | 5 | |

5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [图 6-1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC374 | | SN74HC374 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 2 V | 6 | 12 | | 4 | | 5 | MHz | |
| | | | 4.5 V | 30 | 60 | | 20 | | 24 | | |
| | | | 6 V | 35 | 70 | | 24 | | 28 | | |
| t_{pd} | CLK | Any Q | 2 V | | 63 | 180 | | 270 | | 225 | ns |
| | | | 4.5 V | | 17 | 36 | | 54 | | 45 | |
| | | | 6 V | | 15 | 31 | | 46 | | 38 | |
| t_{en} | \overline{OE} | Any Q | 2 V | | 60 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 16 | 30 | | 45 | | 38 | |
| | | | 6 V | | 14 | 26 | | 38 | | 32 | |
| t_{dis} | \overline{OE} | Any Q | 2 V | | 36 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 17 | 30 | | 45 | | 38 | |
| | | | 6 V | | 16 | 26 | | 38 | | 32 | |
| t_t | | Any Q | 2 V | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 V | | 8 | 12 | | 18 | | 15 | |
| | | | 6 V | | 6 | 10 | | 15 | | 13 | |

5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see [图 6-1](#))

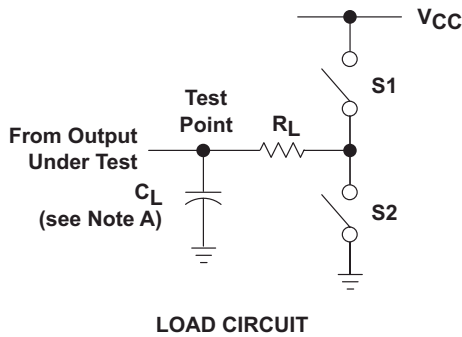
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC374 | | SN74HC374 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 2 V | 6 | 12 | | | | 5 | MHz | |
| | | | 4.5 V | 30 | 60 | | | | 24 | | |
| | | | 6 V | 35 | 70 | | | | 28 | | |
| t_{pd} | CLK | Any Q | 2 V | | 80 | 230 | | 345 | | 290 | ns |
| | | | 4.5 V | | 22 | 46 | | 69 | | 58 | |
| | | | 6 V | | 19 | 39 | | 58 | | 49 | |
| t_{en} | \overline{OE} | Any Q | 2 V | | 70 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 25 | 40 | | 60 | | 50 | |
| | | | 6 V | | 22 | 34 | | 51 | | 43 | |
| t_t | | Any Q | 2 V | | 45 | 210 | | 315 | | 265 | ns |
| | | | 4.5 V | | 17 | 42 | | 63 | | 53 | |
| | | | 6 V | | 13 | 36 | | 53 | | 45 | |

5.8 Operating Characteristics

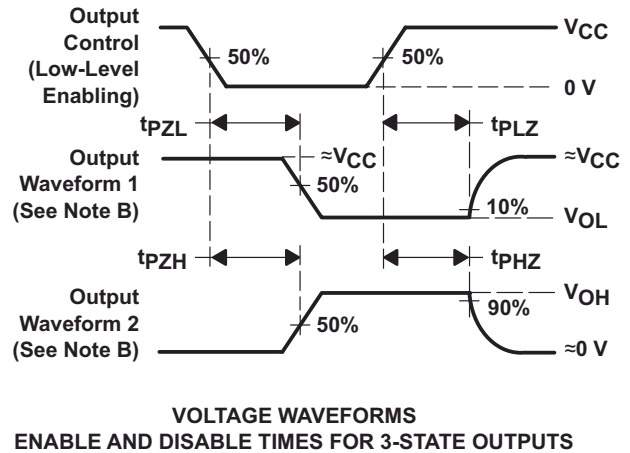
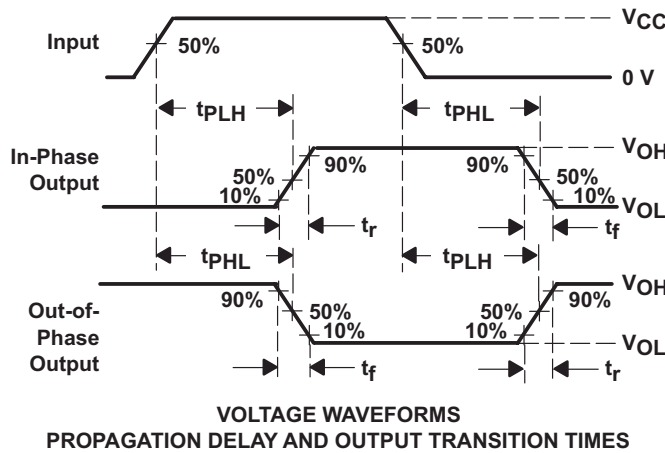
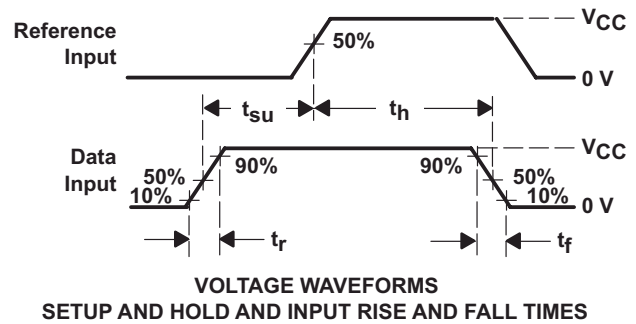
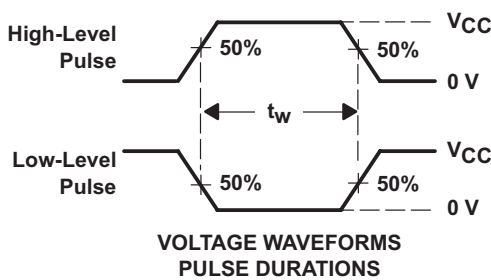
$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance per flip-flop | No load | 100 | pF |

6 Parameter Measurement Information



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | -- | 50 pF or 150 pF | Open | Open |



- NOTES:
- C_L includes probe and test-fixtue capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

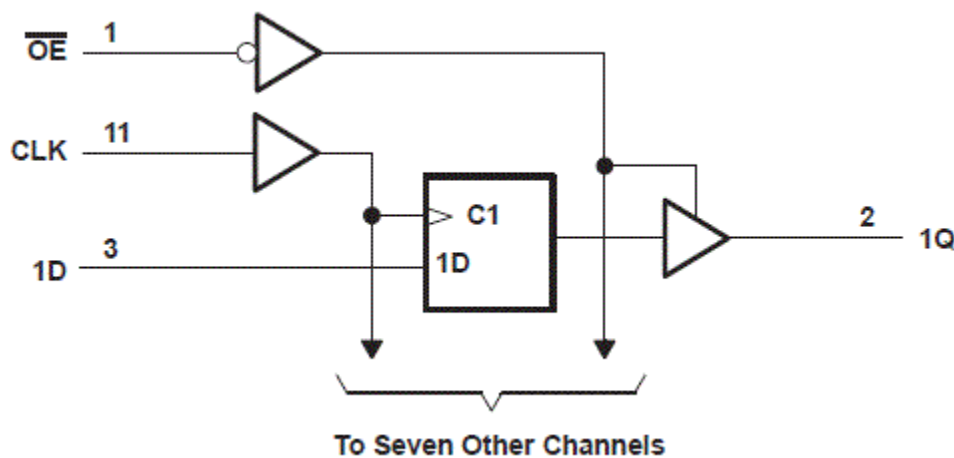
The eight flip-flops of the ' HC374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Function Table
(each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-8407101VRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8407101VR A SNV54HC374J | Samples |
| 5962-8407101VSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8407101VS A SNV54HC374W | Samples |
| 84071012A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 84071012A SNJ54HC 374FK | Samples |
| 8407101RA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8407101RA SNJ54HC374J | Samples |
| 8407101SA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8407101SA SNJ54HC374W | Samples |
| JM38510/65602BRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65602BRA | Samples |
| M38510/65602BRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65602BRA | Samples |
| SN54HC374J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HC374J | Samples |
| SN74HC374DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC374 | Samples |
| SN74HC374DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC374 | Samples |
| SN74HC374DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC374 | Samples |
| SN74HC374N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC374N | Samples |
| SN74HC374NE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC374N | Samples |
| SN74HC374NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC374 | Samples |
| SN74HC374PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC374 | Samples |
| SNJ54HC374FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 84071012A SNJ54HC 374FK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|--------------------------|-------------------------|
| SNJ54HC374J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8407101RA SNJ54HC374J | Samples |
| SNJ54HC374W | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8407101SA SNJ54HC374W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC374, SN54HC374-SP, SN74HC374 :

- Catalog : [SN74HC374](#), [SN54HC374](#)
- Military : [SN54HC374](#)
- Space : [SN54HC374-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC374DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC374DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HC374DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HC374NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74HC374NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74HC374PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74HC374PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC374DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC374DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HC374DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HC374NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HC374NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HC374PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC374PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-8407101VSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 84071012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 8407101SA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74HC374N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC374NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC374FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC374W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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