SBOS266E − JUNE 2003 − REVISED AUGUST 2008

Low-Power, Single-Supply, Fixed-Gain Video Buffer Amplifier

FEATURES

- HIGH BANDWIDTH: 80MHz (G = +2)
- LOW SUPPLY CURRENT: 3.9mA
- FLEXIBLE SUPPLY RANGE:
  +2.8V to +11V Single Supply
  ±1.4V to ±5.5V Dual Supply
- INPUT RANGE INCLUDES GROUND ON SINGLE SUPPLY
- 4.9V_{PP} OUTPUT SWING ON +5V SUPPLY
- HIGH SLEW RATE: 350V/µsec
- LOW INPUT VOLTAGE NOISE: 9.3nV/$\sqrt{Hz}$
- Pb-FREE SOT23 PACKAGE

APPLICATIONS

- SINGLE-SUPPLY VIDEO LINE DRIVERS
- CCD IMAGING CHANNELS
- LOW-POWER ULTRASOUND
- PORTABLE CONSUMER ELECTRONICS

DESCRIPTION

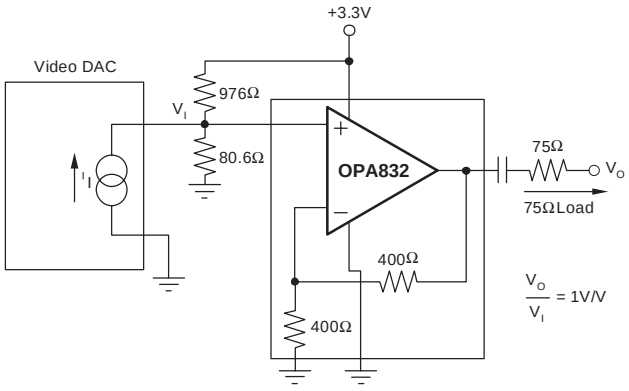
The OPA832 is a low-power, high-speed, fixed-gain amplifier designed to operate on a single +3.3V or +5V supply. Operation on ±5V or +10V supplies is also supported. The input range extends below ground and to within 1V of the positive supply. Using complementary common-emitter outputs provides an output swing to within 30mV of ground and 130mV of the positive supply. The high output drive current and low differential gain and phase errors also make it ideal for single-supply consumer video products.

Low distortion operation is ensured by the high gain bandwidth product (200MHz) and slew rate (850V/µs), making the OPA832 an ideal input buffer stage to 3V and 5V CMOS converters. Unlike other low-power, single-supply amplifiers, distortion performance improves as the signal swing is decreased. A low 9.3nV/$\sqrt{Hz}$ input voltage noise supports wide dynamic range operation.

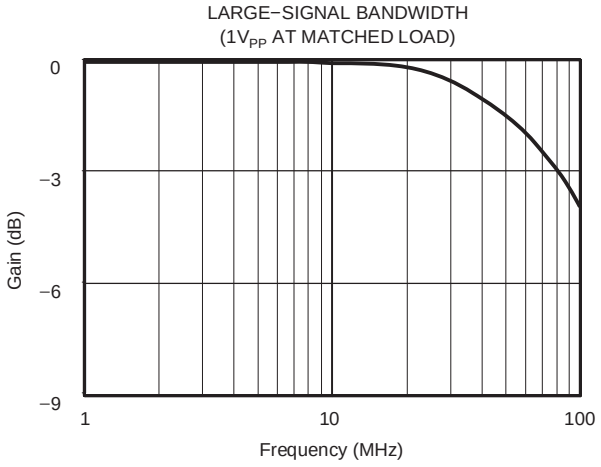
The OPA832 is available in an industry-standard SO-8 package. The OPA832 is also available in an ultra-small SOT23-5 package. For gains other than +1, −1, or +2, consider using the OPA830.

RELATED PRODUCTS

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Medium Speed	OPA830	OPA2830	—	OPA4830
Medium Speed, Fixed Gain	—	OPA2832	OPA3832	—



Single-Supply, Low-Cost Video Line Driver



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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	+12V$_{DC}$
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage(2)	±1.2V
Input Voltage Range (Single Supply)	−0.5V to +V_S + 0.3V
Storage Temperature Range: D, DBV	−65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)	2000V
Charge Device Model (CDM)	1500V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Noninverting input to internal inverting node.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

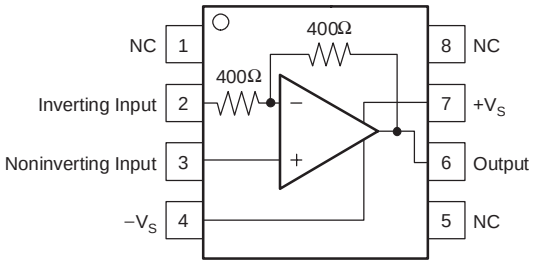
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA832	SO-8 Surface-Mount	D	−40°C to +85°C	OPA832	OPA832ID	Rails, 100
″	″	″	″	″	OPA832IDR	Tape and Reel, 2500
OPA832	SOT23-5	DBV	−40°C to +85°C	A74	OPA832IDBVT	Tape and Reel, 250
″	″	″	″	″	OPA832IDBVR	Tape and Reel, 3000

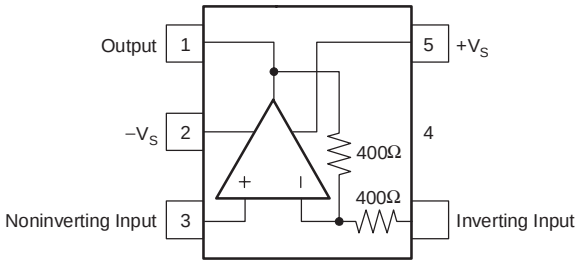
(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

PIN CONFIGURATIONS



SO−8

NC = No Connection



SOT23−5

Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

At T_A = 25°C, G = +2, and R_L = 150Ω to GND, unless otherwise noted (see Figure 3).

PARAMETER	CONDITIONS	OPA832ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	−40°C to +85°C(2)			
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth	G = +2, $V_O \le 0.5V_{PP}$	80	55	54	54	MHz	min	B
	G = −1, $V_O \le 0.5V_{PP}$	99	57	56	56	MHz	min	B
Peaking at a Gain of +1	$V_O \le 0.5V_{PP}$	4.2				dB	typ	C
Slew Rate	G = +2, 2V Step	350	230	230	220	V/µs	min	B
Rise Time	0.5V Step	4.6				ns	max	B
Fall Time	0.5V Step	4.9				ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	45				ns	max	B
Harmonic Distortion	$V_O = 2V_{PP}$, 5MHz							
2nd-Harmonic	R_L = 150Ω	−64	−60	−60	−60	dBc	max	B
	R_L = 500Ω	−66	−63	−63	−63	dBc	max	B
3rd-Harmonic	R_L = 150Ω	−57	−50	−49	−48	dBc	max	B
	R_L = 500Ω	−73	−64	−61	−57	dBc	max	B
Input Voltage Noise	f > 1MHz	9.2				nV/√Hz	max	B
Input Current Noise	f > 1MHz	2.2				pA/√Hz	max	B
NTSC Differential Gain	R_L = 150Ω	0.10				%	typ	C
NTSC Differential Phase	R_L = 150Ω	0.16				°	typ	C
DC PERFORMANCE(4)								
Gain Error	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	min	A
	G = −1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G								
Maximum		400	**455**	460	462	Ω	max	A
Minimum		400	**345**	340	338	Ω	max	A
Average Drift				±0.1	±0.1	%/°C	max	B
Input Offset Voltage		±1.4	**±7**	±8	±8.5	mV	max	A
Average Offset Voltage Drift		—		±20	±20	µV/°C	max	B
Input Bias Current		+5.5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift				±12	±12	nA/°C	max	B
Input Offset Current		±0.1	**±1.5**	±2	±2.5	µA	max	A
Input Offset Current Drift		—		±10	±10	nA/°C	max	B
INPUT								
Negative Input Voltage Range		−5.4	−5.2	−5.0	−4.9	V	max	B
Positive Input Voltage Range		3.2	**3.1**	3.0	2.9	V	min	A
Input Impedance								
Differential Mode		10 || 2.1				kΩ ||pF	typ	C
Common-Mode		400 || 1.2				kΩ ||pF	typ	C
OUTPUT								
Output Voltage Swing	R_L = 1kΩ to GND	±4.9	**±4.8**	±4.75	±4.75	V	max	A
	R_L = 150Ω to GND	±4.6	**±4.5**	±4.45	±4.4	V	max	A
Current Output, Sinking		85	**65**	60	55	mA	min	A
Current Output, Sourcing		85	**65**	60	55	mA	min	A
Short-Circuit Current	Output Shorted to Either Supply	120				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.2				Ω	typ	C
POWER SUPPLY								
Minimum Operating Voltage		±1.4				V	min	B
Maximum Operating Voltage		—	**±5.5**	±5.5	±5.5	V	max	A
Maximum Quiescent Current	V_S = ±5V	4.25	**4.7**	5.3	5.9	mA	max	A
Minimum Quiescent Current	V_S = ±5V	4.25	**4.0**	3.6	3.3	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	68	**63**	62	61	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDBV		−40 to +85				°C	typ	C
Thermal Resistance								
D SO-8		125				°C/W	typ	C
DBV SOT23-5		150				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

At T_A = 25°C, G = +2, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 1).

PARAMETER	CONDITIONS	OPA832ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	−40°C to +85°C(2)			
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth	G = +2, $V_O \le 0.5V_{PP}$	92	56	55	55	MHz	min	B
	G = −1, $V_O \le 0.5V_{PP}$	103	60	58	58	MHz	min	B
Peaking at a Gain of +1	$V_O \le 0.5V_{PP}$	4.2				dB	typ	C
Slew Rate	G = +2, 2V Step	348	230	223	223	V/µs	min	B
Rise Time	0.5V Step	4.3				ns	max	B
Fall Time	0.5V Step	4.6				ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	4.6				ns	max	B
Harmonic Distortion	$V_O = 2V_{PP}$, 5MHz							
2nd-Harmonic	R_L = 150Ω	−59	−56	−56	−55	dBc	max	B
	R_L = 500Ω	−62	−59	−59	−59	dBc	max	B
3rd-Harmonic	R_L = 150Ω	−56	−50	−49	−47	dBc	max	B
	R_L = 500Ω	−72	−65	−62	−58	dBc	max	B
Input Voltage Noise	f > 1MHz	9.3				nV/√Hz	max	B
Input Current Noise	f > 1MHz	2.3				pA/√Hz	max	B
NTSC Differential Gain	R_L = 150Ω	0.11				%	typ	C
NTSC Differential Phase	R_L = 150Ω	0.14				°	typ	C
DC PERFORMANCE(4)								
Gain Error	G = +2	±0.3	±**1.5**	±1.6	±1.7	%	min	A
	G = −1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G, Maximum		400	**455**	460	462	Ω	max	A
Minimum		400	**345**	340	338	Ω	max	A
Average Drift				0.1	0.1	%/°C	max	B
Input Offset Voltage		±0.5	±**5**	±6	±6.5	mV	max	A
Average Offset Voltage Drift		—		±20	±20	µV/°C	max	B
Input Bias Current	V_{CM} = 2.0V	5.5	+**10**	+12	+13	µA	max	A
Input Bias Current Drift				±12	±12	nA/°C	max	B
Input Offset Current	V_{CM} = 2.0V	±0.1	±**1.5**	±2	±2.5	µA	max	A
Input Offset Current Drift		—		±10	±10	nA/°C	max	B
INPUT								
Least Positive Input Voltage		−0.5	−0.2	0	+0.1	V	max	B
Most Positive Input Voltage		3.3	3.2	3.1	3.0	V	min	B
Input Impedance								
Differential-Mode		10 || 2.1				kΩ ||pF	typ	C
Common-Mode		400 || 1.2				kΩ ||pF	typ	C
OUTPUT								
Least Positive Output Voltage	R_L = 1kΩ to 2.0V	0.03	**0.16**	0.18	0.20	V	max	A
	R_L = 150Ω to 2.0V	0.18	**0.3**	0.35	0.40	V	max	A
Most Positive Output Voltage	R_L = 1kΩ to 2.0V	4.94	**4.8**	4.6	4.4	V	min	A
	R_L = 150Ω to 2.0V	4.86	**4.6**	4.5	4.4	V	min	A
Current Output, Sourcing		80	**60**	55	52	mA	min	A
Current Output, Sinking		80	**60**	55	52	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	100				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.2				Ω	typ	C
POWER SUPPLY								
Minimum Operating Voltage		+2.8				V	typ	C
Maximum Operating Voltage		—	+**11**	+11	+11	V	max	A
Maximum Quiescent Current	V_S = +5V	3.9	**4.1**	4.8	5.5	mA	max	A
Minimum Quiescent Current	V_S = +5V	3.9	**3.7**	3.5	3.2	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IDBV		−40 to +85				°C	typ	C
Thermal Resistance								
D SO-8		125				°C/W	typ	C
DBV SOT23-5		150				°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +3.3V

Boldface limits are tested at **+25°C.**

At T_A = 25°C, G = +2, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted (see Figure 2).

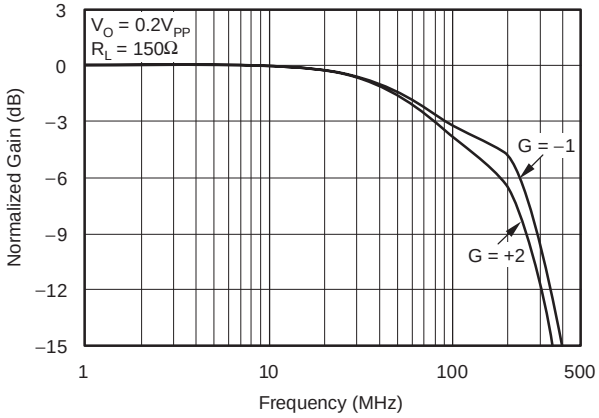
PARAMETER	CONDITIONS	OPA832ID, IDBV			UNITS	MIN/ MAX	TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE				
		+25°C	+25°C(1)	0°C to 70°C(2)			
AC PERFORMANCE (see Figure 2)							
Small-Signal Bandwidth	G = +2, $V_O \le 0.5V_{PP}$	95	59	57	MHz	min	B
	G = −1, $V_O \le 0.5V_{PP}$	103	63	61	MHz	min	B
Peaking at a Gain of +1	$V_O \le 0.5V_{PP}$	4.2			dB	typ	C
Slew Rate	1V Step	170	115	115	V/µs	min	B
Rise Time	0.5V Step	4			ns	max	B
Fall Time	0.5V Step	4.2			ns	max	B
Settling Time to 0.1%	1V Step	48			ns	max	B
Harmonic Distortion	5MHz						
2nd-Harmonic	R_L = 150Ω	−71	−64	−62	dBc	max	B
	R_L = 500Ω	−74	−70	−66	dBc	max	B
3rd-Harmonic	R_L = 150Ω	−66	−60	−55	dBc	max	B
	R_L = 500Ω	−69	−66	−62	dBc	max	B
Input Voltage Noise	f > 1MHz	9.4			nV/√Hz	max	B
Input Current Noise	f > 1MHz	2.4			pA/√Hz	max	B
DC PERFORMANCE(4)							
Gain Error	G = +2	±0.3	**±1.5**	±1.6	%	min	A
	G = −1	±0.2	±1.5	±1.6	%	max	B
Internal R_F and R_G							
Maximum		400	**455**	460	Ω	max	A
Minimum		400	**345**	340	Ω	max	A
Average Drift				0.1	%/°C	max	B
Input Offset Voltage		±1	**±7**	±8	mV	max	A
Average Offset Voltage Drift		—		±20	µV/°C	max	B
Input Bias Current	V_{CM} = 0.75V	5.5	**+10**	+12	µA	max	A
Input Bias Current Drift				±12	nA/°C	max	B
Input Offset Current	V_{CM} = 0.75V	±0.1	**±1.5**	±2	µA	max	A
Input Offset Current Drift		—		±10	nA/°C	max	B
INPUT							
Least Positive Input Voltage		−0.5	−0.3	−0.2	V	max	B
Most Positive Input Voltage		1.5	1.4	1.3	V	min	B
Input Impedance, Differential-Mode		10 ‖2.1			kΩ ‖pF	typ	C
Common-Mode		400 ‖1.2			kΩ ‖pF	typ	C
OUTPUT							
Least Positive Output Voltage	R_L = 1kΩ to 0.75V	0.03	0.16	0.18	V	max	B
	R_L = 150Ω to 0.75V	0.1	0.3	0.35	V	max	B
Most Positive Output Voltage	R_L = 1kΩ to 0.75V	3	2.8	2.6	V	min	B
	R_L = 150Ω to 0.75V	3	2.8	2.6	V	min	B
Current Output, Sourcing		35	**25**	20	mA	min	A
Current Output, Sinking		35	**25**	20	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	80			mA	typ	C
Closed-Loop Output Impedance	See Figure 2, f < 100kHz	0.2			Ω	typ	C
POWER SUPPLY							
Minimum Operating Voltage		+2.8			V	typ	C
Maximum Operating Voltage		—	**+11**	+11	V	max	A
Maximum Quiescent Current	V_S = +3.3V	3.8	**4.0**	4.7	mA	max	A
Minimum Quiescent Current	V_S = +3.3V	3.8	**3.4**	3.2	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	60			dB	typ	C
THERMAL CHARACTERISTICS							
Specification: ID, IDBV		−40 to +85			°C	typ	C
Thermal Resistance							
D SO-8		125			°C/W	typ	C
DBV SOT23-5		150			°C/W	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

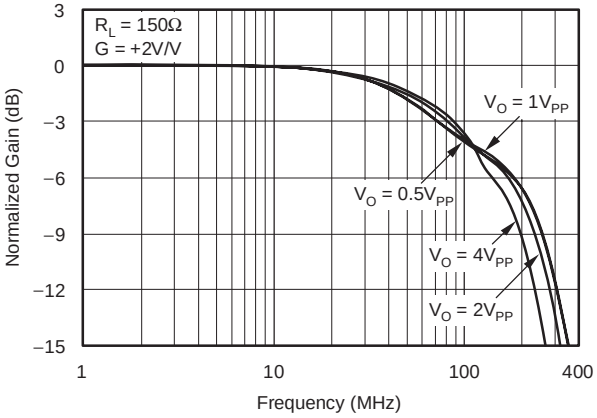
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

At T_A = 25°C, G = +2, and R_L = 150Ω to GND, unless otherwise noted (see Figure 3).

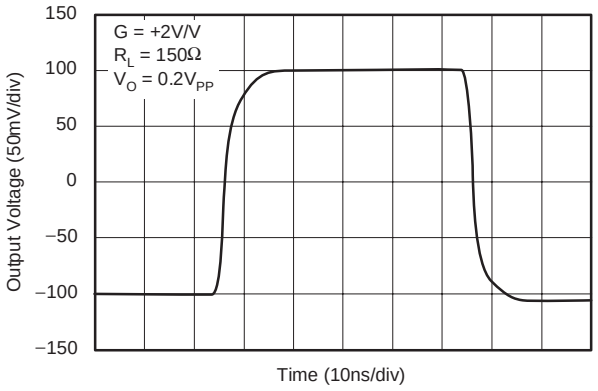
SMALL−SIGNAL FREQUENCY RESPONSE



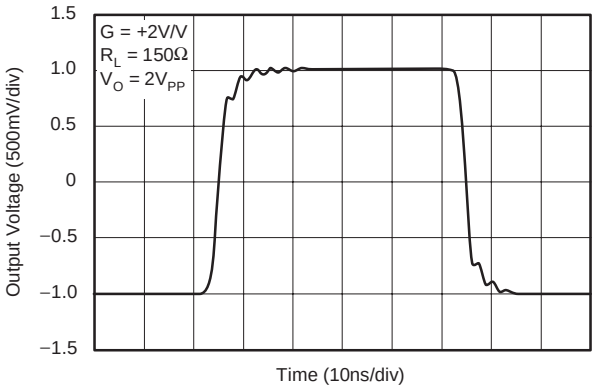
LARGE−SIGNAL FREQUENCY RESPONSE



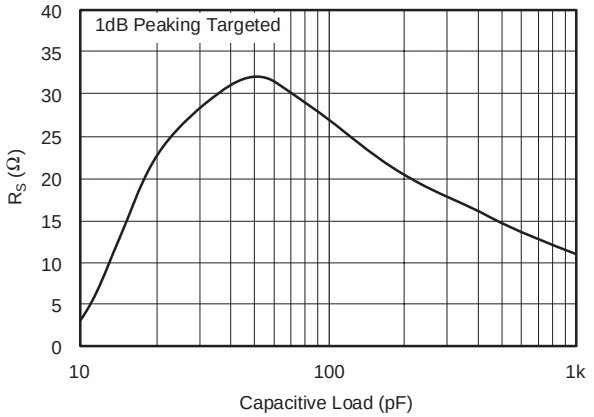
SMALL−SIGNAL PULSE RESPONSE



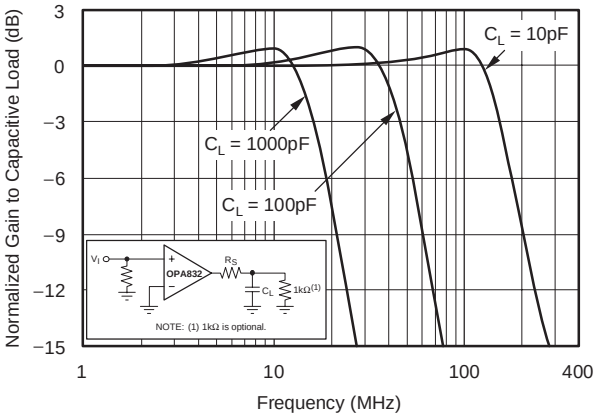
LARGE−SIGNAL PULSE RESPONSE



REQUIRED R_S vs CAPACITIVE LOAD



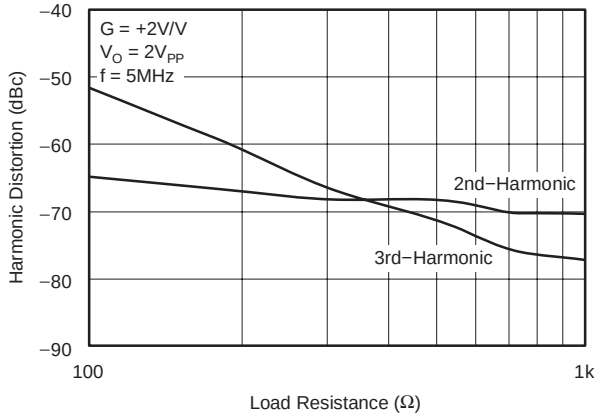
FREQUENCY RESPONSE vs CAPACITIVE LOAD



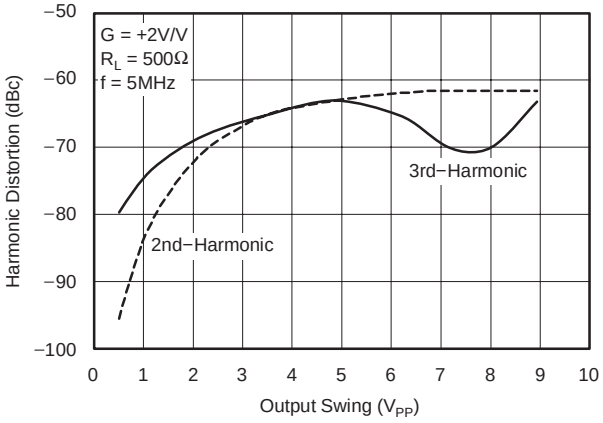
TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = 25°C, G = +2, and R_L = 150Ω to GND, unless otherwise noted (see Figure 3).

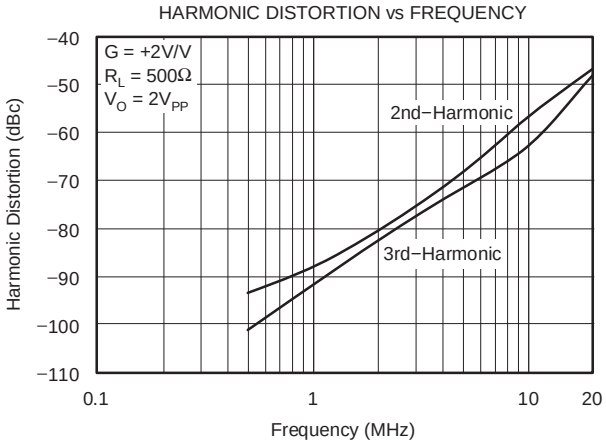
HARMONIC DISTORTION vs LOAD RESISTANCE



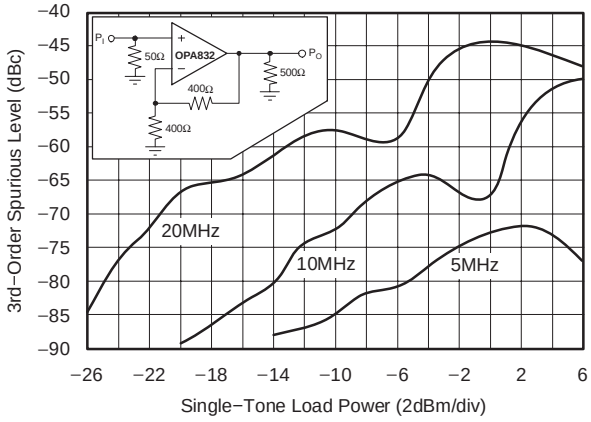
HARMONIC DISTORTION vs OUTPUT VOLTAGE



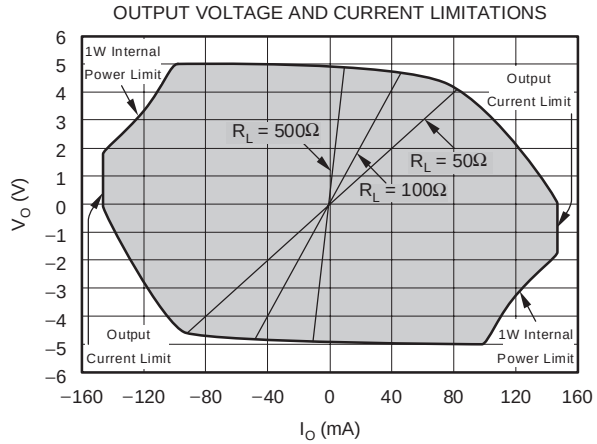
HARMONIC DISTORTION vs FREQUENCY



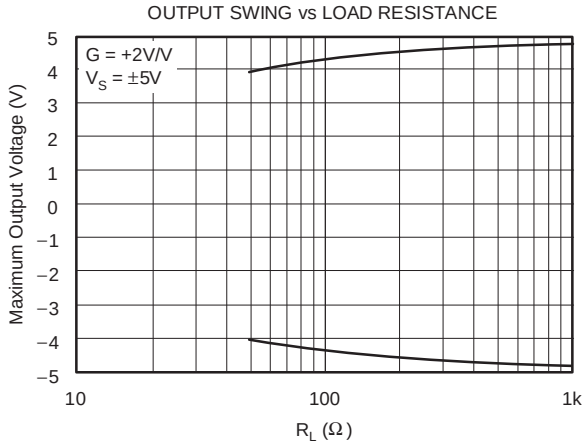
TWO−TONE, 3RD−ORDER
INTERMODULATION SPURIOUS



OUTPUT VOLTAGE AND CURRENT LIMITATIONS



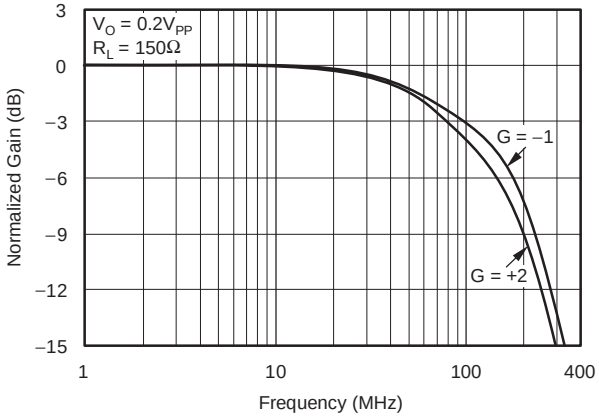
OUTPUT SWING vs LOAD RESISTANCE



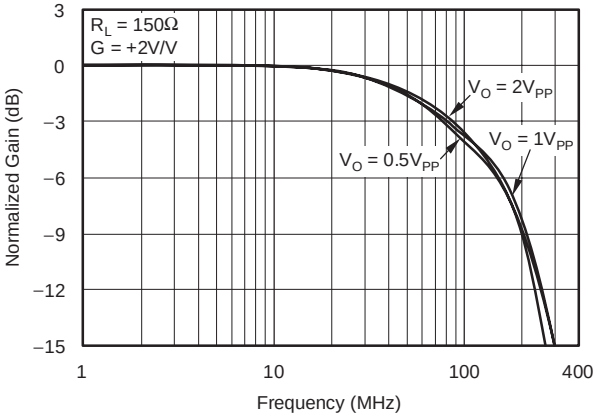
TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = 25°C, G = +2, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 1).

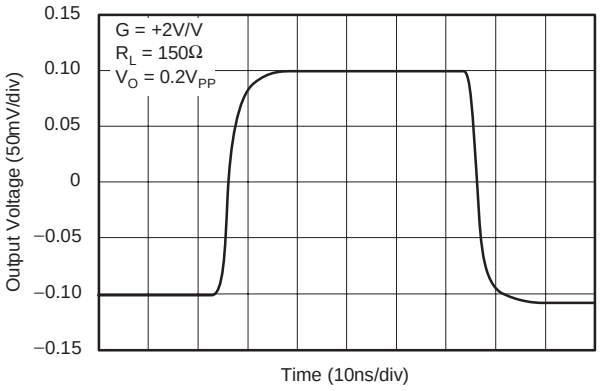
SMALL−SIGNAL FREQUENCY RESPONSE



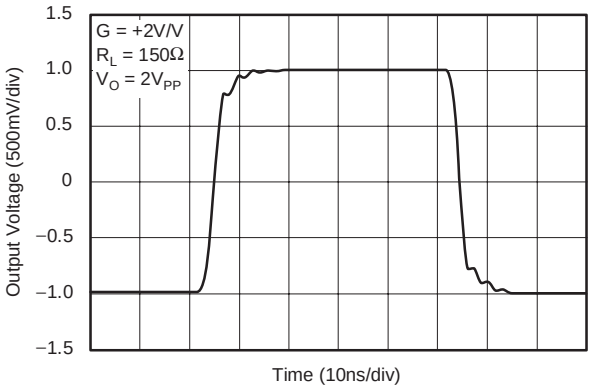
LARGE−SIGNAL FREQUENCY RESPONSE



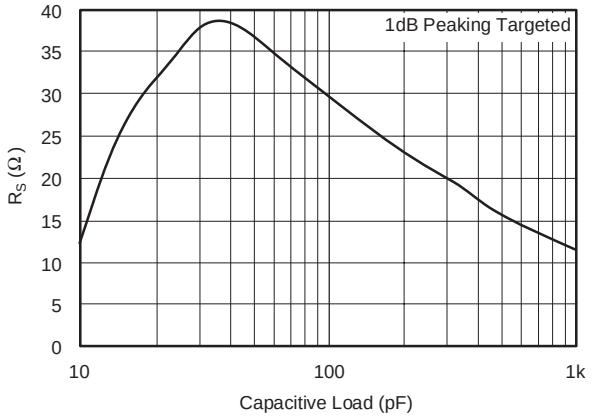
SMALL−SIGNAL PULSE RESPONSE



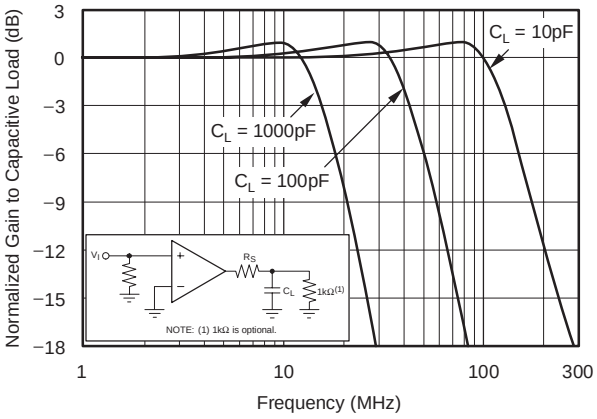
LARGE−SIGNAL PULSE RESPONSE



REQUIRED R_S vs CAPACITIVE LOAD



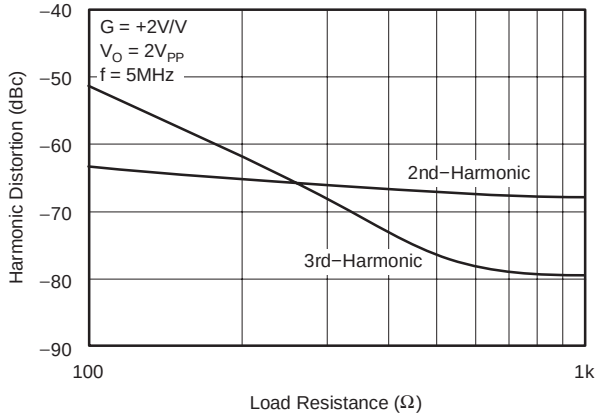
FREQUENCY RESPONSE vs CAPACITIVE LOAD



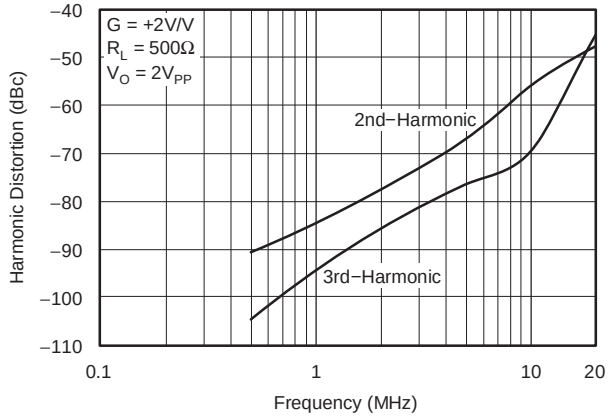
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = 25°C, G = +2, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 1).

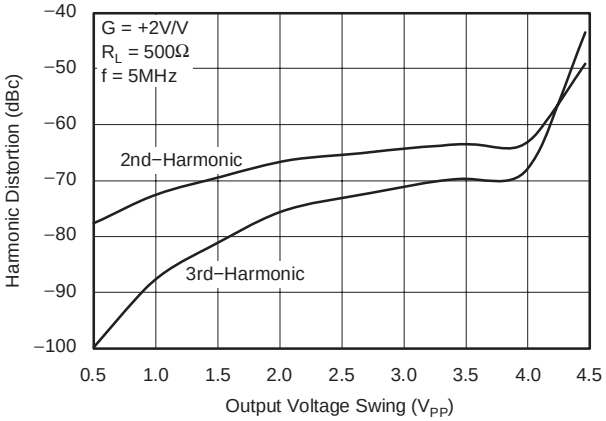
HARMONIC DISTORTION vs LOAD RESISTANCE



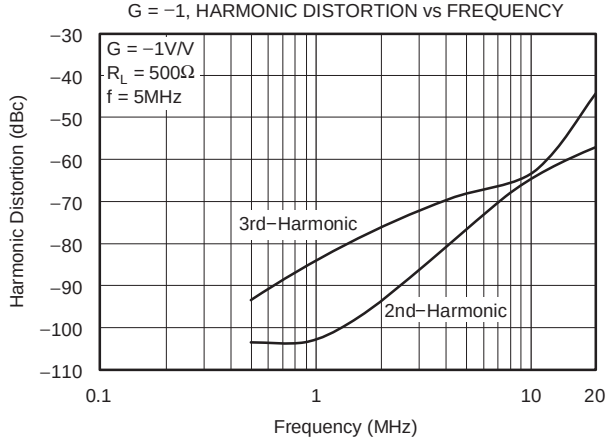
G = +2, HARMONIC DISTORTION vs FREQUENCY



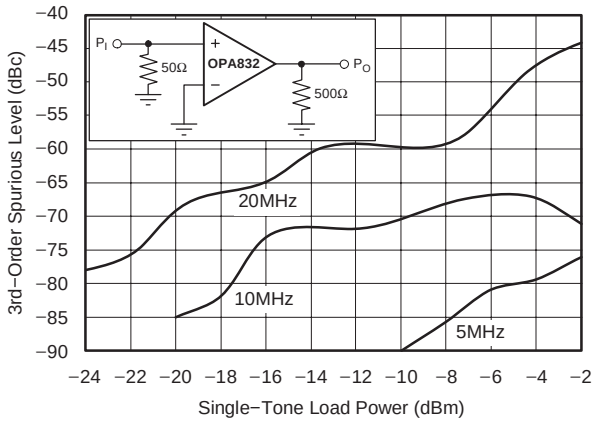
HARMONIC DISTORTION vs OUTPUT VOLTAGE



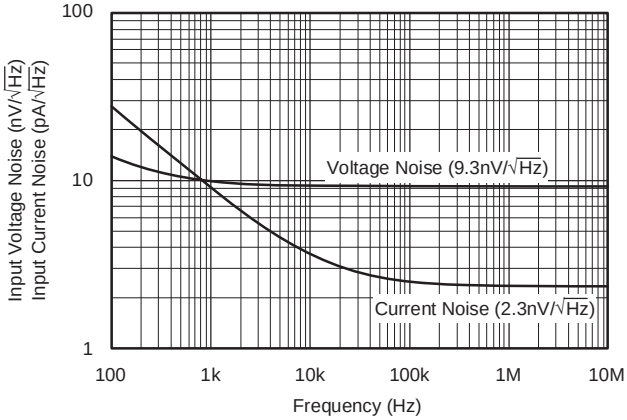
G = −1, HARMONIC DISTORTION vs FREQUENCY



TWO−TONE, 3RD−ORDER
INTERMODULATION SPURIOUS



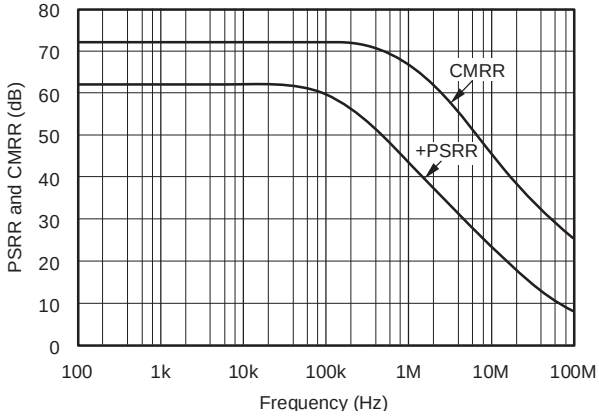
INPUT VOLTAGE AND CURRENT NOISE



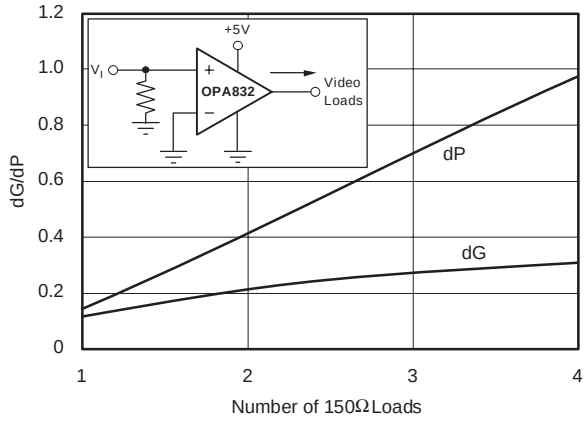
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = 25°C, G = +2, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 1).

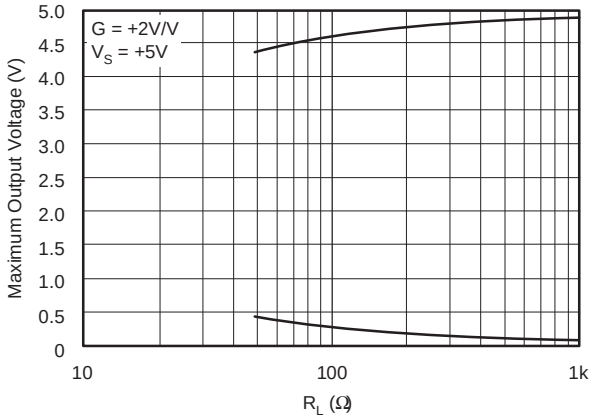
COMMON−MODE REJECTION RATIO AND
POWER−SUPPLY REJECTION RATIO vs FREQUENCY



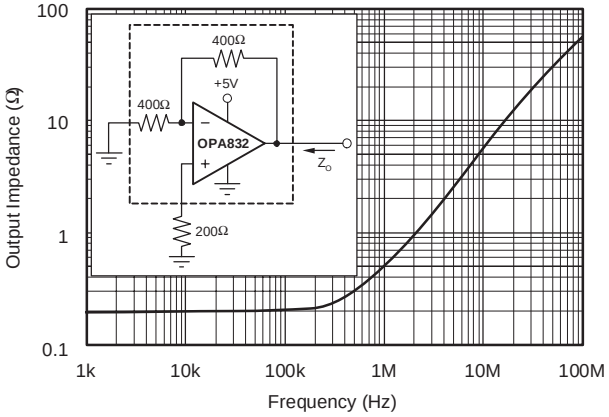
COMPOSITE VIDEO dG/dP



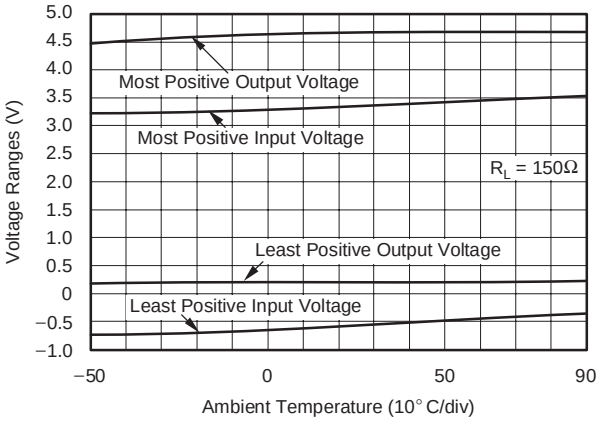
OUTPUT SWING vs LOAD RESISTANCE



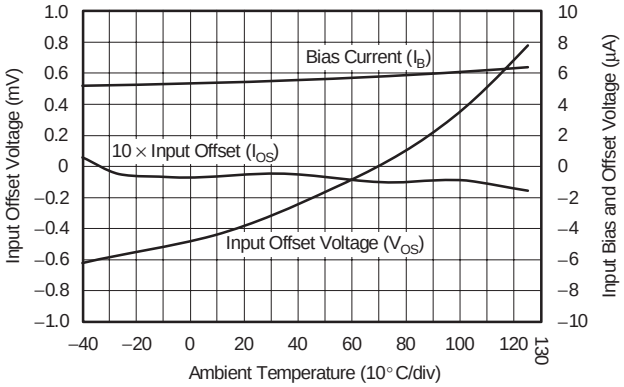
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



VOLTAGE RANGES vs TEMPERATURE

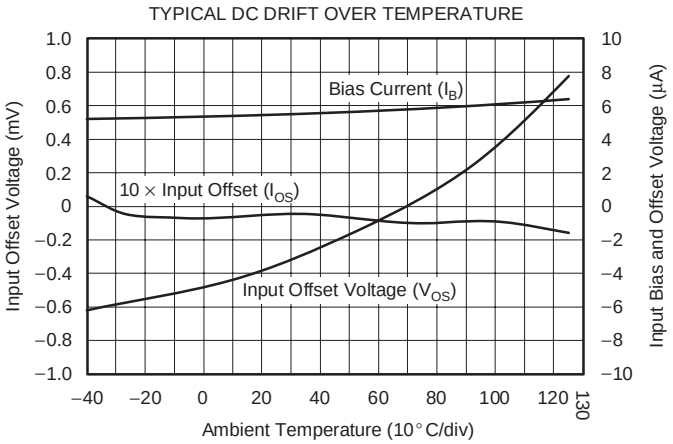


TYPICAL DC DRIFT OVER TEMPERATURE



TYPICAL CHARACTERISTICS: V_S = +5V (continued)

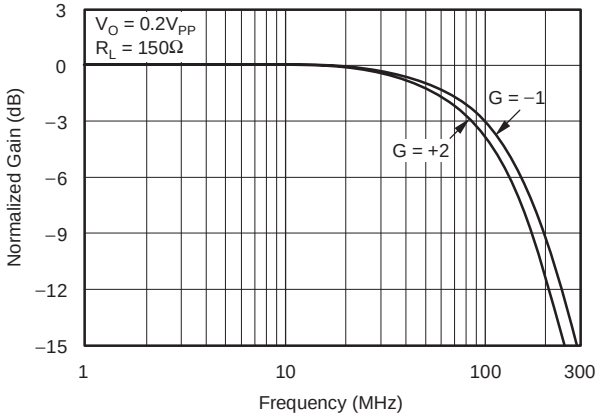
At T_A = 25°C, G = +2, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted (see Figure 1).



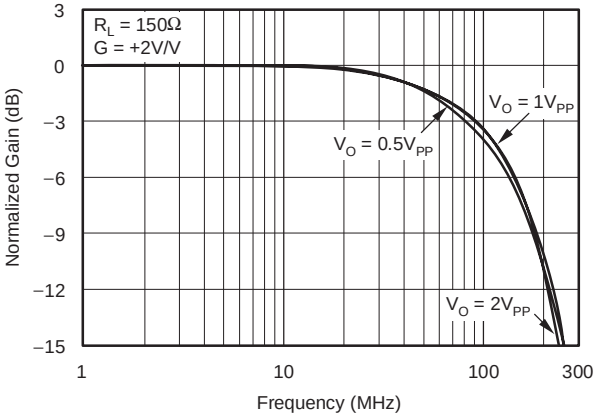
TYPICAL CHARACTERISTICS: V_S = +3.3V

At T_A = 25°C, G = +2, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted (see Figure 2).

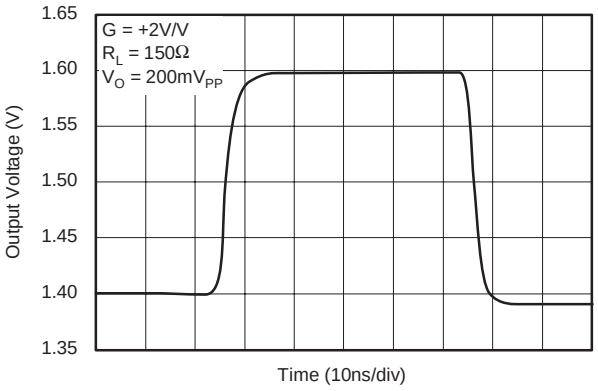
SMALL−SIGNAL FREQUENCY RESPONSE



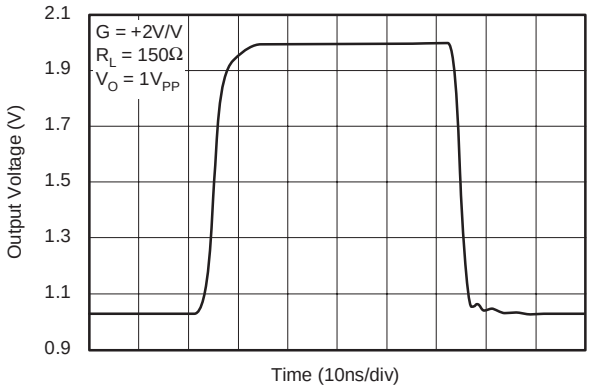
LARGE−SIGNAL FREQUENCY RESPONSE



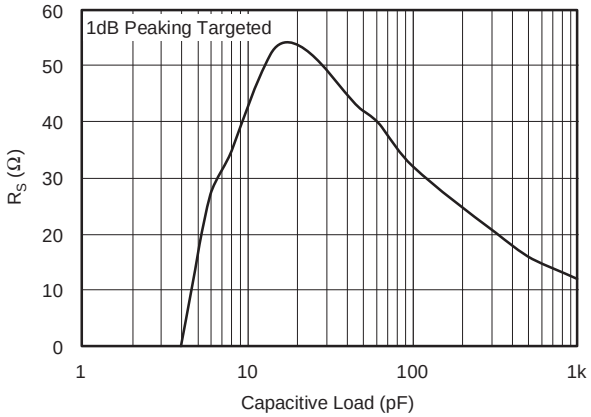
SMALL−SIGNAL PULSE RESPONSE



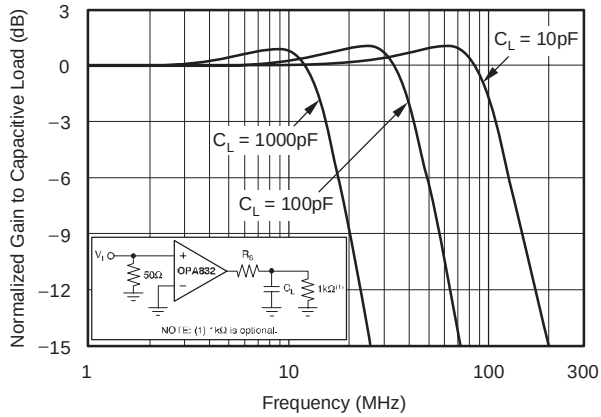
LARGE−SIGNAL PULSE RESPONSE



REQUIRED R_S vs CAPACITIVE LOAD



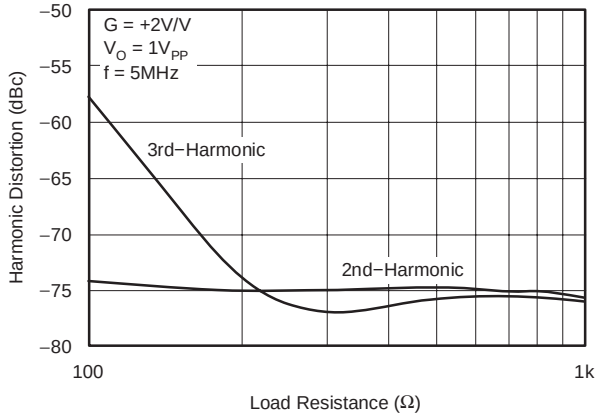
FREQUENCY RESPONSE vs CAPACITIVE LOAD



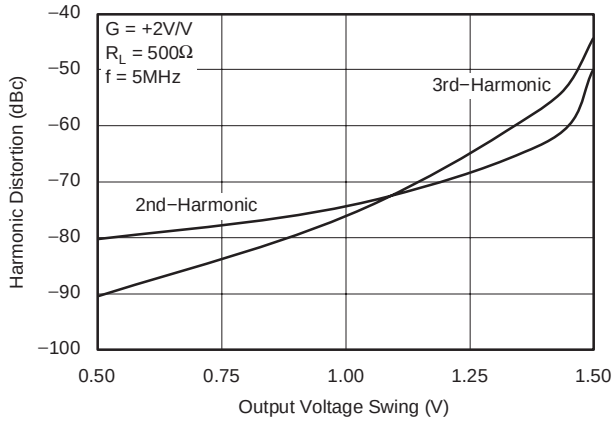
TYPICAL CHARACTERISTICS: V_S = +3.3V (continued)

At T_A = 25°C, G = +2, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted (see Figure 2).

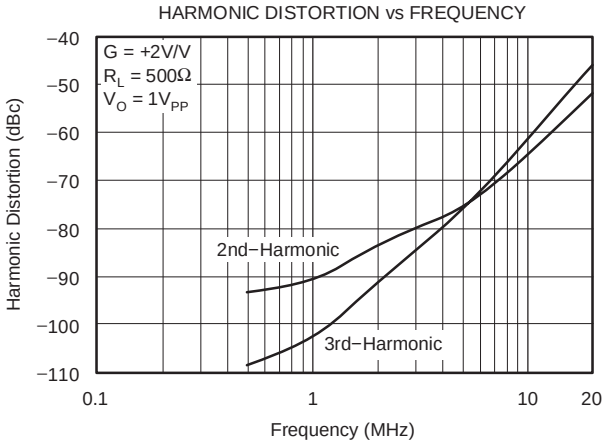
HARMONIC DISTORTION vs LOAD RESISTANCE



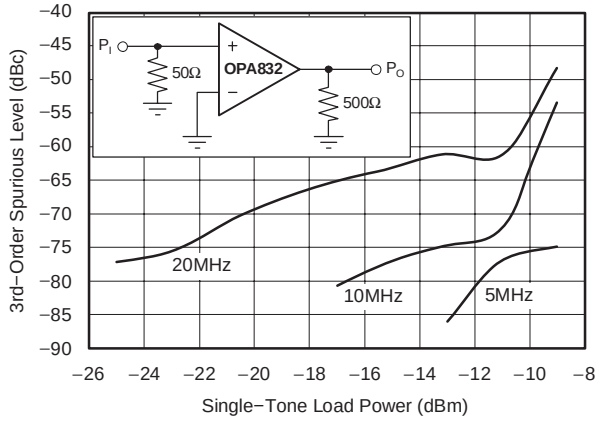
HARMONIC DISTORTION vs OUTPUT VOLTAGE



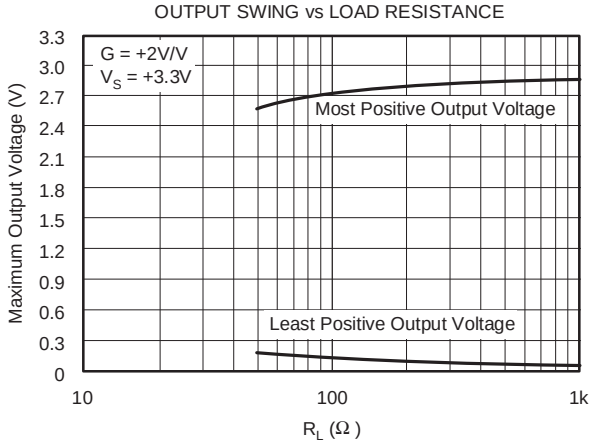
HARMONIC DISTORTION vs FREQUENCY



TWO−TONE, 3RD−ORDER
INTERMODULATION SPURIOUS



OUTPUT SWING vs LOAD RESISTANCE



APPLICATIONS INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA832 is a fixed-gain, high-speed, voltage-feedback op amp designed for single-supply operation (+3V to +10V). It features internal R_F and R_G resistors which make it easy to select a gain of +2, +1, and −1 without external resistors.The input stage supports input voltages below ground and to within 1.7V of the positive supply. The complementary common-emitter output stage provides an output swing to within 25mV of either supply pin. The OPA832 is compensated to provide stable operation with a wide range of resistive loads.

Figure 1 shows the AC-coupled, gain of +2 configuration used for the +5V Specifications and Typical Characteristic Curves. The input impedance matching resistor (66.5Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 1, the total effective load on the output at high frequencies is 150Ω || 800Ω. The 332Ω and 499Ω resistors at the noninverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input (R_F || R_G), reducing the DC output offset due to input bias current.

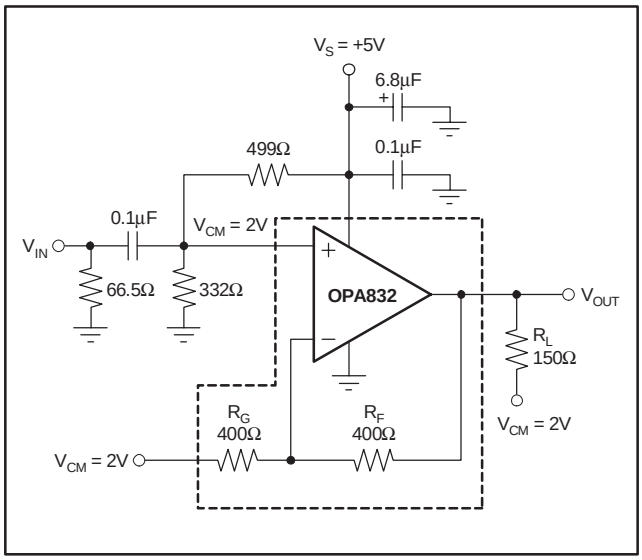


Figure 1. AC-Coupled, G = +2, +5V Single-Supply Specification and Test Circuit

Figure 2 shows the AC-coupled, gain of +2 configuration used for the +3.3V Specifications and Typical Characteristic Curves. The input impedance matching resistor (66.5Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 2, the total effective load on the output at high frequencies is 150Ω || 800Ω. The 887Ω and 258Ω resistors at the noninverting input provide the common-mode bias voltage. Their parallel combination equals the DC resistance at the inverting input (R_F || R_G), reducing the DC output offset due to input bias current.

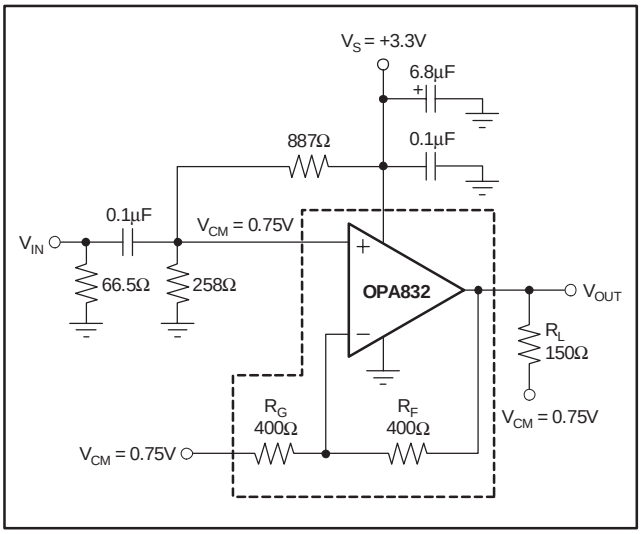


Figure 2. AC-Coupled, G = +2, +3.3V Single-Supply Specification and Test Circuit

Figure 3 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 150Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 3, the total effective load will be 150Ω || 800Ω. Two optional components are included in Figure 3. An additional resistor (175Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 200Ω source resistance seen at the inverting input (see the DC Accuracy and Offset Control section). In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical PC board layouts, this optional capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

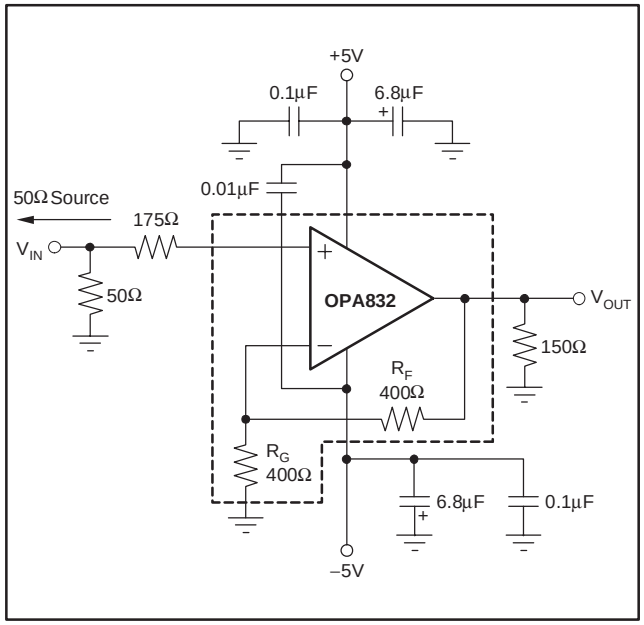


Figure 3. DC-Coupled, G = +2, Bipolar Supply Specification and Test Circuit

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA832 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA832ID	SO-8	DEM-OPA-SO-1A	SBOU009
OPA832IDBV	SOT23-5	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA832 product folder.

MACROMODEL AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA832 and its circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA832 is available through the TI web page (www.ti.com). The applications group is also available for design assistance. These models predict typical small signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

GAIN OF +2V/V VIDEO LINE DRIVER

One of the most suitable applications for the OPA832 is a simple gain of +2 video line driver. Figure 4 shows how simple this circuit is to implement, shown as a ±5V implementation. Single +5V operation is similar with blocking caps and DC common-mode biasing provided.

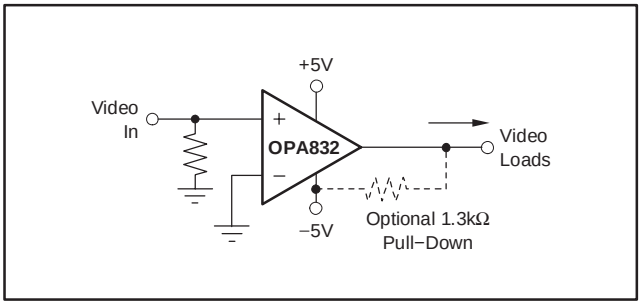


Figure 4. Gain of +2V/V Video Line Driver

One optional element is shown in Figure 4. A 1.3kΩ pull-down to the negative supply will improve the differential phase significantly and the differential gain slightly. Figure 5 shows measured dG/dP with and without that pull-down resistor from 1 to 4 video loads.

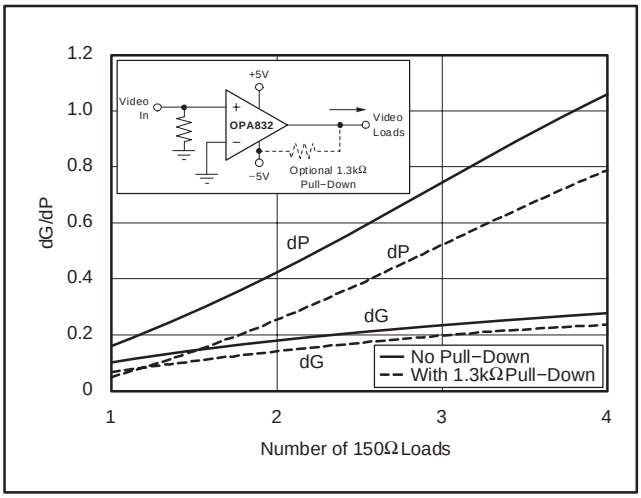


Figure 5. dG/dP vs Video Loads

SINGLE-SUPPLY ADC INTERFACE

The circuit shown in Figure 6 uses the OPA832 as a differential driver followed by an RC filter. In this circuit, the single-ended to differential conversion is realized by a 1:1 transformer driving the noninverting inputs of the two OPA832s. The common-mode level (CML) of the ADS5203 is reduced to the appropriate input level of 0.885V by the network divider composed of R_1 and the CML output impedance, and connected to the transformer center tap, biasing the OPA832s. This input bias voltage is then amplified to provide the correct common-mode voltage to the input of the ADC. Using only 25.1mW power (3.8mA × 2 amplifiers × 3.3V), this configuration (amplifier + ADC) provides greater than 59dB SNR and 70dB SFDR to 2MHz, with all the components running on a low +3.3V supply.

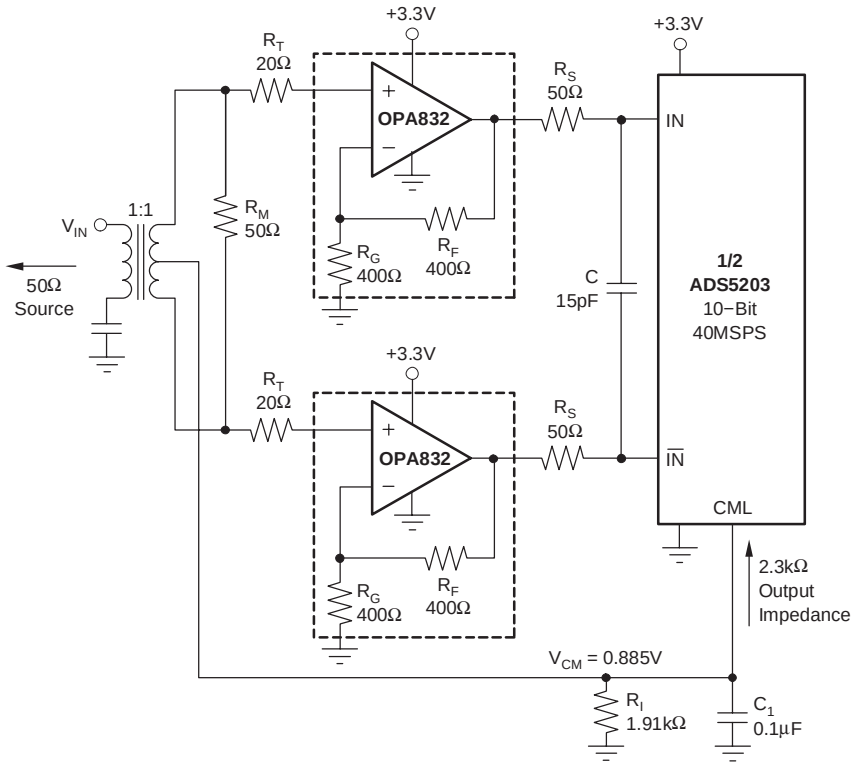


Figure 6. Low-Power, Single-Supply ADC Driver

This circuit removes the peaking by bootstrapping out any parasitic effects on R_G. The input impedance is still set by R_M as the apparent impedance looking into R_G is very high. R_M may be increased to show a higher input impedance, but larger values will start to impact DC output offset voltage. This circuit creates an additional input offset voltage as the difference in the two input bias current times the impedance to ground at V_{IN}. Figure 8 shows a comparison of small-signal frequency response for the unity-gain buffer of Figure 2 (with V_{CM} removed from R_G) compared to the improved approach shown in Figure 7.

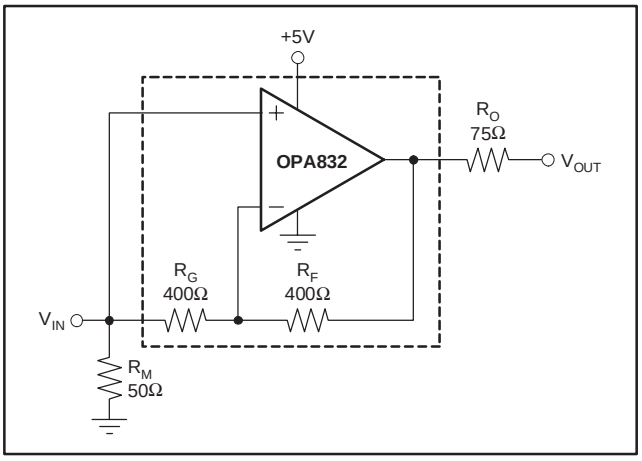


Figure 7. Improved Unity-Gain Buffer

UNITY-GAIN BUFFER

This buffer can simply be realized by not connecting R_G to ground. This type of realization shows a peaking in the frequency response. A similar circuit that holds a flat frequency response giving improved pulse fidelity is shown in Figure 7.

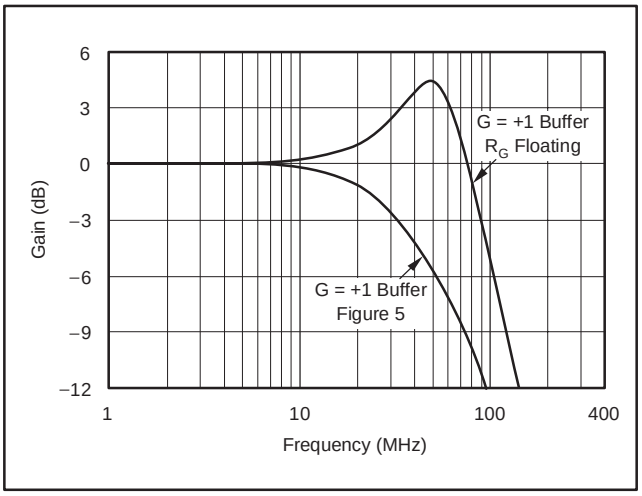


Figure 8. Buffer Frequency Response Comparison

OPERATING SUGGESTIONS

GAIN SETTING

Setting the gain for the OPA832 is very easy. For a gain of +2, ground the −IN pin and drive the +IN pin with the signal. For a gain of +1, either leave the −IN pin open and drive the +IN pin or drive both the +IN and −IN pins as shown in Figure 7. For a gain of −1, ground the +IN pin and drive the −IN pin with the input signal. An external resistor may be used in series with the −IN pin to reduce the gain. However, since the internal resistors (R_F and R_G) have a tolerance and temperature drift different than the external resistor, the absolute gain accuracy and gain drift over temperature will be relatively poor compared to the previously described standard gain connections using no external resistor.

OUTPUT CURRENT AND VOLTAGES

The OPA832 provides outstanding output voltage capability. For the +5V supply, under no-load conditions at +25°C, the output voltage typically swings closer than 60mV to either supply rail.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the min/max tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem, since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin packages) will possibly destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. This will reduce the available output voltage swing under heavy output loads.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high

open-loop gain amplifier like the OPA832 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Characteristic curves show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA832. Long PC board traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see the Board Layout Guidelines section).

The criterion for setting this R_S resistor is a 1dB peaked frequency response at the load. Increasing the noise gain will also reduce the peaking (see Figure 7).

DISTORTION PERFORMANCE

The OPA832 provides good distortion performance into a 150Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +3.3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 3) this is sum of R_F + R_G, while in the inverting configuration, only R_F needs to be included in parallel with the actual load.

Figure 9 shows the 2nd- and 3rd-harmonic distortion versus supply voltage. In order to maintain the input signal within acceptable operating range, the input common-mode voltage is adjusted for each supply voltage. For example, the common-mode voltage is +2V for a single +5V supply, and the distortion is −66.5dBc for the 2nd-harmonic and −74.6dBc for the 3rd-harmonic.

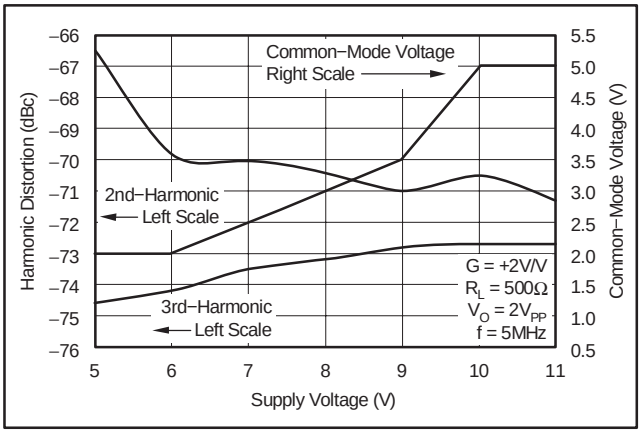


Figure 9. 5MHz Harmonic Distortion vs Supply Voltage

NOISE PERFORMANCE

Unity-gain stable, rail-to-rail (RR) output, voltage-feedback op amps usually show a higher input noise voltage. The 9.2nV/√Hz input voltage noise for the OPA832 however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms (2.8pA/√Hz) combine to give low output noise under a wide variety of operating conditions. Figure 10 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

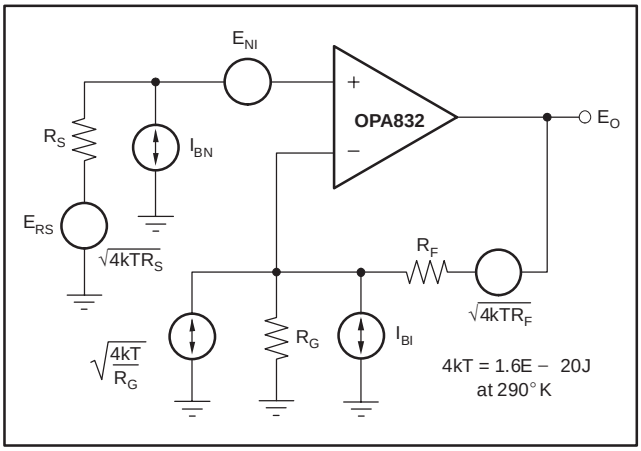


Figure 10. Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 10:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (1)$$

Dividing this expression by the noise gain ($NG = (1 + R_F/R_G)$) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 2:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

Evaluating these two equations for the circuit and component values shown in Figure 1 will give a total output spot noise voltage of 19.3nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 9.65nV/$\sqrt{Hz}$. This is including the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 9.2nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output DC accuracy in a wide variety of applications. The power-supply current trim for the OPA832 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 5μA out of each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. This is done by matching the DC source resistances appearing at the two inputs. Evaluating the configuration of Figure 3 (which has matched DC input resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

(NG = noninverting signal gain at DC)

$\pm(NG \times V_{OS(MAX)}) \pm (R_F \times I_{OS(MAX)})$

$= \pm(2 \times 10mV) \pm (400\Omega \times 1.5\mu A)$

$= \pm 10.6mV$

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques are based on adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source.

If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. Bring the DC offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain and hence the frequency response.

THERMAL ANALYSIS

Maximum desired junction temperature will set the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load; though, for resistive loads connected to mid-supply ($V_S/2$), P_{DL} is at a maximum when the output is fixed at a voltage equal to $V_S/4$ or $3V_S/4$. Under this condition, $P_{DL} = V_S^2/(16 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage, and not into the load, that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA832 (SOT23-5 package) in the circuit of Figure 3 operating at the maximum specified ambient temperature of +85°C and driving a 150Ω load at mid-supply.

$P_D = 10V \times 3.9mA + 5^2/(16 \times (150\Omega \parallel 400\Omega)) = 53.3mW$

Maximum $T_J = +85°C + (0.053W \times 150°C/W) = 93°C$.

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower ensured junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output at high output voltages or sourced from the output at low output voltages. This puts a high current through a large internal voltage drop in the output transistors.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA832 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25”) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout

should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Each power-supply connection should always be decoupled with one of these capacitors. An optional supply decoupling capacitor (0.1μF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the typical characteristic curve Recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA832 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA832 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the typical characteristic curve Recommended R_S vs Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA832 onto the board.

INPUT AND ESD PROTECTION

The OPA832 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 11.

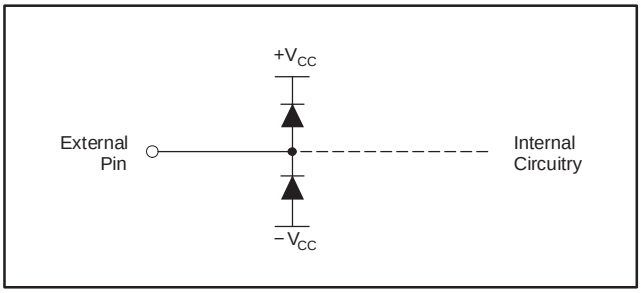


Figure 11. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (that is, in systems with ±15V supply parts driving into the OPA832), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/08	E	2	Absolute Maximum Ratings	Changed Storage Temperature minimum value from −40°C to −65°C.
3/06	D	15	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA832ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 832	Samples
OPA832IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A74	Samples
OPA832IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A74	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

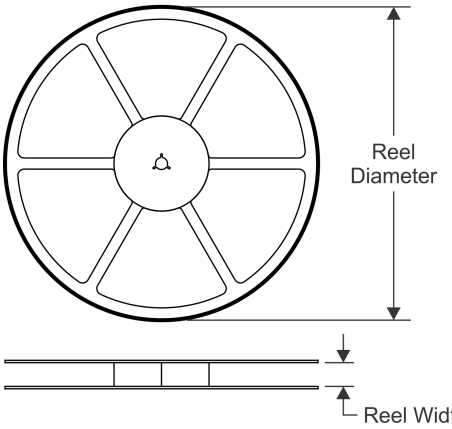
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

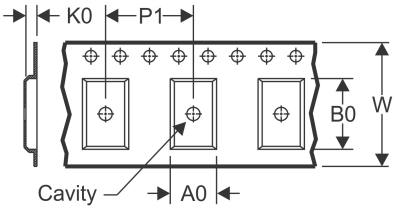
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

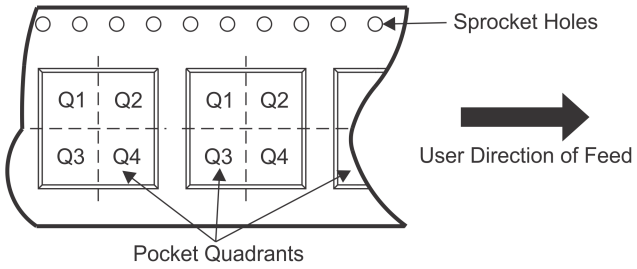


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

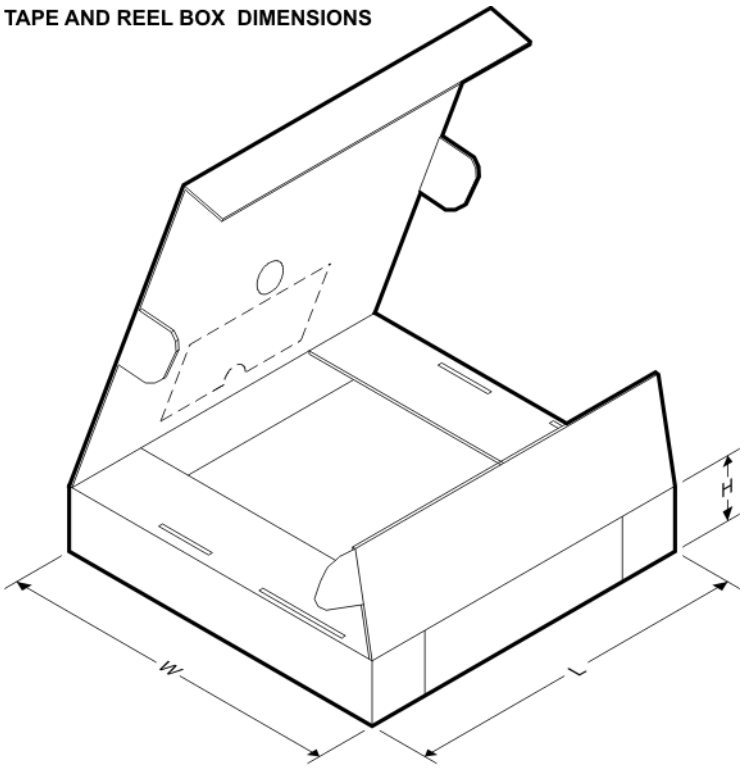
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA832IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA832IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3

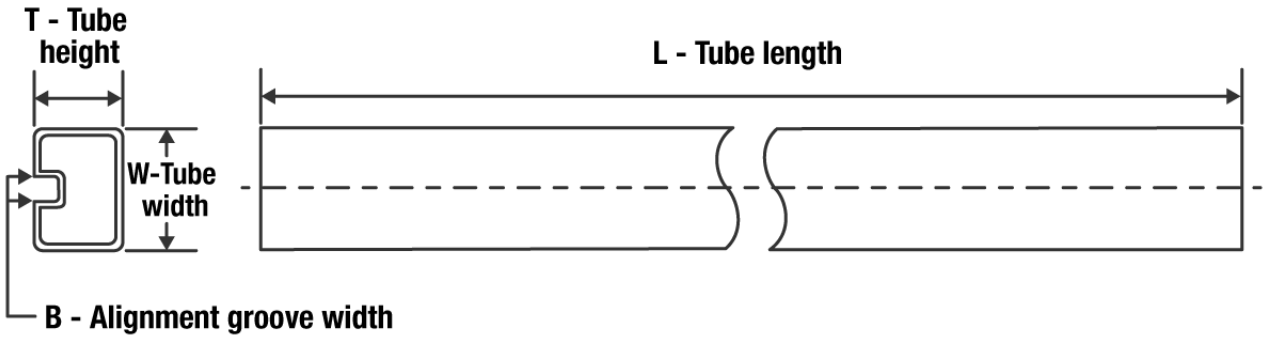
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA832IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA832IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

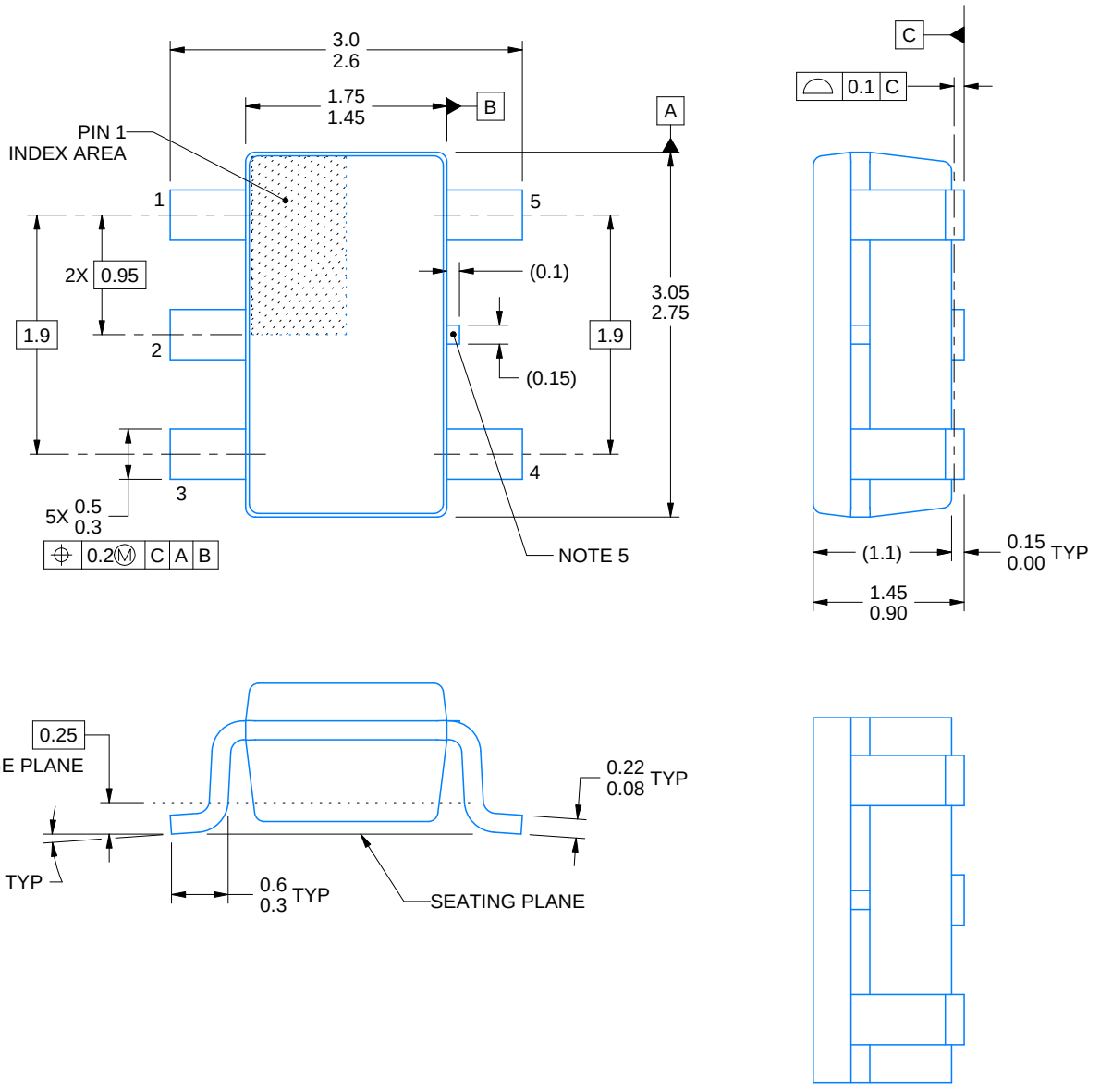
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA832ID	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

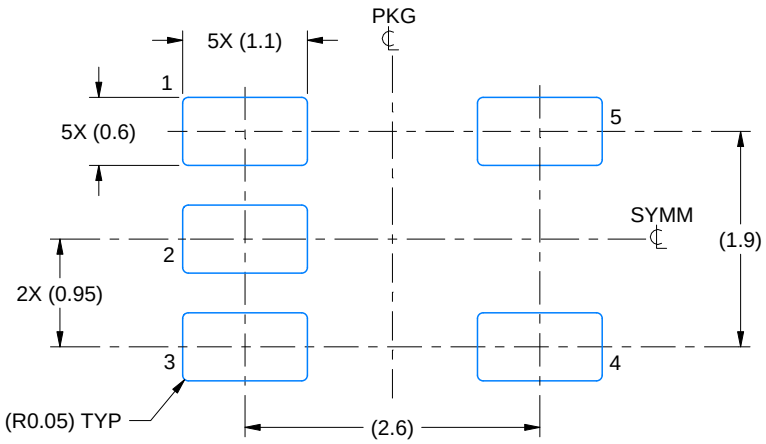


ALTERNATIVE PACKAGE SINGULATION VIEW

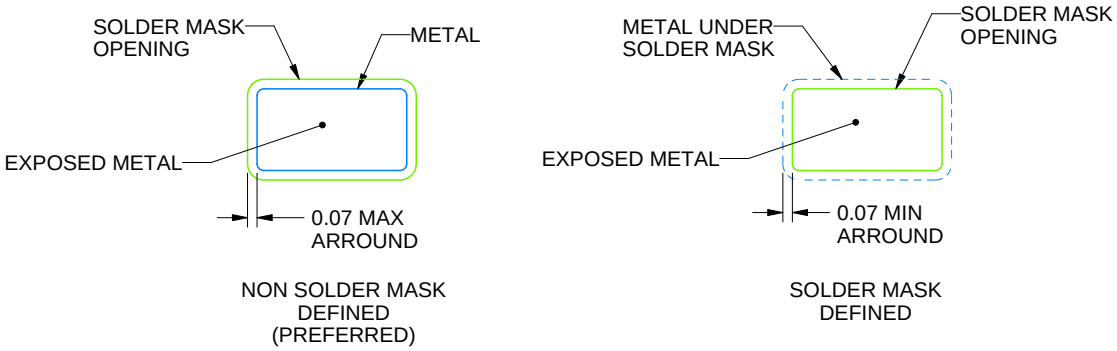
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

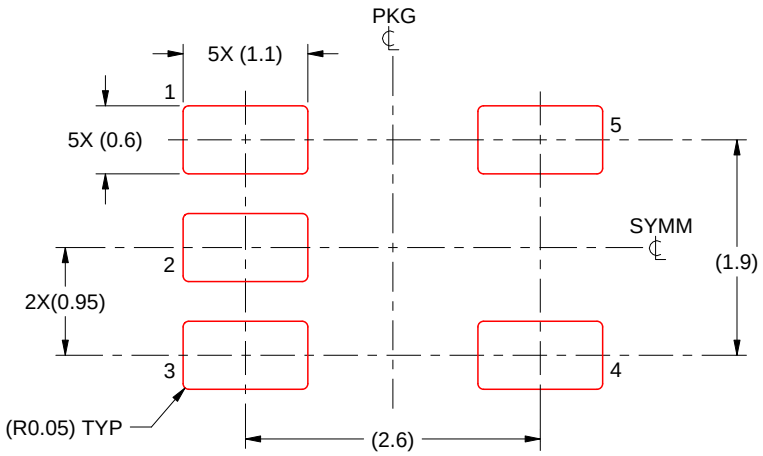


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

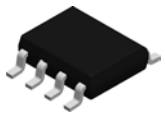


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

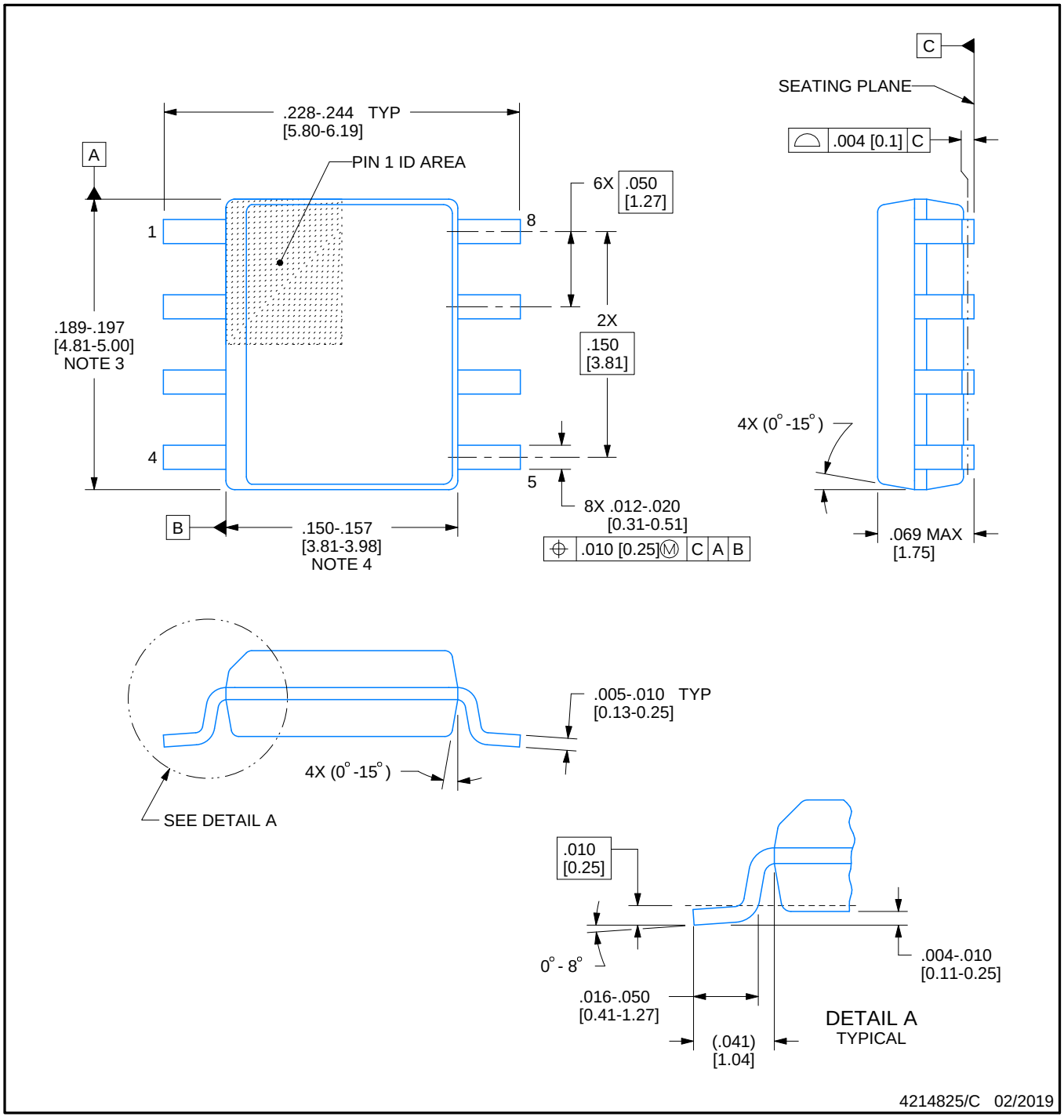


PACKAGE OUTLINE

D0008A

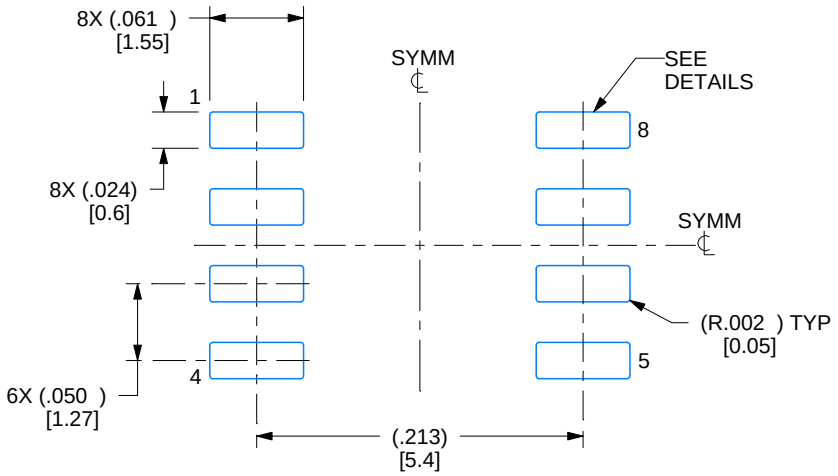
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

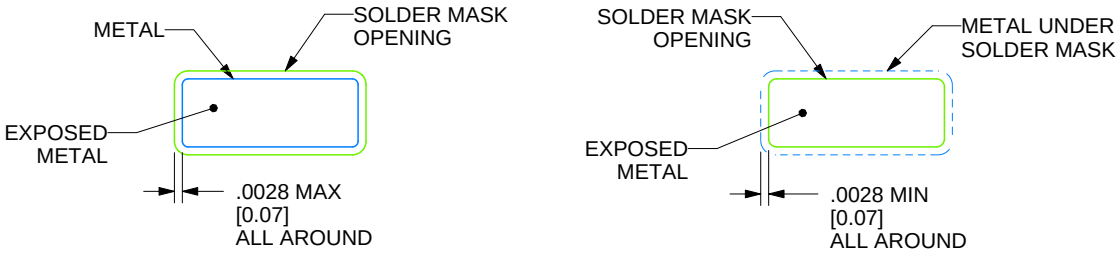


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

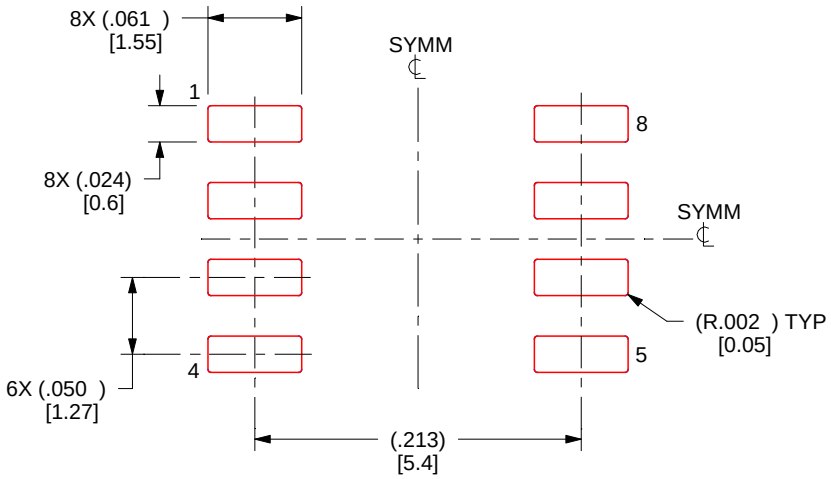
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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