DRV10970 三相无刷直流电机驱动器

1 特性

- 宽电源电压范围：5V 至 18V
- 集成场效应晶体管 (FET)：1A 均方根 (RMS)、1.5A 峰值输出相位/绕组电流
- 总驱动器 H + L R_{DSON}：400mΩ
- 内置 180° 正弦波形和梯形换向
- 休眠模式下的功耗超低 (35µA)
- 自适应驱动角度调整
- 三霍尔传感器或单霍尔传感器两个选项，最大程度地降低系统成本
- 电机旋转方向控制
- 可配置为以 30° 或 0° 放置霍尔传感器
- 可调节的重试时间（电机锁定后）
- 可通过编程设定的电流限制功能
- 转速计 – 在开漏 FG 引脚上提供电机转速信息
- 在开漏 RD 引脚上提供电机锁定报告
- 保护 特性
  - 电源 (VM) 欠压锁定
  - 逐周期电流限制
  - 过流保护 (OCP)
  - 热关断
  - 电机锁定检测和报告

2 应用

- 冷却风扇
- 小型家用电器
- 通用无刷直流 (BLDC) 电机驱动器

3 说明

DRV10970 是一款集成式三相 BLDC 电机驱动器，适用于家用电器、冷却风扇以及其他通用电机控制 应用。该器件内置智能特性，并且拥有小巧外形和简单的引脚分布结构，不仅降低了设计复杂度、节省了电路板空间，而且还降低了系统成本。集成的保护功能提高了系统的稳健性和可靠性。

DRV10970 的输出级包含三个 R_{DSON} 为 400 mΩ (H + L) 的半桥。每个半桥都能够驱动高达 1A RMS 和 1.5A 峰值的输出电流。当器件进入休眠模式时，电流消耗典型值为 35µA。

该器件内置有高级的 180° 正弦波形换向算法，可实现高效率、低转矩纹波和出色的声学性能。自适应驱动角度调整功能可确保器件在任何电机参数和负载条件下获得最优效率。

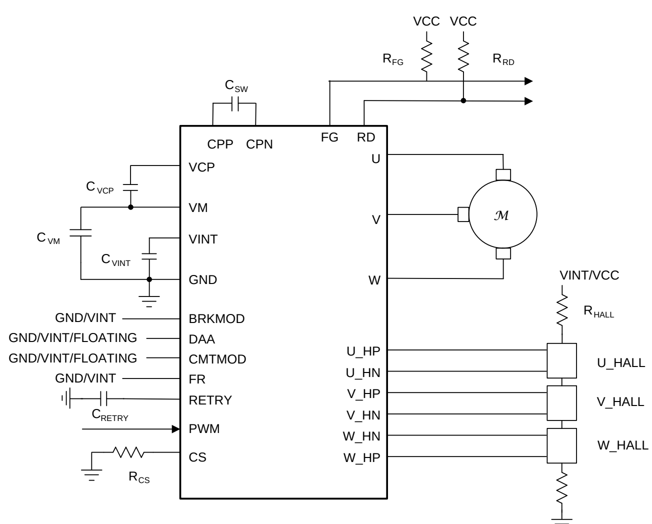
DRV10970 针对基于差分或单端霍尔传感器的应用而设计。差分霍尔信号输入由集成的比较器检测。该器件支持基于三个霍尔传感器和单个霍尔传感器的 应用；单霍尔传感器模式通过减少两个霍尔传感器来降低系统成本。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV10970	TSSOP (24)	7.80mm × 6.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

应用电路



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (February 2016) to Revision A **Page**

- 已更改 器件状态至“量产数据”且已发布完整数据表 ... 1

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5 说明 （续）

该器件实现了一个标准控制接口，其中包含脉宽调制 (PWM) 输入（速度命令）、FG 输出（速度反馈）、FR 输入（正向和反向控制）以及 RD 输出（电机锁定指示）。

DRV10970 器件支持以 30° 和 0° 放置霍尔传感器（相对于对应相的 BEMF）。该器件实现了梯形驱动模式来满足更高的功率需求。

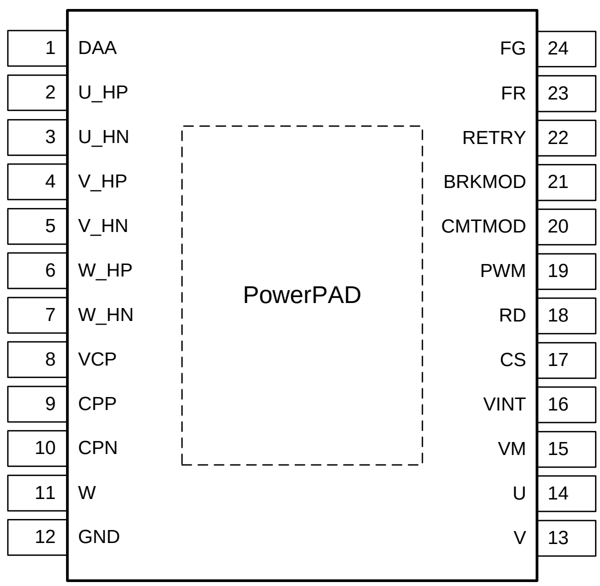
DRV10970 器件根据霍尔传感器输入是否切换开关状态来确定转子锁定情况。该器件会在经过一段可调节的自动重试时间（可通过连接至 RETRY 引脚的电容来配置）后重试旋转电机。

该器件包含多种保护 功能来提高系统稳健性：过流保护、欠压保护、过热保护以及转子锁定检测与报告。

DRV10970 采用耐热增强型 24 引脚薄型小外形尺寸 (TSSOP) 封装（环境友好型：符合 RoHS 标准并且无 Sb/Br）。

6 Pin Configuration and Functions

PWP Package
24-Pin TSSOP with PowerPAD™
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	NO.			
POWER AND GROUND				
CPN	10	—	Charge pump switching node	Connect a 0.1-µF X7R capacitor rated for VM between CPN and CPP
CPP	9	—		
GND	12	PWR	Device ground	Must be connected to board ground
VCP	8	—	Charge pump output	Connect a 16-V, 1-µF ceramic capacitor to VM
VINT	16	PWR	Integrated regulator output	Integrated regulator (typical voltage 5 V) mainly for internal circuits; Provide external power for less than 20 mA. Bypass to GND with a 10-V, 2.2-µF ceramic capacitor
VM	15	PWR	Power supply	Connect to motor supply voltage; bypass to GND with a 10-µF ceramic capacitor rated for VM

Pin Functions (continued)

PIN		TYPE	DESCRIPTION	
NAME	NO.			
CONTROL				
CS	17	—	Current limit setting pin	Connect a resistor to adjust the current limit.
DAA	1	I	Drive angle adjustment configuration pin	Low: 10° drive angle adjustment High: 5° drive angle adjustment Floating: adaptive drive angle adjustment
FG	24	O	Frequency indication pin	Open drain Electrical Frequency Output pin. One toggle per electrical cycle. Requires an external pull-up of 3.3-kΩ.
FR	23	I	Motor direction control	Direction Control Input. When low, phase driving sequence is U → V → W (U phase is leading V phase by 120°). When high, the phase driving sequence is U → W → V.
BRKMOD	21	I	Brake mode setting	Low: Coasting mode (phases are tri-stated) High: Brake mode (phases are driven low)
PWM	19	I	Variable duty cycle PWM input for speed control	Connect to PWM signal.
RD	18	O	Lock indication pin	Pulled logic low with lock condition; open-drain output requires an external pull-up of 3.3-kΩ
RETRY	22	I	Auto retry timing configure	Timing adjustable by capacitor
CMTMOD	20	I	Commutation mode setting	Low: Sinusoidal operation mode with 0° Hall placement High: Sinusoidal operation mode with 30° Hall placement Floating: Trapezoidal operation mode with 30° Hall placement
U_HN	3	I	U-phase negative Hall input	Differential Hall Sensor negative input for U-phase. Connect to hall sensor negative output. When logic level hall IC is used, tie this pin to VINT/2 level. In single Hall mode, the device uses U-phase hall inputs to drive the motor.
U_HP	2	I	U-phase positive Hall input	Differential Hall Sensor positive input for U-phase. Connect to hall sensor positive output. When logic level hall IC is used, connect this to hall IC output. In single Hall mode, the device uses U-phase hall inputs to drive the motor.
V_HN	5	I	V-phase negative Hall input	Differential Hall Sensor negative input for V-phase. Connect to hall sensor negative output. When logic level hall sensor is used, tie this pin to VINT/2 level. In single hall mode, ground this pin.
V_HP	4	I	V-phase positive Hall input	Differential Hall Sensor positive input for V-phase. Connect to hall sensor positive output. When logic level hall IC is used, connect this to hall IC output. Leave this pin floating to enable single Hall operation.
W_HN	7	I	W-phase negative Hall input	Differential Hall Sensor negative input for W-phase. Connect to hall sensor negative output. When logic level hall sensor is used, tie this pin to VINT/2 level. In single hall mode, ground this pin.
W_HP	6	I	W-phase positive Hall input	Differential Hall Sensor positive input for W-phase. Connect to hall sensor positive output. When logic level hall IC is used, connect this to hall IC output. In single hall mode, ground this pin.
OUTPUT STAGE				
U	14	O	U phase output	Connect to motor terminal U
V	13	O	V phase output	Connect to motor terminal V
W	11	O	W phase output	Connect to motor terminal W

External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM}	VM	GND	10-µF ceramic capacitor rated for VM (if VM = 12 V, 25-V capacitor is suggested, if VM = 18 V, 35-V capacitor is suggested)
C_{VCP}	VCP	VM	16-V, 1-µF ceramic capacitor
C_{SW}	CPP	CPN	0.1-µF X7R capacitor rated for VM

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External Components (continued)

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VINT}	VINT	GND	10-V, 2.2-µF ceramic capacitor Rotor Lock Detection and Retry
C_{RETRY}	RETRY	GND	See 公式 2 for capacitor value
R_{CS}	CS	GND	See *Current Limit and OCP* for resistor value
R_{RD}	VCC (1)	RD	>1 kΩ, RD is open-drain output. This component must be pulled up externally.
R_{FG}	VCC (1)	FG	>1 kΩ, FG is open-drain output. This component must be pulled up externally.

(1) VCC is not a pin on the DRV10970. It can be VINT or any other system voltage (for example the 3.3-V or 5-V supply voltage powering the microcontroller). A VCC supply voltage pull-up is required for open-drain outputs RD and FG

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	20	V
Power supply voltage ramp rate (VM)		2	V/µs
Charge pump voltage (VCP, CPP)	–0.3	25	V
Charge pump negative switching pin (CPN)	–0.3	20	V
Internal logic regulator voltage (VINT)	–0.3	5.5	V
Control pin voltage (PWM, FR, RETRY, CMTMOD, BRKMOD, DAA)	–0.3	VINT + 0.3	V
Open drain output current (RD, FG)	0	10	mA
Open drain output voltage (RD, FG)	–0.3	20	V
Output voltage (U,V,W)	–1	20	V
Output current (U,V,W)	0	2	A
Hall input voltage (U_HP, U_HN, V_HP, V_HN, W_HP, W_HN)	0	6	V
Current limit adjust pin voltage (CS)	–0.3	3.6	V
Operating junction temperature, T_{JMAX}	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Referenced with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Power supply voltage	VM	5	18	V
	Logic level input voltage	PWM, FR, CMTMOD, BRKMOD, DAA, RETRY	0	VINT	V
	Open drain output pullup voltage	FG, RD	0	18	V
	Hall input	U_HP, U_HN, V_HP, V_HN, W_HP, W_HN	0	5	V
I_{OUT}	Output current		0	1.5	A

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
f_{PWM}	Applied PWM signal	15	100	kHz
I_{VINT}	VINT external load current		20 (1)	mA
T_{JOPR}	Operating junction temperature	–40	125	°C

(1) VINT is mainly for internal use. For external, it is only suggested to provide bias current for hall circuit.

7.4 Thermal Information

THERMAL METRIC (1)		DRV10970 PWP (TSSOP) 24 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	36.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	17.4	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	14.8	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.4	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	14.5	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VINT)						
VM	VM operating voltage		5		18	V
I_{VM}	VM operating supply current	VM = 12 V, no external load on VINT		3	5	mA
I_{VM_SLEEP}	VM supply current during sleep mode	VM = 5 and 12 V		35	50	µA
VINT	Integrated regulator voltage	VM = 12 V, 0-mA external load	4.5	5	5.5	V
		VM = 12 V, 20-mA external load	4.5	5	5.5	V
		VM = 5 V, 0-mA external load	4.5	4.8	5	V
		VM = 5 V, 20-mA external load	4.5	4.8	5	V
$V_{GND-BGND}$	Ground potential difference between GND pin to PCB ground				300	mV
CHARGE PUMP (VCP, CPP, CPN)						
VCP	VCP operating voltage	VM = 5 V, less than 1-mA load	9	10	11	V
		VM = 12 V, less than 1-mA load	16	18	19.5	V
		VM = 18 V, less than 1-mA load	22	24	25.5	V
CONTROL INPUTS (PWM)						
V_{IL-PWM}	PWM Input logic low voltage	VM = 5 V and VM = 12 V	0		0.8	V
V_{IH-PWM}	PWM Input logic high voltage	VM = 5 V and VM = 12 V	2.4		5.3	V
$V_{HYS-PWM}$	PWM Input logic hysteresis	VM = 5 V and VM = 12 V	400			mV
R_{PU-PWM}	Internal pullup resistance	VM = 5 V and VM = 12 V	70	100	120	kΩ
$R_{PU-PWM-SL}$	Internal pullup resistance in sleep mode	VM = 5 V and VM = 12 V, sleep mode	1	2	2.5	MΩ
CONTROL INPUTS (RETRY)						
$I_{RETRY-SINK}$	Retry timing set sinking current	VM = 5 V and 12 V	9	10	11	µA

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Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{RETRY-SOURCE}$	Retry timing set sourcing current	VM = 5 V and 12 V	9	10	11	µA
V_{RETRY_H}	Retry comparator high threshold	VM = 5 V and 12 V	1.1	1.2	1.3	V
V_{RETRY_L}	Retry comparator low threshold	VM = 5 V and 12 V	0.55	0.6	0.65	V
CONTROL INPUTS (FR, DAA, CMTMOD, BRKMOD)						
V_{IL}	Digital input logic low voltage	VM = 5 V and 12 V	0		0.8	V
V_{IH}	Digital input logic high voltage	VM = 5 V and 12 V	2.2		5.3	V
$V_{IFLOATING}$	Digital input floating voltage	VM = 5 V and 12 V	24% × VINT		36% × VINT	V
R_{PD-FR}	FR pin Internal pulldown resistance	VM = 5 V and 12 V	160	200	240	kΩ
$R_{PD-BRKMOD}$	BRKMOD pin Internal pulldown resistance	VM = 5 V and 12 V	160	200	240	kΩ
CONTROL OUTPUTS (RD, FG)						
I_{OSINK}	OD output pin sink current	VO = 0.3 V	3.5			mA
I_{OSHORT}	OD output pin short current limit	VO = 12 V		10	25	mA
HALL INPUT COMPARATOR						
V_{HR}	Hall input rising	Zero to positive peak including offset. T_A = –40°C, 25°C, 125°C	0	5	10	mV
V_{HF}	Hall input falling	Zero to negative peak including offset T_A = –40°C, 25°C, 125°C	–10	–5	0	mV
V_{HALL_HYS}	Hall input hysteresis	VHP-VHN T_A = –40°C, 25°C, 125°C	5		12	mV
Vcom	Common mode voltage	VM = 5.5 V – 18 V	0.3		4.3	V
		VM = 5 V – 5.5 V	0.3		3.8	V
Finput	Input frequency range		0		1000	Hz
UVLO						
$V_{UVLO-VM-THR}$	UVLO threshold voltage on VM, rising		3.8	4	4.5	V
$V_{UVLO-VM-THF}$	UVLO threshold voltage on VM, falling		3.6	3.8	4.25	V
$V_{UVLO-VM-HYS}$	VM UVLO comparator hysteresis		40		200	mV
$V_{UVLO-VINT-THR}$	VINT UVLO rise threshold		4.1	4.2	4.5	V
$V_{UVLO-VINT-THF}$	VINT UVLO fall threshold		3.8	4	4.2	V
$V_{UVLO-VINT-HYS}$	VINT UVLO comparator hysteresis		100		300	mV
INTEGRATED MOSFET						
R_{DSON}	Series resistance (H + L)	VM = 12 V, VCP = 19 V, I_{OUT} = 1.5 A		0.4	0.6	Ω
CURRENT LIMIT AND OVER CURRENT PROTECTION (OCP)						
I_{LIM}	Current limit threshold	VM = 12 V, Rcs = 20 kΩ	1.3	1.5	1.7	A
V_{ILIM_THR}	Current limit circuit comparator threshold	VM = 12 V	1.15	1.2	1.25	V
A_{CL}	Current limit attenuation factor	VM = 12 V	22000	25000	28000	A/A

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Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCP}	Over current protection threshold. Magnitude of phase current at which driver stage is disabled to protect the device.	VM = 5 V and 12 V	3		5	A
SLEEP MODE TIMING						
T_{SLEEP_EN}	Minimum PWM low time to recognize a sleep command.	VM = 12 V	1.2			ms
T_{SLEEP_EX}	Minimum PWM high to exit from sleep mode.	VM = 12 V	2			µs
THERMAL SHUTDOWN						
T_{SDN_TR}	Shut down temperature threshold	Shut down triggering temperature	150	160	170	°C
T_{SDN_RS}	Shut down resume temperature	Shut down resume temperature	140	150	160	°C
T_{SDN_HYS}	Shut down temperature hysteresis	Shut down temperature hysteresis	5	10	15	°C
LOCK DETECT						
t_{LOCK_EN}	Lock detect time		0.6	0.7	0.8	s
t_{LOCK_EX}	Lock release time	Retry capacitor = 0.33 uF	4	5	6	s

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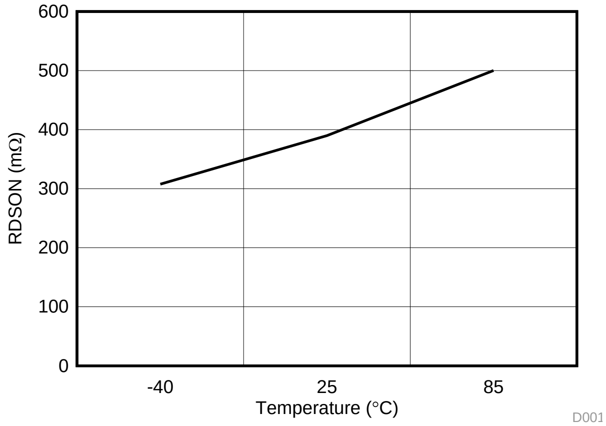
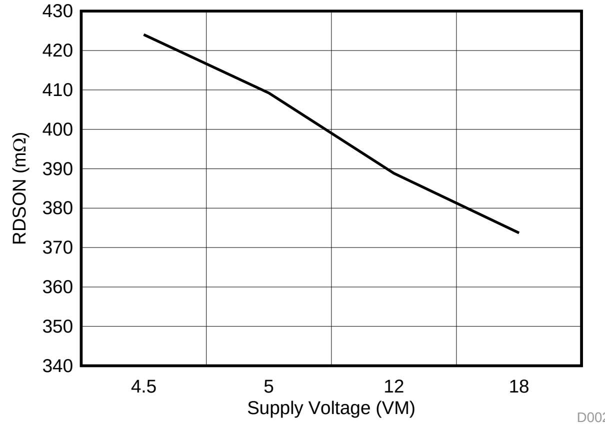
7.6 Typical Characteristics



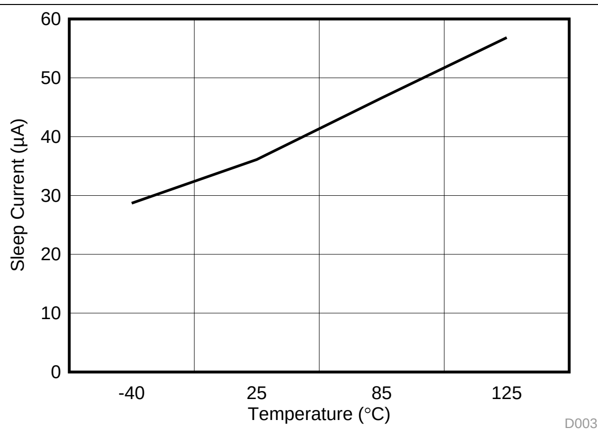
R_{DSON} VM = 12 V

图 1. R_{DSON} Across Temperature at 12 V



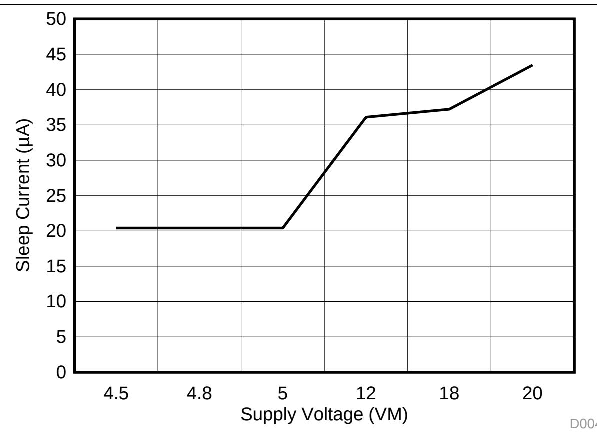
R_{DSON} Temperature = 25°C

图 2. R_{DSON} Across Voltage at 25°C



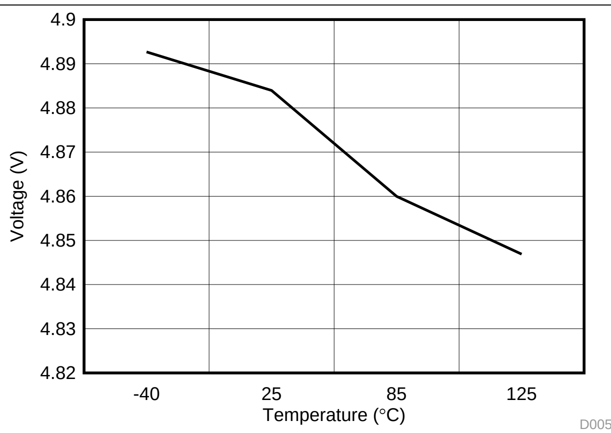
Sleep Current VM = 12 V

图 3. Sleep Current Across Temperature at 12 V



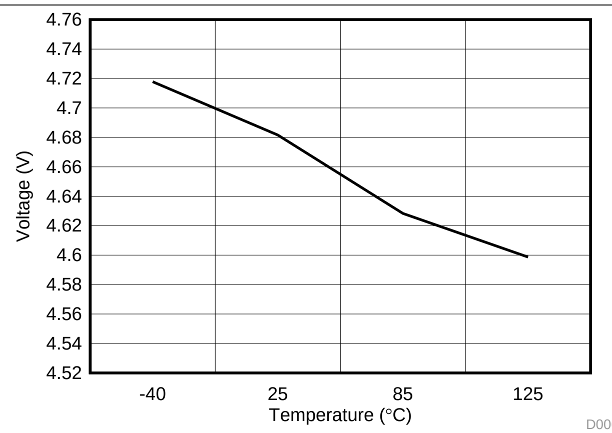
Sleep Current Temperature = 25°C

图 4. Sleep Current Across Voltage at 25°C



5-V Regulator VM = 12 V IL = 20 mA

图 5. VINT LDO Output Voltage Across Temperature, VM = 12 V



5-V Regulator VM = 5 V IL = 20 mA

图 6. VINT LDO Output Voltage Across Temperature, VM = 5 V

Typical Characteristics (接下页)

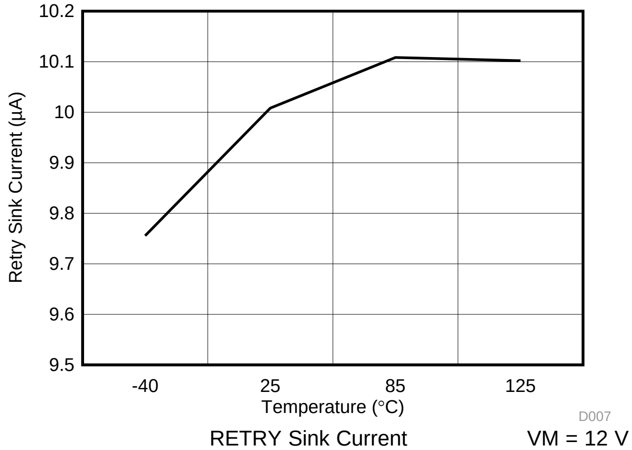


图 7. Retry Sink Current at 12 V

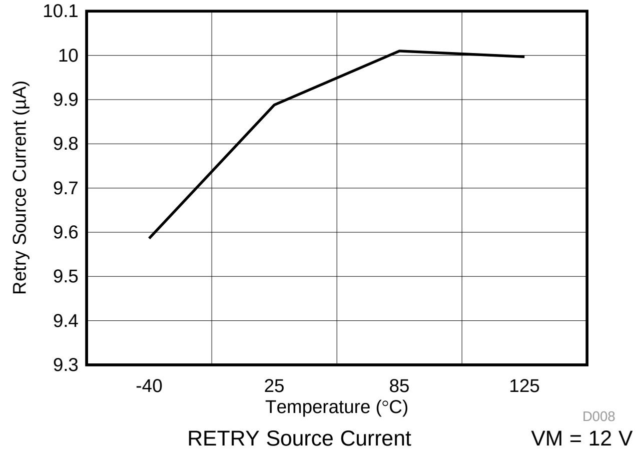


图 8. Retry Source Current at 12 V

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8 Detailed Description

8.1 Overview

The DRV10970 device controls three-phase brushless DC motors using a speed command (PWM) and direction (FR) interface and Hall signals from the motor. The device is capable of driving up to 1-A RMS and 1.5-A peak current per phase.

When the DRV10970 powers up, it starts to drive the motor in trapezoidal communication mode based on the Hall sensor information. If all three Hall sensors are connected, commutation logic relies on all three Hall sensors. If only the U phase Hall sensor is connected (V_HP is floating), DRV10970 starts to drive the motor in single Hall sensor mode.

After 6 electrical cycles, the device switches to sinusoidal drive mode if the CMTMOD pin is not floating. If the motor has Hall sensor 0° placement (set on the CMTMOD pin accordingly), the DRV10970 device automatically adjusts the driving angle based on the feedback from the motor; it optimizes the efficiency regardless of the motor parameters and the load conditions.

The adaptive driving angle adjustment function can be disabled by the DAA pin, in which case, fixed driving angle is available for user to optimize the motor drive efficiency.

The steady-state motor speed is commanded by the PWM input duty cycle, which converts to an average output voltage of VM multiplied by the duty cycle. Floating PWM pin is considered as 100% speed command. Motor rotating direction can be controlled by FR input. Rotational direction can be changed while motor is spinning. The device takes t_{LOCK_EX} time before reversing the direction.

The FG output is aligned with U phase Hall sensor signal which indicates the motor speed. And if the motor is locked by external force for t_{LOCK_EN}, RD output will be asserted to indicate the rotor lock condition, and DRV10970 retries after t_{LOCK_EX} period which is determined by the capacitor on the RETRY pin.

When the motor is stopped, either in lock condition or PWM equals zero, the state of the phases is selected by BRKMOD pin; coasting (phases are floating) or braking (phases are pulled down to GND).

DRV10970 enters sleep mode when PWM is driven low for t_{SLEEP} time and motor comes to a standstill (no FG), internal circuits including regulators are turned off and the power consumption is less than I_{VM_SLEEP}.

Overcurrent, current limit, thermal shutdown and undervoltage protection circuits prevent the system components from being damaged during extreme conditions.

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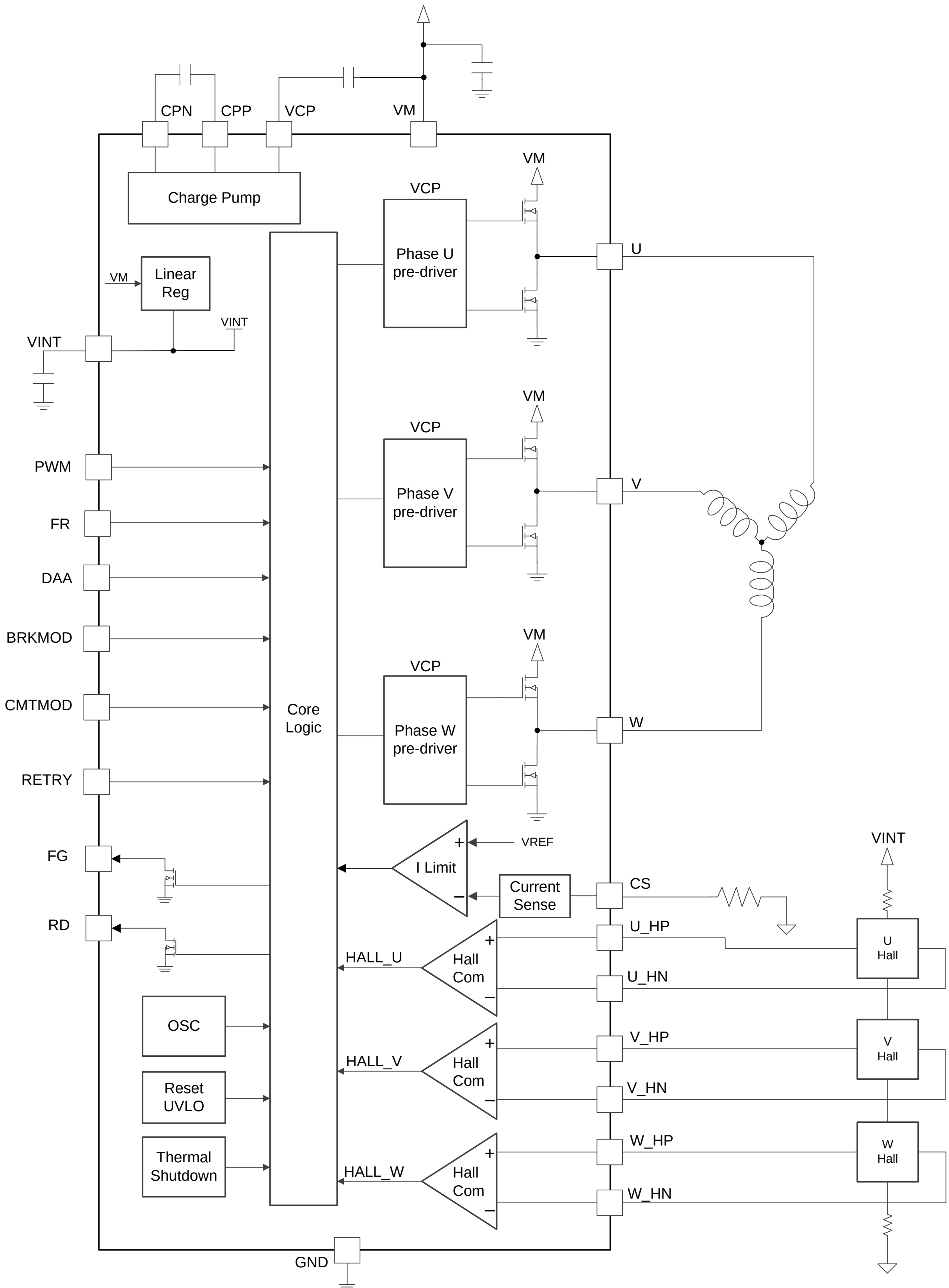
8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Current Limit and OCP

DRV10970 provides two stages of current control, cycle-by-cycle current limit and OCP.

The current limit function limits the motor phase current during the motor operation: during startup, acceleration, sudden load change, and rotor lock condition while spinning. The application specific threshold is achieved by choosing the value of the external resistor connected to the CS pin. 图 9 shows the simplified circuitry of the current limit circuit using the CS pin. The voltage generated on the CS pin is proportional to the value of the external resistor, R_{CS}. The external resistor value is chosen based on the current limit to be achieved (see 公式 1).

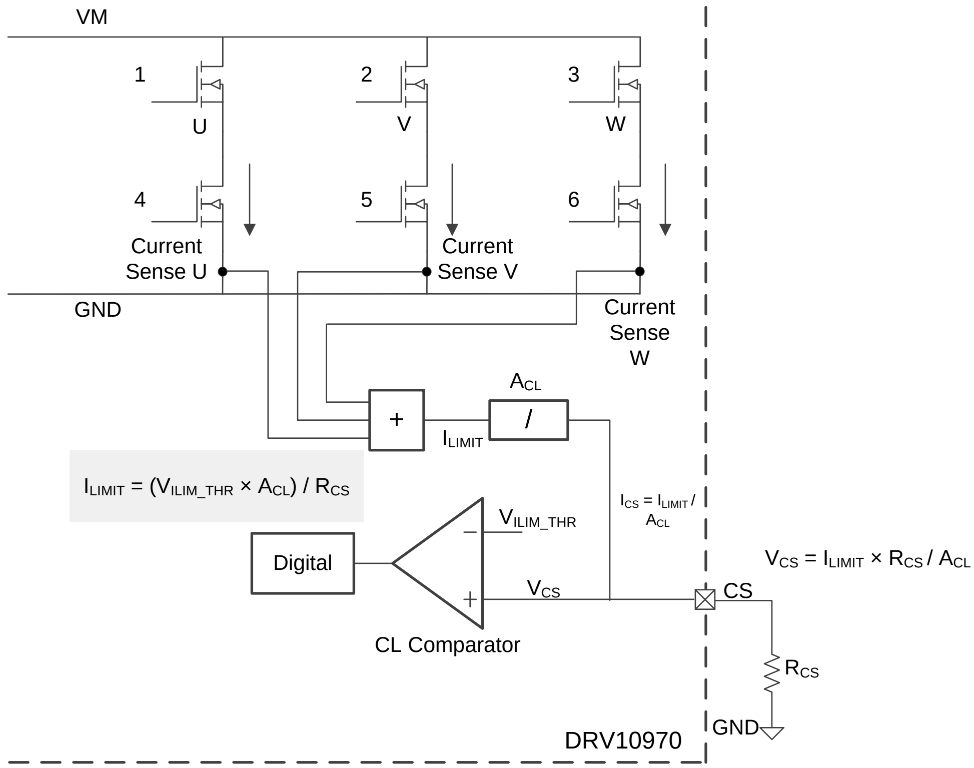


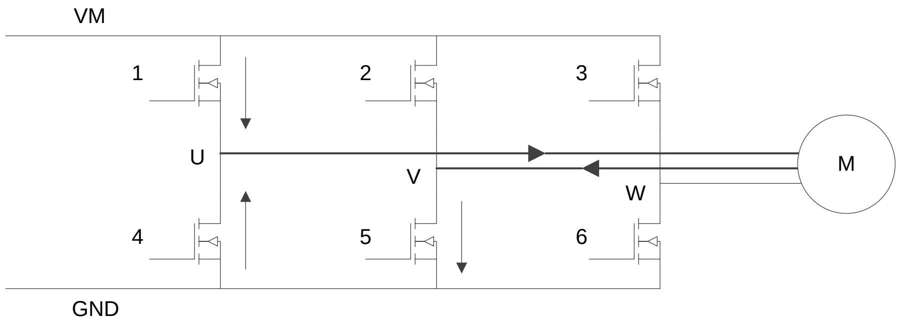
图 9. Current Limit Function Simplified Circuitry

Current limit threshold is set by 公式 1.

$$I_{LIMIT} = (V_{ILIM\_THR} \times A_{CL}) / R_{CS} \quad (1)$$

In trapezoidal operation mode, motor phase current is restricted by means of cycle-by-cycle limit, as shown in 图 10. If the current limit is triggered, one of the conducting MOSFETs is disabled and the complementary side MOSFET is activated until the beginning of the next PWM cycle. In the example shown in 图 10, MOSFET 1 and MOSFET 5 are conducting MOSFETs, MOSFET 1 is disabled, and the complementary MOSFET 4 is activated when the current limit is triggered.

Feature Description (接下页)



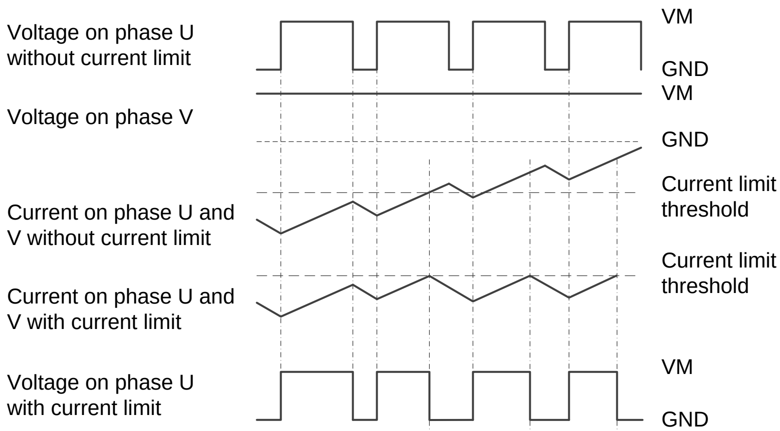


图 10. Cycle-by-Cycle Current Limit in Trapezoidal Mode

If the current limit is triggered in sinusoidal operation mode, DRV10970 device switches to trapezoidal mode of operation to exercise cycle-by-cycle current limiting. If the current limit condition does not show up for 2 electrical cycles, the device will switch back to sinusoidal mode (shown in 图 11). The current limit threshold in sinusoidal mode is 1.5 times the current limit value in the trapezoidal mode. The current limit function can be disabled by connecting CS pin to GND.

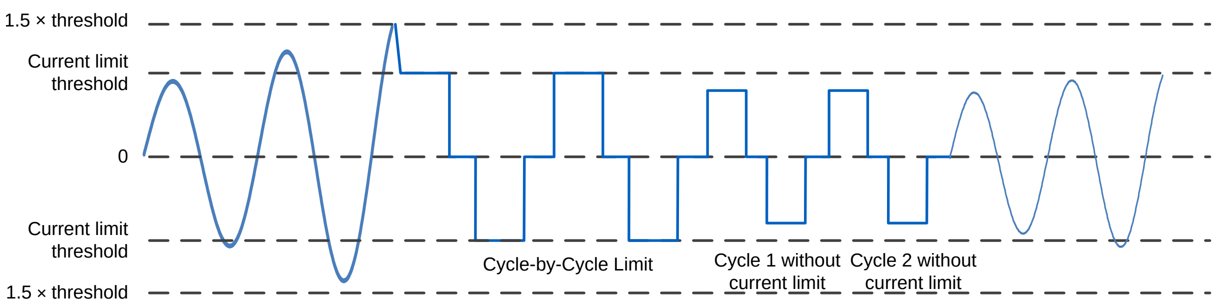


图 11. Current Limit in Sinusoidal Mode

OCP has a fixed threshold I_{OCP}, it can protect the device in catastrophic short-circuit conditions such as phase short to GND, phase short to VM and phase short to another phase. The I_{OCP} limit is similar to the current limit, except that when phase current crosses I_{OCP} threshold (positively or negatively), the device shuts down all the MOSFETs immediately. The device will wait for 2 ms before it starts driving the motor again. If the high current still exists, the device will shut down the MOSFETs and again wait for 2 ms. This process of checking overcurrent will continue until the OC event goes away. The device is capable of handling an OC event continuously for its lifetime. The OC protection feature cannot be disabled.

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Feature Description (接下页)

8.3.2 Thermal Shutdown

If the junction temperature exceeds safe limits, the DRV10970 device places its outputs (U, V, W) in high-impedance mode. After the junction temperature has fallen to a safe level, operation automatically resumes.

8.3.3 Rotor Lock Detection and Retry

A locked rotor condition is detected if the Hall signal stops toggling for t_{LOCK_EN}. The device enters a motor parking state: coasting (if BRKMOD = 0) or braking state (if BRKMOD = 1). In the coasting state, the device places its outputs (U, V, W) in a high-impedance state. In the braking state, it keeps the low-side MOSFETs ON and high-side MOSFETs OFF. The RD pin is asserted to indicate the rotor lock condition. Operation resumes after t_{LOCK_EX} time at the same time RD is deasserted. This process repeats until the locked rotor condition is cleared. RD will be deasserted in sleep mode.

The t_{LOCK_EX} time is determined by the capacitor value connected to the RETRY pin. The accuracy of the capacitor and ground potential difference between the device ground and C_{RETRY} capacitor ground affects the accuracy of the time setting. After the DRV10970 device enters rotor locked state, I_{RETRY}, sourcing current starts to charge the capacitor, C_{RETRY}, until the voltage of the capacitor reaches V_{RETRY_H}, then I_{RETRY} sinking current starts to discharge the capacitor, C_{RETRY}, until the voltage of the capacitor falls below V_{RETRY_L}. This process repeats 128 times which determines the t_{LOCK_EX}, then DRV10970 retry starting the motor.

$$t_{LOCK\_EX} = 15.36 \times 10^6 \times C_{RETRY} \text{ (in seconds)} \quad (2)$$

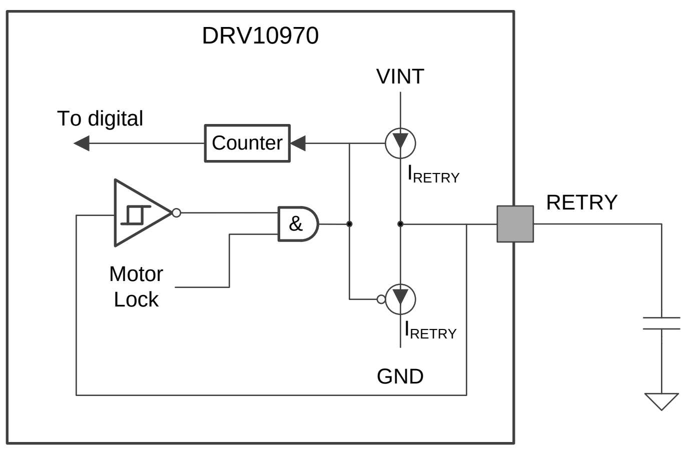

图 12. Lock Release Timing Circuit

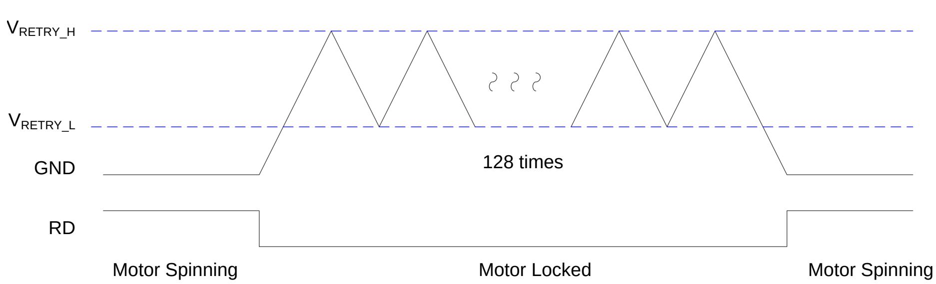

图 13. Lock Release Timing Waveform

8.3.4 Supply Undervoltage Condition (UVLO)

When the supply voltage (VM) level falls below the undervoltage lockout threshold voltage ($V_{UVLO\text{-}Th\text{-}f}$), the DRV10970 will keep phases (U, V, W) in high-impedance mode. Operation resumes when VM rises above the $V_{UVLO\text{-}Th\text{-}r}$ threshold.

Feature Description (接下页)

8.3.5 Sleep Mode

The DRV10970 provides a sleep mode function to save power when the motor is not spinning. The device can be commanded to enter sleep mode by driving logic low on PWM pin for at least t_{SLEEP_EN} seconds. Before entering low-power state, the speed will be ramped down (by brake condition or by coasting) where rotor lock condition is detected. This sequence to bring the motor to a halt condition may take several seconds based on the motor. The device then enters sleep state where reset is asserted and supply is driven to low. Only a small portion of the logic is kept alive to detect the PWM pin high. The device will wake up after PWM goes high (PWM high signal needs to be longer than t_{SLEEP_EX}) and starts to drive the motor again.

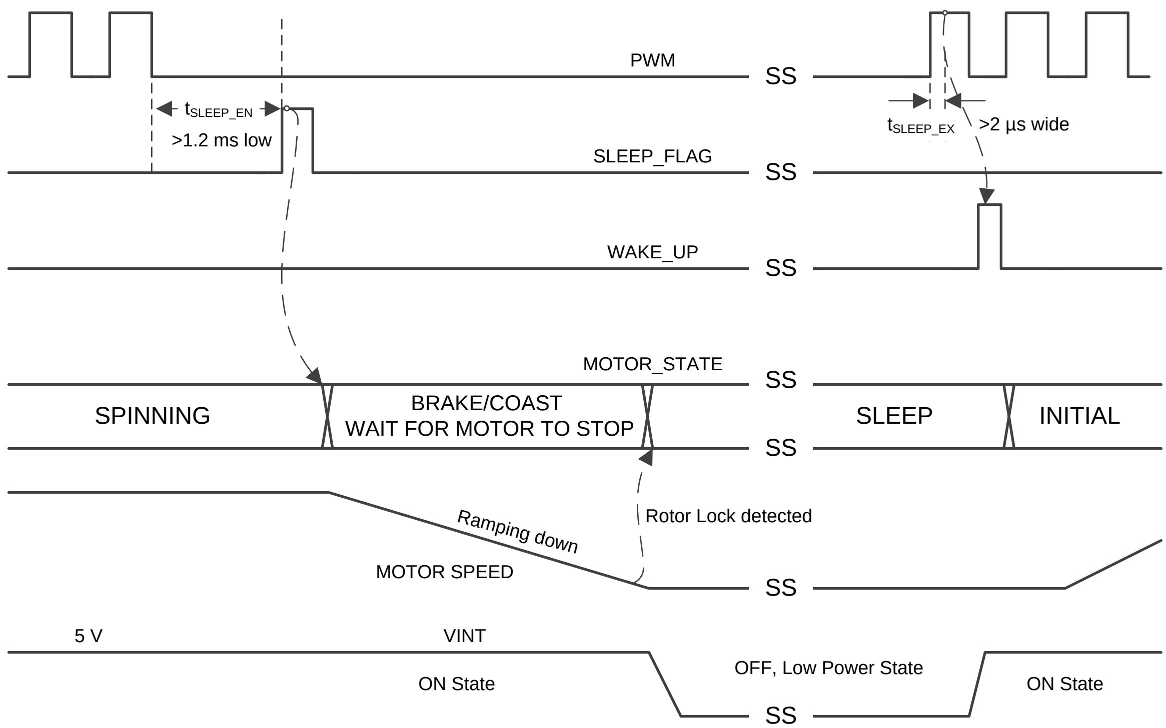

图 14. Sleep Mode Sequence and Timing

The current consumption during sleep mode is less than I_{VM_SLEEP}.

In sleep mode, internal regulator VINT is shut down; if the Hall sensors are powered by VINT, the Hall sensors are also put into power off condition to further save power. The U, V, and W phase outputs are tri-stated, FG and RD pins are de-asserted while in the sleep mode. The device will not be able to perform OCP while in sleep mode.

8.4 Device Functional Modes

8.4.1 Operation in Trapezoidal Mode and Sinusoidal Mode

The DRV10970 device can operate in either trapezoidal mode or sinusoidal mode depending on the setting of CMTMOD pin. Sinusoidal operation mode provides better acoustic performance, which is more suitable for applications like refrigerator fans, HVAC fans, pumps, and other home appliances. Trapezoidal mode provides higher driving torque, which is more suitable for systems with heavy and unpredictable load conditions, such as power tools and actuators.

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Device Functional Modes (接下页)

8.4.1.1 Trapezoidal Control Mode

Trapezoidal control is also called 120° control or 6-step control. In the trapezoidal control mode, the DRV10970 device drives standard six step commutation sequence based on the Hall input states and FR (direction) pin value. Trapezoidal (30° Hall placement) commutation is in accordance with 表 1. The startup scheme of sinusoidal control mode is also based on trapezoidal commutation. Trapezoidal mode does not support single Hall sensor operation; it may cause unpredictable motor operation.

表 1. Trapezoidal Commutation With 30° Hall Placement

STATE	HALL SIGNAL (1)			PHASE OUTPUT (2)					
				FR = 1			FR = 0		
	U	V	W	U	V	W	U	V	W
1	1	1	0	High	Hi-Z	Low	Low	Hi-Z	High
2	1	0	0	High	Low	Hi-Z	Low	High	Hi-Z
3	1	0	1	Hi-Z	Low	High	Hi-Z	High	Low
4	0	0	1	Low	Hi-Z	High	High	Hi-Z	Low
5	0	1	1	Low	High	Hi-Z	High	Low	Hi-Z
6	0	1	0	Hi-Z	High	Low	Hi-Z	Low	High
1x (3)	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
2x (3)	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

(1) Hall signal XHALL = 1 if the positive input terminal voltage (x_HP) is higher than the negative input terminal voltage (x_HN)
(2) Phase output = Hi-Z which means both the high-side and low-side MOSFETs are turned off.
(3) State 1x and 2x are invalid states, DRV10970 will output high impedance for all three phases in this condition. Hall sensor placement or connection needs to be changed.

表 2. Trapezoidal Commutation With 0° Hall Placement

8.4.1.2 Sinusoidal Pulse Wide Modulation (SPWM) Control Mode

If the sinusoidal operation mode is selected, the device will start the motor with trapezoidal operation (based on the commutation table shown in 表 1) and switch to sinusoidal after 6 electrical cycles. If current limit is triggered during trapezoidal startup, the transition will be delayed until current limit is cleared. If current limit is triggered in sinusoidal operation, the device will switch back to trapezoidal mode and will remain until the current limit event goes away (refer to *Current Limit and OCP*).

In sinusoidal control mode, the commutation will only rely on phase U Hall sensor input and ignore the phase V and W Hall sensor input.

The DRV10970 provides sinusoidal voltage shaping in the SPWM mode. The device generates 25-kHz PWM outputs on each phase, which have an average value of sinusoidal waveform on phase to phase. If the phase voltage is measured with respect to ground, the waveform is sinusoidal coupled with third-order harmonics. At any time among the three phases, one phase output equals to zero, as shown in 图 16.

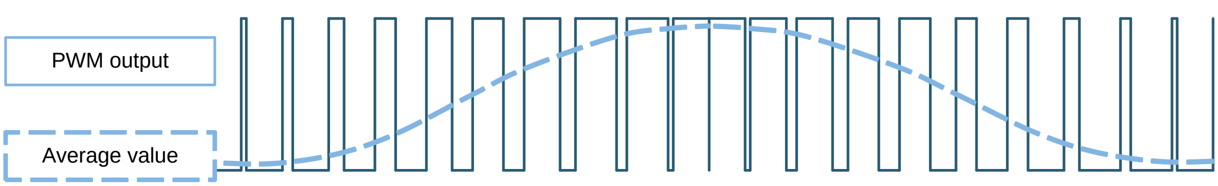

图 15. PWM Output and the Average Value

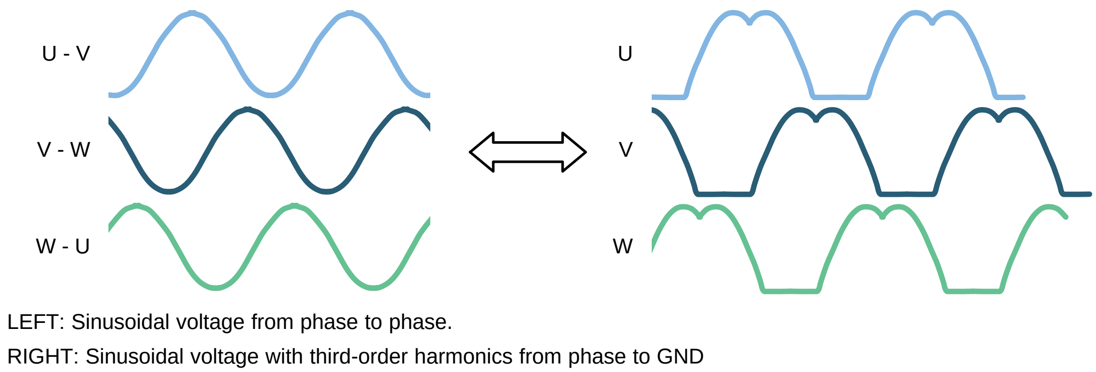

图 16. Sinusoidal Voltage With Third-Order Harmonics Output

The output amplitude is determined by the VM and the maximum PWM duty cycle among one electrical cycle. If VM is used to control the motor speed, the output maximum PWM duty cycle is 100%. The output amplitude is proportional to the VM amplitude.

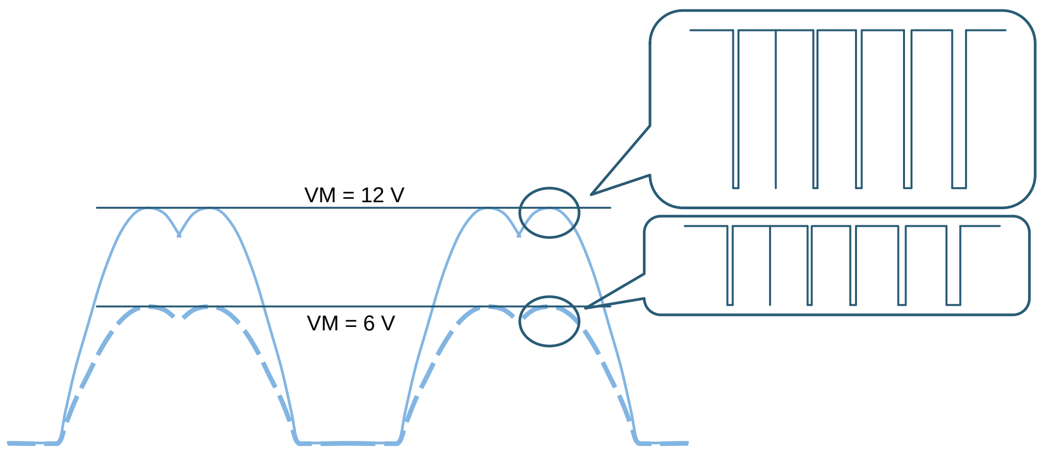

图 17. Adjust VM to Control the Motor Speed

The PWM is used for controlling the motor speed. System calculates the duty cycle of the PWM input as DutyIN, which is converted into sinusoidal PWM output.

The maximum amplitude is when PWM input is 100% and maximum PWM output duty cycle is 100%, the output amplitude will be VM. A lower value such as VM / 2 could be achieved by driving the PWM duty to 50%. When the input duty cycle is less than 10% and greater than 0% DRV10970 keeps the input command at a 10% duty cycle (see 图 18).

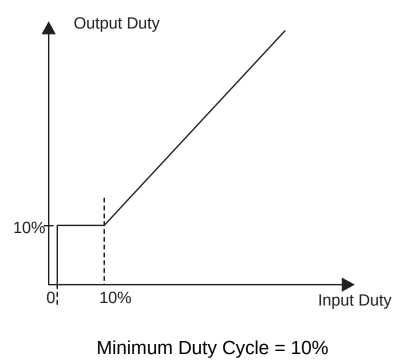

图 18. Duty Cycle Profile

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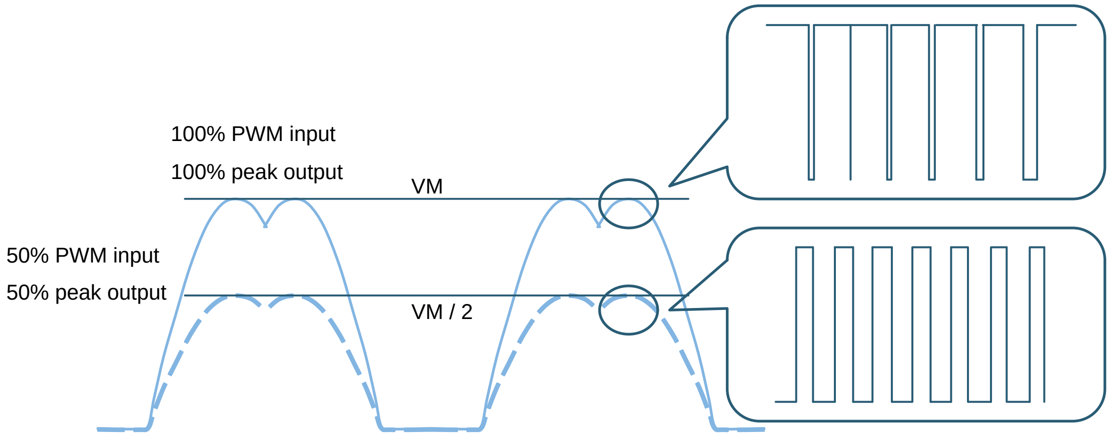

图 19. Adjust PWM Input Duty Cycle to Control the Motor Speed

Note that the speed control PWM input frequency does not reflect to PWM output frequency on the phase outputs. The device supports input PWM frequency in the range of 15 to 100 kHz, the PWM output frequency on the phase is always 25 kHz.

8.4.2 Single Hall Sensor Operation

The DRV10970 device supports single Hall sensor operation to reduce system cost.

If only U phase Hall sensor is connected to the device and V and W phase Hall sensors are not installed in the system, the device automatically drives the motor in single Hall sensor mode. Single Hall sensor operation does not support trapezoidal operation, which may cause unpredictable motor behavior.

In single hall sensor mode, rotor is aligned to a known position for about 700 ms first and then motor is driven with 2-step DC current into the coil, which means instead of 6-step control, the device only outputs 2 steps based on the U phase Hall sensor signal. The direction of driving current is based on the FR input and the commutation mode setting. 表 3 shows the startup logic. For example, if 0° Hall placement is selected (CMTMOD pin equals to High), FR equals to high, and U phase Hall sensor signal is high, DRV10970 will drive U phase PWM and both V and W phase low.

表 3. Single Hall Startup Commutation Table

HALL PLACEMENT	HALL SIGNAL	PHASE OUTPUT					
		FR = 1			FR = 0		
		U	V	W	U	V	W
0°	1	PWM	LOW	LOW	LOW	PWM	PWM
0°	0	LOW	PWM	PWM	PWM	LOW	LOW
30°	1	PWM	LOW	Hi-Z	LOW	PWM	Hi-Z
30°	0	LOW	PWM	Hi-Z	PWM	LOW	Hi-Z
Single Hall Align		Hi-Z	LOW	PWM	Hi-Z	LOW	PWM

Cycle-by-cycle current limit is effective during single Hall sensor startup. After 6 electrical cycles of startup, the device will switch to sinusoidal mode of operation. If current limit is triggered, sinusoidal control will transit back to 2-step drive mode, same as startup sequence. Refer to *Current Limit and OCP*.

Note that single Hall sensor operation mode may exhibit slight reverse spin of the rotor during startup. The reverse movement will be less than 180 electrical degrees.

The rotor locked condition is detected when no U-phase hall switching for about 700ms. For certain low inertia motors or no load condition, the rotor may continue to vibrate when the rotor is locked which may result in a hall signal switching. This condition is not detected by the device as the hall period may look like a normal motor spinning condition. In this scenario, the device may continue to drive the motor. Lowering the OC limit may help resolve this condition.

8.4.3 Adaptive Drive Angle Adjustment (ADAA) Mode

In sinusoidal mode, the phase voltage vector is driven such that phase current and BEMF voltages are aligned (in-phase) in order to achieve the maximum motor efficiency possible. When Hall sensor is placed at 0°, the BEMF voltage will be in-phase with respective Hall signals. The ADAA logic takes advantage of this fact and aligns the U-phase current to the U-Hall sensor input.

If DAA pin is floating, the DRV10970 device will operate in the ADAA mode, in which case, the device continuously monitors the phase difference between the U-phase current and U-phase Hall signal while adjusting the phase voltage driving angle Δθ (with respect to the U-Hall sensor signal, same as U-BEMF zero crossing) to align the current and Hall signal (shown in 图 20). ADAA mode is the recommended mode of operation where the motor efficiency is maximized irrespective of motor parameters, load conditions, and motor speeds. ADAA mode is only available in sinusoidal mode and 0° Hall sensor placement. The motors with 30° Hall placement may use the fixed drive angle feature to achieve maximum system efficiency for a given application.

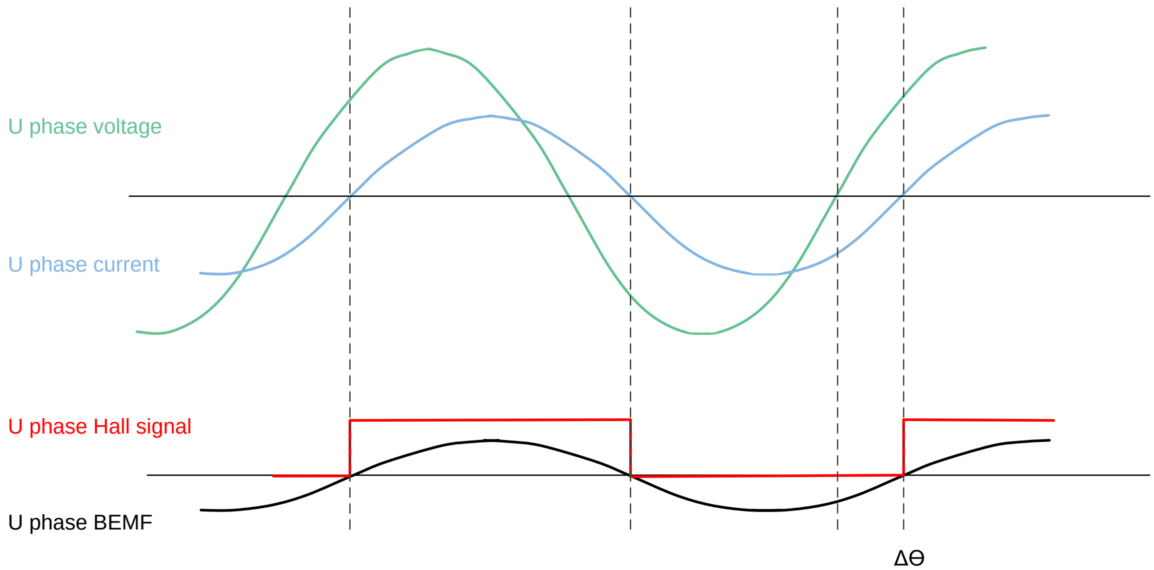

图 20. Adaptive Drive Angle Adjustment

For sinusoidal mode and 0° Hall sensor placement, if DAA pin is connected to GND, voltage driving angle will be fixed at 10°. If DAA pin is connected to VINT, voltage driving angle will be fixed at 5°.

For sinusoidal mode and 30° Hall sensor placement, if DAA is floating, voltage drive angle will be fixed at 0°. DAA pin is connected to GND, voltage driving angle will be fixed at 10°. If the DAA pin is connected to VINT, voltage driving angle will be fixed at 5°.

In trapezoidal operation mode, DAA input is ignored and always control the output based on 表 2.

表 4 shows the DRV10970 operation modes with DAA and CMT_MOD configurations.

表 4. DAA and CMT_MOD Configurations

MODE	MOTOR TYPE	HALL PLACEMENT	DAA = FLOATING	DAA = GND	DAA = VINT	COMMENTS
CMT_MOD = floating	Trapezoidal	30°	Trapezoidal mode, DAA signal is ignored.			The Trapezoidal motor with 0° Hall placement may use 30 degree Hall delay (OTP setting) to achieve optimum driving.
CMT_MOD = GND	Sinusoidal	0°	ADAA	10° drive angle	5° drive angle	BEMF zero crossing and Hall crossing will be in-sync.
CMT_MOD = VINT		30°	0° drive angle	10° drive angle	5° drive angle	The drive angle is specified with respect to BEMF zero crossing. When measured with respect to Hall-U signal, add 30°.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Hall Sensor Configuration and Connections

Hall sensors must be connected to the DRV10970 to provide the feedback of the motor position. The DRV10970 Hall sensor input circuit is capable of interfacing with a variety of Hall sensors, and with two different ways of Hall sensor placement, which are 0° placement and 30° placement.

Typically, a Hall element is used, which outputs a differential signal on the order of 100 mV or higher. The VINT regulator can be used for powering the Hall sensors, which eliminates the need for an external regulator. The Hall elements can be connected in serial or parallel as shown in 图 21 and 图 22.

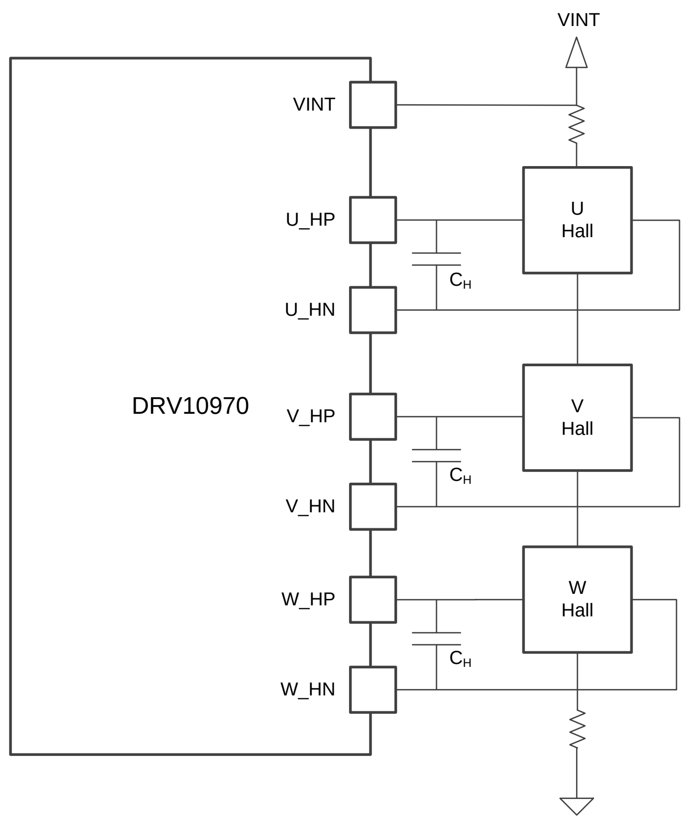

图 21. Serial Hall Element Connection

Application Information (接下页)

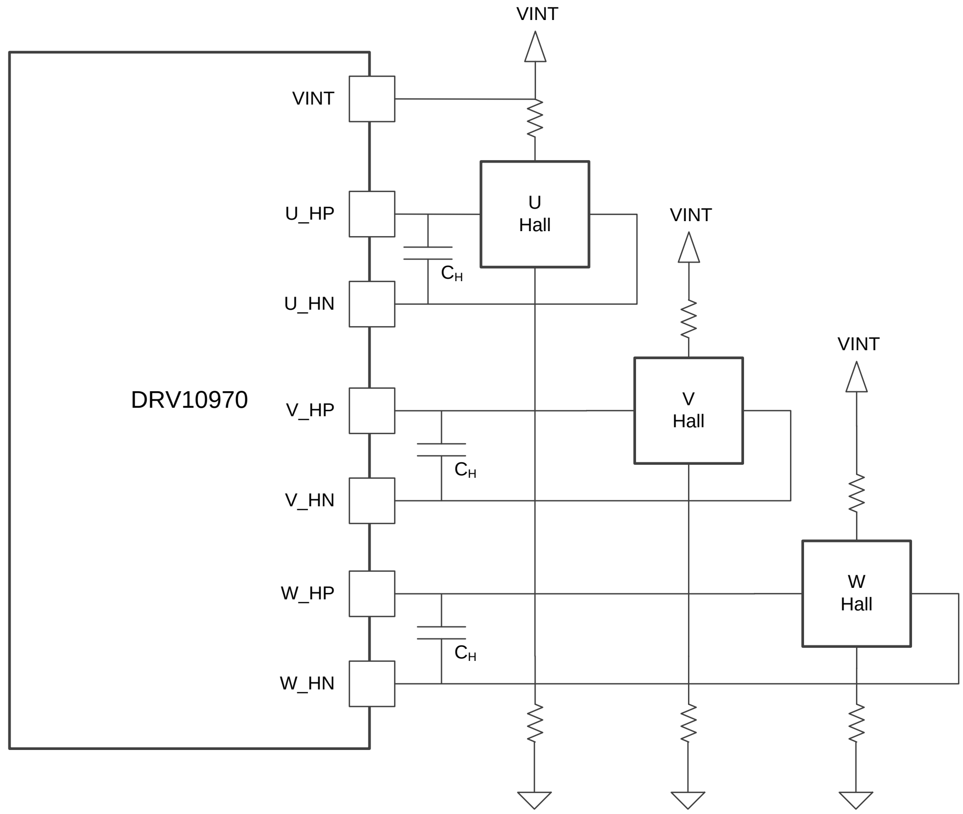

图 22. Parallel Hall Element Connection

Noise on the Hall signal degrades the commutation performance of the device. Therefore, take utmost care to minimize the noise while routing the Hall signals to the device inputs. The device internally has fixed time hall filtering of about 320 µs. To further minimize the high-frequency noise, a noise filtering capacitor may be connected across x_HP and x_HN pins as shown in 图 21 and图 22. The value of the capacitor can be selected such that the RC time constant is in the range of 0.1 to 2 µs. For example, Hall sensor with internal impedance (between Hall output to ground) of 1 kΩ, C_H value is 1 µF for 1-µs time constant.

Some motors integrate Hall sensors that provide logic outputs with open-drain type. These sensors can also be used with the DRV10970, with circuits shown in 图 23. The negative (x_HN) inputs are biased to 2.5 V by a pair of resistors between VINT and ground. For open-drain type Hall sensors, an additional pullup resistor to supply is needed on the positive (x_HP) input, where VINT is used again. The VINT output may be used to supply power to the Hall sensors as well.

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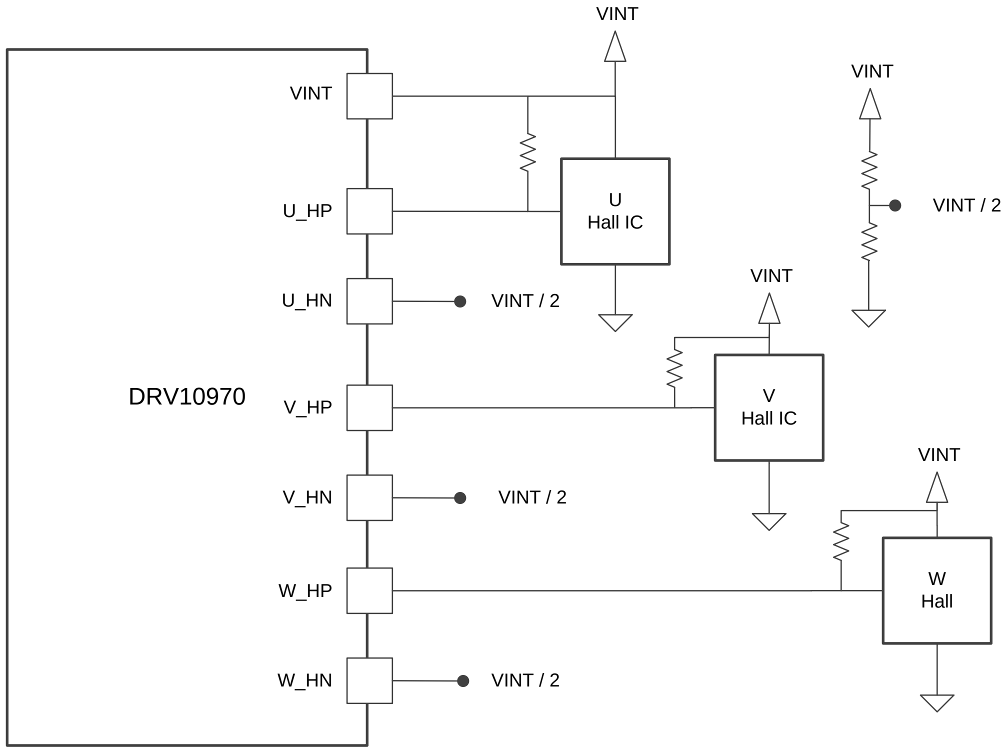

图 23. Hall IC Connection

The correspondence between the phase U, V, W and the Hall signal U, V, W needs to follow the DRV10970 definition, which is:

1. Phase U is leading phase W by 120°, phase W is leading phase V by 120°. The Hall signal positive output is aligned with respective phase BEMF. Choose FR = 1 and 0° placement option (see 图 24).
2. Phase U is leading phase V by 120°, phase V is leading phase W by 120°. The Hall signal positive output is aligned with respective phase BEMF in the opposite direction. Choose FR = 0 and 0° placement option (see 图 25).
3. Phase U is leading phase W by 120°, phase W is leading phase V by 120°. The Hall signal positive output is 30° lagging of respective phase BEMF. Choose FR = 1 and 30° placement option (see 图 26).
4. Phase U is leading phase V by 120°, phase V is leading phase W by 120°. The Hall signal positive output is 30° leading of respective phase BEMF. Choose FR = 0 and 30° placement option (see 表 2 and 图 29).

The correspondence and sequency is also applied to applications using open-drain output Hall ICs. 图 28 is an example of FR = 0, and 30° placement condition.

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Application Information (接下页)

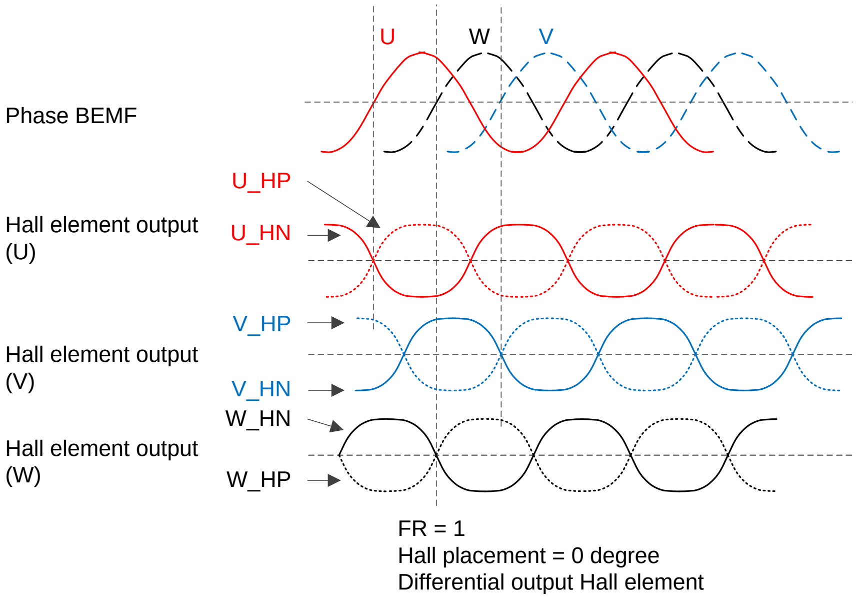

图 24. Correspondence Between Motor BEMF and Hall Signal (FR = 1, 0° Placement)

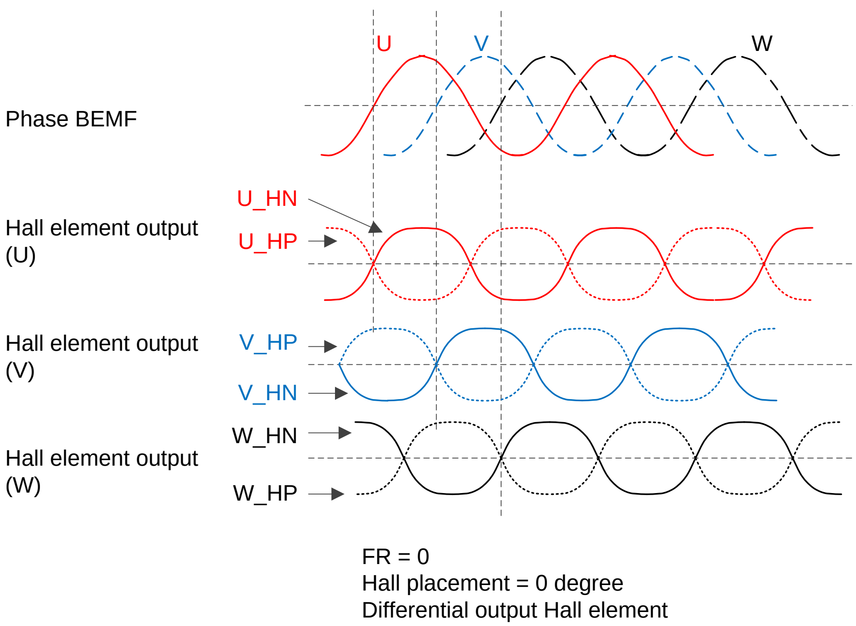

图 25. Correspondence Between Motor BEMF and Hall Signal (FR = 0, 0° Placement)

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Application Information (接下页)

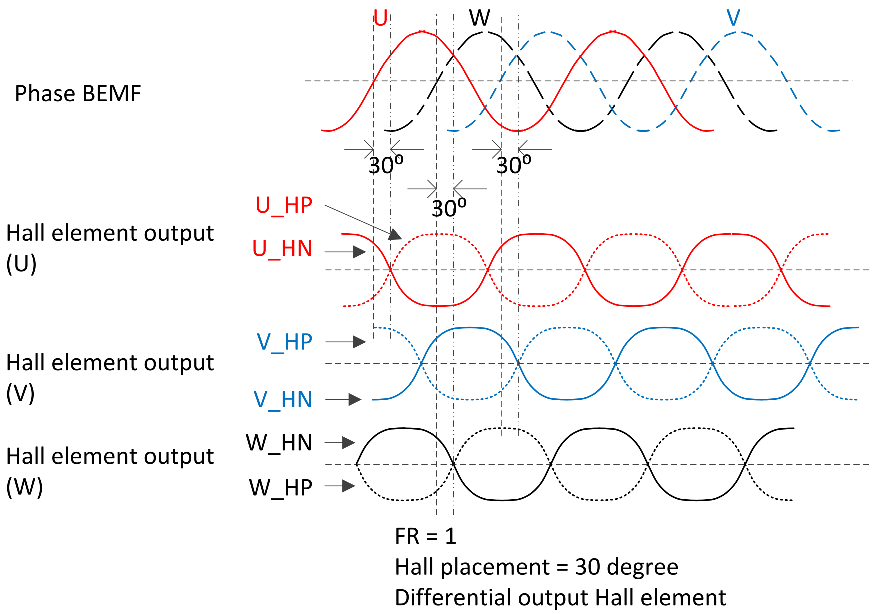

图 26. Correspondence Between Motor BEMF and Hall Signal (FR = 1, 30° Placement)

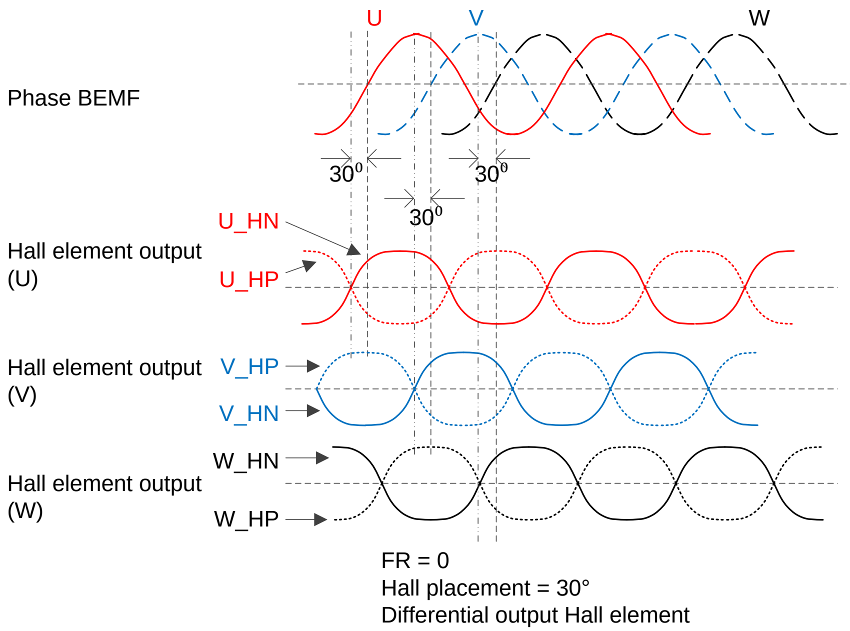

图 27. Correspondence Between Motor BEMF and Hall Signal (FR = 0, 30° Placement)

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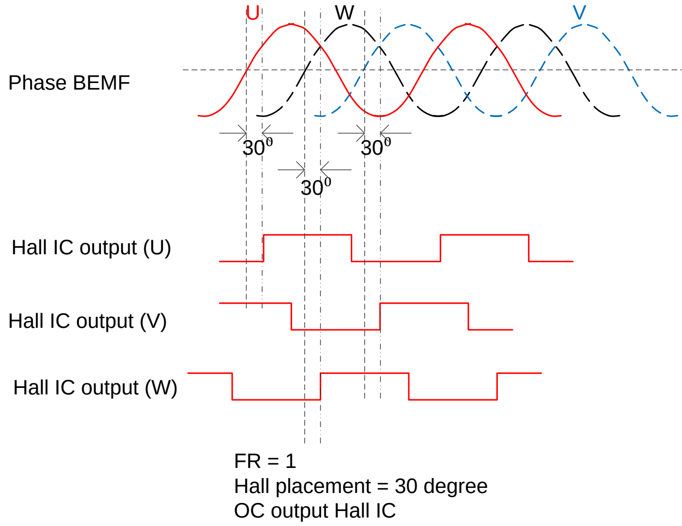

图 28. Correspondence Between Motor BEMF and Hall Signal (FR = 1, 30° Placement, Hall IC)

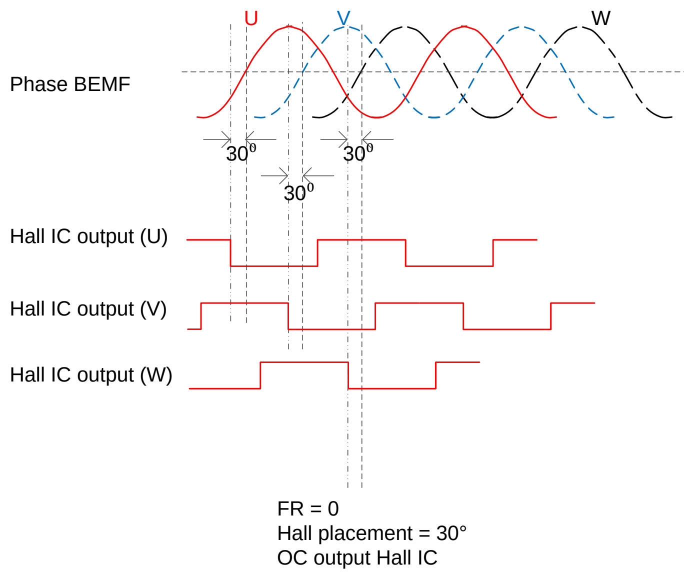

图 29. Correspondence Between Motor BEMF and Hall Signal (FR = 0, 30° Placement, Hall IC)

If the motor terminal definition is different from the previous description, rename the motor phase U, V, W, or the Hall U, V, W, or swap the positive and negative of the Hall sensor output to make it match.

Use these tips to find the correct U, V, and W phases and the respective Hall sensors:

1. Assume motor phases and Hall outputs do not have labels. If named, remove them.
2. Label A, B, C to the motor terminals (phases). Label Da and Db, Ea and Eb, Fa and Fb to the Hall output pairs. If Hall ICs are used, just label the digital outputs as D, E, F.
3. Use three 10-kΩ resistors, connect them to motor terminals - A, B, C with star connection. The center is called COM.
4. Provide power to the Hall sensors.

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Application Information (接下页)

5. Use 4 channel Scope to observe signals. Connect probe -1, 2, 3 to A, B, C terminals of the motor (phases), probe-4 connects to Hall Da (or D). Name the probe 1 (terminal-A) as U-phase. (see 图 30)
6. Turn the rotor manually in clock-wise direction. If the waveform on probe-1 (U-phase) is leading probe-2 (terminal-B) by 120°, name the terminal-B as phase W and terminal-C as phase V. Else if waveform on the probe-2 is leading probe 1 (U) by 120°, terminal-B as V, terminal-C as W. At this stage all three phases of the motor are identified.
7. Motor manufacturers have two popular Hall placement options. The first is 0° Hall placement (BEMF and Hall signals are in-phase) and the second is 30° Hall placement (BEMF leads Hall signal by 30°). If the probe-4 is in-phase (or lagging 30°) with phase-U, name Da as Hall U positive (U_HP), Db as Hall U negative (U_HN). If probe-4 is in-phase with phase U (or lagging 30°), but inverted polarity, name Da as U_HN, Db as U_HP. If the probe-4 is not in-phase (or lagging 30°) with respect to U but aligns with phase-V or W, name accordingly as V_HP/V_HN or W_HP/W_HN. Repeat this step to map Ea/Eb and Fa/Fb in the same way. By end of this step, all three sets of Hall signals are mapped to respective phase signals - phase U & Hall U_HP/HN, phase V & Hall V_HP/V_HN and phase W and W_HP/W_HN. Care should be taken while judging 30° Hall placement, sometimes 30° and 60° look alike. If U phase is leading Hall Da by 60°, there will be another phase (V or W) with in-phase or lagging by 30° relationship. Hence it's important to check all three phases before concluding.
8. When Hall ICs are used, if the Hall D is in-phase or lagging 30° with respect to phase U but inverted polarity, name the Hall D output as U_HN, and 2.5-V reference voltage to U_HP. If Hall D is leading 30°, then turn the rotor in counter clock-wise direction and map remaining E & F Hall outputs.
9. After phase UVW and Hall UVW positive negative are identified, manually rotate the motor again, check if the result matches 图 24 and 图 25 (0° placement) or 图 26 and 图 25 (30° placement).
10. Connect U,V,W and Hall U,V,W to the DRV10970, with the FR = 1, it should rotate with direction you manually spun it. Connect FR = 0, the motor will spin in the other direction.

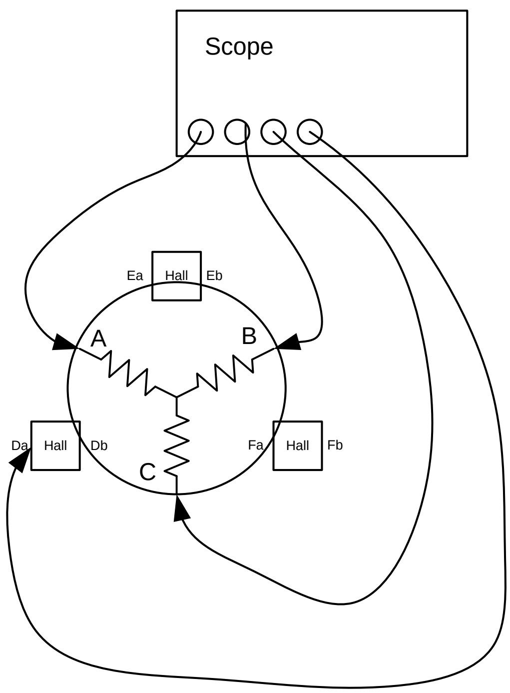

图 30. Motor Measurement

9.2 Typical Application

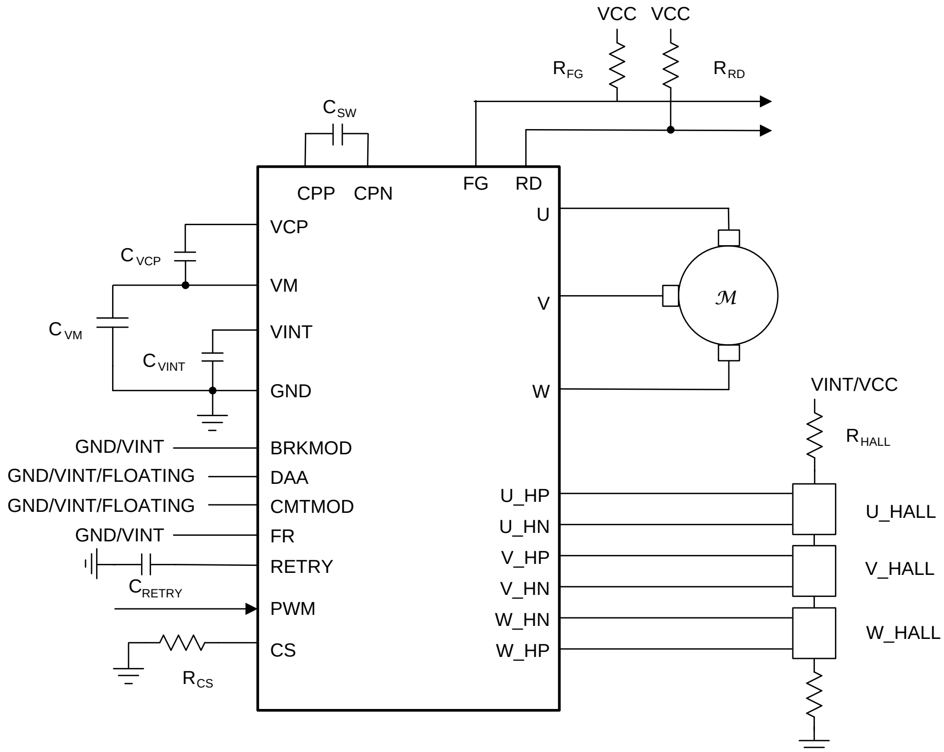

图 31. Typical Application Schematic

9.2.1 Design Requirements

表 5 gives design input parameters for system design.

表 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage	5 to 18 V
Continuous operation current	0 to 1 A
Peak current	1.5 A
Hall sensor differential output peak	>40 mV
PWM input frequency	15 to 100 kHz
PWM duty cycle	0% to 100%

9.2.2 Detailed Design Procedure

- Refer to *Design Requirements* and make sure the system meets the recommended application range.
- Refer to *Hall Sensor Configuration and Connections* and make sure correct phases and corresponding hall signals are identified.
- Refer to *Hall Sensor Configuration and Connections* and make sure hall signals are connected accurately.
- Build your hardware based on *Layout Guidelines*.
- Connect the device into system and validate your system.

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9.2.3 Application Curves

图 32. Three Hall Start-up Sequence

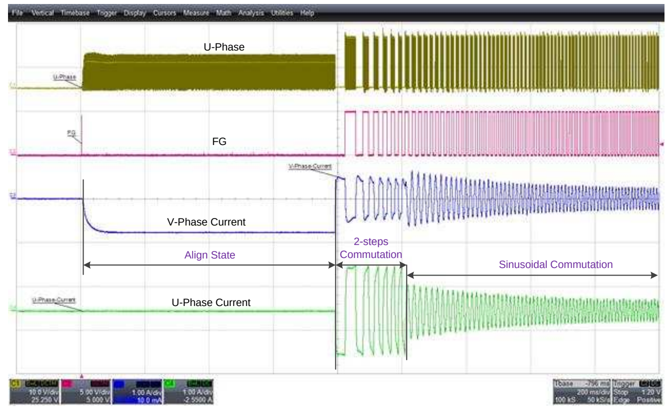

图 33. Single Hall Start-up Sequence

10 Power Supply Recommendations

The DRV10970 is designed to operate from an input voltage supply (VM) range between 5 and 18 V. Place a 10-µF ceramic capacitor rated for VM as close as possible to the DRV10970.

11 Layout

11.1 Layout Guidelines

The VM terminal should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10-µF rated for VM. Place this capacitor as close as possible to the VM pin with a thick trace or ground plane connection to the device GND pin.

The C_{RETRY} capacitor should be placed as close to the RETRY pin as possible with a thick trace or ground plane connection to the device GND pin.

A low-ESR ceramic capacitor must be placed in between the CPN and CPP pins. TI recommends a value of 0.1-µF rated for VM. Place this component as close as possible to the pins.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 1-µF rated for 16 V. Place this component as close as possible to the pins.

Bypass VINT to ground with 2.2-µF ceramic capacitors rated for 10 V. Place these bypassing capacitors as close to the pins as possible.

Because the GND pin carries motor current, take utmost care while planning grounding scheme, keep the ground potential difference between any two points less than 100 mV.

11.2 Layout Example

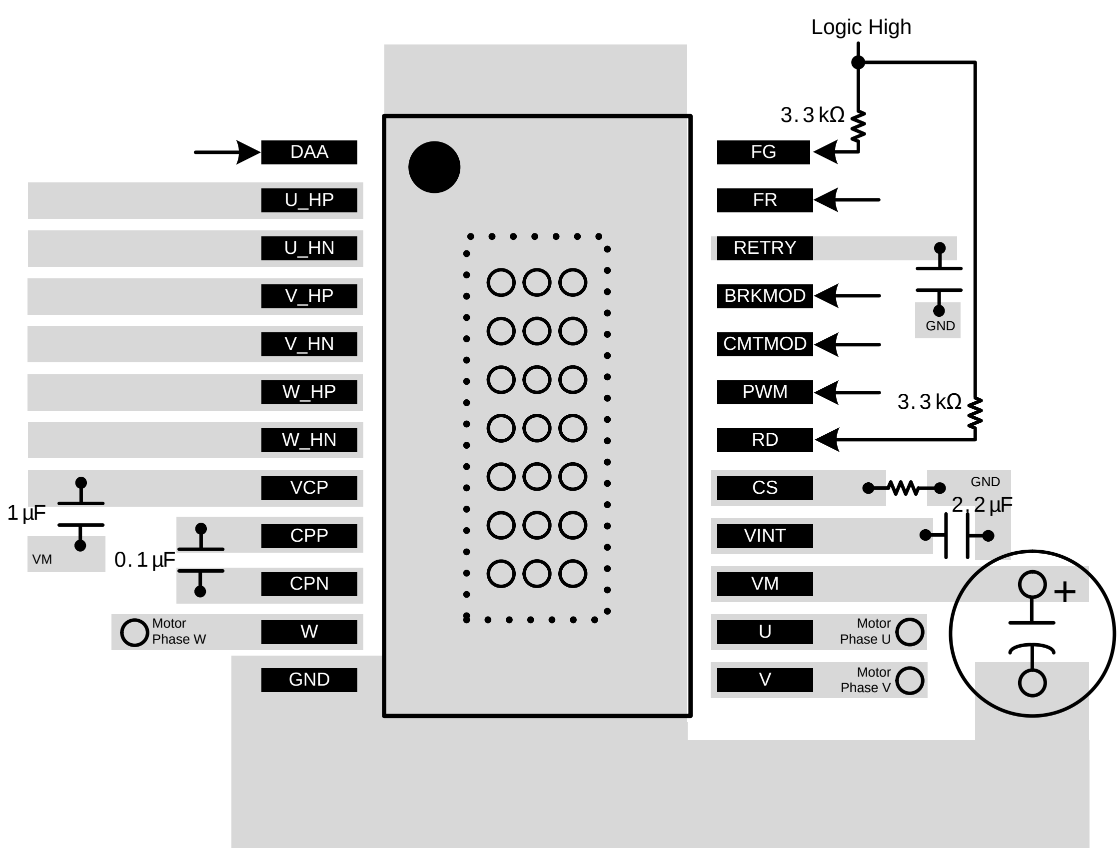

图 34. Layout Schematic

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12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV10970PWP	ACTIVE	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10970	Samples
DRV10970PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10970	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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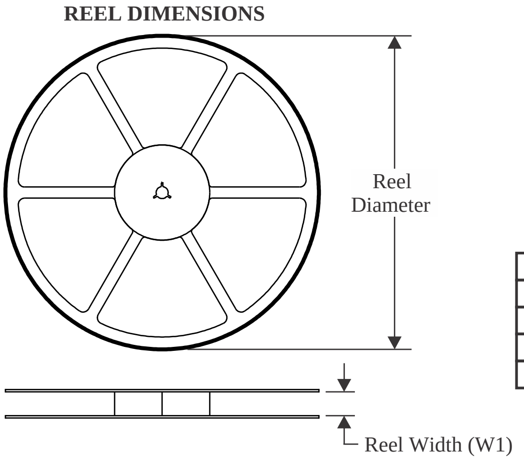
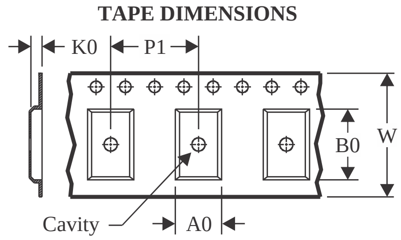
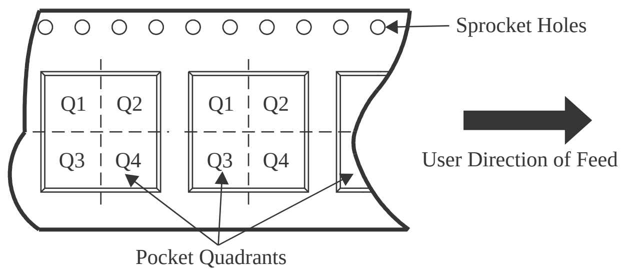
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

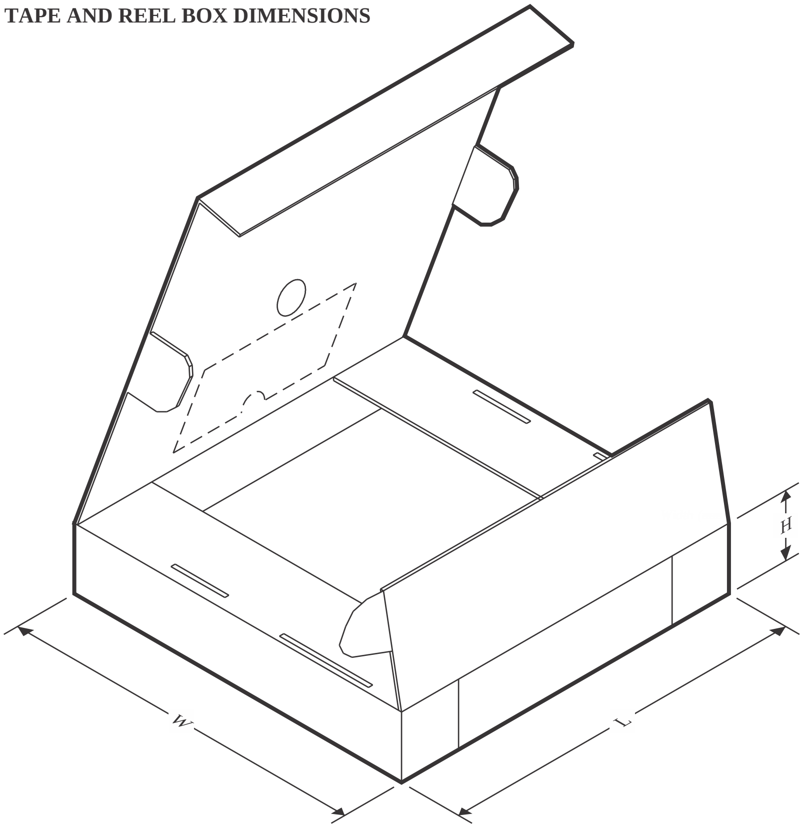
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV10970PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

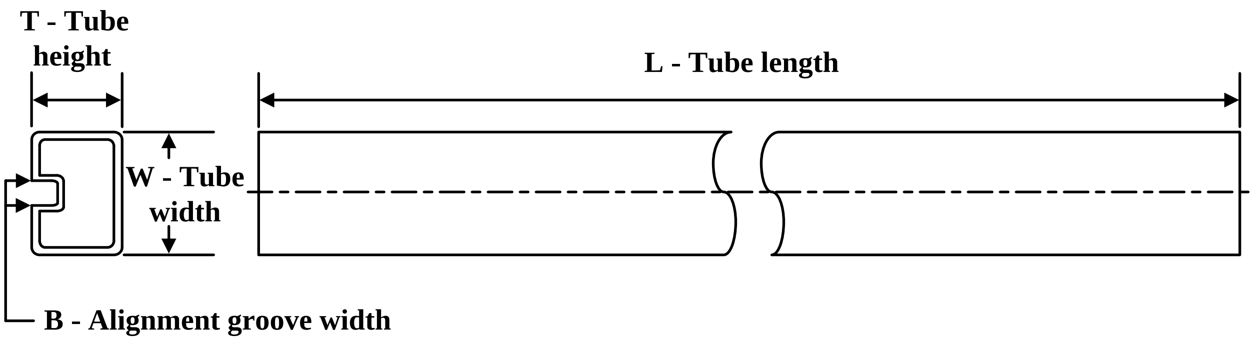
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV10970PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

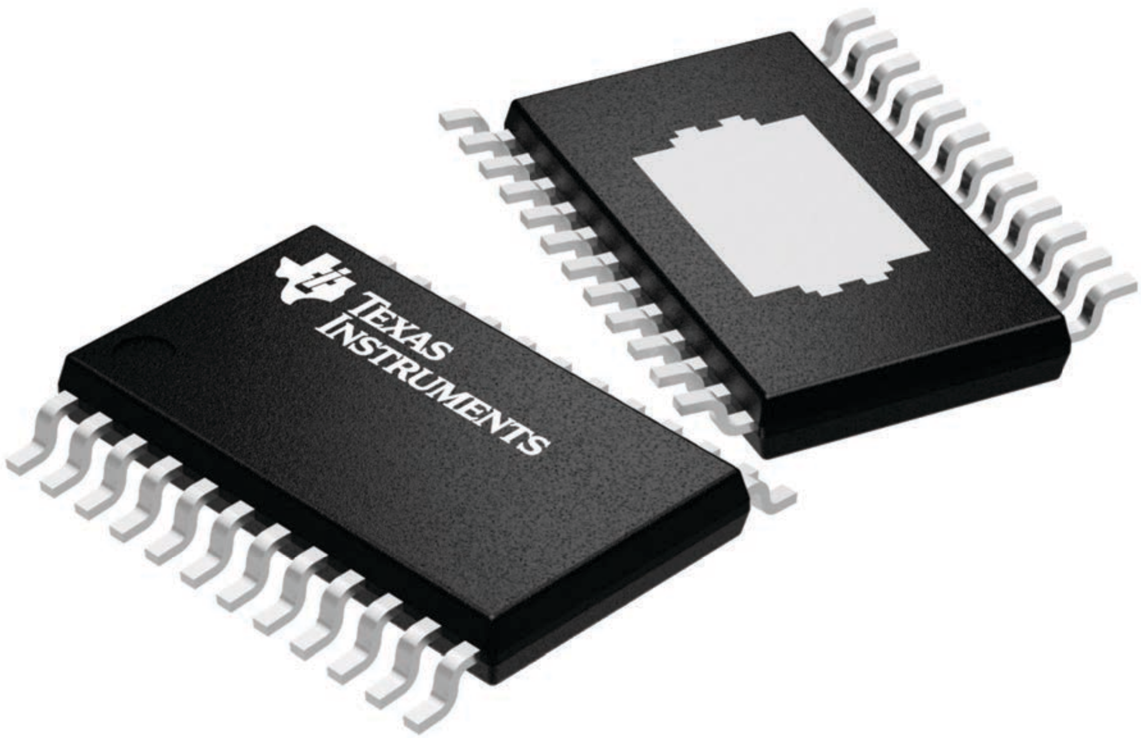
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV10970PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

PWP 24 **PowerPAD™ TSSOP - 1.2 mm max height**

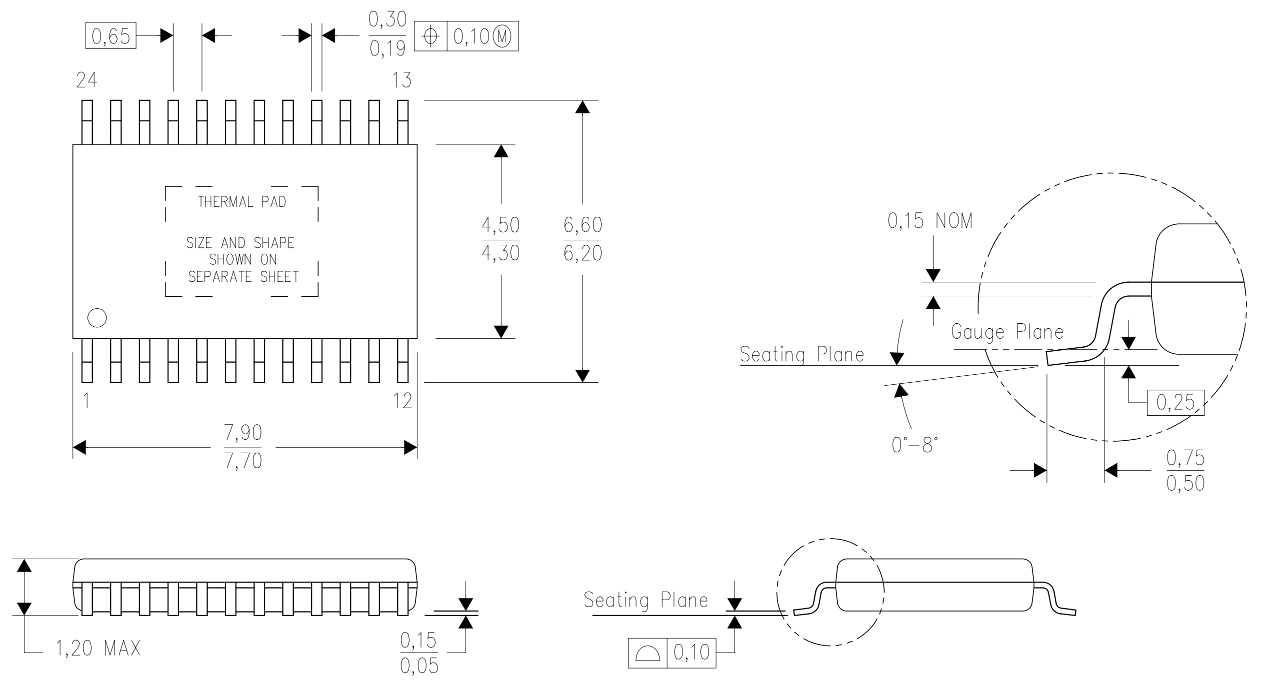
4.4 x 7.6, 0.65 mm pitch PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



4073225–5/I 05/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

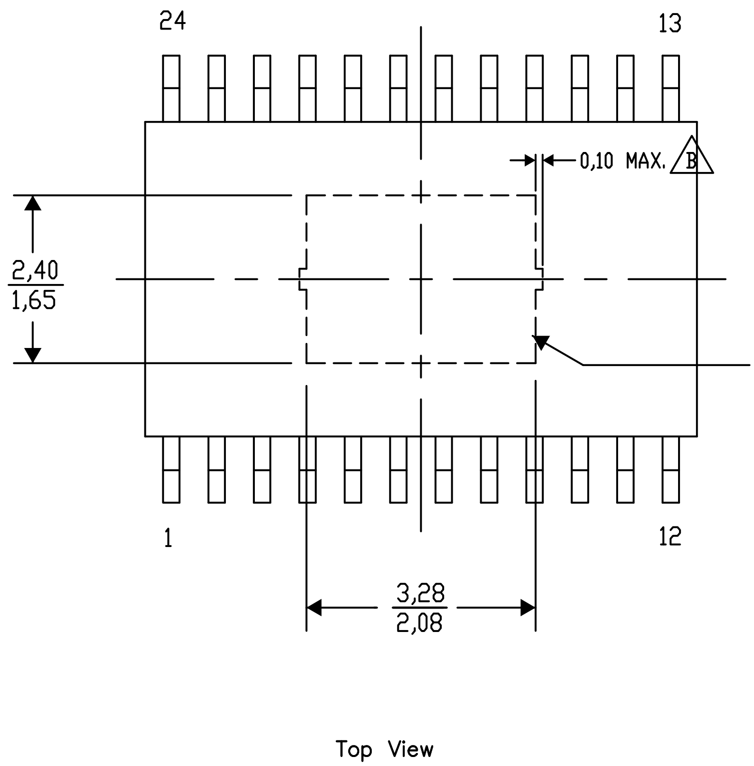
PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



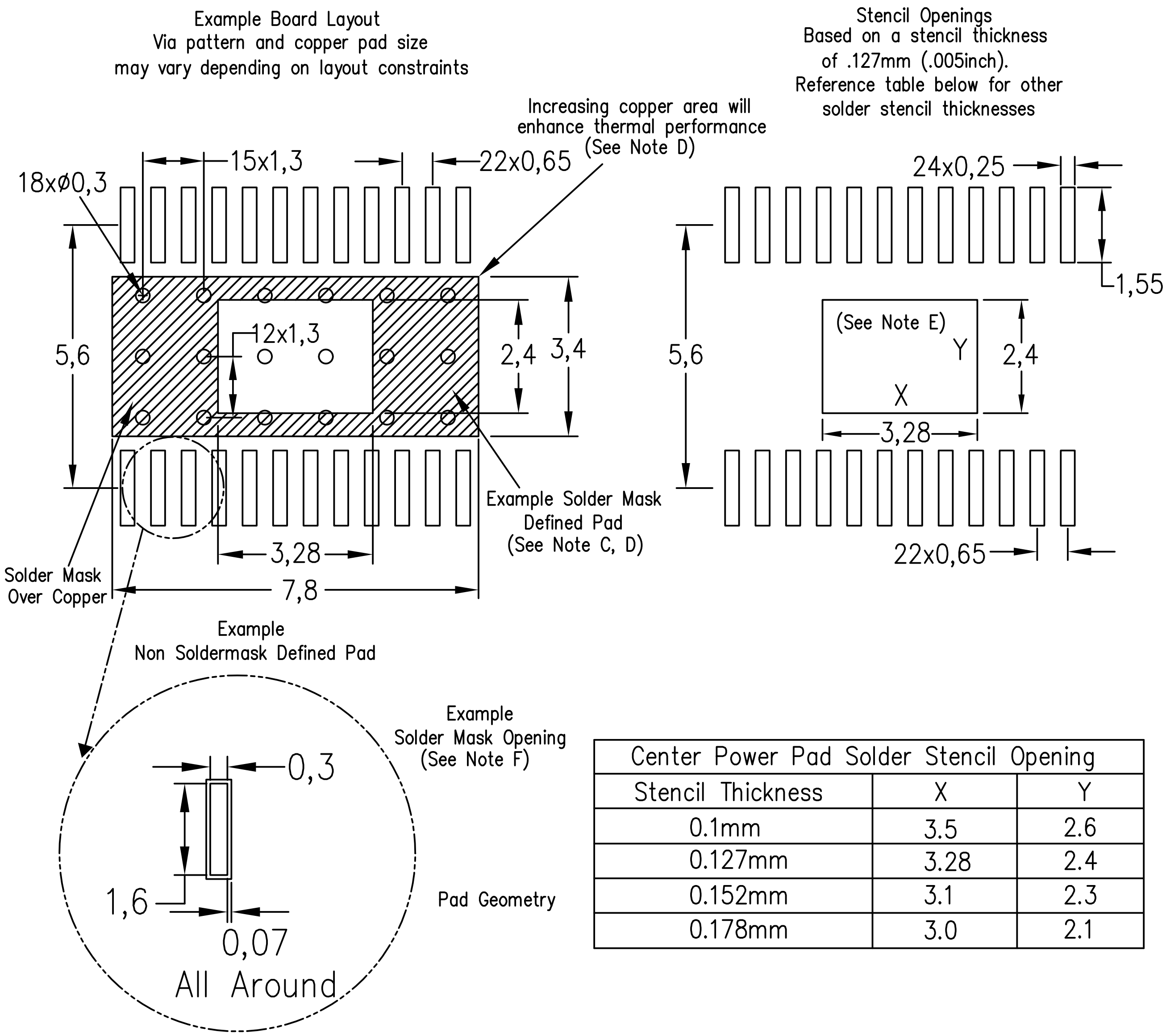
Exposed Thermal Pad Dimensions

4206332-31/AO 01/16

NOTE: A. All linear dimensions are in millimeters
B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.5	2.6
0.127mm	3.28	2.4
0.152mm	3.1	2.3
0.178mm	3.0	2.1

4207609–17/W 09/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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