Application Report
SPRACE0–March 2019

AM437x schematic checklist

Catalog Processors

ABSTRACT

This application report highlights board design recommendations when using the AM437x family of devices. The recommendations are intended to supplement the information provided in the device-specific technical reference manual and data sheet. It is not an all-encompassing list, but rather a succinct reference for board designers that highlights certain caveats and care-abouts related to different use cases.

Contents

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1 Introduction

This application report applies to the AM437x family of devices listed on the AM437x Cortex-A9 Overview. This overview page contains links to TI hardware designs based on AM437x.

For more information, see the device-specific product pages that contain up-to-date information and resources, including application reports and user's guides to facilitate schematic and board design.

2 Recommendations Specific to AM437x

2.1 Unused Signals

Signals on interfaces that are unused can typically be left as no connect. Many of the I/Os have a Pad Control Register, which provides control over the input capabilities of the I/O (RXACTIVE field in each conf_<module>_<pin> register). For more details, see the *Control Module* chapter of the *AM437x and AMIC120 ARM® Cortex™-A9 processors technical reference manual*. Software should disable the receivers I/Os that are no connects (for example, RXACTIVE=0) as soon as possible in initialization. This RXACTIVE field defaults to "input active" for most signals, which means there is a potential for some leakage during powerup of the chip if the input floats to a mid-supply level before the software can initialize the I/O. This should only be a concern if you are attempting to power up the design with a minimum power consumption. Most designs should be able to tolerate this small amount of leakage in each floating I/O until the software has a change to disable it. After disabling the receiver of the I/O, no leakage will occur.

2.2 System Issues

2.2.1 Pinmux

All pinmux settings must be verified using the TI Pinmux tool to ensure valid IOSets have been used. The tool can be downloaded from Pin Mux Tool.

2.2.2 Pullups

- Ensure that all pullups connected to AM437x are pulled up to the correct I/O voltage to avoid any leakage between the I/O rails of the device. Each terminal has an associated voltage used to power its I/O cell. This can be found in the *Ball Characteristics* table in the*AM437x Sitara™ processors data sheet*.
  - For example, if you want to pull up terminal SPI0_CS0 in any mux mode (gpio0_5, i2c1_scl, and so forth), pull up the signal to VDDSHV3.
- nRESETIN_OUT requires an external pullup.

2.2.3 General Debug

Output clocks CLKOUT1 and CLKOUT2 are present on terminals XDMA_EVENT_INTR0 and XDMA_EVENT_INTR1. If these are not used in your design, it is good to have test points on these signals to be able to monitor internal clocks.

2.2.4 Warm Reset

- The WARMRSTn pin (nRESETIN_OUT signal) is an open-drain signal and requires an external pullup.
- If you are using nRESETIN_OUT as a bi-directional reset signal with a push-button, you may need a debounce circuit. Sometimes this is omitted in cases where the button is strictly for development purposes.
- nRESETIN_OUT is undefined during supply ramp. If your external devices require reset to be actively driven low during the entire power-up/down sequence, you can implement a circuit as shown in the *External Buffer for nRESETIN_OUT* figure in the *AM437x and AMIC120 ARM® Cortex™-A9 processors technical reference manual*.

2.2.5 Peripheral Clock Outputs

Several peripheral clocks are required to have RXACTIVE bit set as input because they are used to retime read data returning to the device. A series resistor located as close to the device as possible is recommended to reduce reflections on the clock. For the following peripherals, the associated signals should have a series resistor (33 Ω) in line as close to the processor as possible when used in master mode (AM437x drives the clock).

- GPMC - GPMC_CLK
- MMC - MMC_CLK
- McSPI - SPI_CLK
- QSPI - QSPI_CLK
- McASP (all clocks and frame syncs)

2.2.6 Decoupling

Take note in the data sheet that power rail VDDA1P8V_USB0 requires more decoupling capacitance than VDDA1P8V_USB1. This is because VDDA1P8V_USB0 powers the peripheral PLL in the device as well. For more information, see the *DPLL Power Supply Connectivity* figure in the device-specific data sheet. The VDDA1P8V_USB0 rail should also be filtered similar to other VDDS_PLL_XXX rails on the device.

2.3 Low Power Considerations

If you are designing for low power, here are some tips to help you optimize your design:

- On early prototype boards, it is recommended to include small shunt resistors in the voltage rail paths of each of the following rails of AM437x: VDD_MPU, VDD_CORE, VDDS_DDR, VDDS, VDDSHV1-11. (These are listed in order of priority. So if you cannot add all of them, the most important ones are VDD_MPU, VDD_CORE, and so forth). This will help you measure the power consumption of each rail and potentially pinpoint high power consumption during development. You may also want to add these shunt resistors for other devices power supplies to be able to measure power for key devices. The AM437x EVMs have examples of these shunt resistors.
  - For production, these shunt resistors should be removed from the design (for example, turned into a continuous plane), especially for designs using SmartReflex™.
- Any GPIO can be used as a wakeup source. GPIO0 module (GPIO0_0 to GPIO0_31) signals have lower latency wakeups, so if you have critical timing associated with wakeup, use GPIO0 signals for these wakeup sources.
- For RTC+DDR operation (for example, suspend/resume where the entire AM437x with the exception of RTC is fully powered off, but the DDR remains in self-refresh).
  - The DRAM's power needs to be separate from the AM437x power in order to allow the AM437x to be powered down while keeping the DDR in self refresh. The recommended approach is to use the TPS65218 where DCDC3 powers the DDR3 and is the input to load switch 1 (LS1). LS1 in turn powers the AM437x VDDS_DDR rail, and this power is cut during RTC+DDR mode.
  - During RTC+DDR operation, the DDR3 VREF must be maintained. However, the AM437x DDR_VREF pin cannot tolerate having a reference voltage applied. You correspondingly need to have independent VREF for the processor and the DDR3 IC's. The processor's VREF can be derived from its VDDS_DDR rail (for example, TPS65218 LS1 output). The same could be done for the DDR3 from its rail. In the case of the AM437x EVM, the REFOUT of the TPS51200 was used since it remains powered independent of the EN pin.
  - DDR_RESETn needs a pullup resistor such that the DDR3 is not reset while the processor is powered off. The DDR_RESETn pin is fail-safe, meaning that it can tolerate this voltage despite the fact that VDDS_DDR is not powered.

2.4 Clocking

- If you do not need RTC-only mode and the RTC timer feature, you do not need to include a 32 KHz crystal. The 32 KHz reference can come from the high frequency clock. Leave the RTC_XTALIN/RTC_XTALOUT pins as NC. For more details, see the Section 2.15.
- When using an external crystal, connect VSS_OSC to board ground.
- It is preferable to always have bias and dampening resistors that can help tune the crystal later. For more details, see *Input Clock Requirements* section in the device-specific data sheet.

2.5 General DDR Guidelines

These guidelines are applicable for all DDR designs:

- It is very important to follow the DDR routing guidelines for your DDR type in the device-specific data sheet. These guidelines are very important to ensure a proper DDR design.
- Ensure resistor for DDR_VTP is a high precision resistor as specified in device-specific data sheet. A 49.9 Ω 1% resistor is less expensive than a 50 Ω 2% resistor and can be used for the DDR_VTP pin for cost sensitive designs.
- When using a resistor divider for DDR_VREF, ensure resistors are high precision resistors as specified in the device-specific data sheet.
- Allow for adequate decoupling capacitors on the DDR power rails, both at the AM437x as well as the DDR SDRAM device(s).

- Low power applications implementing DeepSleep or RTC+DDR modes require a split DDR voltage supply to AM437x and the DDR memory. This is so the power to AM437x can be turned off while still maintaining power to the DDR memory. In these cases, DDR_VREF circuits should be separated. That is, two separate voltage dividers: one for AM437x (referenced to VDDS_DDR) and one for the memory (referenced to VDCDC3 from TPS65218).
- All DDR topologies require AM43xx ODT and SDRAM ODT to be enabled by software. CTRL_EMIF_SDRAM_EXT.PHY_RD_LOCAL_ODT register controls the AM43xx side ODT and EMIF4D_SDRAM_CONFIG (bit fields DDR_TERM and DYN_ODT) register bits control the SDRAM ODT side ODT.

2.5.1 DDR Topologies and VTT

Table 1. Supported DDR Topologies

DDR Type	Supported DDR Topology	VTT
LPDDR2 (1)	1x32	NA
LPDDR2 (1)	2x16 balanced T	NA
DDR3L/DDR3	2x16 fly-by	Yes
DDR3L/DDR3	2x16 balanced T (2)	No(2)
DDR3L/DDR3	1x16	Optional (3)
DDR3L/DDR3	4x8 fly-by	Yes
DDR3L/DDR3	2x8 fly-by	Yes
DDR3L/DDR3	2x8 balanced T (2)	No (2)

(1) VTT termination is not necessary for LPDDR2 designs.

(2) For more details, see the *TI design DDR3 reference design without VTT termination using AM437x* [2]. No VTT can be implemented with this topology, however, **careful PCB design along with 3D simulations must be performed to ensure proper signal integrity. Proper high speed design and layout techniques must be employed to ensure stable operation**.

(3) This is a point-to-point topology that typically does not require termination. Be sure to follow the device-specific data sheet layout guidelines.

2.5.2 LPDDR2

DDR_VREF can be derived using a resistor divider with decoupling to both DDR supply and ground. Follow the recommendations as documented in the *LPDDR2 Routing Guidelines* of the device-specific data sheet.

2.5.3 DDR3

- VTT termination: Designs with point-to-point connections between AM437x and DDR3 (that is, one DDR3 device) typically do not need VTT termination. For multiple devices or multi-die packages, see Table 1. When employing VTT, be sure to include a termination regulator to properly terminate the clock/control signals. For proper connection, device-specific data sheet. The information on the links to referenced schematics can be found in the Introduction section of this document. The TPS51200 is recommended.
- Do not connect DDR_RESET or DDR_CKE to VTT termination resistors. These should be connected directly between AM437x and DDR.
- For proper termination voltages, see the device-specific data sheet. Termination for clock signals is VDDS_DDR (along with an AC coupling capacitor), whereas, all other signals need to use VTT for the termination voltage. For details, see the device-specific data sheet.
- If not using VTT, VREF should obtained using a resistor divider (10 KΩ 1%) with capacitive decoupling to ground, and should be used as references for both CA and DQ pins on the memory, as well as the VREF signal on AM437x. Ensure resistor is a high precision (1%) resistor as specified in the device-specific data sheet. When not using VTT, be sure to follow the routing guidelines in the device-specific data sheet.

2.6 MMC

- Include a 33 Ω series resistor on MMCx_CLK (as close to the processor as possible). This signal is used as an input on read transactions and the resistor eliminates possible signal reflections on the signal which can cause false clock transitions.
  - This also requires you to set RXACTIVE=1 in the pinmux configuration for the MMC_CLK signal.
  - When connecting a device (card or eMMC), include 10k pullups on RST#, CMD, and all DAT signals.

NOTE: MMC1 has several pin-out options, but the boot ROM uses the pins gpmc_csn1, gpmc_csn2, and gpmc_ad[11:8] as listed the *Pins Used for MMC1 Boot* table of the *AM437x and AMIC120 ARM® Cortex™-A9 processors technical reference manual*. Furthermore, these pins are not the same as what were used on AM335x, so pay special attention if you are migrating from AM335x.

2.7 I2C

- Pullups on both I2C signals (I2C_DATA and I2C_CLK) should be 4.7K. Ensure the pullups connect to the correct I/O voltage rail. For more information, see the note in Section 2.2.2.
- If you are planning to use TI's software (Processor SDK), be sure to connect I2C0 to the PMIC, as this is the port used for PMIC control.

2.8 Display Subsystem (DSS)

- Connection examples
  - When connecting only 16-bit data to an 18-bit panel (BGR565 to BGR666), connect D0-D4 to B1-B5 on LCD, D5-D10 to G0-G5 on the LCD, and D11-D15 to R1-R5 on LCD. Then connect B0->B5, R0->R5. This allows full color spectrum with some degradation in gradients.
- If migrating from AM335x, the color swapping errata of the AM335x is not applicable on AM437x. You may need to "unswap" your colors if that is the case.

2.9 NAND

Typically, the R/B# signal from the NAND is open drain and connected to the AM437x GPMC_WAIT signal. Be sure to include a 4.7K pullup to the appropriate voltage, depending if the NAND is 1.8 V or 3.3 V.

2.10 Power

- Check the product pages on each device for application notes specific for connecting the PMIC to AM437x. Also check the product data sheet for specific part numbers to be used for the AM437x:
  - TPS65218
  - Discrete Power Solution for AM437x [3]

2.10.1 Power Supply Selection

All AM438x designs require the use of TPS65218 to support tamper module features.

AM437x designs can be powered by either a Power Management IC (PMIC) or a discrete power solution. The requirements for your design may dictate which solution you should use. Table 2 shows certain features that could impact your choice.

Table 2. Power Supply Section

AM437x Feature	PMIC (TPS65218)	Discrete Power Solution
Dynamic Voltage Frequency Scaling (DVFS)	Supported	Not Supported (1)
Fixed OPP Operation for VDD_MPU	Supported	Supported (2)
DeepSleep Low Power mode	Supported	Supported (3)
RTC-only Low Power mode	Supported (4)	Supported (5)
RTC+ DDR Self-Refresh Suspend/Resume Low Power Mode	Supported	Not Supported
Simplified Power Sequencing utilizing only 3.3V I/O for all VDDSHVx domains	Not supported	Supported (6)
Push-button, Integrated Supply supervisors, USB load switch (7)	Supported	Not Supported

(1) TI software offerings fully support MPU DVFS using TPS65218, but do not support any discrete power solutions.

(2) For details, see *Discrete power solution for AM437x*. For Power-on-Hours (POH) implications, as maintaining some high OPP levels may decrease the product lifetime, see the device-specific data sheet.

(3) DeepSleep mode can be achieved with a discrete power solution, but voltage scaling during low power mode is not supported, which will impact power consumption.

(4) Using TPS65218 achieves the lowest power consumption in RTC-only mode as compared to the discrete power solution option, because this solution does not use internal RTC LDO of AM43xx

(5) Requires external power path and 1.8 V regulator from coin cell/battery/super-cap. Higher power for RTC-only mode as compared to TPS65218 solution.

(6) For more details, see *Discrete power solution for AM437x*.

(7) These are specific features of the TPS65218, which would require extra circuitry or devices in a discrete power solution.

2.10.2 General Recommendations

- Ensure current capabilities of DCDC switchers and LDOs meet the maximum demand of all devices that are attached. You can find the maximum current draw of all AM437x I/O rails in the device-specific data sheet. If these rails from the PMIC also power other devices, the maximum current draw of these devices need to be taken into consideration as well.
- Ensure I2C0 is used for communication to PMIC. All TI software distributions (linux SDK) assume the use of this interface with the PMIC.

2.10.3 Simplified Power Sequencing

- Helps to ensure power up/down sequencing between bias voltage and I/O voltage of dual voltage IOs. Also, meets < 2 V differential requirement between bias voltage and I/O voltage of dual voltage IOs.
- Connect VDDS3P3V_IOLDO to the same power supply that is connected to the 3.3 V VDDSHVx terminals.
- Connect CAP_VDDS1P8V_IOLDO to VDDS and VDDS_CLKOUT. A capacitor to ground is also needed in accordance with the device-specific data sheet. CAP_VDDS1P8V_IOLDO is the output of the internal 1.8 V LDO that supplies the bias voltage VDDS for the dual voltage I/Os.
- For more details on implementing discrete power solution for AM437x, see *AM437x Discrete Power Reference Design* [4] and *Discrete Power Solution* [3].
- When not using simplified power sequencing, VDDS3P3V_IOLDO should be grounded, and CAP_VDDS1P8V_IOLDO should be left floating.

NOTE: The simplified power sequencing circuit should not be used when:

- Using the TPS65218 PMIC
- The system requires the RTC feature
- The system uses dual voltage I/Os configured as 1.8 V

2.11 Touchscreen With ADC0

- Recommend adding 0 Ω resistor to VDDA_ADC in case you need to add a filter for noise on the ADC.
- Check that the sampling voltage does not exceed the voltage of reference. Otherwise, it will affect the whole TSC_ADC system. For example, if you add pull up to 3.0 V at the last four channel, this leads to the abnormal work of the whole system, including the first four.

2.12 ADC0/1

Recommend single point connections from VSSA_ADC0 to ground and VSSA_ADC1 to ground as close to the device, as possible.

2.12.1 If ADC0/1 are not Used

Connect all TSC_ADC terminals (VREFP, VREFN, AIN[7:0], VDDA_ADC, and VSSA_ADC) to the same ground as all VSS terminals.

2.13 USB

- For more details, see *High-speed interface layout guidelines* [4].
- The AM437x USB0_ID and USB1_ID terminals should never be connected to any external voltage source. These terminals should be open-circuit when the respective USB port is configured to operate in USB peripheral mode, or should be connected to ground when the respective USB port is configured to operate in USB host mode. Do not connect the ID terminal to a pull down resistor.
- For device operation, USB VBUS decoupling capacitance should be < 10 µF.
- For host operation, USB VBUS decoupling capacitance should be < 120 µF.
- Ensure the VBUS decoupling capacitance is connected close to USB connector.
- USBx_DP and USB_DM should never have any series resistors or capacitance on these signals. These signals should be straight traces to the connector with no stubs or test points.
- Typical connections for a USB peripheral:
  - USBx_DP and USBx_DM are connected directly to the USB connector
  - USBx_CE can be used if supporting charging. This generally would be connected to the enable of a charging source for the battery.
  - USBx_ID can be left unconnected
  - USBx_DRVVBUS is not used and can be left unconnected
  - USBx_VBUS should be connected directly to the VBUS pin on the USB connector
- Typical connections for a USB host:
  - USBx_DP and USBx_DM are connected directly to the USB connector
  - USBx_CE is typically not used and can be left unconnected
  - USDx_ID should be grounded
  - USBx_DRVVBUS should be connected to the enable of the 5 V VBUS power source (see the following note).
  - USBx_VBUS should be connected to the output of the 5 V VBUS power source (see the following note).

NOTE: For instances in which the port is a dedicated USB Host (no DRD, no Device Mode), it is permissible to hard-wire USBx_VBUS to the actual USB port 5V VBUS source and leave USBx_DRVVBUS floating.

- Typical connections for a USB host with USB hub:
  - USBx_DP and USBx_DM are connected directly to the USB hub upstream port. The hub then distributes these signals to the downstream ports as needed.
  - USBx_CE is typically not used and can be left unconnected
  - USDx_ID should be grounded to enable host mode.
  - USBx_DRVVBUS should be connected to the enable of the 5 V VBUS power source.
  - USBx_VBUS should be connected to the output of the 5 V VBUS power source. It is also connected to the VBUS detect on the hub (typically through a resistor divider), which then allows the hub to selectively enable/disable typically through a power switch to each downstream port.

2.13.1 If USB0 or USB1 is not Used

- Connect the respective VDDA1P8V_USB terminal to any 1.8-V power supply and the respective VDDA3P3V_USB terminal to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
  - The OTG_PWRDN and CM_PWRDN bits in the respective USB Control Register (USB_CTRLx) can be used to power down the unused USB PHY to minimize power supply leakage current. These bits default to the powered-up state after the device has been reset. The USB PHY can be powered down by setting both of these bits to "1".
- The respective VBUS, ID, DP, and DM terminals can be connected to ground or left floating.
- The respective CE terminal should be left floating.

2.14 Ethernet

- No series resistors are required for MII signals.
- When choosing boot strapping options for the Ethernet PHY, be sure to exclude support for Gbit, half-duplex. The AM437x Ethernet Controller does not support 1 Gbit, half-duplex. If this is enabled in the Ethernet PHY, a link may be established at 1 Gbit, half-duplex, which prevents Ethernet boot from operating properly (BOOTP will not be transmitted).

2.15 RTC

Table 3 describes what to do with each pin related to RTC functionality. Three use case scenarios are provided:

- RTC-only mode: If you will be using the low power RTC-only mode. This use case allows low power operation of the AM437x by allowing only the RTC power supply to be ON while all the remaining supplies are OFF.
- RTC timer functionality but no RTC-only mode: If you will be using the RTC feature, but do not need RTC-only mode. This use case allows you to use the Real Time clocking features (for example, keeping time), but you do not need to support the low power RTC-only mode.
- RTC feature disabled: If you will never use the RTC features. In this use case, the RTC functions are fully disabled.

Table 3. RTC

Pin	Function	RTC-Only Mode	RTC Timer Functionality but no RTC-only mode	RTC Feature Disabled
VDDS_RTC	1.8 V power supply	Always on RTC 1.8 V power supply output (1)	Any AM437x 1.8 V power supply (3)	Any AM437x 1.8 V power supply (3)
CAP_VDD_RTC	RTC core voltage input/LDO	1 µF decoupling capacitor to VSS	VDD_CORE (4)	VDD_CORE (4)
RTC_KALDO_ENn	Internal LDO enable input	VSS	VDDS_RTC	VDDS_RTC
RTC_PWRONRSTn	RTC power on reset input	1.8 V RTC power on reset (2)	1.8 V PWRONRSTn (5)	VSS
PMIC_POWER_EN	PMIC power enable output	PMIC power enable input	No Connect	No Connect
RTC_WAKEUP	External wakeup input	1.8 V wakeup event signal	VSS	VSS
	Data sheet power up sequencing	Figure 5-4,5,6	Figure 5-4,5,6	Figure 5-7,8

(1) The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC.

(2) If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply.

(3) RTC_PWRONRSTn should be asserted for at least 1 ms for internal RTC LDO output voltage stabilized when internal RTC LDO is enabled.

(4) VDDS_RTC can be ramped independent of other power supplies if the PMIC_POWER_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE.

(5) RTC_PWRONRSTn high level must be 1.8 V. It cannot be 3.3 V. If tied together with PWRONRSTn, both reset inputs high level must be 1.8 V

(6) If using an external LVCMOS input for the 32 kHz clock it must be 1.8 V amplitude since this pin is related to VDDS_RTC.

2.15.1 If RTC Internal Oscillator is not Used

This is the case when:

- A 1.8 V LVCMOS clock source is used rather than a crystal circuit:
  - Connect the clock source to the RTC_XTALIN terminal, leave the RTC_XTALOUT terminal open-circuit, and connect VSS_RTC to VSS.
- The RTC is not used, see the Section 2.15.

2.16 XDMA Pins

This section is discussing the following pins:

- xdma_event_intr0
- xdma_event_intr1
- xdma_event_intr2
- xdma_event_intr3
- xdma_event_intr4
- xdma_event_intr5
- xdma_event_intr6
- xdma_event_intr7
- xdma_event_intr8
- These signals are all active high inputs. The polarity is fixed, so any adjustments must be made at the board level, for example, inverter, and so forth.
- All nine signals are connected to the Cortex A9 interrupt controller.
- Only xdma_event_intr[5:0] are connected to the EDMA. The signals xdma_event_intr[8:6] cannot be used to generate an EDMA event.
- Note that xdma_event_intr2 (ball R25) has an internal pullup active by default after reset. Since these are active high signals, caution should be exercised if using this specific pin.
  - One option might be to use another pin for xdma_event_intr2 since it is muxed to A16 and G24 as well.
  - Another option is to use an external pulldown to override the internal pullup.

3 References

1. Texas Instruments: *DDR3 reference design without VTT termination using AM437x*
2. Texas Instruments: *Discrete power solution for AM437x*
3. Texas Instruments: *AM437x discrete power reference design*
4. Texas Instruments: *High-speed interface layout guidelines*
5. Texas Instruments: *AM437x and AMIC120 ARM® Cortex™-A9 processors technical reference manual*
6. Texas Instruments: *AM437x Sitara™ processors data sheet*

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