Migrating from TMS320C6211B/C6711/C6711B and C6713 to TMS320C6713B

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ABSTRACT

This document describes issues of interest related to migration from the Texas Instruments TMS320C6211B/C6711/C6711B GFN package and TMS320C6713 GDP package to the TMS320C6713B digital signal processor (DSP) GDP package. The objective of this document is to indicate differences between these devices. Functions that are identical between these devices are not included. For detailed information on the specific functions of any of these devices, refer to the device data sheets. Migration issues from C6211B/C6711/C6711B and C6713 to C6713B are indicated with the following symbols, which are included at the beginning of each section:

[H] Means hardware modification is required.

[S] Means system/software modification is required.

[D] Means the C6211B/C6711/C6711B, C6713 and C6713B are different (usually due to added features on the C6713B), but no modification is necessary for migration (that is, the devices are different but compatible).

With detailed description in this document, migration and development of C6713B systems can be accomplished with ease. For information about migrating from C6211B/C6711/C6711B to C6713B see section 1 for details. A summary of differences between C6713 and C6713B is also presented for C6713 and C6713B system migration; see section 2 for details.

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List of Tables

1 Migrating From C6211/C6711/C6711B to C6713B

The following sections detail differences you must address when migrating from the C6211B/C6711/C6711B devices to C6713B. In addition, hardware and software workarounds may no longer be needed in this newer silicon revision, as described in the device-specific silicon errata.

1.1 Core Power [H]

The core voltage of C6713B is now either 1.20V with 5% or 1.26 V with 5% tolerance; down from 1.8 V on the C6211B/C6711/C6711B and 1.9 V on the C6711. The power supply circuit on the board needs to be modified to support this.

1.2 Package and Pins [H, S]

The GDP package of the C6713B has 272 pins. The GDP package is very similar to the C6211B/C6711/C6711B's 256-pin GFN package, plus the addition of 16 ground thermal pins in the middle. The mechanics of the GDP package is also slightly different. Refer to Appendix A for C6713B-GDP mechanical specifications.

1.2.1 CLKOUT1 Pin no Longer Exists [H, S]

The CLKOUT1 pin does not exist on the C6713B. The D7 pin that is the CLKOUT1 pin on the C6211B/C6711/C6711B now becomes a reserved, no-connect pin on the C6713B.

1.2.2 Connect Pin Y20 to GROUND [H]

This pin is a reserved pin on the C6211B/C6711/C6711B. This pin must be connected to GROUND on the C6713B.

1.2.3 Pullup CLKS1/SCL1 (E1) and DR1/SDA1 (M2) Pins [H]

The McBSP1/I2C1 pins E1 and M2 on the C6713B do not have internal pullup/down resistors. These pins must be externally pulled up.

1.2.4 EMU2 Pin Location Change [H]

The EMU2 pin location is changed from D10 (now CLKOUT3) to D3 (was reserved, no-connect). This EMU2 pin is unused, so it should not pose any implication.

1.2.5 Pullup Pins N1 and N2 [H]

Pin N1 is a DV_{DD} pin on the C6211B/C6711/C6711B, and pin N2 is a reserved, no-connect pin. On the C6713B, these are I2C0 pins and must be pulled up with external resistors.

1.2.6 Pulldown Pin D12 [H]

Pin D12 is a reserved, no-connect pin on the C6211B/C6711/C6711B. On the C6713B, this reserved pin must be pulled down with an external resistor for proper device operation.

1.2.7 Pins B11 and A12 are Now Reserved [H]

Pins B11 and A12 are connected to Vss and CVDD, respectively, on C6211B/C6711/C6711B. These pins are reserved on C6713B and are recommended to remain connected to VSS and CVDD on the new 6713B designs. It is recommended for users who will design a new board to connect those pins to CVDD/VSS on new 6713B designs. However, old designs remain unchanged if the pins are left disconnected.

1.2.8 Internal/External Pull Resistors [H]

For C6713B, the recommended external pullup and pulldown resistors used to oppose the internal pull should not be greater than 4.4 kΩ and 2.0 kΩ, respectively. This is compatible with the recommended C6211B/C6711/C6711B external pullup and pulldown resistor values (1 kΩ). However, the internal pullup (IPU) and internal pulldown (IPD) value for C6713B is now 18 kΩ (approximate) and 13 kΩ (approximate), respectively. For C6211B/C6711/C6711B, both the IPU and IPD are 30 kΩ.

1.2.9 No Internal Pullup Resistor on \RESET (C6713B Only) [H]

C6211B/C6711/C6711B have an internal pullup resistor on the \RESET pin. C6713B does not have an internal pull resistor. New designs using C6713B should incorporate either a voltage supervisor with an active drive on this pin, or should include an external pullup resistor.

1.3 PLL and PLL Controller [H, S, D]

The PLL controller is a new peripheral on C6713B. In addition to a new software programmable PLL, it also includes a reset controller, plus a set of software programmable pre-scalers and post-dividers. See the *TMS320C6000 PLL Controller Peripheral Reference Guide* (SPRU233) for details on this peripheral. Also see the C6713B data sheet for the PLL circuit and other device-specific PLL information.

1.3.1 In PLL Mode, External PLL Components/Circuit Must be Modified [H, PLL Mode Only]

The new PLL on the C6713B requires a new external PLL circuit. Pin C5 is now the analog 3.3-V power pin (PLLHV) for the C6713B PLL. The PLL pins on the C6211B/C6711/C6711B, which are A4, C6, and B5 now, become CV_{DD}, GROUND, and Reserved (no-connect), respectively. For details on the external PLL circuit, see the device-specific data sheet.

In bypass mode, the PLL circuit is still required. However, regardless of bypass or PLL mode, the PLL controller peripheral must be programmed to generate desired clocks.

1.3.2 CLKMODE0 Pin Must Always be Pulled High [H, S]

The CLKMODE0 pin definition is now changed. On the C6211B/C6711/C6711B, the CLKMODE0 selects between x1 and x4 PLL mode. On the C6713B, the CLKMODE0 pin must always be pulled high (default). Therefore, if the existing board is in PLL bypass mode (CLKMODE=0), the pulldown resistor must be removed to set CLKMODE=1 (default due to internal pullup resistor). The PLL Controller registers must then be programmed in software to the desired PLL mode and clock frequencies.

1.3.3 Reset Timing [S, D]

The PLL controller on the C6713B has a reset controller logic that internally lengthens the reset signal, to ensure that input clocks are stable before internal reset is released. See the Reset Timing section of the data sheet, *TMS320C6711, TMS320C6711B, TMS320C6711C Floating-Point Digital Signal Processors* (SPRS088) and the *TMS320C6000 DSP Phase-Locked Loop (PLL) Controller Peripheral Reference Guide* (SPRU233). The following is affected by the difference in C6713B reset timing:

- Pin states during reset [S]

  During the reset sequence, the states of clocks and other pins are slightly different from those of the C6211B/C6711/C6711B. On the C6211B/C6711/C6711B devices, for instance, ECLKOUT will continue to clock as long as ECLKIN is provided. However, on C6713B, ECLKOUT is inactive during reset.

- HPI boot mode [S]

  If the HPI boot mode is enabled (HD[4:3] = 00b), the host must wait until reset is released internally before starting boot load. Furthermore, the C6713B device comes up in bypass mode by default out of reset; therefore, the clock rate is initially slow. When migrating from an existing system, the host needs to take into account that the device is initially in bypass mode. It may be necessary for the host to slow down the HPI interface, to insure that the slower DSP can recognize the host commands.

- EMIF boot mode [D]

  If the EMIF boot mode is employed, then no change is needed. The EMIF boot will start automatically after the internal reset signal is released.

1.4 New EKSRC and EKEN Register Bits [S, D]

The EKSRC bit in the DEVCFG register selects EMIF input clock source between the internal clock, SYSCLK3 (default), and ECLKIN.

- EKSRC = 0: EMIF input clock is SYSCLK3 (default).
- EKSRC = 1: EMIF input clock is ECLKIN.

The SYSCLK3 frequency is software-programmable via PLLDIV3 register in the PLL controller peripheral.

For existing systems using ECLKIN, EKSRC should be set to 1 in order to use ECLKIN. If SYSCLK3 (default) is desired, PLLDIV3 must be set to the desired clock rate prior to any EMIF accesses.

The ECLKOUT pin on the C6211B/C6711/C6711B is always running as long as the EMIF input clock source ECLKIN is supplied. On C6713B, the EKEN bit is added to the EMIF global control register to enable or disable ECLKOUT. The EKEN bit functions as follows:

- EKEN=0: ECLKOUT held low
- EKEN=1: ECLKOUT enabled to clock (default)

1.5 New General-Purpose Input/Output (GPIO) Module With 5 Pins (GP[7:4, 2]) [S, D]

In order to use these pins as GPIO pins, the GPxEN bits in the GPIO Enable Register (GPEN) and the GPxDIR bits in the GPIO Direction Register (GPDIR) must be properly configured, where x is 7, 6, 5, 4, or 2.

- GPxEN = 1: GPx pin enabled
- GPxDIR = 0: GPx pin is an input
- GPxDIR = 1: GPx pin is an output

1.5.1 EXT_INT4−7 are Now GP4−7 [S, D]

External interrupts 4−7 now go through the GPIO module. When these pins are used as interrupt inputs, the GP4−7 must be configured to be inputs (in GPDIR register) and enabled (in GPEN register), in addition to enabling the interrupts in the Interrupt Enable Register (IER).

Furthermore, EXT_INT4-7 timing requirements for C6211B/C6711/C6711B for high/low pulse width is 2P, where P is the input clock period in nanoseconds. Since the external interrupts for 6713B go through the GPIO module, the timing requirements for EXT_INT4-7 are now 4P nanoseconds for the high/low pulse width. See the device-specific datasheet for more details.

1.5.2 GP2 Pin is Muxed With CLKOUT2 Pin [D]

The GP2 pin is multiplexed with the CLKOUT2 pin; default is CLKOUT2. In order to use this pin as GPIO pin (GP2), the GPxEN bits in the GPEN register and the GPxDIR bits in the GPDIR register must be properly configured.

1.6 Power-Down Modes [H, S]

The power-down modes, PD2 and PD3, operation differs for the C6713B device in bypass mode. When bypassing the PLL, the device still receives clocks from the external clock input. PD2 and PD3 is only effective in PLL mode. See the *TMS320C6713, TMS320C6713B Digital Signal Processor Silicon Errata (Silicon Revision 2.0, 1.1)* (SPRZ191) for more details.

1.7 Boundary Scan Mode [H]

For the Boundary Scan mode, the $\overline{\text{RESET}}$ pin needs to be driven low for the C6713B device. This is not a requirement for C6211B/C6711/C6711B.

1.8 AC Timings [H, S]

To view the differences in AC timings, see the device-specific data sheet.

1.9 I/O Buffers are Different [H]

The I/O buffers are different on the C6713B device. Systems migrating should use the C6713B IBIS models to run board level signal simulations.

1.10 Package Thermal Resistance Characteristics [H]

C6713B has different package thermal resistance characteristics. See the *TMS320C6713, TMS320C6713B Floating-Point Digital Signal Processor* data sheet (SPRS186) for more details.

1.11 Pin Migration Summary

Table 1 summarizes all the pin-related modifications needed when migrating from C6211B/C6711/C6711B to C6713B.

Table 1. Pin Migration Summary

Pin	C6211B/C6711/C6711B	C6713B
D7	CLKOUT1	Reserved
Y20	Reserved, no-connect	GROUND
C5	DV_{DD}	PLLHV. Analog 3.3-V power for PLL.
A4	PLL analog Vcc connection	CV_{DD}
C6	PLL analog GND connection	GROUND
B5	PLL low-pass filter connection to external components	Reserved, no-connect
E1 and M2	Have IPD, IPU; respectively	No IPU/IPD. Must be externally pulled up.
D10	EMU2	CLKOUT3
D3	Reserved, no-connect	EMU2
N1 N2	DV_{DD} Reserved, no-connect	I2C0 pins. Must be externally pulled up.
D12	Reserved, no-connect	Must be externally pulled down.
B11†	V_{SS}	Reserved − V_{SS}
A12†	CV_{DD}	Reserved − CV_{DD}

NOTE: Do not oppose the IPU/IPD settings of non-configuration HD pins (HD[15:9, 7:5, 2:0])

† On C6713B designs that currently have these pins unconnected may remain unconnected, but are encouraged to be connected to [Vss/CVDD] on new designs.

1.12 New/Enhanced Peripherals [D]

The C6713B DSP features new or enhanced peripherals over the C6211B/C6711/C6711B. These include:

- **Larger L2 SRAM**

  The SRAM size of the L2 memory on C6713B DSP has been increased by 192K bytes, bringing the total L2 size to 256K bytes. Of 256K bytes total, 64K bytes are programmable to be L2 cache or SRAM, while the other 192K bytes are SRAM only.

- **PLL and PLL Controller**

  The multiplier factor of the PLL on C6713B DSP is programmable to be x4, x5, up to x25. In addition to the new PLL, the C6713B also features the PLL Controller peripheral. The PLL Controller is a flexible, programmable clock generator, capable of generating DSP core clock, CLKOUT3, EMIF and other peripheral clocks. See section 1.3 for migration issues regarding this peripheral.

- **General-Purpose Input/Output (GPIO)**

  The C6713B has a dedicated GPIO module consisting of 16 pins. The GPIO module can be programmed to generate CPU interrupts and EDMA events.

- **Multichannel Audio Serial Port (McASP)**

  The C6713B has two McASP modules. Each of the McASPs features two independent clock zones (for transmit and receive) and 8 data pins. The McASP supports data interface in Time-Division Multiplexed (TDM) format, burst format, and Digital Audio Interface Transmit (DIT) format, where the bit stream is encoded for S/PDIF, AES-3, IEC-60958 transmissions.

- **Inter-Integrated Circuit (I2C) Port**

  The C6713B has two I2C ports. Each of them is capable of transmitting and receiving in both master and slave interfaces.

Note that some peripheral pins are multiplexed with other pins. This means that some peripherals cannot be used with others. See the device data sheet for detailed information on available device configurations.

See also *How to Begin Development Today with The TMS320C6713 Floating-Point DSP* (SPRA809) for details on differences between the C6711B and the C6713 DSPs.

2 Migrating From C6713 to C6713B

The following sections detail differences you must address when migrating from the C6713 device to C6713B.

2.1 C6713B Versus C6713 New Features [D]

In addition to the new/enhanced peripherals listed in section 1.12, the C6713B DSP features new enhancements over the C6713 device. These features are compatible with existing C6713 designs.

- P-bit in Cache Configuration (CCFG) register

  The C6713B device includes an enhancement to the cache configuration (CCFG) register. A ”P” bit (CCFG.31) allows the programmer to select the priority of accesses to L2 memory originating from the transfer crossbar (TC) over accesses originating from the L1D memory system. While the EDMA normally has no issue accessing L2 memory due to the high hit rates on the L1D memory system, there are pathological cases where certain CPU behavior could block the EDMA from accessing the L2 memory for long enough to cause a missed deadline when transferring data to a peripheral such as the McASP or McBSP. This can be avoided by setting the P bit to ”1” because the EDMA will assume a higher priority than the L1D memory system when accessing L2 memory. For more details on this feature, see the *TMS320C6713, TMS320C6713B Floating-Point Digital Signal Processor* data sheet (SPRS186) and the *TMS320C6713, TMS320C6713B Digital Signal Processor Silicon Errata (Silicon Revision 2.0, 1.1)* (SPRZ191).

- EMIF Big Endian correctness

  The C6713B device allows the flexibility to change the EMIF data placement on the EMIF bus. When using the default setting of pin HD12 (pulled high) for the C6713B, the EMIF will present 8-bit or 16-bit data on the ED[7:0] side of the bus if using Little Endian mode and to the ED[31:24] side of the bus if using Big Endian mode. When pin HD12 is pulled low for the C6713B, the EMIF will present 8-bit or 16-bit data on the ED[7:0] side of the bus, regardless of the endianess. For more details on this enhancement, see the *TMS320C6713, TMS320C6713B Floating-Point Digital Signal Processor* data sheet (SPRS186).

2.2 Systems Migrating from C6713 to C6713B [H]

C6713 and C6713B are pin, package and software compatible. For more information on these devices, please refer to the *TMS320C6713, TMS320C6713B Floating-Point Digital Signal Processor* data sheet (SPRS186).

- System modifications

  Possible system modifications include ac timing differences for McBSP (SPI mode and data delay 0 mode only) and CLKOUT3, as well as the internal pull up resistor removal on the C6713B \RESET pin. C6713B designs should incorporate either a voltage supervisor, which drives when in the inactive state (\RESET = 1), or should include an external pull up resistor on the \RESET pin.

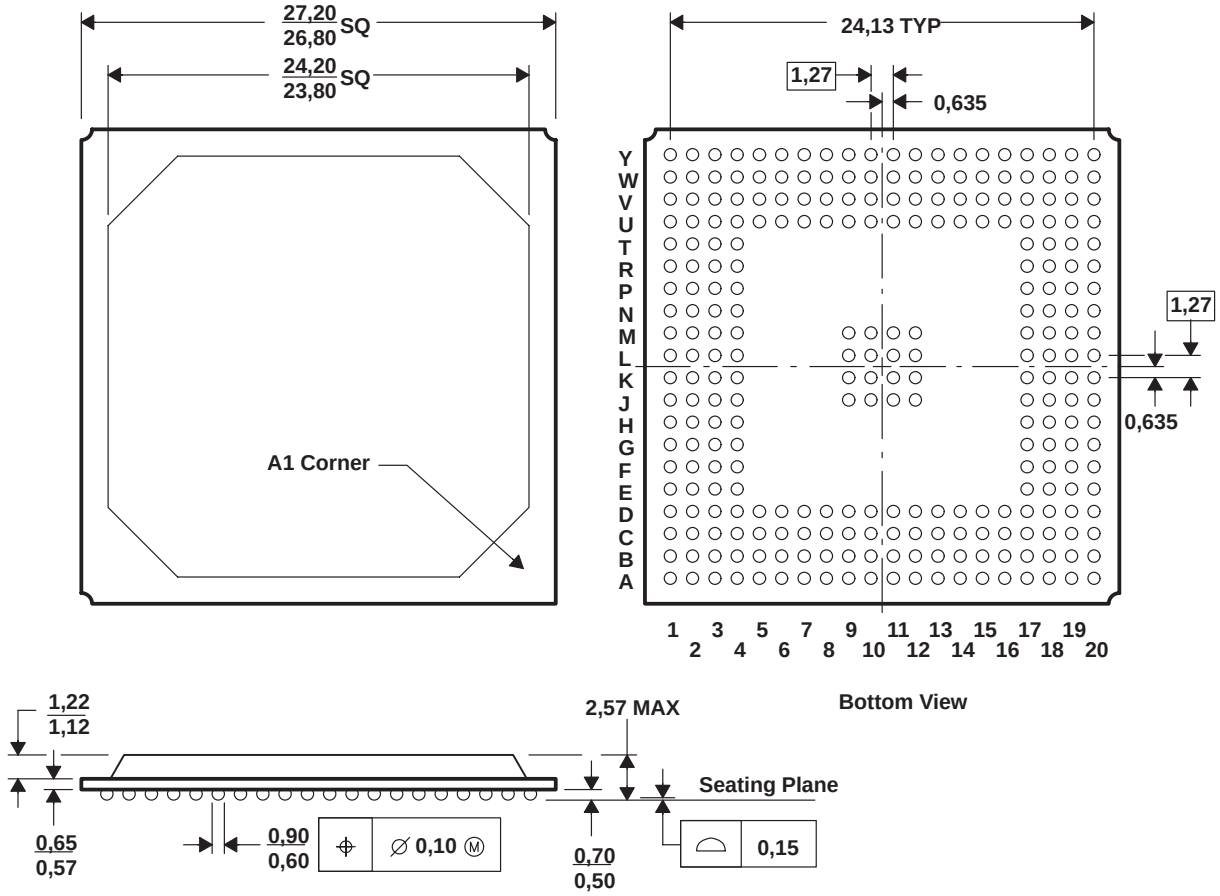
- CLKOUT3 buffers are different

  The CLKOUT3 buffer is different on the C6713B device. Systems migrating should use the C6713B IBIS models to run board level signal simulations with the updated CLKOUT3 buffer information.

3 References

1. *TMS320C6711, TMS320C6711B, TMS320C6711C, TMS320C6711D Floating-Point Digital Signal Processors* data sheet (SPRS088).
2. *TMS320C6211, TMS320C6211B Fixed-Point Digital Signal Processors* data sheet (SPRS073).
3. *TMS320C6713, TMS320C6713B Floating-Point Digital Signal Processor* data sheet (SPRS186).
4. *TMS320C6711/C6711B/C6711C/C6711D DSPs Silicon Errata (Revisions 1.0, 1.1, 1.2, 1.3, 2.0, 2.1)* (SPRZ173).
5. *TMS320C6713, TMS320C6713B Digital Signal Processor Silicon Errata (Silicon Revision 2.0, 1.1)* (SPRZ191)
6. *How to Begin Development Today With the TMS320C6713 Floating-Point DSP* (SPRA809).
7. *TMS320C6000 DSP Phase-Locked Loop (PLL) Controller Peripheral Reference Guide* (SPRU233).
8. *TMS320C6000 DSP Multichannel Audio Serial Port (McASP) Reference Guide* (SPRU041).
9. *TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU175).

Appendix A GDP (S-PBGA-N272) Plastic Ball Grid Array



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-151

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