SCANSTA101,SCANSTA111,SCANSTA112, SCANSTA476

JTAG Advanced Capabilities and System Design

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JTAG Advanced Capabilities and System Design

— By David Morrill, Principal Applications Engineer

The JTAG bus, originally intended for board-level manufacturing test, has evolved into a multipurpose bus also used for In-System Programming (ISP) of FPGAs, FLASH, and processor emulation. This article's intent is to provide a brief overview of JTAG. Several system-level design options will be proposed, from the simplest board-level JTAG chain through a complex embedded multidrop system. Finally, an appendix is included that contains some useful definitions.

Overview: What is JTAG?

The Joint Test Action Group (JTAG) is an industry group formed in 1985 to develop a method to test populated circuit boards after manufacture. The group's work resulted in the IEEE 1149.1 standard entitled Standard Test Access Port and Boundary-Scan Architecture. The terms 1149.1, JTAG, "dot 1", and SCAN all refer to the same thing, the IEEE 1149.1 Standard for Boundary Scan Test.

What is JTAG and what does it do?

1) It is a serial test bus.
2) It adds a Test Access Port (TAP) consisting of four pins to an IC (five with optional RESET) as shown in ***Figure 1***.
   - TDI (Test Data In)
   - TDO (Test Data Out)
   - TCK (Test Clock)
   - TMS (Test Mode Select)
   - $\overline{\text{TRST}}$ (Test Reset)

JTAG provides access to interconnected digital cells on an IC:

1) with a method of access for test and diagnostics and the
   - ability to do factory and remote testing and diagnostics,
   - ability to perform software debug, and
   - reduce "No-Fault-Found" problems
2) with a method for in-circuit upgrades and the
   - ability to remotely perform system-wide firmware upgrades

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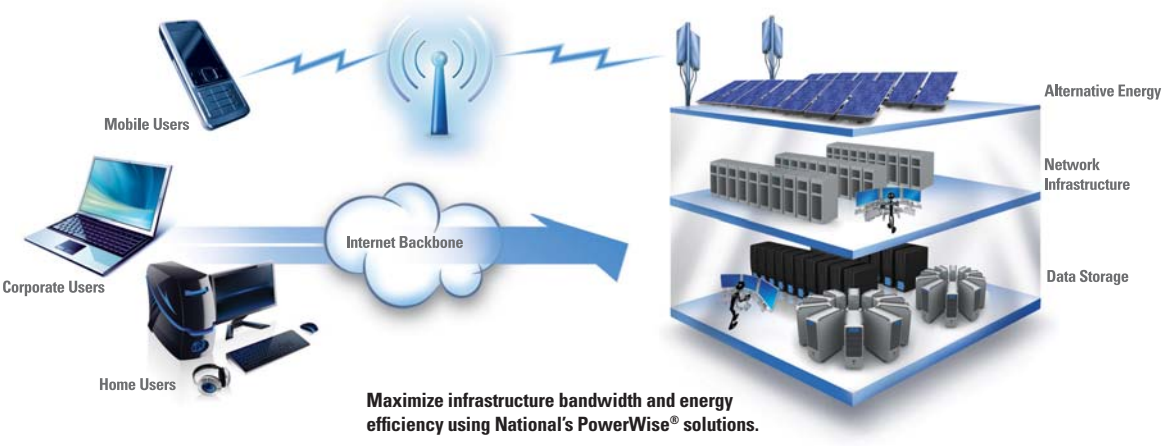

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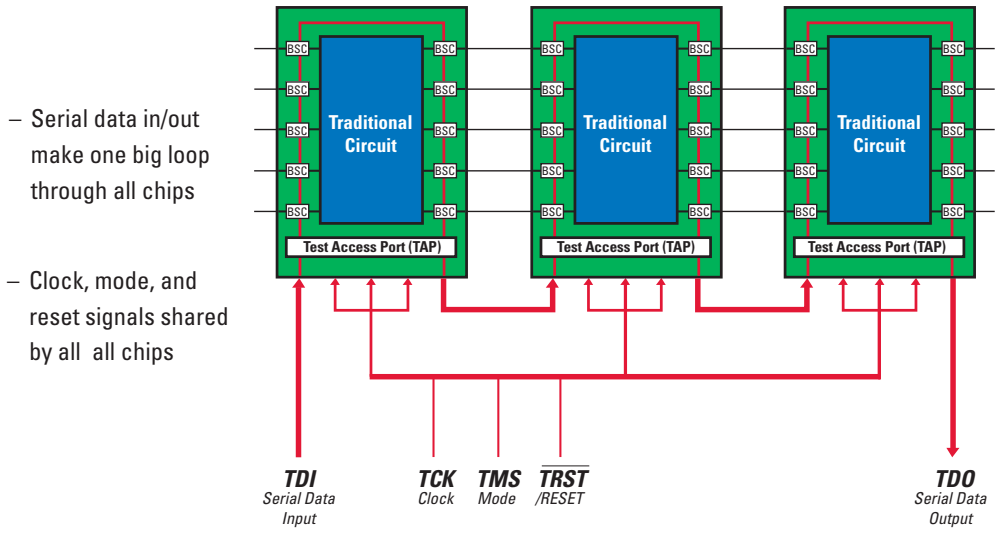

Figure 1. Basic JTAG Chain Interconnect

All chips are driven by one TMS, TCLK, and $\overline{\text{TRST}}$ signal from the test device. The TDI and TDO signals are daisy-chained together serially as shown in ***Figure 1*** and below:

Test device → Chip 1 TDI
Chip 1 TDO → Chip 2 TDI
Chip 2 TDO → Chip 3 TDI
…
Chip n-1 TDO → Chip n TDI
Chip n TDO → Test device

Basic JTAG Application

Figure 2 shows a basic JTAG chain consisting of JTAG-enabled devices connected in series through TDI and TDO. TCK, TMS, and $\overline{\text{TRST}}$ are common to each device and are not shown. This chain is very simple and relatively easy to implement, but it is slow and does not provide focused testing. For example to access ASIC2, data must be serially shifted through the backplane interface, microprocessor (µP), ASIC2, ASIC1, FPGA, and the daughter card. In this simple example five devices can be seen on a chain. On a typical card, there can be dozens of devices. FLASH can also be programmed via the JTAG chain.

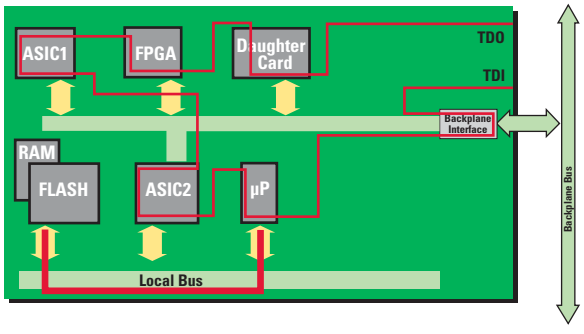

Figure 2. Basic Board with JTAG

Figure 3 shows how a JTAG chain can be partitioned to increase speed, access, and flexibility. The SCANSTA111/112 is an addressable JTAG port (also known as "bridge") that allows the JTAG bus to be partitioned onto local scan ports (LSP) to reduce the size of the individual JTAG chains. This means the JTAG master can select one or more of these chains via LSP for focused testing or, in the case of FPGAs and FLASH memory, (re)programming. This is necessary for multi-board testing and highly desirable for FPGA programming. Breaking one long JTAG chain into smaller chains also can improve access/test time significantly. The LSPs can

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be accessed in parallel via an address mask for bulk programming/testing. The SCANSTA111 can be used for up to three partitions; the SCANSTA112 up to seven. The devices also can be cascaded; for example, a STA112 connected to a LSP of another STA112.

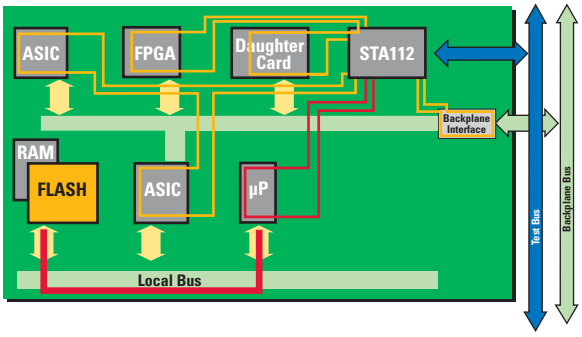


Figure 3. Board with Partitioned JTAG Chains using SCANSTA112

Embedded JTAG Master

Assuming board-level or system-level JTAG test capability exists, the next level of capability is to develop an embedded JTAG system. Embedded JTAG provides a means to implement self diagnostics and reconfiguration, system-level test, and remote test/upgrades. This can be done with the on-host processor. However, this process is not automated and requires custom and costly development effort. This is a tedious task that is difficult to both debug and ensure full test coverage.

In contrast, the SCANSTA101-embedded JTAG test master enables system designers to embed their test vectors easily from their automatic test pattern generator (ATPG) tools into the production system. National Semiconductor provides a free SCANEASE conversion utility to port the ATPG vectors directly to the SCANSTA101. As shown in ***Figure 4***, the SCANSTA101 interfaces between the host processor and the serial JTAG bus. It offloads this work from the host processor and drives the JTAG bus with test vectors.

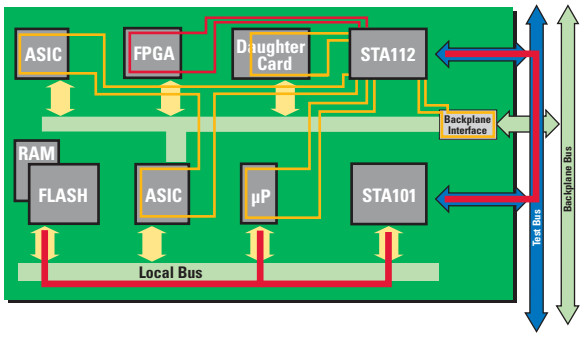


Figure 4. Board with SCANSTA101-Embedded Master and Partitioned JTAG Chains using SCANSTA112

Multidrop JTAG

Next, the multidrop system will be discussed. This multidrop system consists of a backplane and test bus with several add-in cards as shown in ***Figure 5***. The cards contain partitioned chains and, if needed, a STA101 master. A configuration of this type allows access and testing of the interconnect, ASICs, FLASH/RAM (via the local bus), FPGAs, daughter cards, the backplane interface, and the local buses of all boards on the backplane bus. The STA111/112's address masks allow all boards to be accessed in parallel if desired, which greatly increases speed. A STA101 could be added to the second board for redundancy.

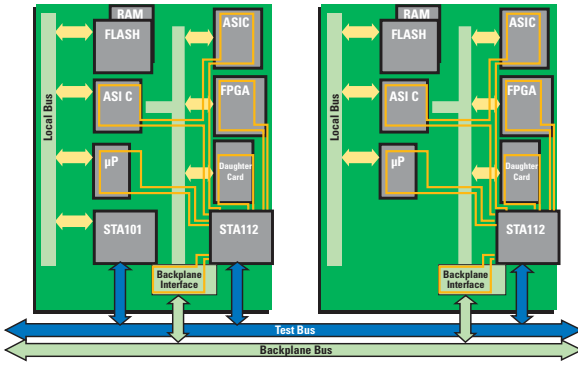


Figure 5. Multidrop System with SCANSTA101-Embedded Master and Partitioned JTAG Chains using SCANSTA112

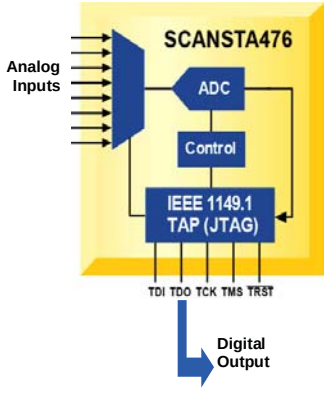


Figure 6. Block Diagram of SCANSTA476

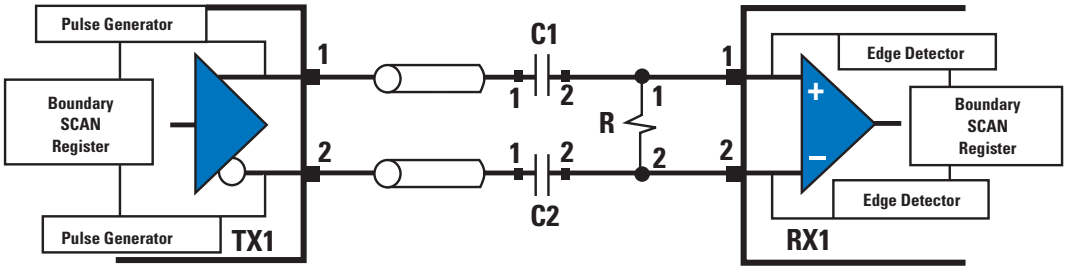
Analog Monitoring via JTAG

It would be useful to have voltage measurement capability during board/system testing through IEEE1149.1. For example, it may be necessary to measure critical power supplies during development and factory test. Access to analog nodes that don't have physical access, or even require online voltage testing for health monitoring and prognostics may be required. The SCANSTA476 is an analog voltage monitor that has eight inputs that are fed to an analog-to-digital converter (ADC). The digital result is stored in a JTAG register, all accessible via a fully 1149.1-compliant digital TAP. ***Figure 6*** shows a block diagram of the SCANSTA476. Having the ability to add voltage measurement capability to a system through a JTAG chain is a powerful tool for the system designer.

Differential Signals, AC Coupling, and JTAG

Most modern systems use high-speed, AC-coupled differential pairs. While 1149.1 is an excellent tool for testing and diagnosing digital systems, it was designed for DC-coupled, TTL-level nets. AC coupling and differential signals are not compatible with 1149.1. An IEEE working group studied the problem and developed a solution that became IEEE1149.6.

The solution required edge detectors to be added to both polarities of the differential pair receiver as shown in ***Figure 7***. During a JTAG test, the 1149.6-enabled transmitter produces pulses under the control of the Boundary Scan Register (BSR) instead of static DC levels (as was done in 1149.1).



1	TX1 pin1 open	6	TX1 pins 1,2 shorted together	11	RX1 pins 1,2 shorted
2	C1 pin2 open	7	C1 pins 1,2 shorted together	12	TX1 pin1 short to TX2 pin1
3	RX1 pin1 open	8	C1 pin 1 short to C2 pin 2	13	RX1 pin1 short to RX2 pin1
4	TX1 pin1 short to VDD	9	RX1 pin1 short to VDD	14	R (term) pin1 open
5	TX1 pin1 short to GND	10	RX1 pin1 short to GND		

Figure 7. Schematic Showing Potential Defects Detectable by an 1149.6-Enabled Device for an AC-Coupled Differential Transmission Line

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These pulses pass through the AC-coupling capacitor resulting in an edge at the receiver. The receiver detects these edges and passes this information to the BSR which can be read to determine if a defect is present.

A very important consideration is that IEEE1149.6 uses the identical protocol and TAP as IEEE1149.1, making it compatible with existing JTAG systems. National offers an entire array of 1149.6 products including cross points, mux buffers, and SerDes.

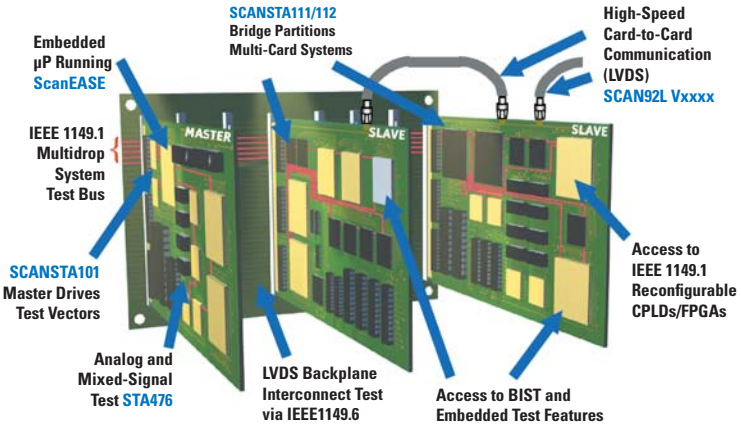


Figure 8. Total System

Putting It All Together

Figure 8 provides an example of how a typical high-performance telecom or datacom system might look. Much of the design and component selection has been driven by the requirements of the market place such as high performance, flexibility, and very high availability. Thus, there are many components with JTAG and built-in-test features as well as dense FPGAs for quick turn and flexibility. These test features and the ability to reconfigure components during manufacturing and in the field provide a cost-effective solution to the demanding requirements of deployed systems.

The JTAG test bus is used to access the test features on each board. The STA101 interfaces to the processor bus and drives the JTAG bus with ATPG vectors. The STA111/112 bridge is used to convert the IEEE JTAG test bus to a multidrop addressable environment and adds partitioning capabilities for JTAG path management. JTAG is used to access CPLDs for reconfiguration/programming, BIST features, and embedded test features for other complex devices. Card-to-card, AC-coupled differential interconnects are tested with 1149.6 enabled devices, and analog nodes are sampled with the STA476.

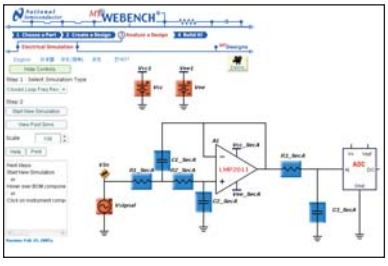
Conclusion

System-level JTAG can be a powerful tool, allowing manufacturing, remote test, diagnostics, and re-configuration. The system designer should pay careful attention to the level of access and speed required when designing a system, and use the proposed architectures as a starting point when beginning a design. National provides products, software, and support for simple through complex embedded JTAG systems and can provide access and interconnect test to digital, analog, and differential nets.

Appendix: Useful Definitions

- JTAG –Joint Test Action Group
- ISP – In-System Programming
- TAP – Test Access Port
- BSDL –Boundary Scan Description Language
- BSR – Boundary Scan Register
- ATPG –Automated Test Program Generation
- BIST –Built-In Self Test
- SCANEASE –National Semiconductor's SVF Converter
- SVF – Serial Vector Format
- LSP – Local Scan Port

Design Tools



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