Application Report
SNLA074A–October 2005–Revised April 2013

# AN-1398 Printed Circuit Board Design Techniques for DS40MB200

**ABSTRACT**

The high speed, high gain and fast edge rate attributes of any high-speed circuit requires you to use the high-speed printed circuit board (PCB) techniques to achieve good performance. This application report outlines the techniques to achieve this goal.

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## 1 Introduction

The DS40MB200 is a high speed 2:1 multiplexer and 1:2 fan-out repeater designed to support redundancy and extend copper backplanes up to 4 Gb/s. The output driver features fast edge rates, typically about 80 ps. Each input stage features fixed equalizer, followed by a high-gain limiting amplifier that re-shapes the output waveforms. The DS40MB200 accepts input signal as low as 100 mV (peak-to-peak).

## 2 Differential Pairs

The DS40MB200 uses a 48-lead lead-less LLP package. The LLP offers low package parasitics and is the package of choice for high-speed communication designs. The high speed differential IO's are assigned to the center portion of the package such that each differential pair is sandwiched by a power or ground pin, providing isolation and ground shielding. Coupled microstrip board traces are the preferred transmission line structures for best signal fidelity. The optimum trace width is 10 mils, being equal to the 10-mil landing pad of the LLP-48 package. Finer trace width, such as 5 mils, can also be used with slightly higher impedance mismatch caused by changes in trace width between the traces and the pads. The differential board traces should be routed with constant spacing to ensure impedance uniformity along the length of the traces. Figure 1 shows a partial layout arrangement with 5-mil trace width.

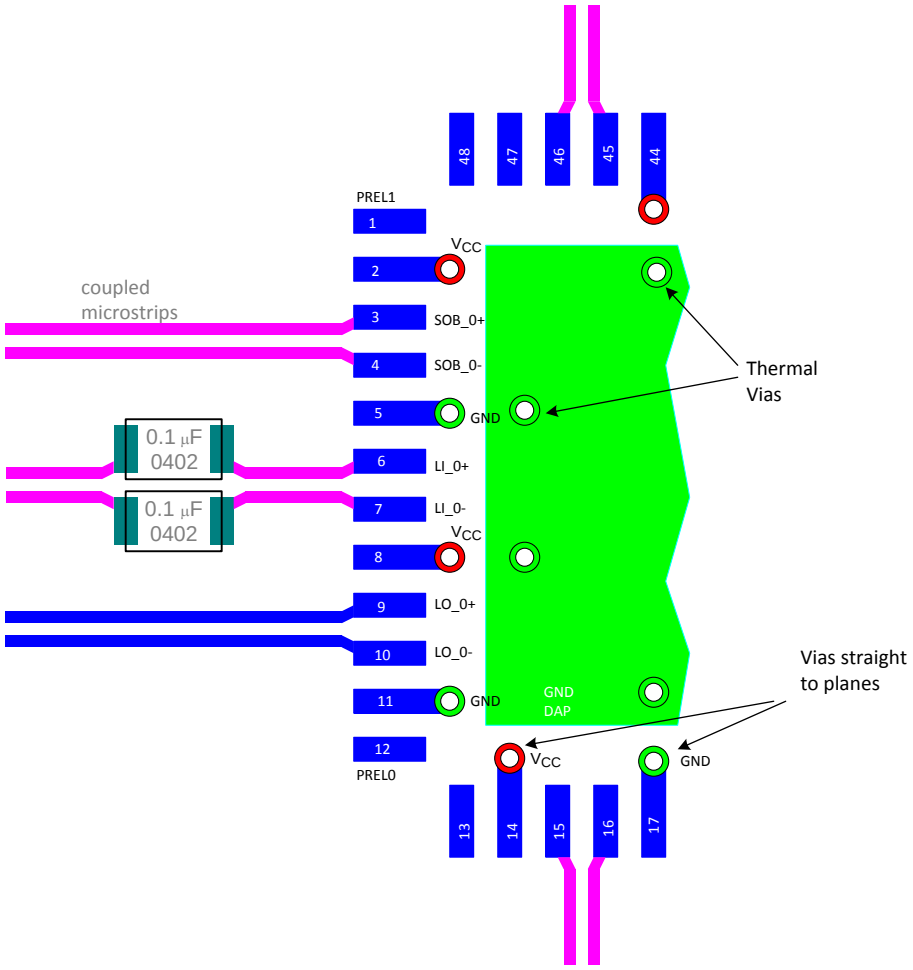


**Figure 1. DS40MB200 Routing Example Using Coupled Microstrips**

In high routing density boards, coupled striplines are commonly used, but requires the use of plated through holes. These plated through holes introduce parasitic capacitance and may degrade signal fidelity. Small via, with less than 8 mils hole size, should be used to minimize mutual capacitive coupling between the via and nearby ground or power planes. Differential via structure with shared oval-shaped anti-pad can further reduce parasitic capacitance. Figure 2 shows a pair of differential vias with shared oval anti-pad.

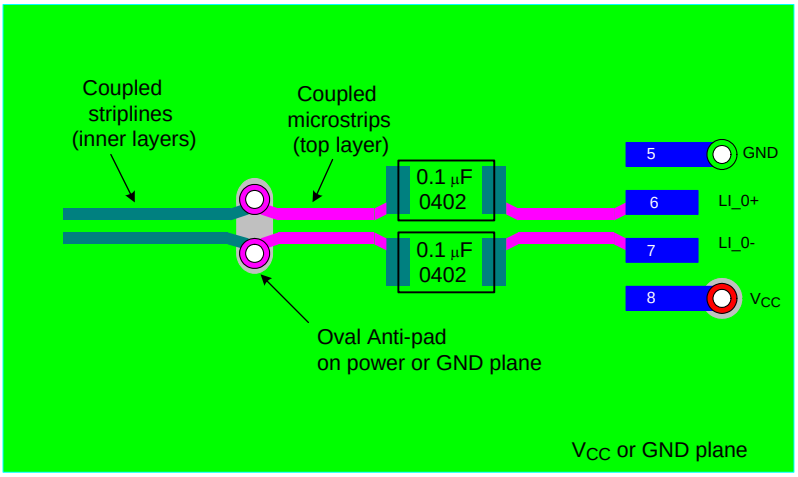


**Figure 2. Differential Vias With Oval Anti-Pad**

The electrical length of each differential pair should be well matched. As a rule of thumb, the delay skew of the complimentary signals are matched within a small fraction of the signal's edge rate. With an edge rate of about 80 ps, it is acceptable to have a delay skew within 10 ps. For a FR4 board, matching trace lengths within 50 mils achieves less than 10 ps skew between the complimentary signals of the differential pair. Note that it is the matched electrical length instead of matched physical length that matters. Identical geometries should be used for the complimentary signals, and their trace widths in each signal layer should be matched.

In adjusting the trace lengths of a pair of coupled board traces, never disrupt the uniform spacing of the differential pair. Figure 3 shows a bad example of matching trace lengths. Disrupting the uniform spacing of the coupled differential pair will create impedance discontinuity and impact signal quality. Figure 4 shows a good example of matching trace lengths. In this example, the lengths of the uncoupled segments of the differential pair are adjusted to achieve the desired match lengths. The coupled board traces maintain their uniform spacing, while the trace width of the uncoupled traces are slightly widened to maintain the same characteristic impedance.

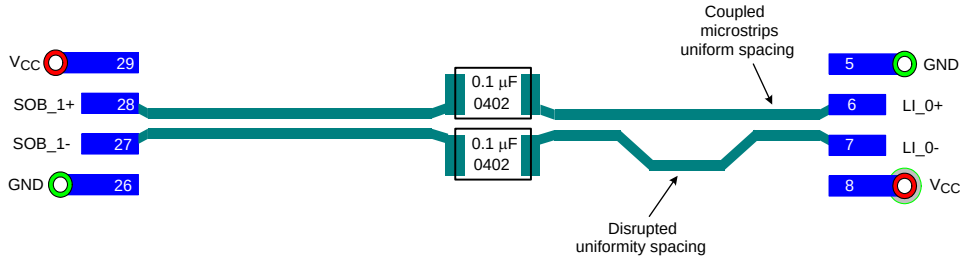


**Figure 3. Bad Example Of Matching Trace Length Of Coupled Board Traces**

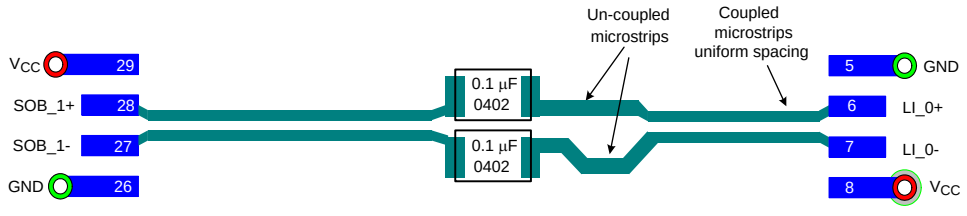


**Figure 4. Good Example Of Matching Trace Length Of Coupled Board Traces**

## 3 Components' Landing Pads

AC coupling capacitors should be placed on the receive inputs of the DS40MB200. The transition time of the bit stream at the receive side is significantly slowed down by interconnect, making it more tolerant to impedance mismatch caused by the AC coupling capacitors and the parasitic capacitance caused by their landing pads. Small physical size, surface mount capacitors, such as 0402, should be used to reduce impedance mismatch caused by the landing pads of the capacitors.

When fine trace width is used with large components, the landing pads of the components are huge relative to the trace width. Figure 5 shows an example of 5-mil traces routing to an edge connector with 20 mil pads.

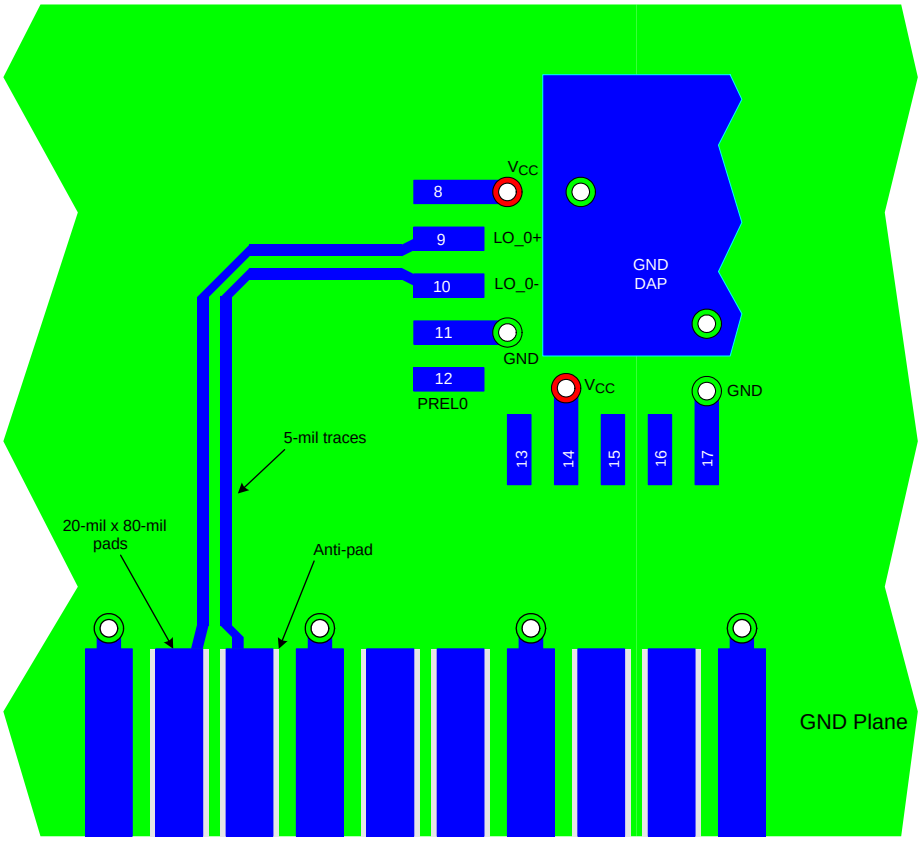


**Figure 5. Fine Board Traces Used With Large Component Landing Pads**

The huge landing pads of the edge connector effectively form a short segment of wide trace, significantly lowering the impedance and introduce relatively large excess capacitance between the pad and the ground plane immediately below it. Figure 6 depicts the cross-sectional view of the board showing the effect of impedance drop from landing pads.

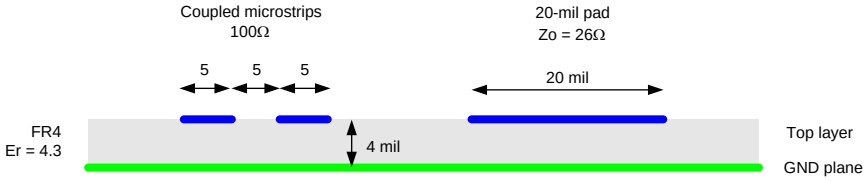


**Figure 6. Cross-Section Of Board Trace And Component Pad**

You can use anti-pads on the power and ground planes below the landing pads. This technique is used to reduce the parasitic capacitance formed between the pad and the nearby power or ground plane. Figure 5 illustrates anti-pads used with an edge connector to minimize excess capacitance. A 3-D electromagnetic field solver is usually used to determine the size of the anti-pad to optimize compensation.

## 4 Power Pins

Each power or ground lead of the DS40MB200 should be connected to the power or ground plane through a low impedance path. For best results, one or more vias should be used to connect a power or ground pin to nearby power or ground plane. Ideally, vias are placed tangent to the IC pads to avoid adding trace inductance. Placing power planes closer to the top of the board reduces the length and inductance of the vias.

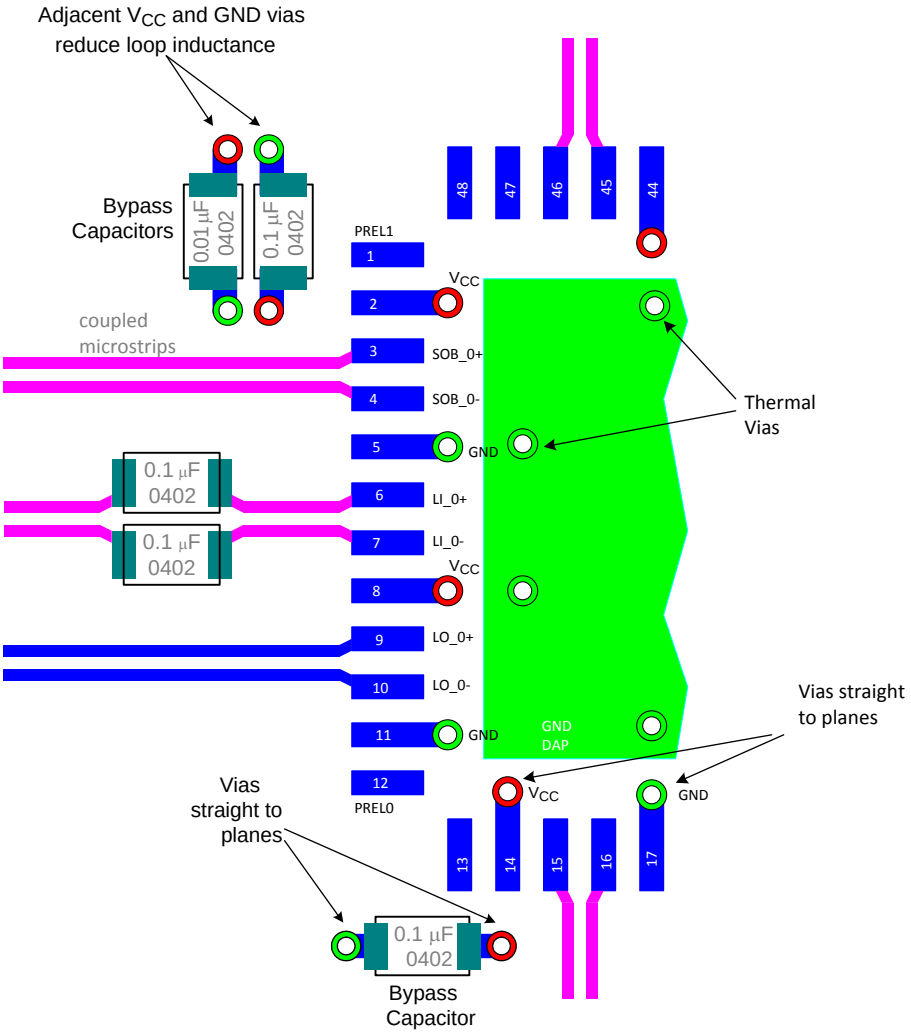


**Figure 7. $V_{CC}$ and GND Hook-Up For The DS40MB200**

Bypass capacitors should be placed close to VCC pins. They can be conveniently placed at four corners of the LLP package. Small physical size capacitors, such as 0402, X7R, surface mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor. Figure 7 shows $V_{CC}$ and GND hook-up for the DS40MB200 and placement of bypass capacitors.

An X7R surface mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 20–30 MHz, X7R capacitors behave as low impedance inductors. To extend the operating frequency range of these capacitors to a few hundred MHz, an array of different capacitance ranging from 100 pF, 1 nF, 0.01 µF, 0.1 µF are commonly used in parallel. A more effective bypass capacitor can be built using sandwiched layers of power and ground planes at a separation of 2–3 mils. An ideal high frequency bypass capacitor is formed. With a 2-mil FR4 dielectric, there is about 500 pF capacitance per square inch. Figure 8 depicts a PCB stack-up with $V_{CC}$-GND planes placed on the top side of the board. This stack-up arrangement provides a high frequency “buried” capacitor, and lowers the inductance of power and ground via by reducing the lengths of the vias.

The center dap of the package should be connected to ground plane through an array of vias. The array of via reduces the effective inductance to ground, and also offer enhanced thermal performance for the package.

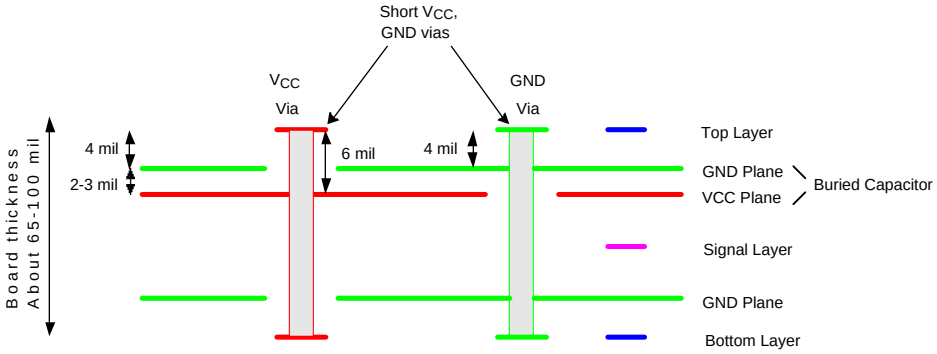


**Figure 8. PCB Stack-Up With "Buried" Capacitor And Short $V_{CC}$/GND Vias**

## 5 Conclusion

High speed printed circuit boards require designers to go beyond connectivity. Multi-gigabit boards require attention to board geometry details. These details include dimensions of trace width, component pads, plated-through holes, anti-pads, board thickness and board stack-up. Board material properties such as dielectric constant and loss tangent are important considerations in choosing proper board structures. The techniques described in this application report apply to multi-gigabit board design, with examples illustrated for DS40MB200 mux and buffer. In a multi-gigabit board design, board designers have to find the unwanted L's and C's and devise geometries to overcome their impacts. Very often, a 2-D electromagnetic field solver is used to predict the electrical behavior of board traces, and a 3-D field solver is needed to deal with 3-dimensional geometries such as via and anti-pad. With a little extra time spent on attention to details, the reward is a high performance board running at multi-gigabit and beyond.

## 6 Reference

- *Dual 4.0 Gbps 2:1/1:2 CML Mux/Buffer With Transmit Pre-Emphasis and Receive Equalization Data Sheet* SNLS144
- *AN-1389 Setting Pre-Emphasis Level for DS40MB200 Dual 4Gb/s Mux/Buffer* (SNLA073)
- *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401)

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