How to Calculate the Period Jitter σ_T from the *SSCR* $\mathcal{L}(f_n)$ with Application to Clock Sources for High-Speed ADCs

Alfio Zanchi

Texas Instruments, Inc. – Wireless Infrastructure Data Converters
12500 TI Boulevard - 75243 Dallas, TX (U.S.A.)
alfio.zanchi@ieee.org

ABSTRACT

This document introduces a general formula to translate the phase noise of a clock source, rated via the Single Sideband to Carrier Ratio (SSCR), to the cycle-to-cycle jitter of the oscillation period. The link allows to seamlessly aggregate the external clock source phase noise, usually given in dBc/Hz, to the phase stability figure of the on-chip clock synchronization circuitry, usually rated in ps-RMS. This permits in turn to evaluate their impact on the total aperture jitter of a sampling circuit, finally enabling the determination of the SNR for systems like, as shown in this document, an analog-to-digital converter.

The validity of the relationship between the time- and frequency-domain figures of merit has been first tested on the phase noise spectrum featured by bipolar and CMOS integrated VCOs; thereafter, the most popular case of PLL-based frequency synthesizers has been treated both by adopting time-to-amplitude conversion techniques, or dedicated phase-noise testing equipment.

The optimal performance enabled by a state-of-the-art aperture jitter, optimized by making use of the formulas here proposed and rigorously quantified in 250fs, is demonstrated on Texas Instruments ADS5420, a high-speed 14b 65MSps ADC for 3G wireless infrastructure BTS applications.

INTRODUCTION

The increasingly challenging requirements posed on ADC performance by the newest CDMA multi-carrier standards, by low-IF single-heterodyne receivers, and by sophisticated power amplifier linearization techniques call for device flexibility in terms of speed, gain, matching, and linearity, nowadays available primarily in very advanced technologies. At the same time, the integration of RF front-end and IF A-to-D conversion potentially allowed by a common BiCMOS platform, or of the ADC with a digital downconverter (DDC), could eliminate important bottlenecks in front of the final DSP. The main limitation to the resolution of the system becomes the Signal-to-Noise Ratio (SNR) of the ADC, which is in turn limited by jitter when the intermediate frequency (IF) of the receiver is pushed higher than 70MHz. The timing uncertainty is given by the RMS combination of external clock synchronization source and on-chip clock conditioning and distribution network.

The unification of the figures of merit used for rating the phase noise of time reference circuits becomes essential exactly at the boundary between external instrumentation and integrated circuit. While mixed-signal designers are more prone to adopt time jitter as the figure of choice for assessing the stability of the sampling clock and ultimately the SNR, RF instrumentation data sheets tend to rate the same phenomenon in terms of phase noise, expressed via the Single Sideband to Carrier Ratio (SSCR). σ_{To} is defined as the RMS standard deviation of the statistical distribution obtained by collecting the time duration of the oscillation periods. The $SSCR(f_n)$, instead, is the spectral profile given by the ratio of the phase noise power found in a 1-Hz bandwidth at the offset f_n from the carrier, and the carrier power concentrated at f_0.

In a previous work [1] the link between the time-domain and frequency-domain parameters used to evaluate the phase noise (respectively *jitter* and *SSCR*) was demonstrated. Among the numerous definitions given for the jitter we will discuss the *cycle jitter* of a periodical waveform, or *period jitter* σ_{To}, since it is the parameter that determines the SNR in the well-known expression [2]:

$$SNR = -20 \cdot \log\left(2\pi f_{IN} \sigma_{To}\right) \tag{1}$$

With the aid of the formula presented hereinafter, Eqs. 14 or 16, the jitter can be derived from the phase noise spectrum via the numerical computing of an integral, without any additional effort. From the experimental standpoint, the formula allows for the estimation of the timing deviation without relying on jitter-specific test instrumentation, but only on a standard spectrum analyzer, as shown in the last part of this discussion.
This study lead to the optimization of the total source+clock jitter in the design of a critical circuit: we will introduce a 14b 65MSps switched-capacitor pipeline ADC, whose specifications target base-stations for 3G wireless standards requiring IF sampling capability of 70MHz to 220MHz. The ADC eventually showed a period jitter as low as 250fs, the best figures proven to date for CMOS-based clocks, enabling excellent SNR of 69.3dBFS at 65MSps, 220MHz IF. The circuit has been designed in Texas Instruments' proprietary RFSiGe1 silicon-germanium very high-speed BiCMOS process.

DERIVATION OF THE GENERALIZED SSCR ↔ JITTER FORMULA

The formula developed in [1] (reported for convenience in Eq. 2) was obtained based on the assumption of a classical phase noise profile featuring f_n^{-2} tails around the carrier (Fig. 1a):

$$\sigma_{T_0}^2 = \frac{f_n^2}{f_0^3} \cdot SSCR(f_n) \tag{2}$$

However, a lot of practical situations exist which divert from such a behavior. For instance, the flicker noise of a CMOS VCO transfers into a characteristic f_n^{-3} slope in the output spectrum sidebands. More important, for a number of applications synchronized to an external source, the spectrum synthesized by a PLL remains flat within the loop bandwidth *BW* centered at f_0 (Fig. 1b). Since the characteristics of phase stability of the PLLs found in instrumentation (e.g., the HP8644B source) are usually rated in SSCR terms, or expressed in dBc/Hz @ offset f_n from the carrier, a generalized equation linking any SSCR profile to the period jitter σ_{To} can be gained from the same standard derivation.

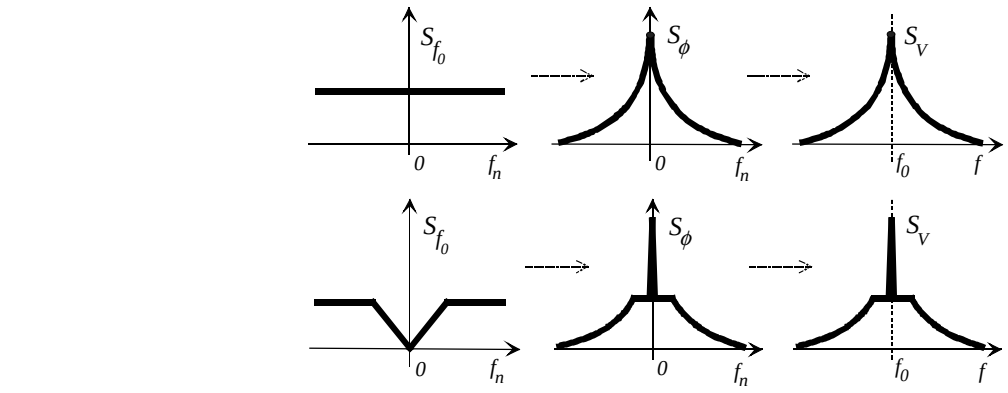

Fig. 1. Power spectral densities of frequency noise, phase noise, and output voltage noise in the case of a) a free-running oscillator, b) a PLL frequency synthesizer

What represented in Fig. 1 can be easily obtained with an *ad-hoc* Matlab simulation, where for example the built-in *vco()* function is fed with a white noise in the first instance, and with an highpass-shaped noise in the second case. The results obtained when the PLL bandwidth is set to a broad 10% of the center frequency (100MHz vs. 1GHz) are represented in Fig. 2. Of course, within the simulated environment it is also easy to retrieve the jitter from the definition (standard deviation of the Gaussian distribution of the period's durations), which yields 2.48ps for the VCO and 2.13ps for the PLL arrangement respectively.
The following is a demonstration of the mathematical foundations and assumptions upon which the frequency-to-time domain formula relies. The mathematical procedure leading to the generalized formula has been presented in [3] and is here reported for the reader's convenience; if only concerned with the final outcome, the reader can conveniently skip to Eq. 14 without loss of logical continuity in the Application Note.

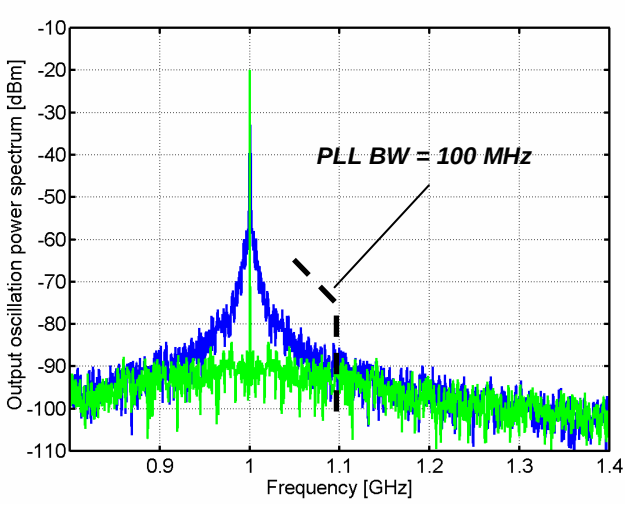

Fig. 2. Matlab simulated signals spectra in detail. The upper spectrum pertains to oscillators showing white frequency noise (free running VCO), the lower one by highpass-filtered frequency noise (typical of PLL)

Let us consider two noise components at offset $\pm f_n$ rotating in the frame of the phasor representing the carrier, which rotates at frequency f_0 (Fig. 3). In order to generate an orthogonal phasor to the carrier, which eventually perturbs the angle of the carrier phasor and leads to phase noise (PM), these phasors must be equal in amplitude and be positioned as shown in Fig. 3. In this case in fact, to a first order the composition of noise tones affects only the phase of the carrier without modifying its module, which would translate into amplitude noise (AM).

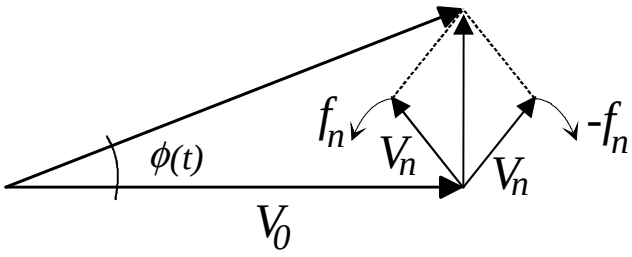

Fig. 3. Phasor-plane representation of the carrier affected by the two side tones responsible for sole phase modulation

It is very common to deal with noise contributions that can be modeled with narrowband FM noise. The phase modulation due to these components is therefore

$$\phi(t) = 2V_n \sin(2\pi f_n t)/V_0 \tag{3}$$

Since $d\phi/dt = 2\pi f$, the phase error $\phi(t)$ causes an instantaneous frequency deviation given by

$$\Delta f_0 = f_n \cdot 2V_n \cos(2\pi f_n t)/V_0 \tag{4}$$

The phase disturbances affecting the carrier can be modeled as a random process, identified by the power spectrum S_ϕ, or S_{fo} as an alternative. Spectra will be always considered bilateral throughout the derivation. The link between the two functions is provided by the differentiation rule for the Fourier transform:

$$S_{f_0}(f_n) = f_n^2 \cdot S_\phi(f_n) \tag{5}$$

When considering only the two tones of Fig. 3, by taking the integration bandwidth df at offset f_n it is:

$$\frac{V_n^2}{4} = S_V(f_0 \pm f_n)\,df \tag{6}$$

and therefore, according to Eq. 3:

$$\langle \phi^2 \rangle = \frac{1}{2} \cdot \frac{4V_n^2}{V_0^2} = \frac{4 \cdot S_V(f_0 \pm f_n) \cdot df}{V_0^2/2} = 2 \cdot SSCR(f_n) \cdot df\ /1Hz \tag{7}$$

But since, by definition:

$$\langle \phi^2 \rangle = 2 \cdot S_\phi(f_n)\,df \tag{8}$$

by equating the two expressions above we get:

$$S_\phi(f_n) = SSCR(f_n) \tag{9}$$

Thus the spectrum of the voltage noise observed on a spectrum analyzer does represent the spectrum of the phase of the signal, for small deviations – which is by far the most common case. Let now σ_{To} denote the RMS jitter of the single oscillation period $T_o = 1/f_o$. Since

$$\Delta T_0 = -\Delta f_0 / f_0^2 \tag{10}$$

Then, by applying the statistical definition of variance:

$$\sigma_{T_0}^2 = 1/f_0^4 \cdot \sigma_{fo}^2 \tag{11}$$

where σ_{fo} is the RMS value of the frequency deviation *observed over one period* T_0, i.e., the cycle jitter. Now it is possible to evaluate σ_{fo} after $S_{fo}(f_n)$ by making use of the Wiener-Khintchine theorem. In particular, σ^2_{fo} can be determined after the integration of the frequency noise over one single period T_0. In the frequency domain, this means filtering the spectrum with the *sinc* transfer function of a "gated integrator" spanning T_0 over time. Therefore:

$$\sigma_{f_0}^2 = \int_{-\infty}^{+\infty} S_{f_0}(f_n) \cdot |W(f_n)|^2 df_n \tag{12}$$

where, as is well known, the weight function is the Fourier transform of a rectangle, or:

$$W(f_n) = sin\left(\pi \frac{f_n}{f_0}\right) \Big/ \left(\pi \frac{f_n}{f_0}\right) = sinc\left(\pi \frac{f_n}{f_0}\right) \tag{13}$$

Eventually, by recalling Eqs. 11 and 12 we obtain:

$$\begin{aligned} \sigma_{To}^2 &= \frac{1}{f_0^4}\sigma_{f_0}^2 = \frac{1}{f_0^4}\int_{-\infty}^{+\infty} S_{f_0}(f_n) \cdot |W(f_n)|^2 df_n = \\ &= \frac{1}{f_0^4}\int_{-\infty}^{+\infty} f_n^2\ S_\phi(f_n) \cdot |W(f_n)|^2 df_n \end{aligned} \tag{14}$$

which constitutes the *general link* between the jitter of the period duration and the phase noise spectrum measured on a clock signal.

Let us now consider the two cases in Fig. 1. For a free-running oscillator the noise density $S_{fo}(f_n)$ is white, therefore it can be denoted simply by S_{fo}, and after straightforward processing the integral in Eq. 14 reduces to:

$$S_{f_0} \cdot 1/T_0 = S_{f_0} \cdot f_0 \tag{15}$$

where the expression of the equivalent noise bandwidth of the gated integrator has been used. From Eq. 14 we essentially recovered Eq. 1, otherwise to be obtained with way more complicated derivation. When the formula is applied to the simulated Matlab cases reported in Fig. 2, the σ_{To} of the distribution results about 2.50ps for the unlocked VCO, against the 2.48ps obtained by the cycle jitter definition. As expected, the identity of the paradigm under which the formula has been derived and the idealized simulation setup leads to a tiny error, only 0.8%.

In the case of an oscillator locked into a PLL instead, as shown in Fig. 1, the spectrum $S_{fo}(f_n)$ is highpass-filtered with a bandwidth *BW*. No closed-form solution is given for Eq. 14; however, once the spectrum S_ϕ is known after the oscillator simulation, the multiplication by the standard *sinc* filter profile followed by the integral between f_{n1} and f_{n2} becomes a numerical expression:

$$\sigma_{T_0}(T_0) \cong \frac{1}{f_0^2}\sqrt{\sum_{f_{n_1}}^{f_{n_2}}\left[2 f_n^2 \cdot SSCR(f_n)\cdot \mathrm{sinc}^2\left(\pi \frac{f_n}{f_0}\right)\Delta f_n\right]} \tag{16}$$

The formula (16) can be computed in an uncomplicated automated way, using built-in functions widely available in waveform analysis software such as NI's LabView®. The numerical solution of Eq. 16 can be employed for example to obtain the variance σ^2_{To} and, eventually, the RMS jitter for the second spectrum of Fig. 2: the jitter value calculated this way is 2.15ps. Once again, the time jitter estimated from the spectrum $S_\phi(f_n)$ matches within 1% the σ_{To} value that would be obtained from the direct – but lengthy... – statistical extraction of the jitter from the distribution of the occurrences of zero-crossings.

To summarize, the expression converts the phase noise spectrum into frequency noise spectrum (according to the Laplace transform rule $S_f = j\omega S_\phi$) and weights it through the *sinc* function, to account for the uniform jitter accumulation in the time span $0 \rightarrow T$ (i.e., rectangular weight function $h(t)$). The integral of the noise spectral density is extended from the reciprocal of the total observation time $f_1 = 1/T_{obs}$ to the maximum offset frequency allowed by the spectrum analyzer instrumentation f_2.
The formula in Eq. (16) is the practical tool that allows to pass from SSCR to jitter, and can be solved in closed form in a number of cases (again, a VCO without flicker noise! whose solution is in [1]).

EXPERIMENTAL VALIDATION OF THE FORMULA

A lab apparatus suitable to characterize the time stability of the test oscillators is schematically represented in Fig. 4.

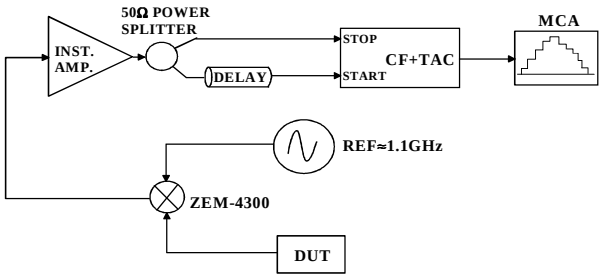

Fig. 4. Block diagram of the lab setup. A low-noise instrumentation amplifier can provide for image rejection, whereas the coaxial stub is used to synchronize the operation of the zero-crossing detector [3]

In fact, by plugging in Eq. 2 the typical numbers featured by RF oscillators for communications – i.e., running at 1 GHz or so and with SSCR below –110dBc/Hz @ 100kHz offset; or even worse, featured by crystal signal sources suitable to drive high-IF performance ADCs – i.e. running at 100MHz with SSCR of –140dBc/Hz @ 1kHz, it can be recognized that we deal with time jitters on the order of a picosecond, or lower. In the laboratory practice, this problem can be substantially relaxed by *rigidly* translating the oscillation spectrum at lower frequencies. Intuitively speaking, working on a number of the original periods allows for the jitter to build up with time, and eases the observation of it. After some mathematical processing (or,

more heuristically, even using the simplistic Eq. 2 for the same SSCR profile at two different center frequencies) it turns out that the jitter which will be observed after the downconversion is:

$$\sigma_{T_1}^2 = \sigma_{T_0}^2 \cdot \left(\frac{f_0}{f_1} \right)^3 \tag{17}$$

Of course, the device to be used to lower the frequency without affecting the spectrum is a low-noise mixer. Frequency dividers would alter the spectrum, lowering the jitter and complicating the estimation, and are usually noisier. Nowadays an increasing number of high-end oscilloscopes offer a high-frequency jitter characterization option; however, this alternative method features a resolution that can be enhanced by selecting advantageous frequency ratios, and is very flexible.
The assessment of the time jitter of the slower waveform can be easily accomplished either via a cheaper oscilloscope card, or through time-to-amplitude conversion. The blocks involved in implementation of the latter, as depicted in Fig. 4, were a zero-crossing detector (comparator) with standard square digital pulses as output, which also rejects any contribution of AM noise, allowing for the only PM to pass through; a Time-to-Amplitude Converter (TAC), basically a ramp integrator whose voltage output level is proportional in amplitude to the duration of the pulse received at the input; and a Multi Channel Analyzer (MCA) storage system, constituted by a memory bank addressed by an input ADC, in order to sort into a histogram the amplitudes of the pulses sampled at its input. Due to the limited speed of each module, the original oscillation signal frequency must be shifted down to 50kHz maximum.

1. Free-running LC-tank VCO

The measurement system described above has been employed to prove the validity of Eq. (16) over a bipolar spiral-inductor *LC*-tuned VCO used in a RF wireless DAB application [4], with 2.2GHz center frequency. The results of the test carried out on the oscillator when operated "standalone" (actually, setting its PLL *BW* to a few 100Hz) are presented in Fig. 5. As emphasized by the upper curve (diamonds) the VCO's phase noise decays according to a fairly regular power law, dropping like $1/f^2$ all the way after 500Hz.

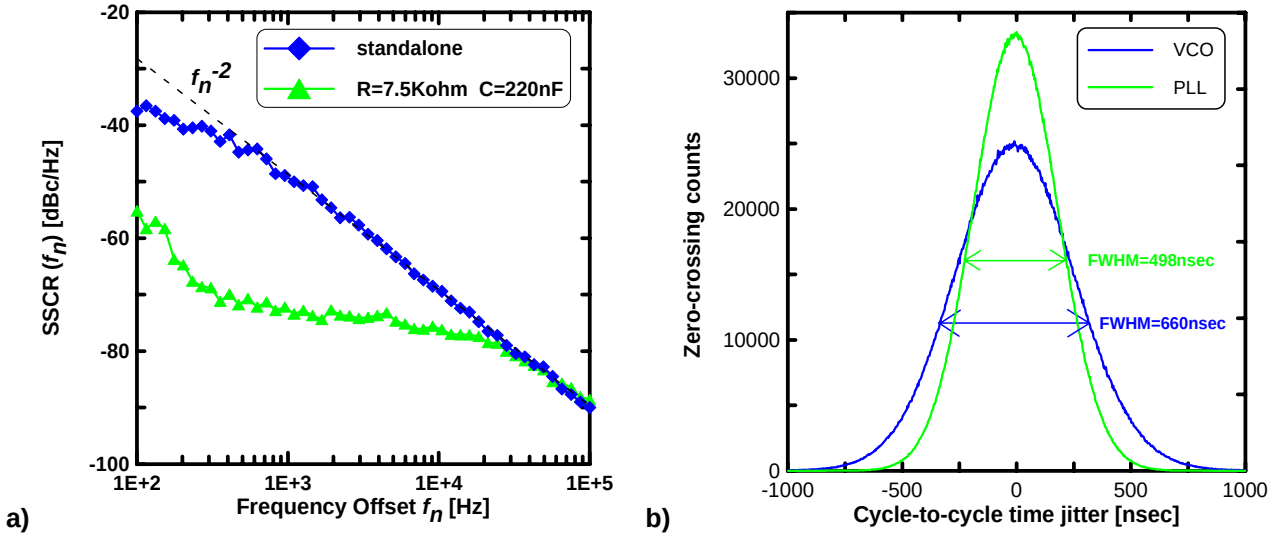

Fig. 5. a) Experimental SSCR curves for the LC-tuned VCO and PLL built around it. The discrepancy with the pure $1/f^2$ trend of the VCO plot is due to a residual PLL action. b) Statistical distributions of the period duration as collected at the MCA of the setup in Fig. 4

The standalone condition is here effectively reproduced by using a very narrowband PLL in order to avoid the issues due to jitter divergence (that would require the introduction of complex *structure functions* in the theory, see [5] or [6]) and thermal drifts. The oscillation spectrum of Fig. 5a has then been downconverted to 50kHz, and the time occurrences of the waveform's zero-crossings were detected and memorized. Fig. 5b reports the histogram of the time period distribution as recorded by the MCA apparatus. The wider plot shows a Gaussian-shaped profile with a standard deviation σ_{To} = 280ns (that is, 30.3fs on the original oscillation as computed through Eq. 17). The corresponding jitter estimation obtained when Eq. 16 is numerically

applied to the phase noise spectrum, truncated at only 200kHz and thus leaving out a considerable part of the spectrum, gives 260ns - meaning a limited 7.1% error against the experimental data.

2. Phase-Locked Loop tests

The experiment described in the previous paragraph permitted to double-check the correctness of the proposed formula when used for VCOs. A case of huge practical relevance is to be analyzed by locking the bipolar VCO into an integrated PLL, whose principle scheme is depicted in Fig. 6. The loop filter consists of a standard charge-pump circuit driving an adjustable off-chip passive network.

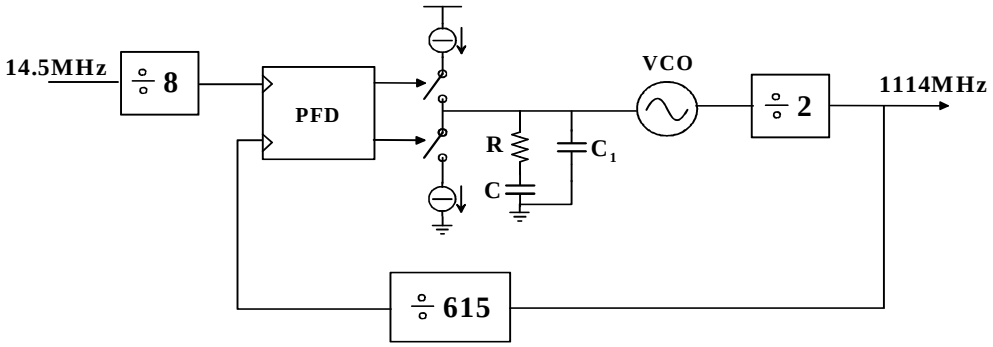

Fig. 6. Scheme of principle for the integrated phase-locked loop used in the experimental validation

By adopting a simple *R-C* series filter (R = 7.6kΩ, C = 220nF, C_1 = 0) the *BW* of the system was set to approximately 30 kHz. In Fig. 5a, the superposition of standalone and locked-in (triangles) noise spectra testifies the prevalence of the VCO noise beyond such a bandwidth. The numerical integration of the relationship given in Eq. 16 returns for the PLL a jitter estimate of 185ns at the 50kHz frequency. When weighted against the 260ns computed for the free-running VCO, the data highlights how the PLL removed a considerable amount of close-in phase noise, as expected especially in integrated oscillators' implementations.

The measurement performed on the output of the PLL still leads to a Gaussian-shaped histogram (Fig. 5b, narrower plot) whose standard deviation is 195ns. The discrepancy with the prediction from the formula (16) still keeps to about 5.1%, even though the integration was stopped to 200kHz only.

To make the analysis even more comprehensive, a 0.25μm *LC*-tuned CMOS VCO built for 5GHz operation has been locked in a PLL using a phase noise analyzer (HP3048A). The instrumentation employed allows for the PLL bandwidth to be adjusted by simply switching a filter bank: the *BW* values chosen for the test were 21, 43, and 92kHz, producing the spectra reported in Fig. 7a. As clearly appreciable from the slopes indicated inside the plot, and expected from the nature of the technology used to fabricate the circuit, the flicker noise component is considerable for this kind of VCO under test. The jitter prediction based on the computation of Eq. 16 for each of the spectra sketched in figure, when referred to the 50-kHz final oscillation, provides the following RMS results: $\sigma_T(T_0)$ = 750ns @ BW = 21kHz, 519ns @ 42kHz, and 358ns @ 92kHz. The accuracy of the system was as good as 7ppm, translating into a negligible 140ps uncertainty for a 50kHz input.

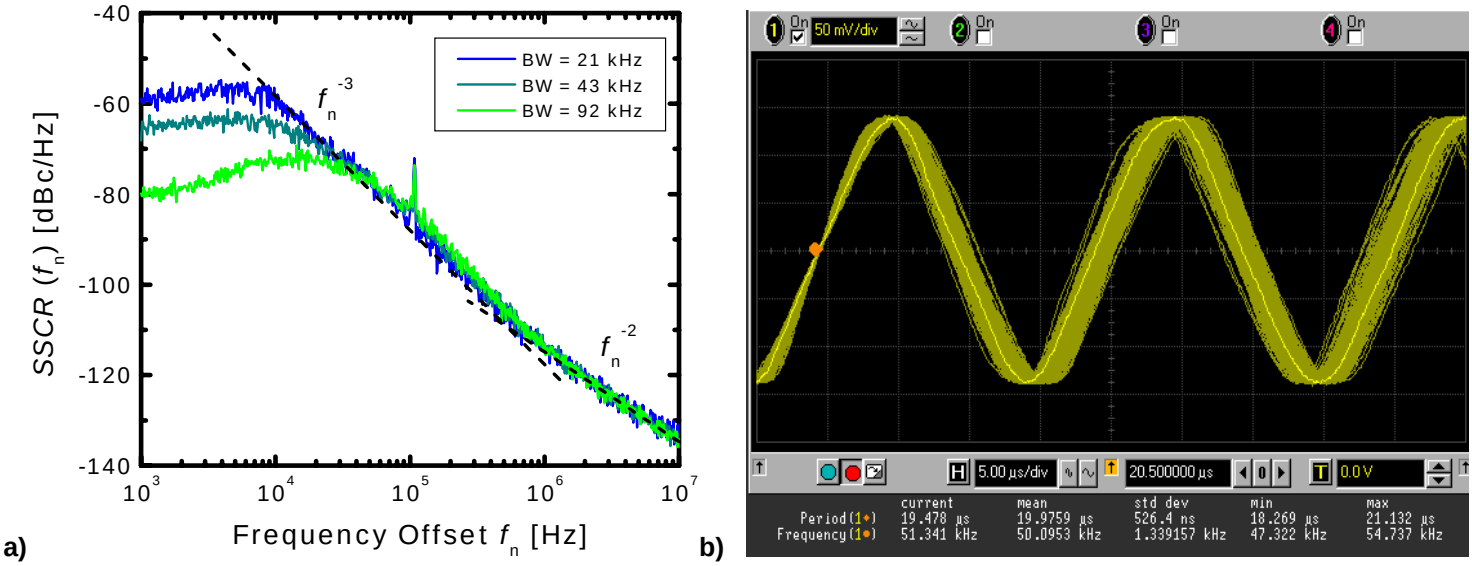

Fig. 7. a) Experimental SSCR plots for the CMOS PLL frequency synthesizer operated with different bandwidths. b) The jittering zero-crossings of the PLL output, as captured with an Agilent Infiniium™ oscilloscope

Once the synthesized waveform is mixed down to 50kHz, the jitter analysis can be easily carried out – for sake of practicality, this time via an Agilent Infiniium™ oscilloscope. The trigger could be synchronized on the first oscillation crossing, and the period test menu provided a very straightforward measurement of the variance. The deviations obtained by this method were $\sigma_T(T_0)$ = 798ns, 526ns, and 361ns, respectively for the three PLL bandwidths *BW* mentioned above. The simpler setup, along with the 10MHz extended span of the numeric integral, led to achieve relative errors even smaller than before: respectively, 6.0% @ *BW* = 21kHz, 1.3% @ 42kHz, and only 0.8% @ 92kHz. This complete series of validation test provides a full proof to the SSCR-to-period jitter link proposed in this document, making it a valuable tool for both silicon and system design and optimization.

APPLICATION: CLOCK SOURCE JITTER FOR HIGH-SPEED ADCs

The best proof and application of the formula's validity has been accomplished in a very practical case: the measurement of the clock jitter due to the external source driving TI's ADS5420, a 14b 65MSps Analog-to-Digital converter. The case can be viewed as a corollary of the situation described in paragraph C above, since pretty much every commercial synthesizer adopts a PLL scheme inside, although it features way better specs than the ones reported in Fig. 7a.

To maximize the dynamic range required by wireless communication protocols, while containing the power consumption, a multibit-per-stage architecture has been chosen. As shown in Fig. 8, the ADC is comprised of five 2.5b stages (2 effective bits + 1 bit redundancy for digital correction) followed by a 4b flash. Although a dynamic element matching (cap shuffling) algorithm was initially designed in the ADC, the inherent matching of the passives of the TI technology used proves acceptable to 14b level without need for dynamic shuffling, nor one-time trimming, nor calibration of any sort.

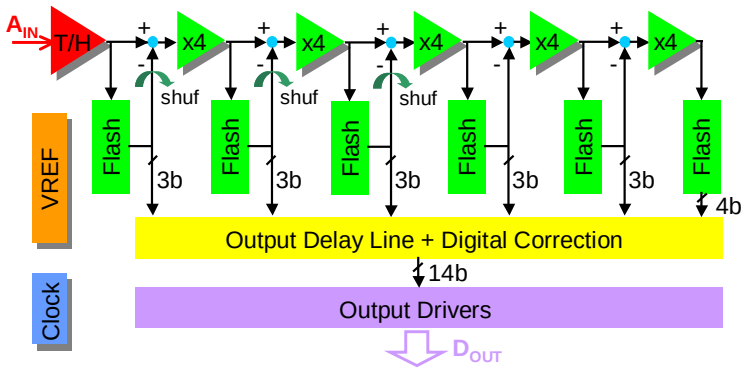

Fig. 8. Pipelined converter architecture (2.5 bit per stage), with integrated internal references and on-chip clock driver

The Analog Front-End (AFE) of the circuit is based on a Sample/Hold stage implemented with a *flip-around* architecture. This block is where the sampling of the input occurs, storing the voltage signal on capacitors by means of a CMOS switch: hence the phase stability of the clock signal opening the S/H switches is the main concern for the SNR at high IF. In fact, the sampled input voltage will vary a lot if the sampling instant occurrence is undetermined by 1ps or more. Therefore, when experimental data documenting the performance of the part are collected without optimizing the external reference source, the Signal-to-Noise Ratio (SNR) featured by the circuit rapidly degrades at high input frequencies (> 100MHz). Since the noise is largely dominated by jitter contributions at such an IF range, SNR can be determined via the well-known formula already reported in Eq. 1. By the same token, the formula can be reversed and from the SNR a jitter figure can be inferred. When this exercise is performed on the ADS5420 fed with non-optimized clock signal, featuring SNR @ 220MHz in the order of 55dBFS, the total aperture jitter affecting the S/H block turns out to be in excess of 1.3ps - well above the designed spec! Same behavior affects the performance of any other device based on the same sampling principle, even at the 12 bit level (see for example the case of a 12b 80MSps device in [7]).

Final goal of the chip designer, as well as of the PCB-designer's analysis, is to improve the clock circuit in order to reduce the jitter figure and enhance SNR. This entails the discrimination of the jitter components due to the *external* clock source, and to the *internal* clock conditioning and distribution tree. The first task can been accomplished in the lab by using a phase noise measurement system, e.g. the PN9000 by Aeroflex Comstron Inc., targeted at avionics tests (VOR), operated in phase-lock mode and fed with the clock source running at sampling rate f_s (about 30MHz in the example illustrated in Fig. 9). The plot represents the function of phase noise (*SSCR* or $L(f_n)$) vs. offset frequency f_n of the external source, as detected by this instrument.

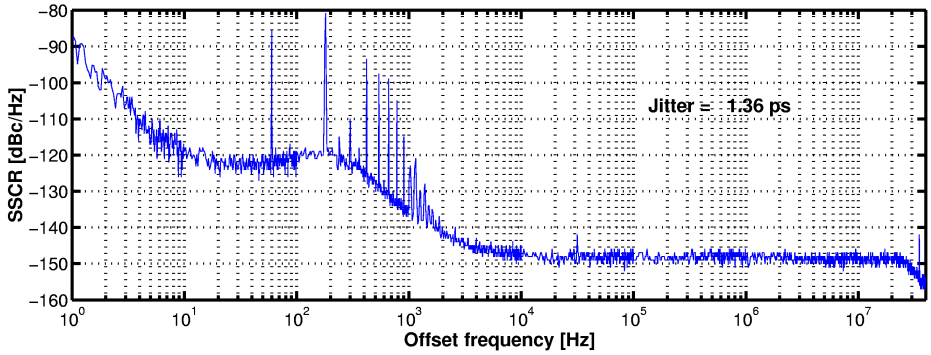

Fig. 9. *SSCR* vs. f_n offset frequency profile of the external source at 30MHz, as obtained from the Aeroflex PN9000 phase noise analyzer

The phase noise profile shown in the figure can be exported in ASCII data stream to be processed in a math program such as Matlab, and now be plugged into the formula (16), where the integral of the noise spectral density is extended from the inverse of the total observation time, about 4kHz in this case, to the maximum frequency sensed by the PN9000, about 40MHz in our setup. The experiment returns a cycle jitter as high as 1.36ps. Notice that, since the *X*-axis of Fig. 9 is logarithmic, the close-in phase noise does not matter as much, whereas the flat spectrum range extends for 3+ decades to constitute the bulk of the noise.

This is not usually the case in integrated oscillators, where the phase noise is way higher close to the carrier and swamps out the white spectrum contributions. A clear indicator of the difference between the two situations is the absolute value of the jitter: for the same center frequency, σ_{To} can be tens of picoseconds in the first case, and sub-picosecond for a good, stabilized quartz (OXCO).
Since the white floor cannot be abated, and since in the formula the $1/f_n$ roll-off of the sinc is balanced by the f_n term, the contribution of a steady white floor becomes exponentially dominant on the logarithmic abscissa of Fig. 9. But by applying again the link in Eq. 16 to the spectrum in Fig. 9 after a reasonably tight bandpass filter (4MHz bandwidth using a standard LC filter) has been used after the source, the jitter is calculated in only 25fs. The equation provided then a unique insight about the reason of this happening. Only a small fraction of the jitter (25fs against 1.36ps, or 1360fs!) actually comes from the 1kHz-1MHz span, the remainder being contributed by the floor from 10MHz to 25MHz.

These state-of-the-art numbers emphasize both the accuracy, as well as the extreme difficulty of the measurement. The contribution figured out above is to be discounted from the aperture jitter inferred from SNR by means of Eq. 1, to isolate the additional aperture uncertainty introduced by the on-chip regeneration/distribution circuitry. Finally, the RMS subtraction returns 250fs as the impact of the on-chip preamplifier / clock buffer circuit of Fig. 8, way closer to the designed-in specs. The number is fully confirmed by the improvement in SNR shown by the plot in Fig. 10, where the overall noise performance taken @ 61.44MSps and 220MHz increased dramatically from the ~54.5dBFS previously observed (w/o BP filter) to 69.3dBFS (w/BP filter).
Such an excellent aperture jitter figure can be directly measured via a novel coherent sampling technique [8], and qualifies as the best performance reported to date for CMOS-based (i.e., non-ECL/PECL) clock circuits. A figure of 250fs enables very limited roll-off in SNR at higher input frequency, as corroborated by the very intuitive plot of SNR against the full IF axis in Fig. 10. As a benefit of the jitter optimization, the low-IF performance of the ADC measured in 73.2dBFS SNR, 11.9 ENOB, 92dBc SFDR at 65Msps and 1MHz keeps to 69.3dBFS SNR, 10.7ENOB, 70dBc SFDR at 220MHz, making the ADS5420 uniquely suitable for aggressive single-downconversion receiver chains.

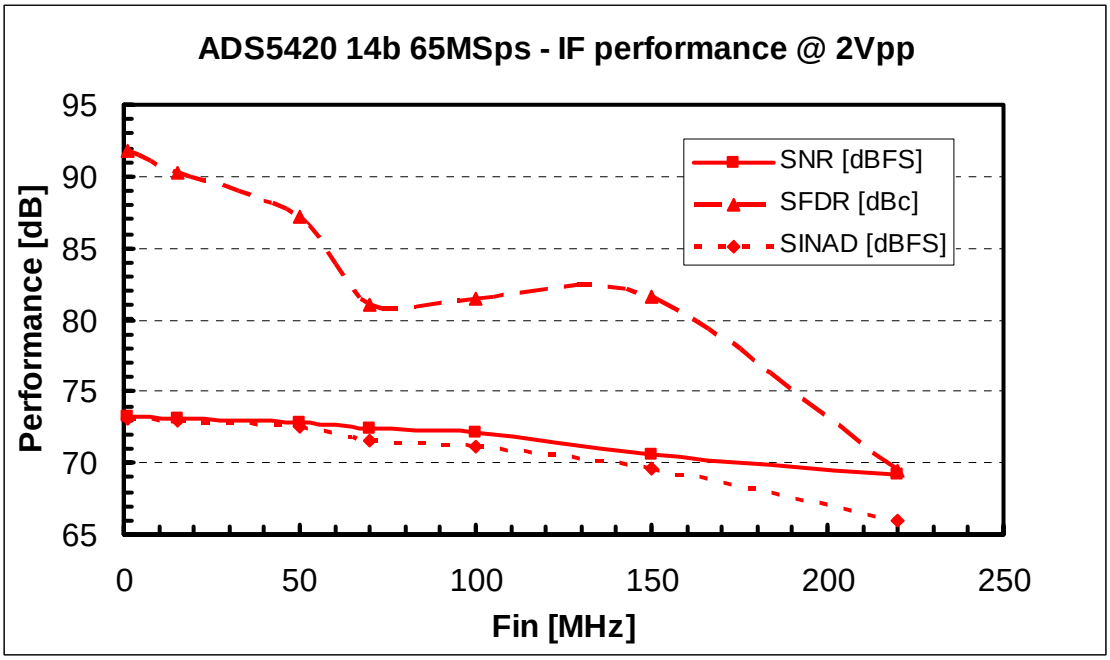

Fig. 10. f_{IN} sweep at 65MSps sampling rate on TI's ADS5420 14 bit 65MSps A-to-D converter for wireless infrastructure applications

The characteristic concave profile of the SNR starting at 100MHz IF is the signature of the prevalence of jitter contributions on the SNR from 100MHz onwards. The total power consumption of the ADC is about 1W at 65MSps, internal voltage reference, dissipated from 3.3V analog and digital supply, and 3.3V output driver supply. The latter can be lowered to 1.8V achieving yet better SNR performance, without putting in jeopardy the data capture window. When external voltage references are provided to the circuit, the consumption is lowered to about 900mW.

All data was collected with a sinusoidal input of –1dBFS amplitude, to avoid clipping. The chip is provided in standard 64-pin TQFP package with PowerPad® TI technology, which guarantees minimal performance variations between –40°C and +85°C of full temperature range operation, and from 2.7V up to 3.6V extended analog/digital supply range.

CONCLUSION

In conclusion, despite the variety of synthesizers tested and the simplicity of the final numerical tools employed, the matching between jitter estimation and measurement keeps always below 7%. In force of this, the analysis proposed and the formulas devised (Eqs. 14 and 16) become a powerful tool for the designer to interpret simulation results obtained after frequency-domain software (SpectreRF), and for the test engineer to interface SSCR specs with jitter specs in order to perform calculations to dis/aggregate the data along the clock chain, and optimize the setup for best jitter parameter.

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TO PROBE FURTHER

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