LED Driver Based on UCC28060 Interleaved ACDC Single Stage Flyback

Application Report

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ABSTRACT

UCC28060 can be implemented in an ACDC single stage solution with transition mode interleaved Flyback topology. This note will discuss the design considerations and give a practical design example.

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1 Single stage LED lighting Introduction

A recent trend in LED lighting is to implement the driver with a single stage offline ACDC. A single stage ACDC employs only one controller and one Flyback power stage to implement an isolated PFC (power factor correction) solution. The benefit is a very low BOM cost and high efficiency.

The usual approach is to employ a transition mode Flyback topology for increased efficiency, as well as a regulated constant t_{on} (switch on-time) to implement the PFC. This solution can significantly decrease the turn-on power loss not only in the main MOSFET, using valley voltage mode, but also the turn-off power loss in the secondary side rectifier with ZCS (zero current switching).

However, the one phase transition mode, with boundary current mode in the transformer, produces much higher input and output ripple current than continuous current mode. This significantly reduces EMI performance and efficiency, so that a bigger EMI filter is necessary. The higher the power rating of the ACDC, the higher the ripple current and EMI filter volume. Moreover, very high peak currents in a one phase single stage LED driver may increase the risk and cost on the main MOSFET and output rectifier.

An interleaved transition mode PFC controller such as the UCC28060, can be used to implement an interleaved, two phase single stage Flyback, which significantly decreases the ripple current due to the ripple current cancellation effect. Thereby the input EMI filter and output capacitor volume can be decreased greatly. It also allows for higher flexibility in selecting the MOSFET, rectifier etc. because they only handle half the peak current of the original single phase.

2 Design considerations

2.1 Transition mode single stage analysis

Using the following parameter definitions and analysis of the transition mode single stage flyback can be performed.

AC input voltage (RMS): V_{AC}; Line AC frequency: f_{AC}; Rated input power: Pin

Output voltage: V_O; Transformer turns ratio: $n=Np/Ns$;

Let: $\omega = 2\pi f_{AC}$;

On the primary side, it's essential that the transition mode single stage can maintain the switching current and input average current as shown in figure1.

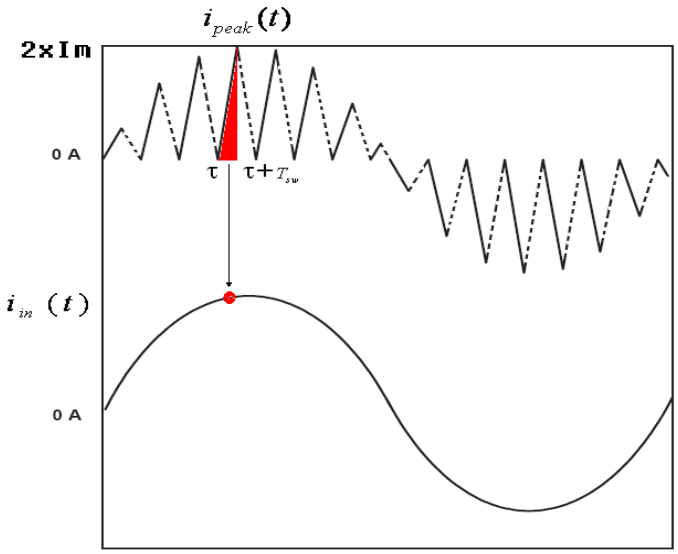

Figure 1. Primary side switching current and input average current waveforms.

During the high frequency switching cycle t∈[τ, τ+T_{sw}], the duty cycle and primary side peak current should follow the equations below:

$$D(\omega t)=\frac{nV_o}{nV_o+\sqrt{2}V_{AC}Sin(\omega t)};\ i_{peak}(\omega t)=\frac{\sqrt{2}V_{AC}t_{ON}}{L_p}Sin(\omega t)$$

Let: $K=\frac{\sqrt{2}V_{AC}}{nV_o}$, And $I_m=\frac{\sqrt{2}V_{AC}}{2L_p}t_{ON}$, then the duty cycle is:

$$D(\omega t)=\frac{1}{1+K\times Sin(\omega t)};\ \text{And peak current}\ i_{peak}(\omega t)=2I_mSin(\omega t)$$

As a result, during the high frequency switching cycle $t \in [\tau, \tau+T_{sw}]$, the continuous input current can be solved as below:

$$i_{in}(\omega t) = I_m \frac{Sin(\omega t)}{1 + K \times Sin(\omega t)} \quad \text{(Eq.1)}$$

Considering a practical design for peak current mode, “K” should be greater than “1”.

The above equation shows the input current isn’t a pure sine wave, but contains higher order harmonic elements.

The total input RMS current can be found as below:

$$I_{in} = \sqrt{\frac{\int_0^{\pi} i_{in}^{2}(\omega t)\, d\omega t}{\pi}} = \frac{I_m}{\sqrt{\pi}} \sqrt{\int_0^{\pi} \frac{Sin^{2}(\omega t)}{(1 + K \times Sin(\omega t))^{2}} d\omega t}$$

Then,

$$I_{in} = \frac{I_m}{\sqrt{\pi}K} \sqrt{\pi - 4K + 2\frac{(2K^2-1)}{(K^2-1)}\left(K + \frac{Ln(K-\sqrt{K^2-1})}{\sqrt{K^2-1}}\right)} \quad \text{(Eq.2)}$$

Considering the harmonic elements of the input current, the 1st harmonic RMS current would be:

$$I_{1RMS} = \frac{1}{\sqrt{2}}\frac{2}{\pi}\int_0^{\pi} i_{in}(\omega t) Sin(\omega t) d\omega t = \frac{\sqrt{2}}{\pi}\int_0^{\pi} I_m \frac{Sin^2(\omega t)}{1 + K \times Sin(\omega t)} d\omega t$$

Then:

$$I_{1RMS} = \frac{\sqrt{2} I_m}{\pi K^2}\left[2K - \pi + \frac{2Ln(K+\sqrt{K^2-1})}{\sqrt{K^2-1}}\right] \quad \text{(Eq.3)}$$

In practice, most of the input power comes from the input line AC voltage times the 1st harmonic RMS current.

The total harmonic distortion “THD” should be:

$$THD = \sqrt{1 - \frac{2\left(2K - \pi + 2\frac{Ln(K+\sqrt{K^2-1})}{\sqrt{K^2-1}}\right)^2}{\pi K^2\left[\pi - 4K + \frac{2(2K^2-1)}{K^2-1}\left(K + \frac{Ln(K-\sqrt{K^2-1})}{\sqrt{K^2-1}}\right)\right]}} \quad \text{(Eq.4)}$$

Figure 1 shows how THD changes with different “K” values.

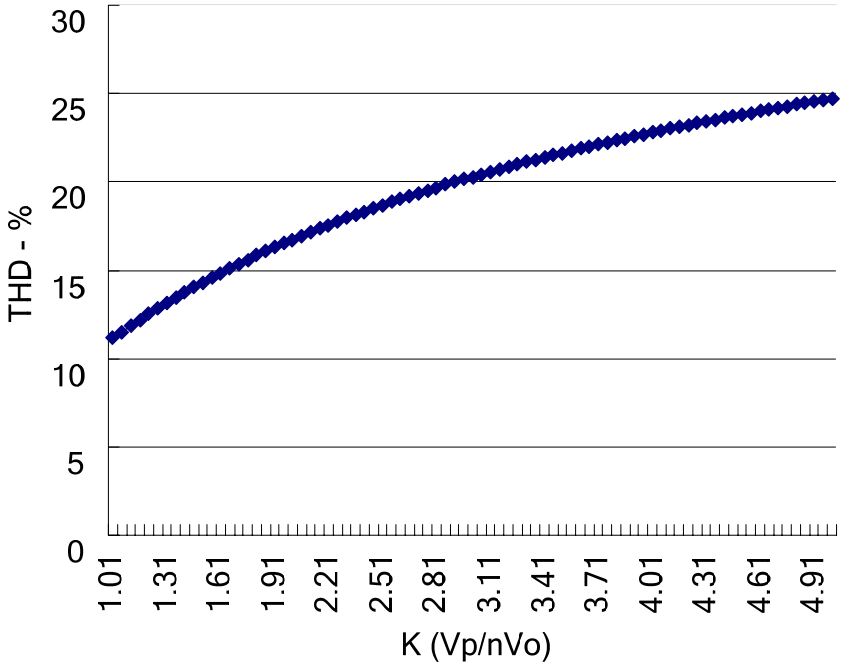

Figure 2. THD Vs. K (K=Vp/nVo)

Figure 2 shows that increasing “K” increases “THD” (total harmonic distortion). Also, the higher the input voltage, the higher the “THD”. The transformer turns ratio, n (n=Np/Ns) should be high enough to allow for a lower “K”.

Then the calculated values for the primary side parameters can be found in table 1.

Table 1. Parameter table for primary side single stage

K (K=1.414xVin/nVout)	I_{1RMS}/I_m	I_{in}/I_m	THD(%)
1.1	0.369906584	0.372508356	11.79836876
1.7	0.294776679	0.298289401	15.30155777
2.3	0.245307257	0.249340574	17.91373988
2.9	0.210200682	0.214517309	19.95998672
3.2	0.196199425	0.200599691	20.83025343
3.35	0.18988264	0.194313938	21.2343145
3.5	0.183963855	0.188420071	21.61978758

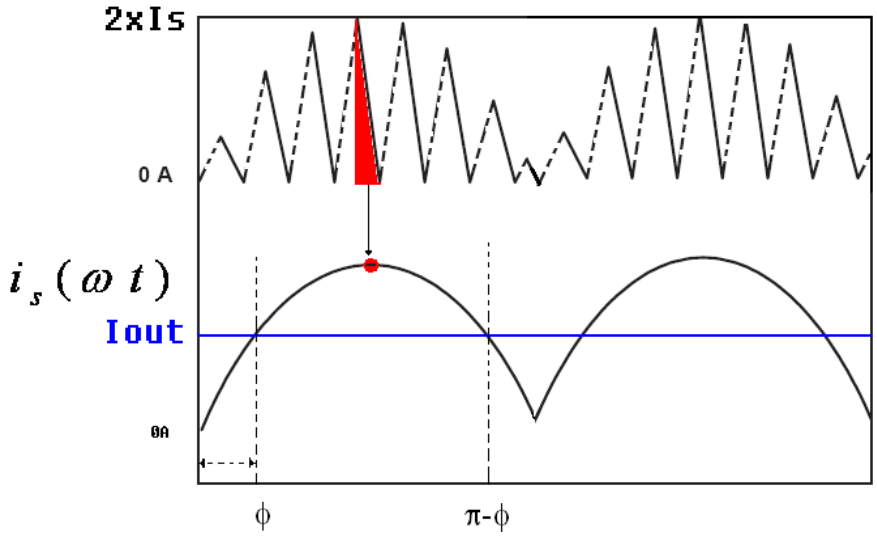

Figure 3. Secondary side peak current and average current waveforms.

On the transformer secondary side, during the high frequency switching cycle t∈[τ, τ+T_{sw}], the average output current of the secondary side transformer can be found as below:

$$i_s(\omega t) = I_S Sin(\omega t)[1 - D(\omega t)] = I_S \frac{K \times Sin^2(\omega t)}{1 + K \times Sin(\omega t)}$$

2 x I_S is the peak current of the secondary side transformer.

Consider a low frequency cycle ωt∈[0,π], during ωt∈[ϕ,π-ϕ], the output capacitor is being charged, and during ωt∈[0,ϕ]∪[π-ϕ,π], the output capacitor is being discharged. Then:

$$i_s(\phi) = I_{out} = I_S \frac{KSin^2\phi}{1+KSin\phi}$$

$$I_{out}\pi = \int_0^{\pi} i_S(\omega t)d\omega t$$

Then:

$$I_{out} = \frac{I_S}{\pi K}[2K - \pi + \frac{2Ln(K+\sqrt{K^2-1})}{\sqrt{K^2-1}}] \quad \text{(Eq.5)}$$

And

$$\frac{\pi Sin^2\phi}{1+KSin\phi} = \frac{[2K - \pi + \frac{2Ln(K+\sqrt{K^2-1})}{\sqrt{K^2-1}}]}{K^2} \quad \text{(Eq.6)}$$

According to table 2 and figure 4, the approximated rectifier angle "ϕ" is 0.72rad.

Obviously the ripple frequency in the secondary is double the line AC frequency. An approximated analysis is to use the 1st harmonic element to estimate the output ripple. Based on this assumption, we can get the results below:

Consider the AC current part, $i_s(t) - I_{out}$, and a doubled AC line frequency, the amplitude of the 1st harmonic element should be:

$$I_{SAC-1} = \frac{2}{\pi}\int_0^{\pi}[I_{out} - i_s(\omega t)]Cos(2\omega t)d\omega t$$

Then:

$$I_{SAC-1} = \frac{8I_s}{\pi K^3}[\frac{2}{3}K^3 - \frac{\pi}{4}K^2 + K - \frac{\pi}{2} + \frac{Ln(K+\sqrt{K^2-1})}{\sqrt{K^2-1}}] - 2I_{out} \quad \text{(Eq.7)}$$

$$\frac{I_{SAC-1}}{I_{out}} = \frac{8}{K^2}\frac{[\frac{2}{3}K^3 - \frac{\pi}{4}K^2 + K - \frac{\pi}{2} + \frac{Ln(K+\sqrt{K^2-1})}{\sqrt{K^2-1}}]}{[2K - \pi + \frac{2Ln(K+\sqrt{K^2-1}}{\sqrt{K^2-1}}]} - 2 \quad \text{(Eq.8)}$$

Table 2 and Figure 4 reveals a critical phenomena is the current ratio "I_{SAC-1}/I_{out}", it is almost constant with an approximated value of 0.85.

2.1.1 With “CC” load

The output peak to peak ripple voltage:

$$\frac{U_{p-p}}{I_{out}} = \frac{I_{SAC-1}}{I_{out}} \times \frac{1}{2\pi f_{AC} C_{out}} \approx \frac{0.85}{2\pi f_{AC} C_{out}} \quad \text{(Eq.9)}$$

The calculated values for the secondary side parameters for various K values can be found in table 2.

Table 2. Parameter table for secondary side.

K **(K=1.414xVin/nVout)**	I_s/I_{out}	ϕ **(RAD)**	U_{p-p}/I_{out} **(C=1mF)**	I_{SAC-1}/I_{out}
1.1	3.475604	0.7411552	2.352463628	0.886859968
1.7	2.822104	0.7300354	2.267692253	0.854901838
2.3	2.506552	0.7225061	2.206355423	0.831778344
2.9	2.319973	0.7171003	2.15957335	0.814141876
3.5	2.196415	0.7130522	2.122532599	0.800177809

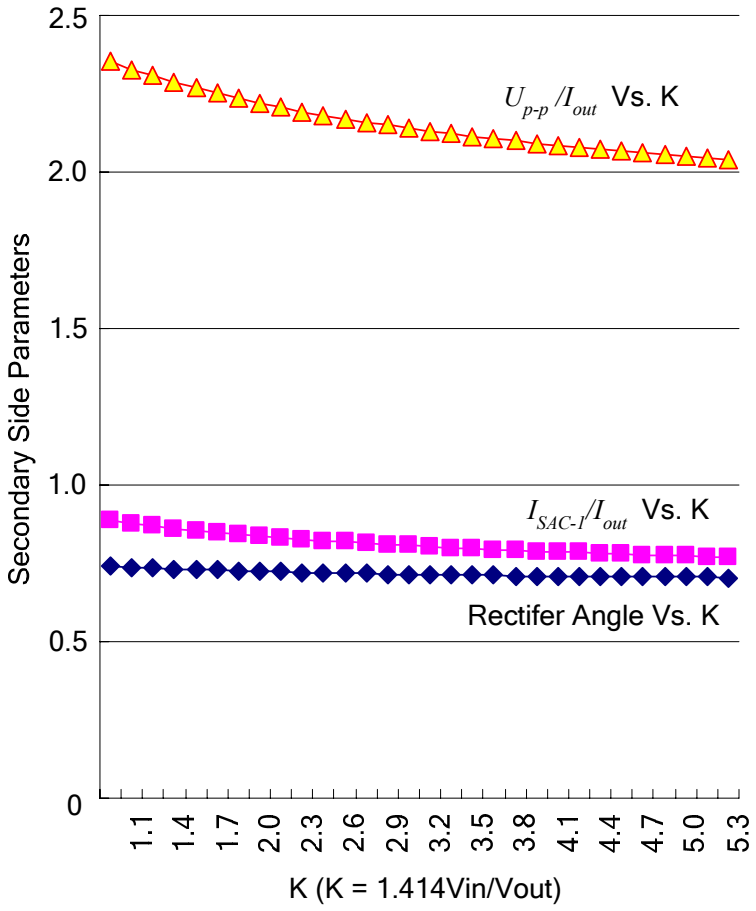

Figure 4. Secondary side parameters Vs. "K" with "CC" load.

With "LED" or "CR" load setup, the ripple current flowing into capacitor "Cout" can be decreased by a part of it flowing into "RLED" or "RL", which decreases the output ripple voltage significantly. The lower the "RLED" or "RL" resistance, the lower the output ripple voltage.

2.1.2 With “LED” load

A typical “V-I” characteristic of an LED:

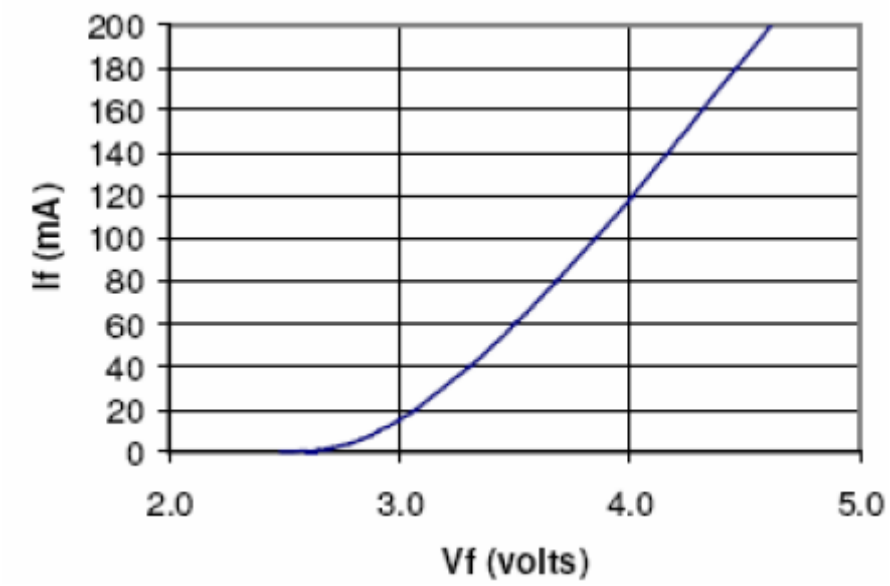

Figure 5. A typical V/I characteristic of a single die LED

$R_{LED} = n_{LED} \frac{\Delta V_{LED}}{\Delta i_{LED}}\Big|_{I_{LED}=I_{out}}$; This represents the slope rate at the working point specified for the light brightness.

“n_{LED}” is the quantity of the LEDs in series.

Based on the V/I characteristic, the practical electrical characteristic can be simulated by the circuit below :

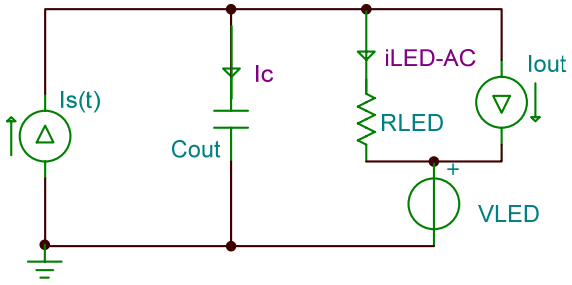

Figure 6. Dynamic model for an LED load

The output peak to peak ripple voltage Up-p should be:

$$\frac{U_{p-p}}{I_{out}} = \frac{I_{SAC-1}}{I_{out}} \times \frac{2R_{LED}}{\sqrt{1+16\pi^2 R_{LED}^2 C_{out}^2 f_{AC}^2}} \approx \frac{1.7R_{LED}}{\sqrt{1+16\pi^2 R_{LED}^2 C_{out}^2 f_{AC}^2}} \quad \text{(Eq.10)}$$

With RLED=3R & Cout=1000uF, the secondary side parameters are as shown in Figure 7.

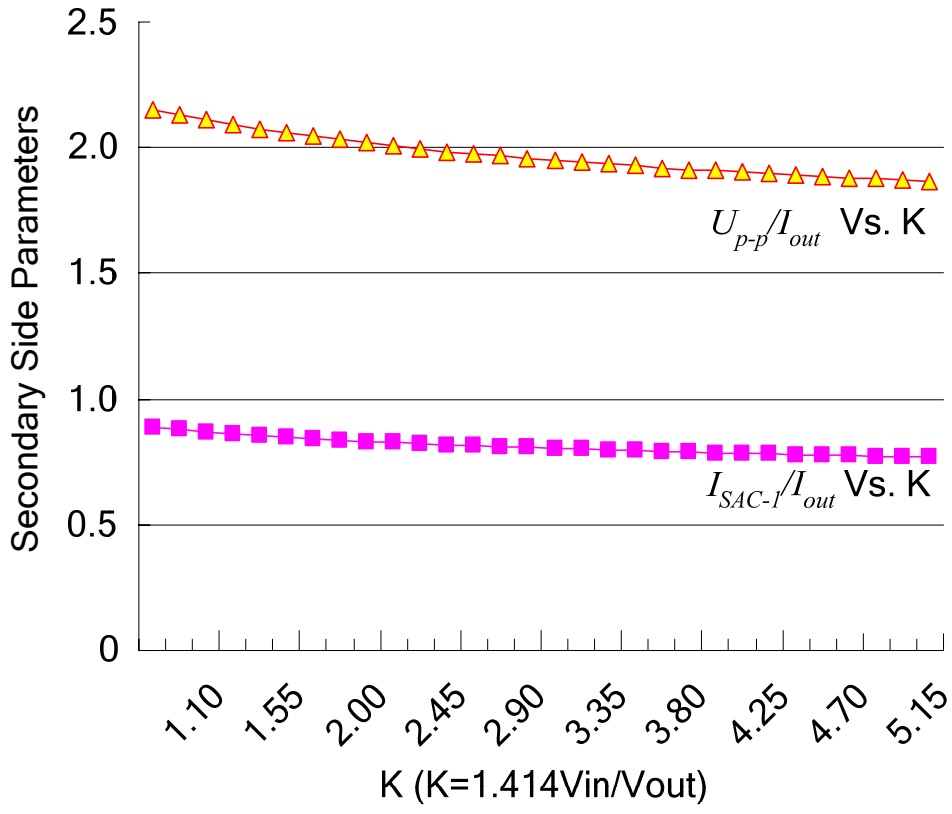

Figure 7. Secondary side parameters Vs "K" with "LED" load (Cout=1000uF, RLED=3R)

2.1.3 With “CR” load

Similar to the “LED” load, the output peak to peak ripple voltage will be:

$$\frac{U_{p-p}}{I_{out}} = \frac{I_{SAC-1}}{I_{out}} \times \frac{2R_L}{\sqrt{1+16\pi^2 R_L^2 C_{out}^2 f_{AC}^2}} \approx \frac{1.7R_L}{\sqrt{1+16\pi^2 R_L^2 C_{out}^2 f_{AC}^2}}$$

2.2 Ripple current cancellation of UCC28060 single stage

The UCC28060 employs natural interleaving transition mode control. Two flyback power stages work in transition mode allowing for lower switching power dissipation in the MOSFET and rectifier because of valley voltage switching in MOSFET and zero current turn-off of the secondary side rectifiers, this also results in a better EMI performance. Furthermore, considering the higher input peak current in transition mode than in average mode, UCC28060’s natural interleaving mode, with peak current ripple cancellation, can significantly decrease the current ripple, which benefits the volume reduction of the EMI filter, and also increases the efficiency.

2.3 Interleaved single stage design considerations for the UCC28060

Step 1: Define the input maximum power, AC voltage range and output voltage range:

$$P_{MAX}; V_{ACMIN}; V_{ACMAX}; V_{outMAX}; V_{outMIN}$$

Step 2: Transformer design.

$$K = \frac{\sqrt{2}V_{ACMIN}}{nV_{outMAX}} > 1$$

According to the THD analysis in 2.1, a lower “K” produces a lower “THD”. So for example we can let K=1.1 at low line. Thereby we can get a turns ratio “n” for the transformer.

At low line input:

A. the 1st harmonic RMS current in each phase will be:

$$I_{1RMS} = \frac{P_{MAX}}{2V_{ACMIN}};$$

B. Assuming a minimum operating frequency is “f_{MIN}”, then the constant On-Time is

$$t_{on} = \frac{1}{f_{MIN}(1+K)} \qquad \text{(Eq.11)}$$

According to Eq.3, we can get “I_m” as

$$I_m = \frac{I_{peak}}{2} = \frac{\sqrt{2}V_{ACMIN}}{2L_p} t_{on} \quad \text{(Eq.12)}$$

Per the above "t_{on}" and "I_m", we can find the primary side inductor value "L_p".

Step 3. From the datasheet for the UCC28060:

$$t_{on} = K_T(V_{comp} - 125mv)$$

Using "t_{on}" and "K_T", a maximum "V_{comp}" at low line can be calculated. An optimized "K_T" can be used to set up a suitable "V_{comp}", considering a typical limit value of 4.95V.

A resistor on "TSET" pin of the UCC28060 can configure an optimized "K_T".

Step 4. According to equation 9, the output capacitor can be selected by the pre-decided output low frequency peak to peak ripple voltage:

According to equation 9, or table 2, as input AC Line varies from 85V to 265V, or K varies from "1.1" to "3.4", assuming an output peak to peak ripple voltage range, then the output capacitor value can be found.

3 Loop stability analysis

Consider the boundary mode, the magnetizing current of the transformer will be discharged fully, and the lossless resistor “Rm” and constant transferred power “P” model can be used to describe the average model per figure 8.

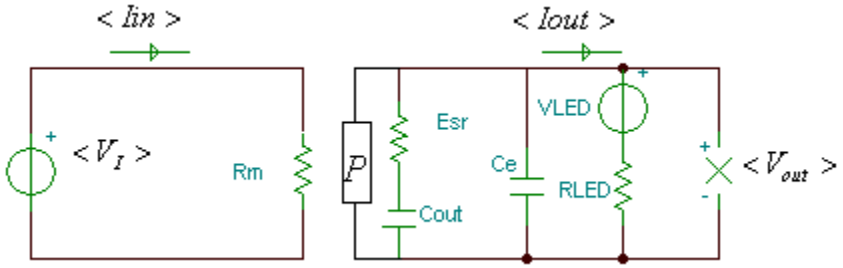

Figure 8. The average model of the single stage

Here, $Rm = \dfrac{2L_p(1+\dfrac{<V_I>}{n<V_{out}>})}{t_{on}}$; And $P = \dfrac{<V_I>^2}{Rm}$

Note, <*> means the average value during a switching cycle.

The small signal circuitry can be found as in figure 9:

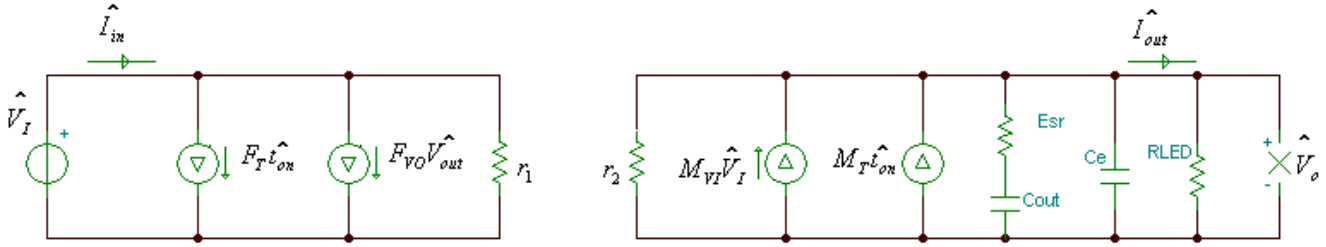

Figure 9. The small signal model of the single stage

And,

$$F_T = \frac{V_I}{2L_p(1+\frac{V_I}{nV_o})};\quad F_{VO} = \frac{V_I^2 t_{on}}{2nL_p V_{out}^2(1+\frac{V_I}{nV_{out}})^2};\quad r_1 = \frac{2L_p(1+\frac{V_I}{nV_{out}})^2}{t_{on}}$$

$$M_T = \frac{V_I^2}{2L_p(1+\frac{V_I}{nV_{out}})V_{out}};\quad M_{VI} = \frac{V_I(2+\frac{V_I}{nV_{out}})t_{on}}{2L_p V_{out}(1+\frac{V_I}{nV_{out}})^2};\quad r_2 = \frac{2L_p(1+\frac{V_I}{nV_{out}})^2 V_{out}^2}{V_I^2 t_{on}}$$

Here, $V_I = \sqrt{2}V_{AC}$

Thereby, the control block diagram can be implemented as in figure10:

Consider the low frequency ripple, a lower crossover frequency is necessary to dampen the low frequency ripple caused by the input AC voltage. The recommended crossover frequency should be far less than the AC line frequency.

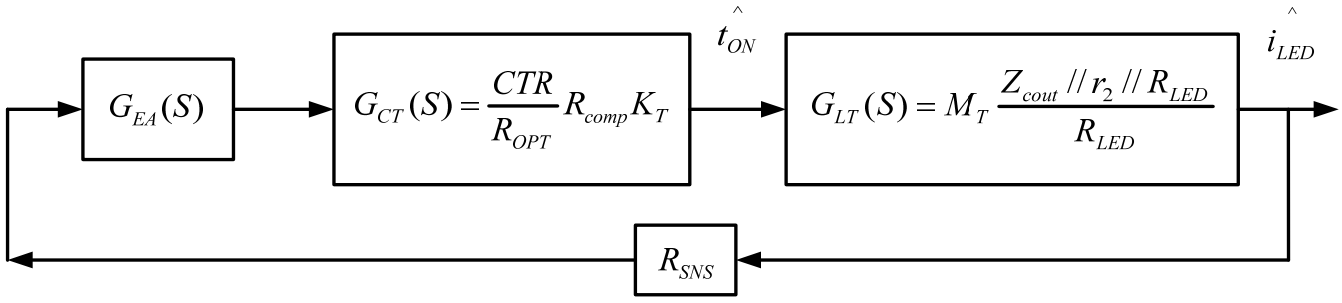

Figure 10. The LED current closed loop control implementation

4 A practical interleaved single stage LED driver design based on the UCC28060

$P_{MAX} = 60W; V_{ACMIN} = 85V; V_{ACMAX} = 265V; V_{out} = 35V$

Using the steps in section 2.3, assuming "f_{MIN}=65Khz" and "K=1.1" at low line input AC voltage, the transformer can be designed as below:

L_p = 440uH; n = 3

At low line input, on time of the UCC28060 is 7.12us.

At high line input, on time of UCC28060 is 1.46us.

The input current and 1st harmonic element in phase A or B can be simulated as below:

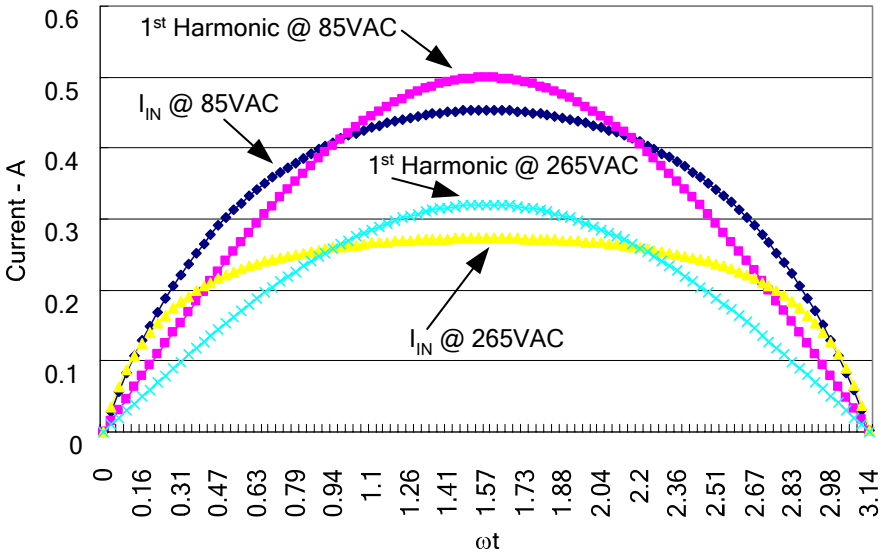

Figure 11. Input RMS current and its 1st Harmonic at 85VAC & 265VAC

Output capacitor on the secondary side:

According to table 2, as input AC line varies from 85V to 265V, or K varies from "1.1" to "3.4", assuming "RLED=3R", and the output peak to peak ripple voltage is within 1.7V, then the output capacitor can be selected based on equations (8) and (10).

$$I_{out} = \frac{60W}{35V} = 1.7A$$

Then $$\frac{U_{p-p}}{I_{out}} = \frac{1.7}{1.7} = 1$$

$$C_{out} \approx 2200uF$$

As a result, we can use 3x 680uF/68V Capacitors in parallel for the output capacitor configuration.

Loop compensation consideration:

According to the compensation solution in figure 9, loop compensation can be implemented as figure 9. The simulated closed loop regulation bode plot are shown in figures 12 and 13.

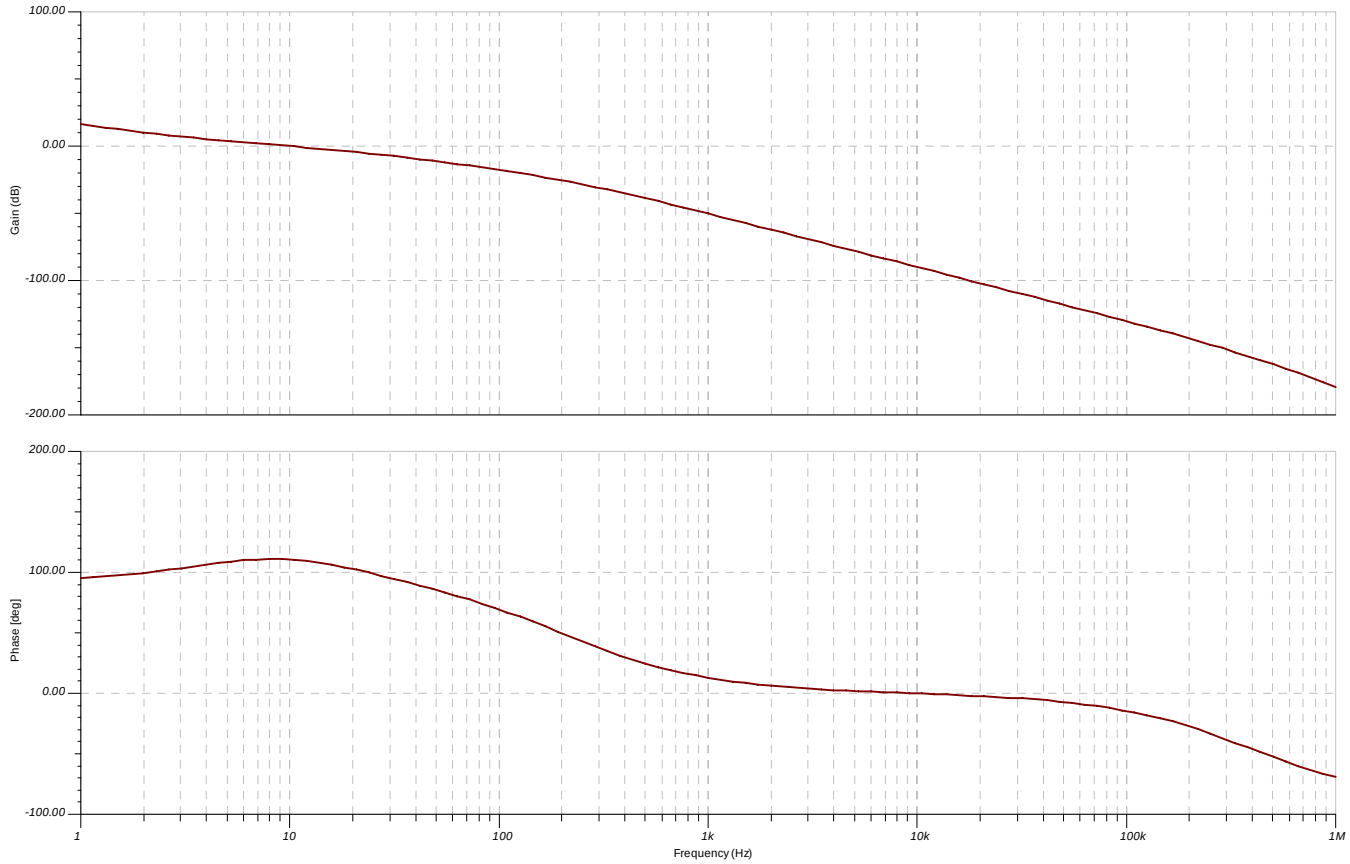

Figure 12. Closed-loop compensation with 85V line input

At 85V AC input, the phase margin is 110^{O}, and crossover frequency is 10Hz.

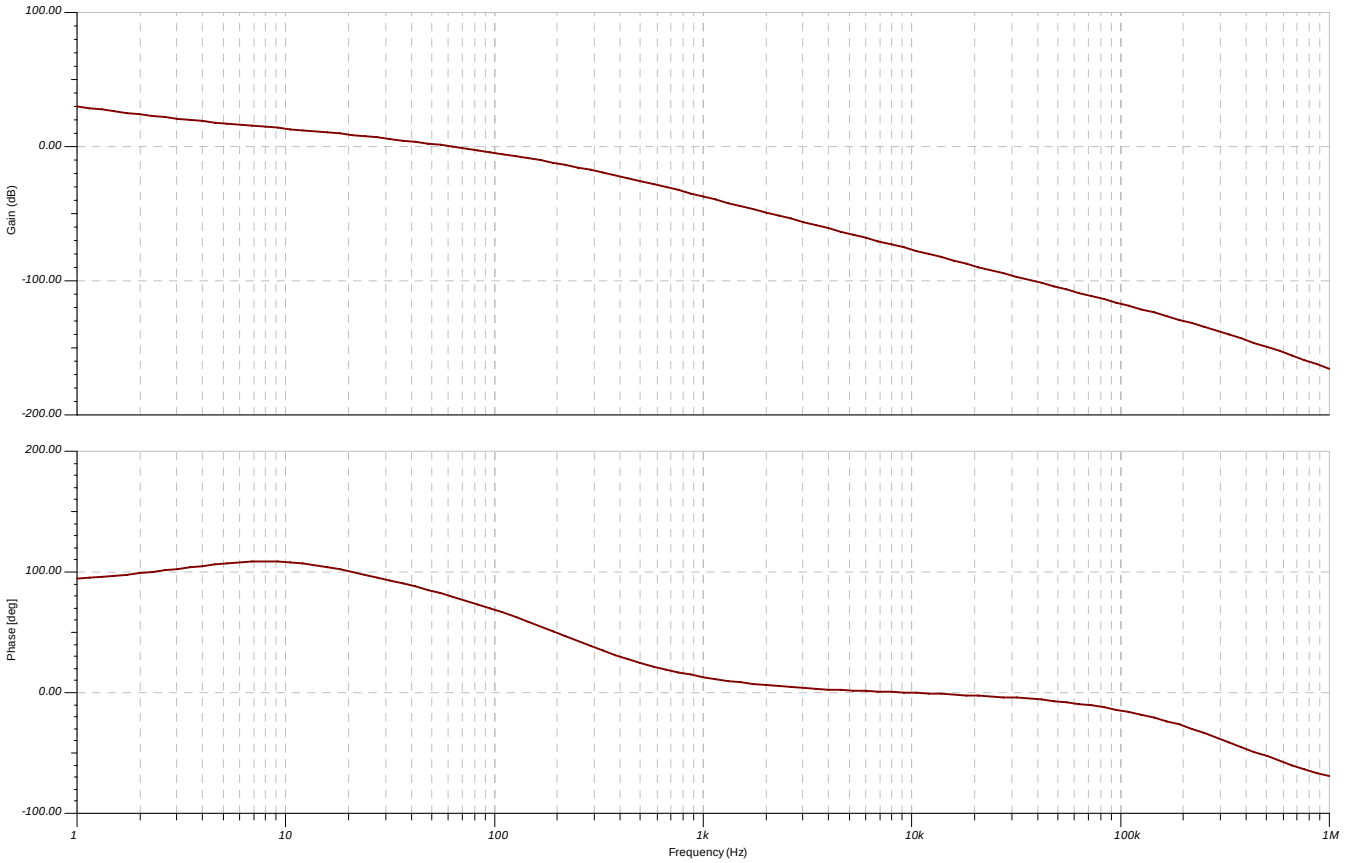

Figure 13. Closed-loop compensation with 265V line input

With 265VAC input, phase margin is 80^{O}, and crossover frequency is 60Hz.

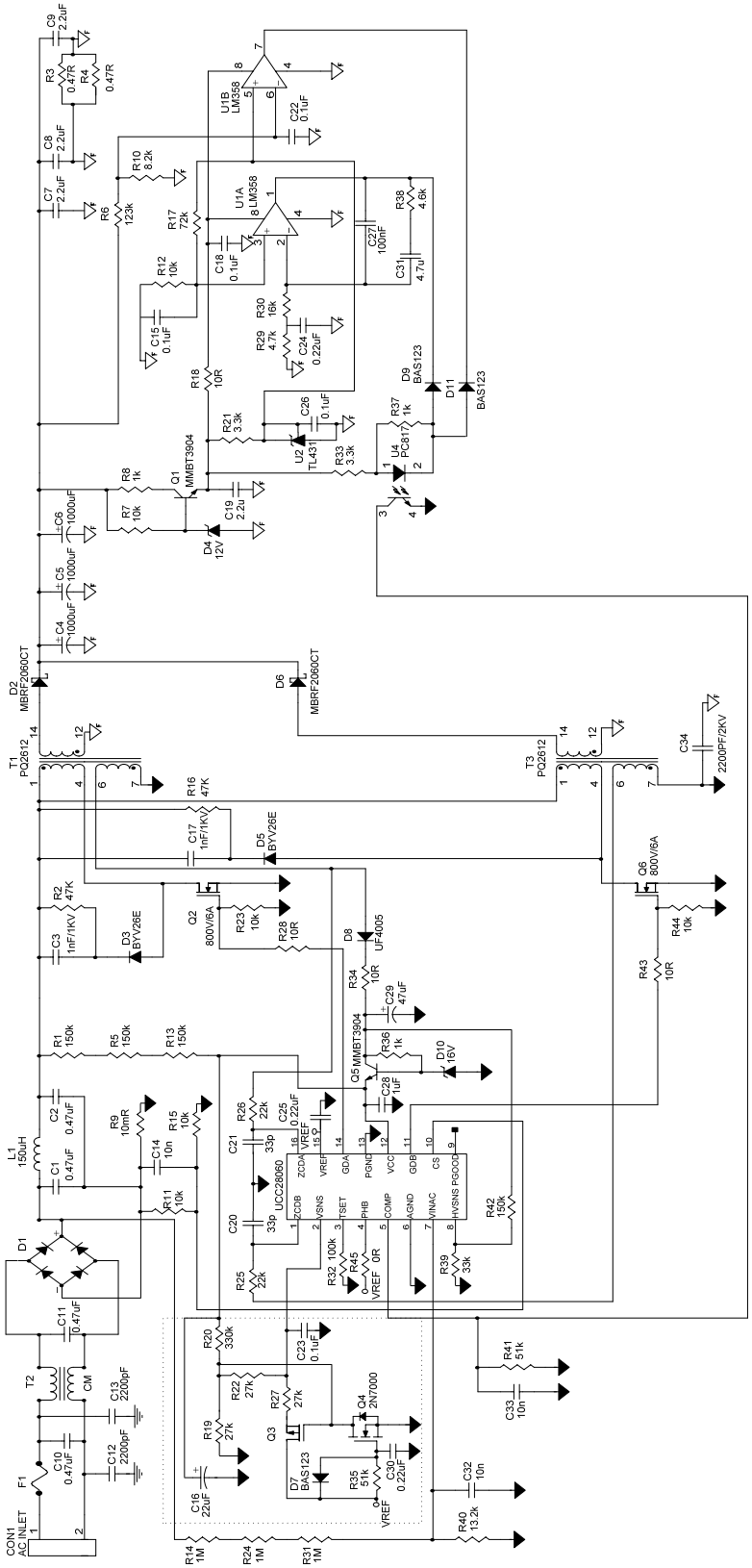

Figure 14. A 60W LED driver overall schematic

5 150W Interleaved Single Stage Design and Test Results

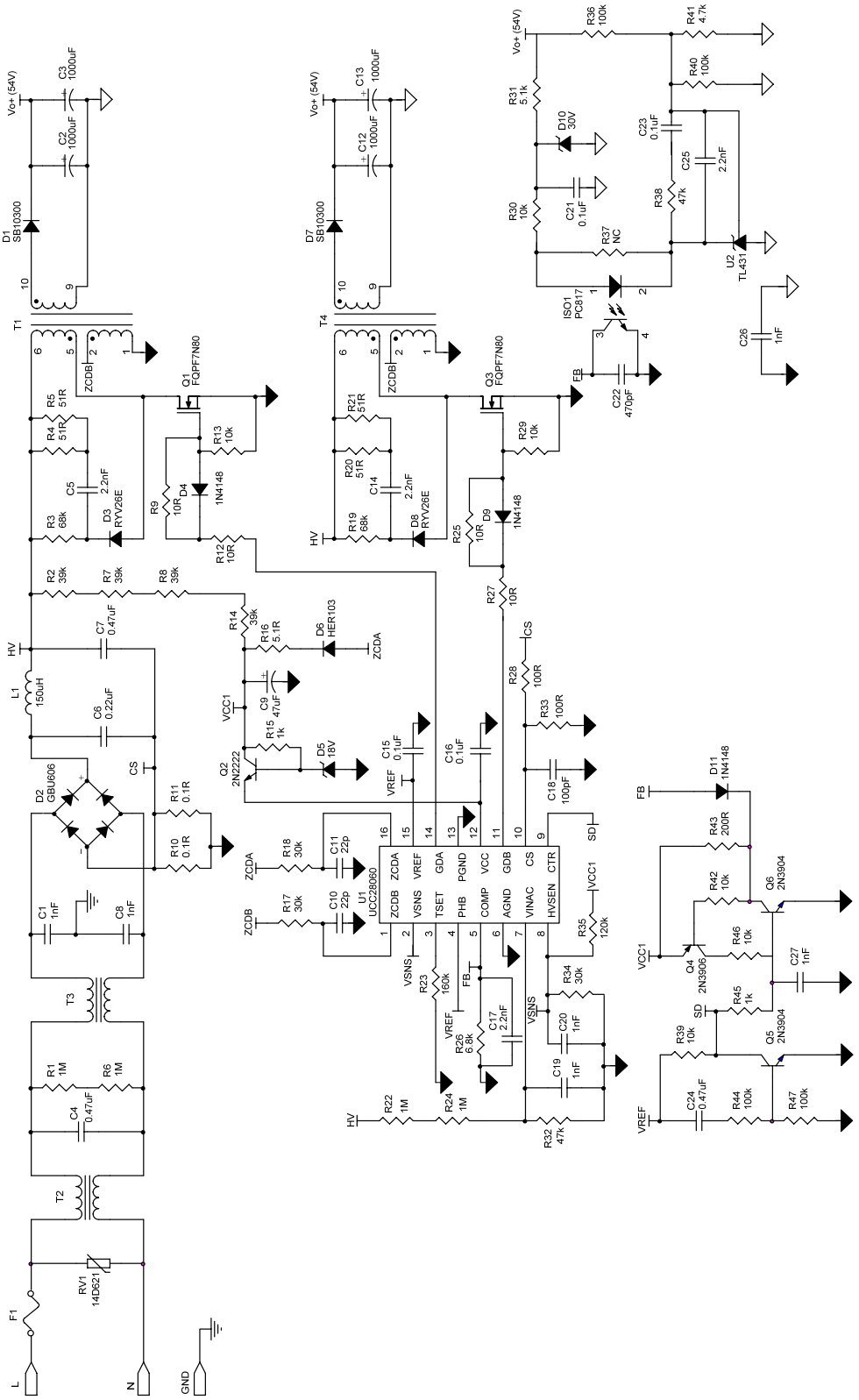

Figure 15. 150W Interleaved Single Date Schematic

5.1 Test Data

5.1.1 Efficiency versus Line

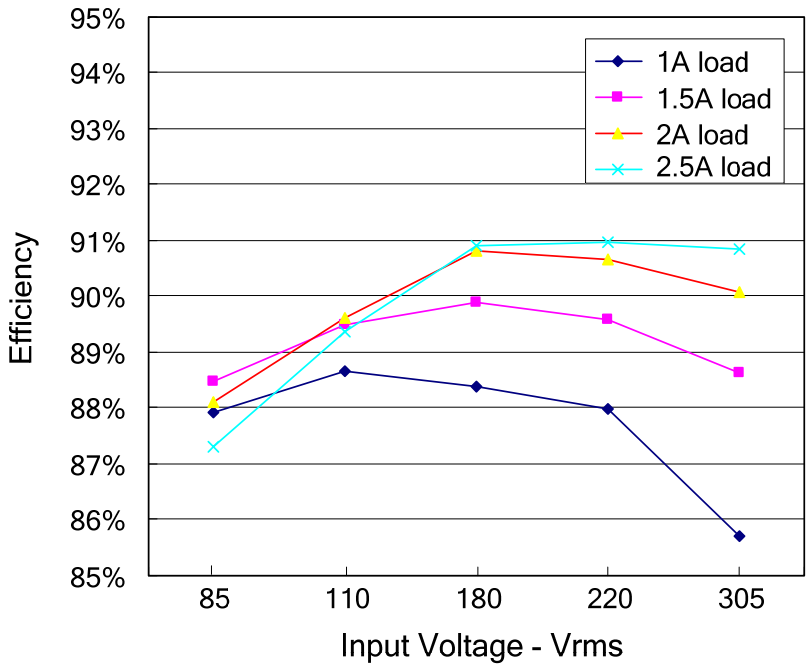

Figure 16. 150W Efficiency versus input voltage and load

5.1.2 Power Factor versus Line Voltage

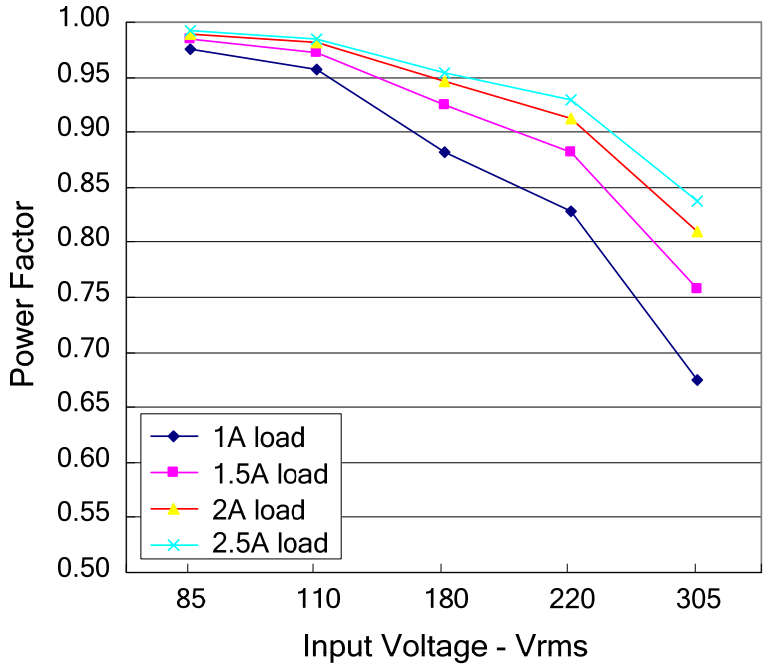

Figure 17. Power factor versus input voltage and load

5.1.3 Output Peak to Peak Ripple Voltage

Test conditions: Input = 220Vrms at 50Hz. Output current 3A.

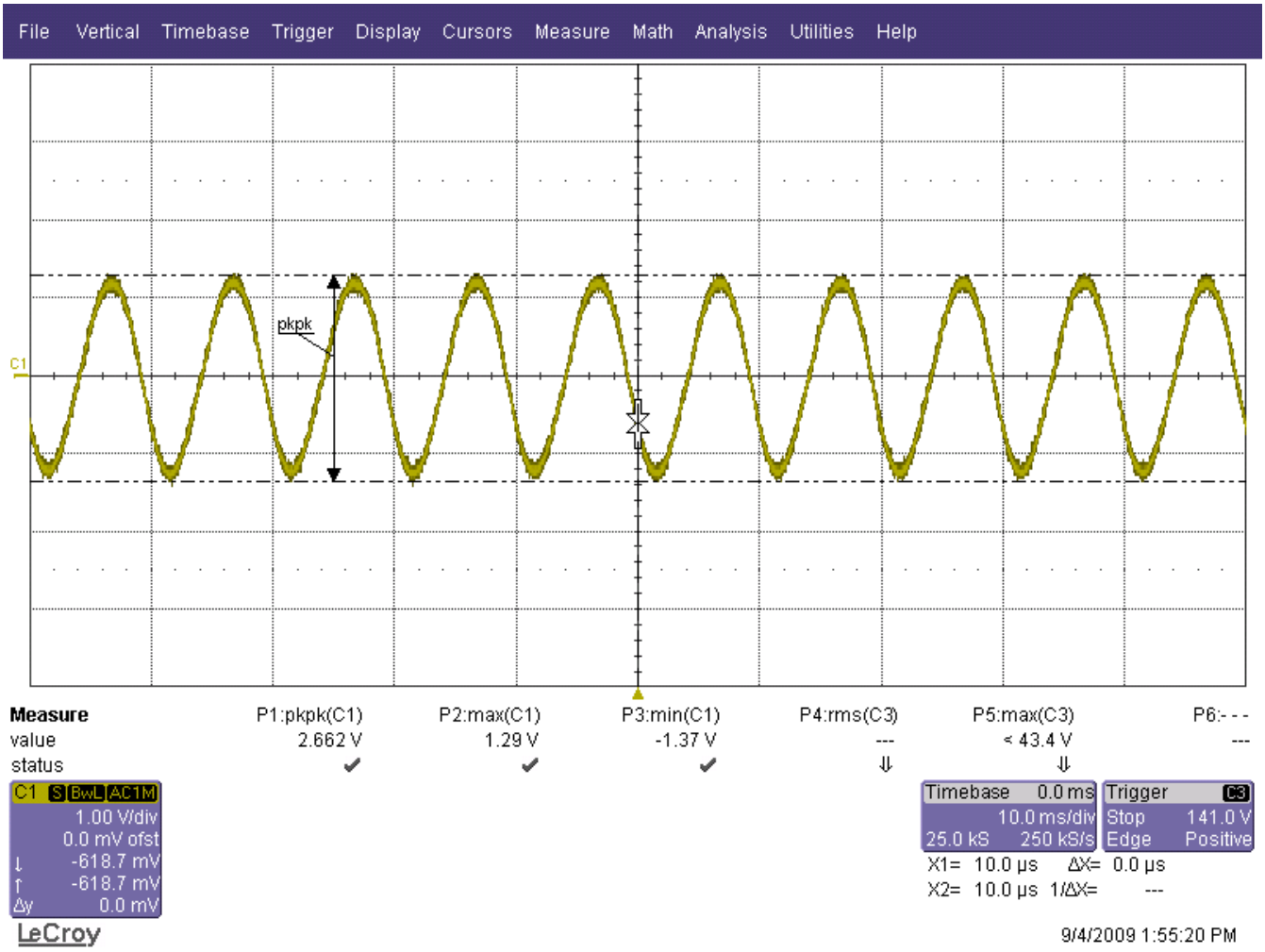

Figure 18. Output peak to peak ripple voltage, 2.6Vpp

6 Conclusion:

This note shows the analysis of a single stage Flyback LED driver, and the benefit of using an interleaved single stage topology for an LED driver based on the UCC28060. Meanwhile, a practical design has been implemented. It showed UCC28060 solution benefits with low cost and high efficiency.

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