Application Report
SCAA119–September 2012

Crystal Oscillator Performance of the CDCLVC1310

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ABSTRACT

Limiting the current flowing into a crystal resonator is crucial for extending its lifetime. Crystal manufacturers specify the maximum power the crystal resonator can dissipate without degrading the lifetime, also called drive level. To obtain the maximum drive level the current dissipated in the crystal has to be controlled by the oscillator IC. This is done with a damping resistor. This application note provides a simple guide for choosing the right damping resistor in different applications for the CDCLVC1310.

In addition, this application note presents data demonstrating the ultra-low phase-noise outputs of the CDCLVC1310 when used as crystal buffer.

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1 Introduction

The CDCLVC1310 is a highly versatile, low-jitter, low-power clock fanout buffer which distributes one of three inputs to ten low-jitter LVCMOS clock outputs. The device primary and secondary inputs features differential or single-ended signals and a third input adds a crystal input. Such a buffer is intended for use in a variety of wireless and wired infrastructure, data communication, computing, low power medical imaging and portable test and measurement applications. The input is fail-safe proved and translate any illegal input level, into a defined output state. The core can be set to 2.5 V or 3.3 V and output can be set to 1.5 V, 1.8 V, 2.5 V or 3.3 V. The CDCLVC1310 is easily configured through pin programming. The overall additive jitter performance is 30 fs_{RMS} (typ).

The shown test results were obtained under ideal conditions (clean power supply, no other noise source (such as close-by ICs) near the device under test and room temperature).

2 CDCLVC1310 used as Crystal Buffer

The CDCLVC1310 distributes 10 low-noise copies of the crystal input signal. The oscillator stage accepts crystals from 8 MHz up to 50 MHz. Figure 1 shows the typical wiring and the typical on-chip load capacitance.

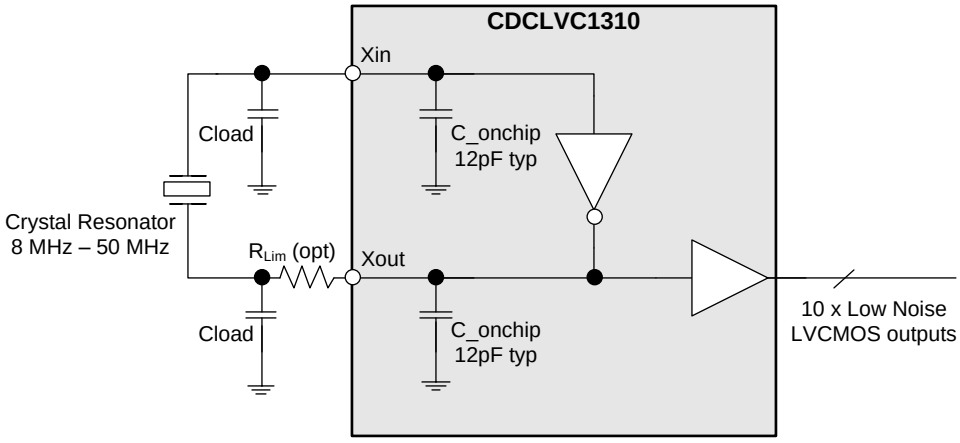

Figure 1. Simplified Block Diagram: CDCLVC1310 used as Crystal Buffer

3 Choosing the Right damping Resistor R_{Lim}

This section explains the typical crystal specifications and provides a simple lookup table to choose the right damping resistor if the CDCLVC1310 is used as a crystal buffer.

3.1 Typical Crystal Specifications

Load capacitance (CL) is the value measured or calculated across the connection points of the crystal. It is used to fine tune the crystal frequency.

By knowing the total CL from the crystal specification and C_onchip from the datasheet, it is possible to calculate the additional external Cload.

$$C_{Load} = CL - \frac{C\_onchip^2}{2 \times C\_onchip} \quad (1)$$

The **equivalent series resistance (ESR)** also called resonant resistance is the resistance of the crystal at the series resonant frequency. It does not reflect the motional resistance (R1).

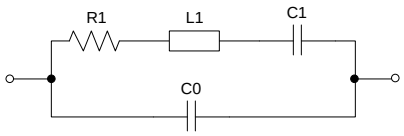

Figure 2. Equivalent Circuit of a Crystal

The **motional resistance (R1)** represents the real resistive losses within the crystal. It is used to calculate the power dissipated in the crystal.

The **shunt capacitance (C0)** represents the capacitance across the crystal. It is the sum of all parasitic capacitances of the electrodes, pins and enclosure.

Drive level refers to the power dissipated in the crystal. Crystal manufacturers specify the maximum drive level the crystal can sustain. Exceeding the maximum drive level may cause shorter lifetimes, frequency shift, and/or physical damage of the quartz and eventual failures. The drive level can be limited with an appropriate series damping resistance.

Table 1. Typical Crystal Specifications

Parameter	Value
Frequency	25 MHz
Load Capacitance (CL)	18 pF
Shunt Capacitance (C0)	7 pF (max)
Equivalent Series Resistance (ESR)	30 Ohm (typ)
Drive Level	100 µW (max)

The motional resistance (R1 and additionally L1 and C1) is typically not given in crystal specifications and it have to be requested from the Manufacturer itself.

It is also possible to estimate the motional resistance using this formula in Equation 2:

$$ESR = R1 \times \left(\frac{CL + C0}{CL} \right)^2 \tag{2}$$

The real or typical value of R1 is greater than the result of this formula since C0 is given as maximum.

With the values from Table 1 R1 can be calculated to:

$$R1 = \frac{ESR}{\left(\frac{CL + C0}{CL} \right)^2} = \frac{30\ \Omega}{\left(\frac{18\ pF + 7\ pF}{18\ pF} \right)^2} = 15.6\ \Omega \tag{3}$$

3.2 Select Damping Resistor R_{Lim} for CDCLVC1310

Figure 3 shows an easy way to select the right damping resistance for different motional resistances and drive level. With the calculated R1 from Section 3.1 a damping resistance is not needed to limit the drive level lower as the specified maximum drive level of 100 µW. If the drive level should be limited to 80-µW maximum, a 10-Ω damping resistor must be used.

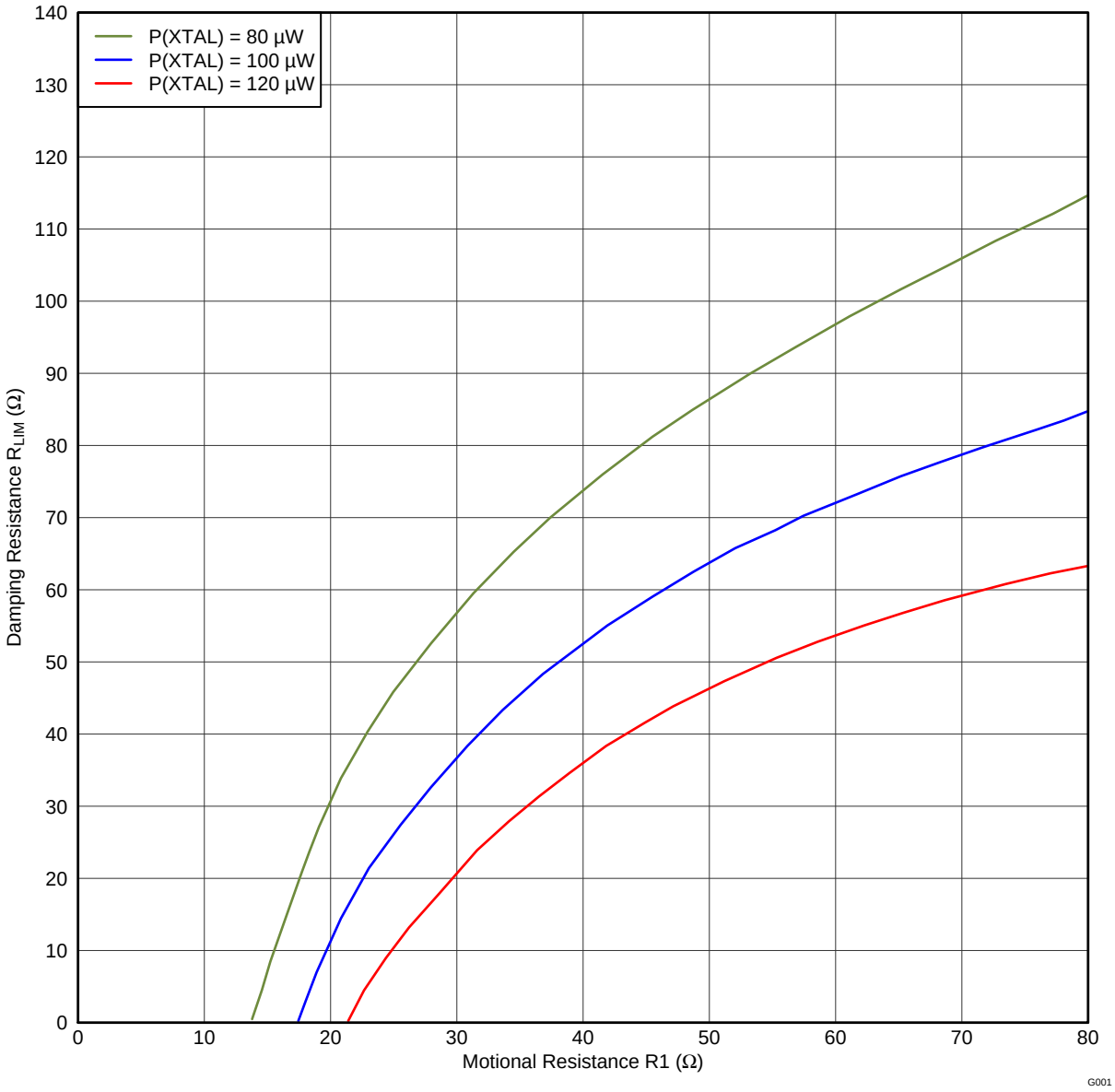

Figure 3. Damping Resistor, R_{Lim}, for Different Drive Levels, V_{DD} = 3.3 V, T_a = RT

4 Phase-Noise Performance

Section 4.1 and Section 4.2 show phase-noise measurements with different crystal frequencies. Each section shows a summary of the phase-noise measurements and the measurement results. The measurements were done with the standard CDCLVC1310EVM with a 25- and 50-MHz crystal. The load capacitance was removed.

Section 4.3 shows phase-noise measurements in comparison to crystal buffer from competition and TI internal crystal buffer.

4.1 25-MHz Xtal

4.1.1 Performance Measurement Summary

Table 2 summarizes the phase-noise measurements of the CDCLVC1310 in crystal-buffer mode. It shows the phase noise between a frequency offset of 100 Hz and 5 MHz and the rms phase jitter in a frequency band of 10 kHz to 5 MHz. The measurements were taken with different V_{DD}/V_{DDO} combinations.

Table 2. Crystal Oscillator Phase-Noise Performance with 25-MHz Crystal Resonator

Phase Noise [dBc/Hz]	f_{offset} [Hz]							Rms Phase Jitter [fs] 10 kHz–5 MHz
V_{DD}/V_{DDO} Supply Range	10	100	1 k	10 k	100 k	1 M	5 M	
3.3 V/3.3 V	–90.2	–120.2	–147.9	–164.5	–169.3	–169.5	–169.9	65.5
3.3 V/2.5 V	–91.7	–119.0	–145.7	–161.3	–168.3	–169.7	–169.6	67.3
3.3 V/1.8 V	–89.9	–119.3	–140.2	–154.4	–167.9	–169.6	–169.7	68.3
3.3 V/1.5 V	–92.9	–117.3	–133.9	–148.4	–166.4	–168.6	–169.0	78.9
2.5 V/2.5 V	–86.4	–113.6	–140.9	–157.1	–164.8	–166.1	–166.3	99.8
2.5 V/1.8 V	–87.3	–112.8	–136.9	–152.5	–164.3	–166.0	–166.1	103.1
2.5 V/1.5 V	–82.4	–113.2	–134.2	–148.1	–163.4	–165.6	–165.6	109.7
1.8 V/1.8 V	–78.6	–106.8	–133.6	–150.1	–158.3	–160.5	–160.7	193.4
1.8 V/1.5 V	–75.5	–106.2	–132.1	–146.8	–157.8	–160.3	–160.6	198.7
1.5 V/1.5 V	–73.1	–101.4	–128.7	–143.8	–152.3	–155.5	–156.0	340.9

4.1.2 Measurement Results

Figure 4 through Figure 6 show the measured results for output phase noise with different V_{DD}/V_{DDO} combinations.

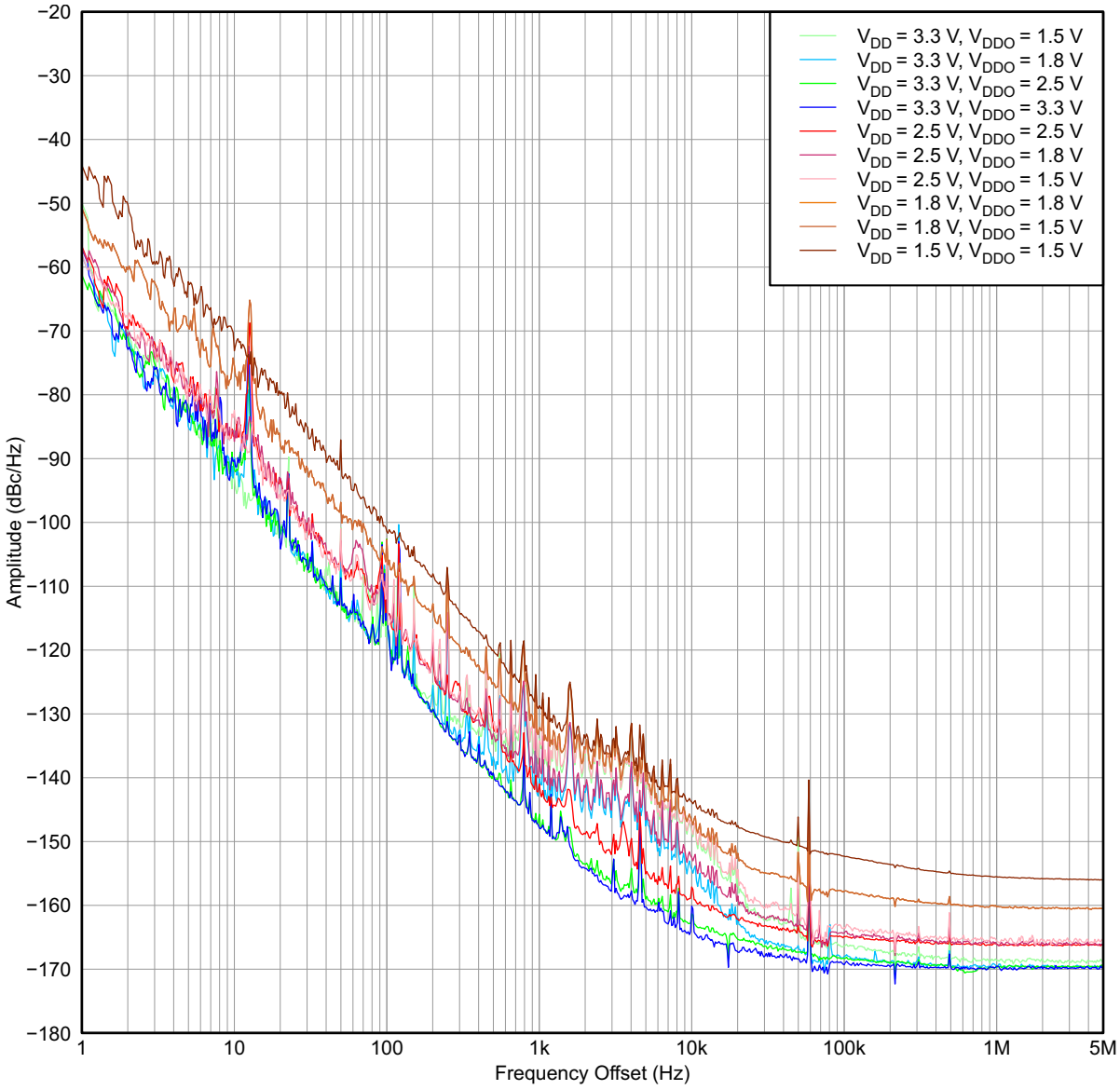

Figure 4. 25-MHz Xtal Output Phase Noise

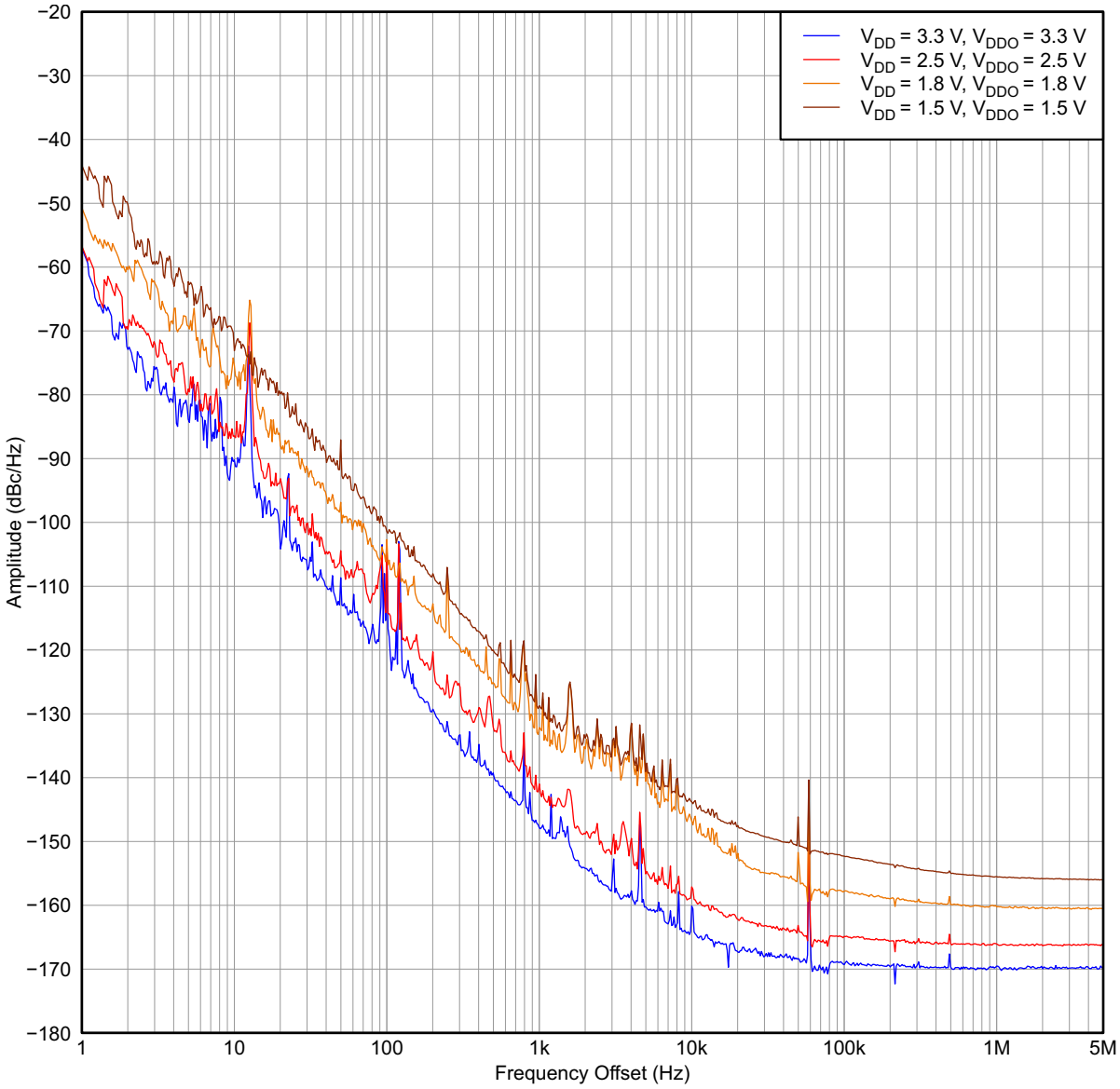

Figure 5. 25-MHz Xtal Output Phase Noise at V_{DD} = V_{DDO}

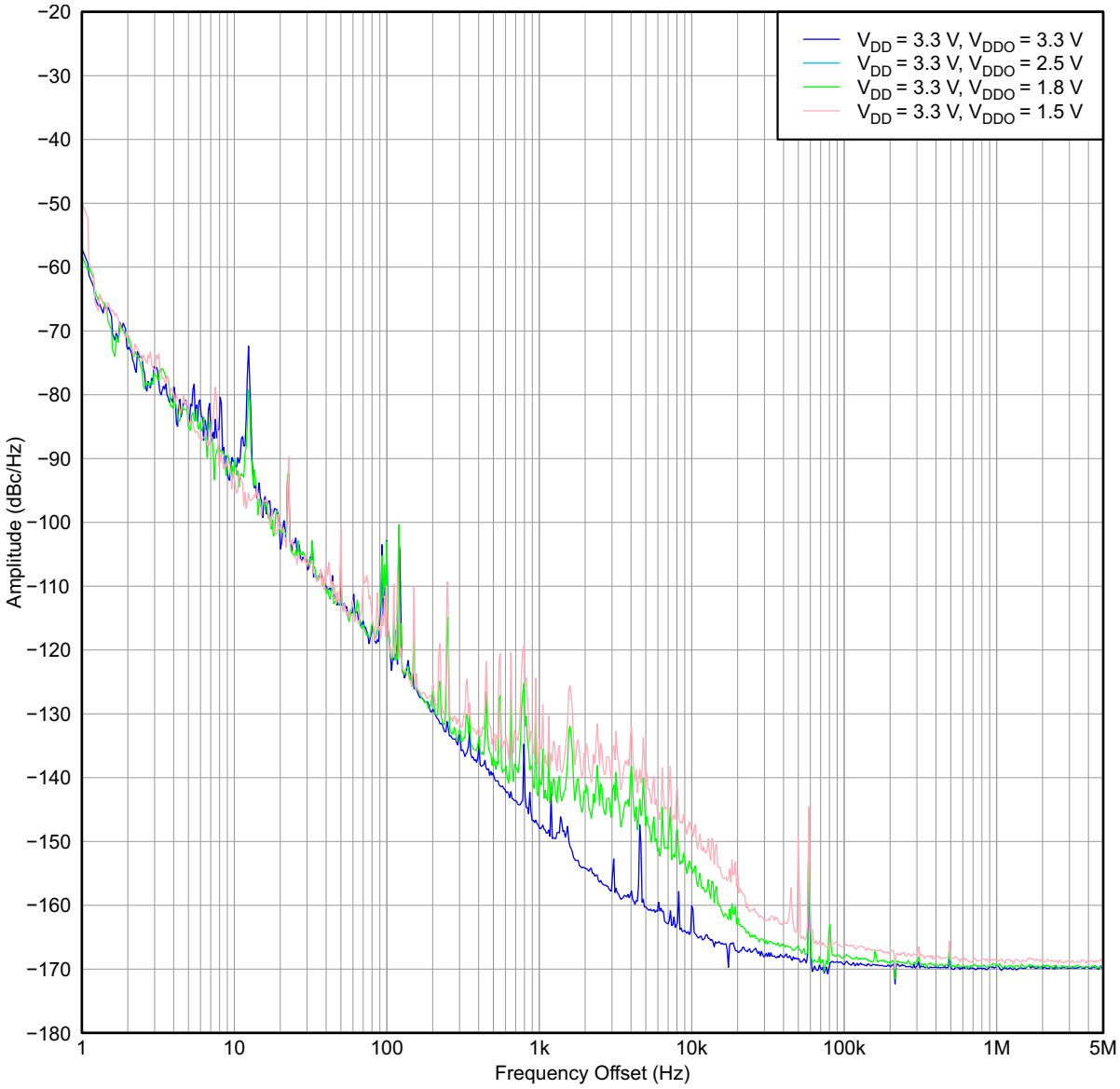

Figure 6. 25-MHz Xtal Output Phase Noise at V_{DD} = 3.3 V

4.2 50-MHz Xtal

4.2.1 Performance Measurement Summary

Table 3 summarizes the phase-noise measurements of the CDCLVC1310 in crystal-buffer mode. It shows the phase noise between a frequency offset of 10 Hz and 10 MHz and the rms phase jitter in a frequency band of 10 kHz to 20 MHz. The measurements were taken with different V_{DD}/V_{DDO} combinations.

Table 3. Crystal Oscillator Phase-Noise Performance with a 50-MHz Crystal Resonator

Phase Noise [dBc/Hz]	f_{offset} [Hz]							Rms Phase Jitter [fs] 10 kHz–20 MHz
V_{DD}/V_{DDO} Supply Range	10	100	1k	10 k	100 k	1 M	10 M	
3.3 V/3.3 V	–74.5	–109.3	–141.1	–160.8	–167.3	–169.2	–169.8	68.9
3.3 V/2.5 V	–76.5	–108.3	–137.5	–156.3	–166.9	–168.9	–169.3	71.1
3.3 V/1.8 V	–75.2	–106.8	–131.1	–148.3	–164.6	–167.6	–168.6	81.1
3.3 V/1.5 V	–79.5	–107.3	–123.4	–143.1	–162.3	–165.6	–167.0	99.0
2.5 V/2.5 V	–75.2	–103.7	–136.9	–154.7	–162.7	–165.2	–165.9	106.7
2.5 V/1.8 V	–75.8	–107.3	–133.0	–147.7	–161.6	–164.6	–165.5	113.9
2.5 V/1.5 V	–76.2	–100.8	–128.8	–142.9	–160.2	–163.1	–164.4	127.4
1.8 V/1.8 V	–71.8	–98.1	–129.5	–145.6	–155.0	–158.9	–160.0	212.7
1.8 V/1.5 V	–70.4	–99.1	–127.7	–141.8	–154.3	–158.6	–159.7	220.9

4.2.2 Measurement Results

Figure 7 and Figure 8 show the measured results for output phase noise with different V_{DD}/V_{DDO} combinations.

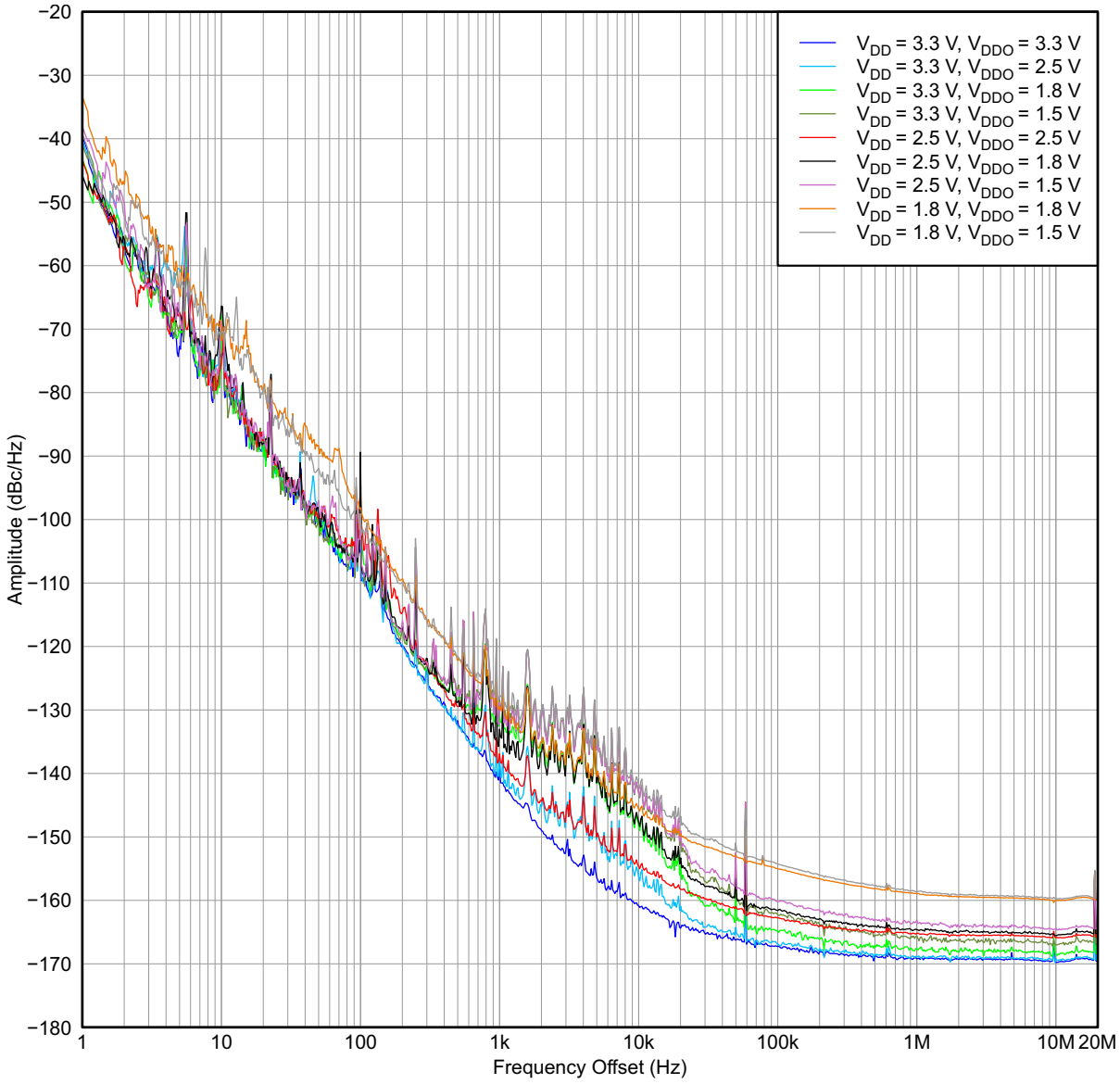

Figure 7. 50-MHz Xtal Output Phase Noise

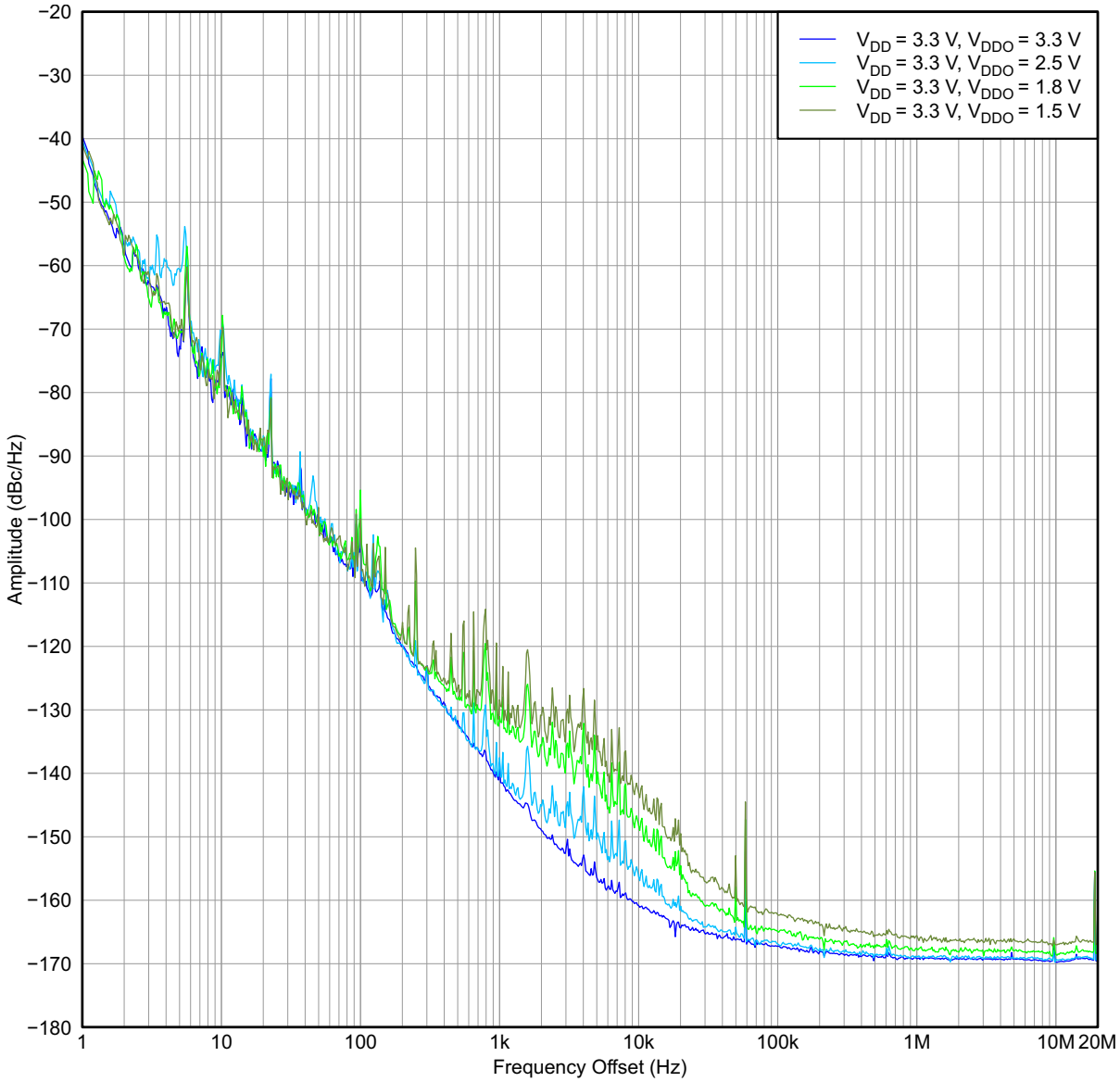

Figure 8. 50-MHz Xtal Output Phase Noise at V_{DD} = 3.3 V

4.3 CDCLVC1310 Versus Competition

As shown in Figure 9 the phase-noise profile of the CDCLVC1310 is around 12 dBc/Hz lower than the competition.

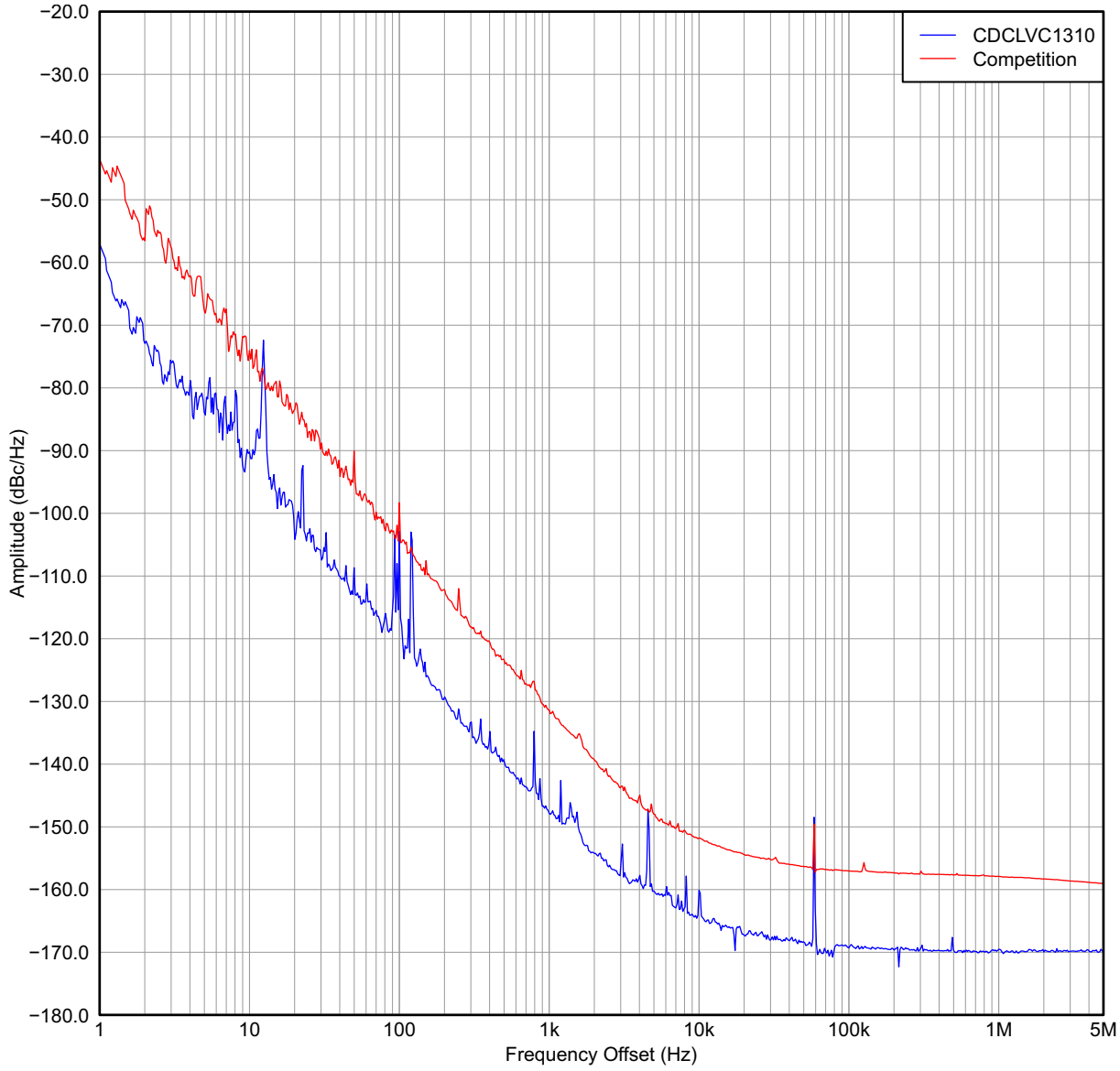

Figure 9. 25-MHz Xtal Output Phase Noise Versus Competition at V_{DD} = V_{DDO} = 3.3 V

5 References

1. *CDCLVC1310 Datasheet* (SCAS917)
2. *Phase Noise Performance of CDCLVC1310* (SCAA115)

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